Impact of the Vertical SOI "DELTA" Structure on Planar Device Technology

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***Abstract*—A fully depleted lean channel transistor (DELTA) with its gate incorporated into a new vertical ultra-thin SOI structure is presented. In the deep-submicrometer region, selective oxidation produces and isolates an ultra-thin SOI MOSFET that has high crystalline quality, as good as that of conventional bulk single-crystal devices. Experiments and three-dimensional simulations have shown that this new gate structure has effective channel control, and that the vertical ultra-thin SOI structure provides superior device characteristics: reduction in short-channel effects, minimized subthreshold swing, and high transconductance.**

I. Introduction

Conventional planar MOSFET's with LOCOS isolation have certain merits: simple self-aligned fabrication process, as well as the performance improvement that comes with scaling down the device feature size. Therefore, up to the present generation of devices, other structures were never considered to be of practical use.

However, as MOSFET's are scaled down to the deep-submicrometer region (0.3–0.1 μm), device sizes and isolation lengths become approximately equal to the depletion layer widths. Since the depletion layers merge, short-channel effects, parasitic MOS effects, and device interactions become serious problems. Moreover, to reduce power consumption and to solve device reliability problems, a low supply voltage is essential [1], [2]. A low supply voltage requires special device characteristics including a low subthreshold voltage and a minimum subthreshold swing to maintain the ratio of on/off channel current.

To eliminate these problems and provide superior performance, we believe a three-dimensional device structure is attractive. Two different three-dimensional device structure concepts have been proposed as alternatives to scaling [3].

The first concept makes the effective device length longer than the depletion layer width by using a vertical structure, such as vertical MOSFET's and trench isolation [4]–[6]. However, it is clear that these vertical structures require a complex fabrication process and that device performance is reduced because of the long gate length that is required. Moreover, it is evident that these structures are difficult to contact to the substrate, and thus suffer from a substrate floating effect.

The second concept makes the device thickness smaller than the depletion-layer width to intentionally deplete the channel. This can be done with thin-film SOI technology, such as SIMOX and recrystallization [7], [8]. This concept is ideal because the structure has the same merits as conventional MOSFET's, however, it requires making ultra-thin SOI substrates, a difficult task. Still, an interesting feature of ultra-thin-film SOI devices is that the interaction between the front and back channel results in device characteristics different from those of conventional MOS devices. By controlling the back-channel conditions, high immunity to short-channel effects, high transconductance, and a reduction in the kink caused by substrate floating effects were found [7]–[9].

This paper proposes a new device structure that offers a simple process, meaning that no new processes for making ultra-thin-SOI structures are required, enabling proper control of the back gate [10]. The special features of this fully depleted lean-channel transistor (DELTA) are as follows.

1) Bulk single-crystal SOI is formed by selective oxidation using the same process as for LOCOS. 2) The entire channel potential is determined by the gate, which produces SOI device characteristics in a vertical ultra-thin substrate. 3) The channel current flows along the vertical surface as well as the horizontal surface. Therefore, the effective channel width becomes larger than that of conventional devices, and this offers superior drivability.

The relationship between the subthreshold swing and channel length as a function of SOI-channel thickness has been studied in detail, because this characteristic determines the device structure for low supply voltages. The authors also present a simple model for DELTA based on charge sharing and clarify the subthreshold-swing suppression mechanism by using three-dimensional field effects when the gate length is short.

II. Device Design and Fabrication Process

The unique feature of the DELTA process is selective-oxidation-formed bulk single-crystal SOI [11], [12]. The DELTA process flow is schematically shown in Fig. 1(a)–(c). Boron-doped 10-$\Omega \cdot$ cm (100) wafers are used. On a 25-nm thermal oxide pad, 200 nm of CVD nitride is de-

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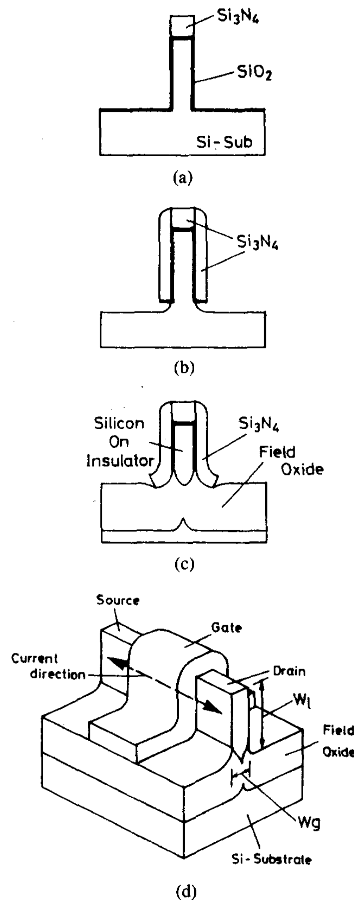

Fig. 1. (a)–(c) Process flow of selective oxidation. (d) Schematic cross section of DELTA.

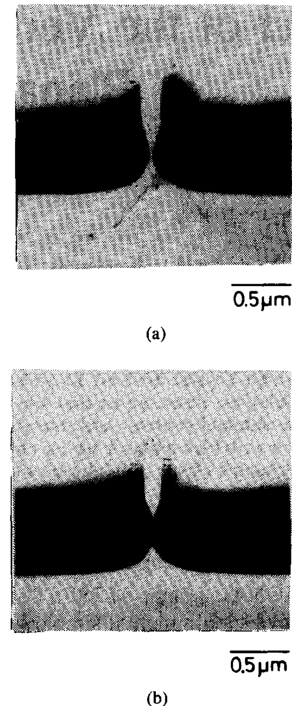

Fig. 2. Cross-sectional TEM pictures of both (a) non-SOI and (b) SOI structures using selective oxidation.

posited. The nitride, thermal oxide pad, and silicon substrate are then etched using anisotropic reactive ion etching (RIE), forming a Si island (Fig. 1(a)). The height of the Si island (W_l) is determined by the etching selectivity in the polysilicon gate fabrication process and is 0.4 μm. Next, 10 nm of thermal oxide is grown, and a 100-nm CVD nitride layer is deposited. Then, using RIE, nitride spacers are formed on the sides of the Si island. The underside of the Si island is then etched by HF/HNO_3 (Fig. 1(b)). Oxidizing the substrate at 1100°C, a SOI structure is formed, as shown in Fig. 1(c).

After removing the nitride-selective oxidation mask, 10 nm of thermal oxide is grown to remove the dry-etching-damaged layer from the Si-island surface. Then the sacrifice oxide layer is etched by HF, and 8.5 nm of gate oxide is grown. Phosphorus-doped 100-nm polysilicon and 100-nm CVD silicon dioxide are deposited. Using anisotropic RIE, the gate structure, which steps over the Si island, is formed and source–drain regions are exposed. Using the gate as an arsenic ion mask, the source and drain are implanted. The schematical DELTA device structure is shown in Fig. 1(d).

Depositing 500-nm dielectric interlayer, contact windows to the top and side surfaces of the Si island are opened, taking advantage of the Si-island height. 900 nm of Al/Si is used for the metallization. During post-SOI processes, there was no problem relating to Si-island strength. Thus except for the nitide-selective oxidation mask fabrication step, the DELTA process is the same as that of conventional self-aligned-gate NMOSFET processes. Therefore, this process is highly compatible with conventional LOCOS processes.

Cross-sectional TEM pictures of both a non-SOI and SOI structures are presented in Fig. 2(a) and (b), respectively. Both pictures show that the gate oxides, which show no electrical breakdown problems for gate voltages of up to 5 V, are as smooth as with conventional MOSFET's.

Fig. 2(a) shows that selective oxidation creates defects at the field oxide edge along the slipping surface (111). However, Fig. 2(b) shows that once the SOI structure is formed, no defects appear. This can be understood as follows:

The nearly identical bird's beak shapes in Fig. 2(a) and (b) imply that there is no difference in stress between (a) and (b). As a result, one would expect the same defects to be formed during the selective oxidation process. However, this is not the case, as the photographs clearly show. In addition, the selective oxidation temperature is not high enough to eliminate the defects. Therefore, it seems that no defects are created during oxidation and the excess de-

fects in Fig. 2(a) are formed during the post-cooling period after oxidation. During this cooling time, the SiO_2 layer under the Si relieves the stress from the SOI, instead of producing defects.

III. Device Characteristics

The DELTA gate effectively controls the channel potential from three sides and induces ultra-thin-SOI effects vertically. A three-dimensional simulation of the potential distribution is shown in Fig. 3. Compared with conventional devices, the potential bend is small and the potential distribution is rather flat. This means there is a low surface electric field and a flat inversion charge distribution. This results in the following measured superior device characteristics, even if the substrate is thicker than that of conventional ultra-thin-SOI devices [7]–[9].

A. Short-Channel Effect

Subthreshold characteristics for $W_g = 0.2$ μm (DELTA) and 10 μm (conventional), both the $L_{eff} = 0.15$ μm, $T_{ox} = 8.5$ nm, and identical impurity profiles, are shown in Fig. 4(a) and (b), respectively. For $W_g = 10$ μm, punchthrough leakage occurs for all values of V_{ds}, but for $W_g = 0.2$ μm it does not occur for V_{ds} less than 2 V.

The short-channel effect immunity of DELTA seems to result from its novel substrate and gate structure. That is, the substrate punchthrough path is replaced by the buried SiO_2 layer and the electric field effect of the DELTA gate structure suppresses the penetration of the drain potential into the channel.

B. Current Drivability

The channel width of DELTA consists of the top surface (W_g) and both side surfaces (W_l), so the effective channel width is $W = W_g + 2W_l$. This means that for the same layout width (W_g) the height of the Si island determines the channel width and its current drivability.

The dependence of the transconductance on W is shown in Fig. 5. Since the ultra-thin structure reduces the surface electric field and induces high carrier mobility, DELTA has a high transconductance. G_m is 1.5 times higher than $G_m^* \propto W_g + 2W_l$ for $W_g = 0.15$ μm.

The I–V characteristics for $L_{eff} = 0.57$ μm and $W_g = 0.15$ μm are shown in Fig. 6. Because of a high transconductance and large W compared with standard MOSFET's, DELTA's drain current is much larger.

In addition, Fig. 6 shows that the effects of the electric field concentration at the top corners and the pointed bottom edge (see Fig. 1(d)) are negligible as no humps appear in the curves in Fig. 6.

C. Subthreshold Swing

An important characteristic of ultra-thin-SOI devices is their small subthreshold swing [13]. This is because the depletion layer capacitance that determines the swing depends strongly on the substrate thickness. The subthreshold swing S is generally written as [14]

$$S = \ln 10 \times kT/q \times (1 + C_d/C_s) \qquad (1)$$

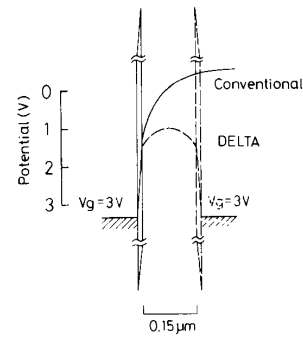

Fig. 3. Simulated potential distribution across channel region in middle of source-drain nodes ($V_{ds} = 3$ V, $V_g = 3$ V).

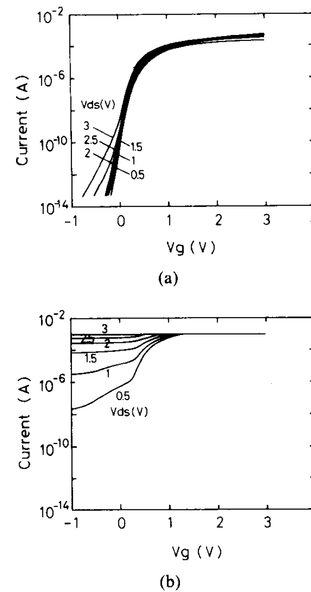

Fig. 4. Subthreshold characteristics for various V_{ds}. (a) $W_g = 0.2$ μm, $L_{eff} = 0.15$ μm. (b) $W_g = 10$ μm, $L_{eff} = 0.15$ μm.

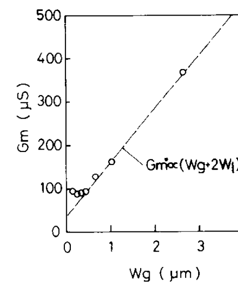

Fig. 5. Relationship between transconductance and W_g ($L_{eff} = 1.0$ μm, $V_{ds} = 3$ V).

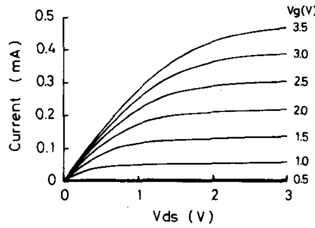

Fig. 6. Typical I-V characteristics for $L_{eff} = 0.57$ μm and $W_g = 0.15$ μm.

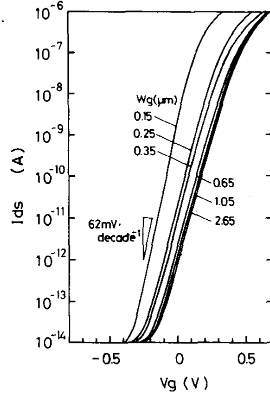

Fig. 7. Subthreshold characteristics as a function of W_g.

where kT/q is the thermal voltage, C_d is the channel depletion layer capacitance and C_s is the gate capacitance. When the channel thickness is less than the depletion layer width, the whole channel is depleted and C_d becomes small. Therefore, C_d/C_s can be neglected and S approaches $\ln 10 \times kT/q$.

The dependence of subthreshold swing on channel width is shown in Fig. 7. A decrease in substrate thickness to less than 0.3 μm results in a smaller swing. Consequently, with this new gate structure, ultra-thin effects are expected for a device thinner than 0.3 μm. For $W_g = 0.15$ μm, the swing decreases to 62 mV/decade. Furthermore, the curves in Fig. 7 show that the top corners and the pointed bottom edge do not affect the off-state leakage current.

Fig. 8 shows the dependence of S on W_g at room temperature, with gate length as a parameter. Note that W_g represents the SOI channel thickness. The width at which the slopes of the curves in Fig. 8 reach unity (W_{gcr}) is presented in relation to effective channel length in Fig. 9. A decrease in gate length results in an increase in W_{gcr}. When the gate length is more than 0.8 μm, however, W_{gcr} is constant.

The S value corresponds to the channel depletion ratio. Therefore, the small subthreshold swing value of the short gate-length device shows that the channel is depleted. With regard to the W_{gcr} dependence on gate length, this depleting is caused by source and drain charge as well as by gate charge. Thus in the short gate-length ultra-thin SOI device, the channel is depleted three-dimensionally by the source, drain, and gate charges.

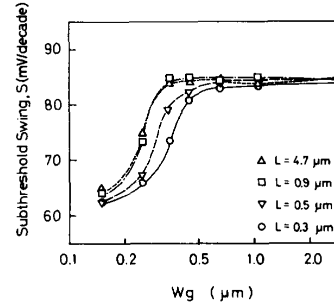

Fig. 8. Subthreshold swings versus channel thickness with the gate length as a parameter.

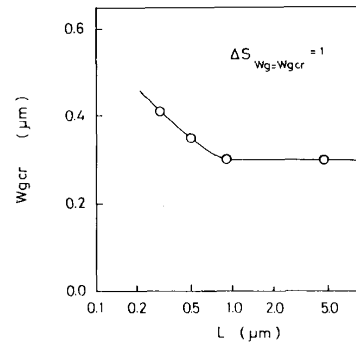

Fig. 9. Relationship between critical channel thickness and gate length.

IV. Discussion

Subthreshold swing reduction in ultra-thin-SOI devices and specifically in DELTA structures, is discussed below. This reduction depends on channel length and results in a limited immunity from short-channel effects.

The device potential in the subthreshold region of a conventional SOI device is shown schematically in Fig. 10(a). The potential Φ of this system is described by the Poisson equation, and its boundary conditions at the front and back interfaces are derived from Gauss' law [14], [15]. That is

$$\frac{d^2\Phi(x)}{dx^2} = \frac{q \cdot N_a}{\epsilon_s\epsilon_0} \qquad (0 \leqq x \leqq t_{\mathrm{sol}}) \tag{2}$$

and

$$\frac{d\Phi_i}{dx} = \frac{\epsilon_{\mathrm{ox}}(V_{gi} - \Phi_s)}{\epsilon_s T_{\mathrm{ox}_i}}, \qquad i = f, b. \tag{3}$$

Here $\Phi(x)$ is the potential at distance x from the SOI film-gate oxide interface. (For the back side, gate x is replaced by $-x$ to maintain consistency with the front side.) The q is the elementary charge, ϵ_s, ϵ_{ox}, ϵ_0 are silicon, silicon dioxide, and vacuum permittivity, respectively, N_a is the channel acceptor density, T_{ox} is the gate oxide thickness, t_{SOI} is the channel SOI film thickness, Φ_s is the surface potential, V_{gf} is front gate voltage and V_{gb} is the surface voltage of the substrate. To simplify the model the inter-

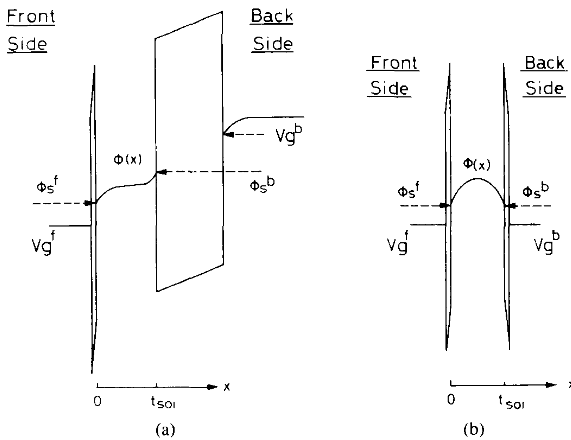

Fig. 10. Cross-sectional potential distribution model in the subthreshold region. (a) Conventional ultra-thin-SOI structure. (b) DELTA structure.

face-trap charge density and gate work function are eliminated.

To control the channel potential of ultra-thin-SOI MOSFET's, it is important to set adequate back-channel conditions [15]. However, due to a large T_{ox_b}, the substrate field effect can affect the channel only slightly. Moreover, it is difficult to change the V_{gb} in practical device operation. This is because the substrate has a large parasitic capacitance.

For the DELTA device, however, instead of the back-gate conditions, we can apply symmetrical boundary conditions at the center of the channel (see Figure 10(b)). That is, replace t_{SOI} with W_g, and the back side boundary condition becomes

$$\frac{d\Phi}{dx} = 0 \quad \left(\text{at } x = \frac{W_g}{2}\right). \tag{4}$$

From (2)–(4), the channel potential Φ is given by

$$\Phi(x) = \frac{q \cdot N_a}{2\epsilon_s}(x^2 - W_g \cdot x) + \Phi_s. \tag{5}$$

When W_g is small compared with the depletion-layer width, the channel surface potential Φ_s is

$$\Phi_s = V_g - \frac{q \cdot N_a \cdot W_g \cdot T_{ox}}{2\epsilon_{ox}}. \tag{6}$$

Equation (6) shows that, when W_g is small, the surface potential is equal to V_g.

For short-channel DELTA devices, it is necessary to make an approximation with a parameter δ based on the charge-sharing model. δ is the charge-sharing component of the source and drain. The effective channel charge $N_{a^{\mathrm{eff}}}$, can be given by

$$N_a^{\mathrm{eff}} = (1 - \delta) \cdot N_a. \tag{7}$$

With (6), the short-channel device subthreshold current I_d is, therefore, expressed as a function of gate bias V_{gs} and drain bias V_{ds} by

$$I_d = C_i \cdot \exp\left[\frac{-q}{kT}\left(-V_{gs} + \frac{q \cdot N_a^{\mathrm{eff}} \cdot W_g \cdot T_{ox}}{2\epsilon_{ox}}\right)\right] \cdot [1 - \exp(-q/kT(V_{ds})] \tag{8}$$

where C_i is a device-dependent parameter [14]. When the channel length is short and δ is unity, (8) is reduced to

$$I_d \propto \exp[q/kT(V_{gs})]. \tag{9}$$

This shows that scaling down the channel length of DELTA results in a three-dimensional depletion of the channel and a small subthreshold swing.

For conventional MOSFET's, the channel depletion layer penetrates deeply into the substrate when δ becomes large. Increasing the layer's distance from the gate reduces controllability, thus causing punchthrough current. This results in a large subthreshold swing.

For DELTA, however, the distance is determined by the SOI film thickness, and does not depend on N_a. Therefore, gate controllability is not reduced and the gate field affects the channel carriers directly, even in the short-channel devices. In the subthreshold region, holes must accumulate in the channel. Thus if SOI film thickness is reduced with device size, punchthrough leakage can be suppressed.

V. Conclusion

A new vertical ultra-thin-SOI device structure (DELTA) has been presented and its superior device performance has been examined. DELTA performs as good as, if not better than previously reported planar ultra-thin-SOI devices [7], [8], [13].

Both experiment and simulation have shown that DELTA's vertical ultra-thin-gate structure is effective in producing superior device characteristics. Furthermore, DELTA has strong immunity to short-channel effects and has superior subthreshold characteristics, even if the substrate is thicker than that of a conventional ultra-thin-SOI devices. Therefore, DELTA is suitable as a deep-submicrometer device with low supply voltages.

In the fabrication process, it was shown that selective oxidation can be used to make a high-quality single-crystal SOI device. So, in spite of its vertical structure, DELTA has high compatibility with a conventional MOSFET process flow, in terms of layout and fabrication. Thus DELTA will benefit the planar device technology for three-dimensional device structure fabrication and rival conventional MOSFET structures in the deep-submicrometer region.

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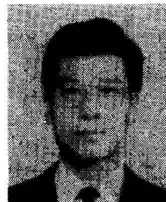

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