OSFP MSA

Specification for

OSFP OCTAL SMALL FORM FACTOR PLUGGABLE MODULE

Rev 4.1

August 2nd, 2021

Abstract:

This specification defines the electrical connectors, electrical signals and power supplies, mechanical and thermal requirements of the OSFP Module, connector and cage systems. The OSFP Management interface is described in a separate document, Common Management Interface Specification for 8/16X Pluggable Transceivers.

This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules.

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Revision History:

Rev 4.1	8/2/2021	Cage latch flap radius is enlarged. Cage shoulder keepout added to the stacked SMT cage (Sec 5). Cage assembly tolerance is relaxed (Sec 5).
Rev 4.0	5/28/2021	Type 2 and 3 modules with bigger front are added (Fig 3-3). Module latch release feature is further clarified (Sec 3.7). Optional riding heatsink is added (Sec. 4.5). Case temperature location requirement and connector environmental requirement are added (Sec. 8). OSFP-RHS nose shape is updated to avoid a potential interference with a connector (Fig 9-8). OSFP-RHS heatsink contact area is adjusted (Sec. 9). 800G OSFP specification is added, with PMDs (Sec. 10.2) and electrical information (Sec. 11.4). More optical connector configurations are added (Section 10.3). Max current to the module is increased to 10A, supporting 30W module (Sec. 11.6). Lower power mode is added to allow up to 2W (Table 11-8).
Rev 3.0	3/14/2020	Specifications for the stacked SMT connector and its cage are added to section 5. Reference design of cage vent holes are added to SMT single row cage. Universal MIS is added to the reference section.
Rev 2.0	1/14/2019	Major updates including: Touch temperature (section 3.9), stacked cage/connector (section 5), OSFP-RHS (section 8) and informative pull tab length (Appendix B) are added. Impedance requirement for the OSFP is relaxed (section 7.2). Management interface speed is increased (Section 10.5). Power class definition are updated, with increase of max power to 21.1W (section 10.6). GD&T of the drawings are updated. MPO-12 two row and MPO-16 lane assignments are added (section 9.8).
Rev 1.12	8/1/2017	Editorial updates, as of: Note 1 in the Figure 1 is clarified with “0.00mm max from top”. PMD in the section 7 and titles are updated, including Figure 49 and 50 the optical receiver/transmitter lane numbers are revised to avoid any confusion. In section 8, word “must” replaced with “shall”. Legal claim at page 1 “fitness or any..” typo fixed as “fitness for any..”.
Rev 1.11	6/26/2017	Editorial updates, as of: Typo in the figure number in the figure table of contents fixed; Revision history added.
Rev 1.1	6/7/2017	Minor updates, as of: MPO 24 lane assignment (section 7.7.3) removed, to remove conflict with other industry conventions ; PCB location with respect to the module is specified with MMC modifier, to provide better dimensional control (Figure 8) ; Test ambient condition (20C, sea level) specified for the clarification in the module airflow impedance (Figure 42) ; In section 8.5, "optional" added to the fast and high-speed bus mode to clarify that those modes are optional ; In table 8-6, T_hplp description is updated for better clarification of the feature ; Power filter inductance adjusted to increase the power supply margin (Figure 59)
Rev 1.0	3/17/2017	Initial Release

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Tables

1 Scope

The OSFP specification defines:

- The OSFP module mechanical form factor, including latching mechanism;
- Host cage together with the mating connector;
- Electrical interface, including pin-out, data, control, power and ground signals;
- Mechanical interface, including package outline, front panel and printed circuit board (PCB) layout requirements;
- Thermal requirements and limitations, including heat sink design and airflow;
- Electrostatic discharge (ESD) requirements, and;
- The module management interface (contained in the OSFP Management Specification).

2 References

- IEC 61754-7-1:2014: Fibre optic interconnecting devices and passive components - Fibre optic connector interfaces - Part 701: Type MPO connector family – One fibre row
- IEC 61754-20:2012: Fibre optic interconnecting devices and passive components - Fibre optic connector interfaces - Part 20: Type LC connector family.
- TIA-604-18, FOCIS 18 Fiber Optic Connector Intermateability Standard – Type MPO-16
- CS® Connector Specification, Rev 1.0, September 18th, 2017, http://www.qsfp-dd.com/cs-optical-connector/
- SFF-8636: Specification for Management Interface for Cabled Environments, Rev. 2.7 January 26, 2016
- UM10204, I^2C-bus specification and user manual, Rev 6 – 4 April 2014
- MIPI $I3C^{SM}$ HCI^{SM} v1.0, MIPI Alliance, September 29, 2017
- SFF-8679: Specification for QSFP+ 4X Base Electrical Specification, Rev 1.8 October 4, 2018
- SFF-8024: Specification for SFF Cross Reference to Industry Products, Rev 4.1 June 27, 2016
- EN61000-4-2:2008: Electromagnetic compatibility (EMC)- Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test
- ANSI/ESDA/JEDEC JS-001-2014: Electrostatic Discharge Sensitivity Testing - Human Body Model (HBM) - Component Level
- IEEE802.3bs: Media Access Control Parameters, Physical Layers and Management Parameters for 200 Gb/s and 400 Gb/s Operation
- IEEE802.3cd: Media Access Control Parameters for 50 Gb/s and Physical Layers and Management Parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s Operation
- IEEE802.3bj: Amendment 2: Physical Layer Specifications and Management Parameters for 100 Gb/s Operation Over Backplanes and Copper Cables
- IEEE802.3bm: Amendment 3: Physical Layer Specifications and Management Parameters for 40 Gb/s and 100 Gb/s Operation over Fiber Optic Cables
- EIA-364-70: Temperature Rise Verus Current Test Procedure for Electrical Connectors and Sockets
- GR-63-CORE, $NEBS^{TM}$ Requirements: Physical Protection, Issue 4, April 2012
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- QSFP-DD Hardware Specification for QSFP Double Density 8X Pluggable Transceiver, Revision 3.0, September 19, 2017
- 400G BiDi MSA, https://www.400gbidi-msa.org/
- Interface Specification for MDC Receptacle, Rev 4, February 6 2020, USC11383001, US Conec
- Specification for SN® Transceiver Receptacle, SN® Connector Specification SN60092019 Rev 1.0, Senko
- Common Management Interface Specification for 8/16X Pluggable Transceivers, Rev 4.0, QSFP-DD MSA, http://www.qsfp-dd.com/
- OIF-CEI-04.0, Common Electrical I/O (CEI) - Electrical and Jitter Interoperability agreements for 6G+ bps, 11G+ bps, 25G+ bps I/O and 56G+ bps, 2017, Optical Internetworking Forum
- Press Release, AirMT™ series Non-contact MT Technology, https://global-sei.com/company/press/2019/09/prs072.html
- 3M™ Expanded Beam Optical Connector (EBO), https://www.3m.com/3M/en_US/data-center-us/applications/interconnect-optical/
- USConec MXC® Expanded Beam Connector, https://www.usconec.com/connectors/mxc-expanded-beam

3 OSFP Module Mechanical Specification

3.1 Overview

A typical OSFP module is shown in Figure 3-1. An assortment of connector types are shown. Connector and cable variations not shown here are allowed, including as depicted in Section 10.3.

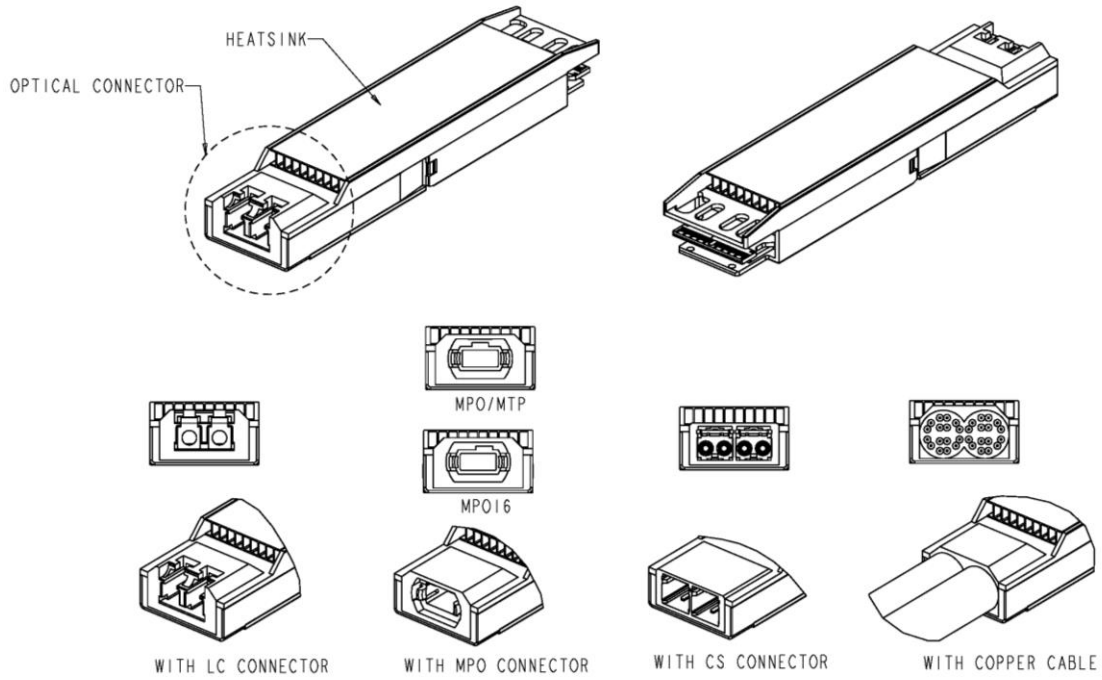


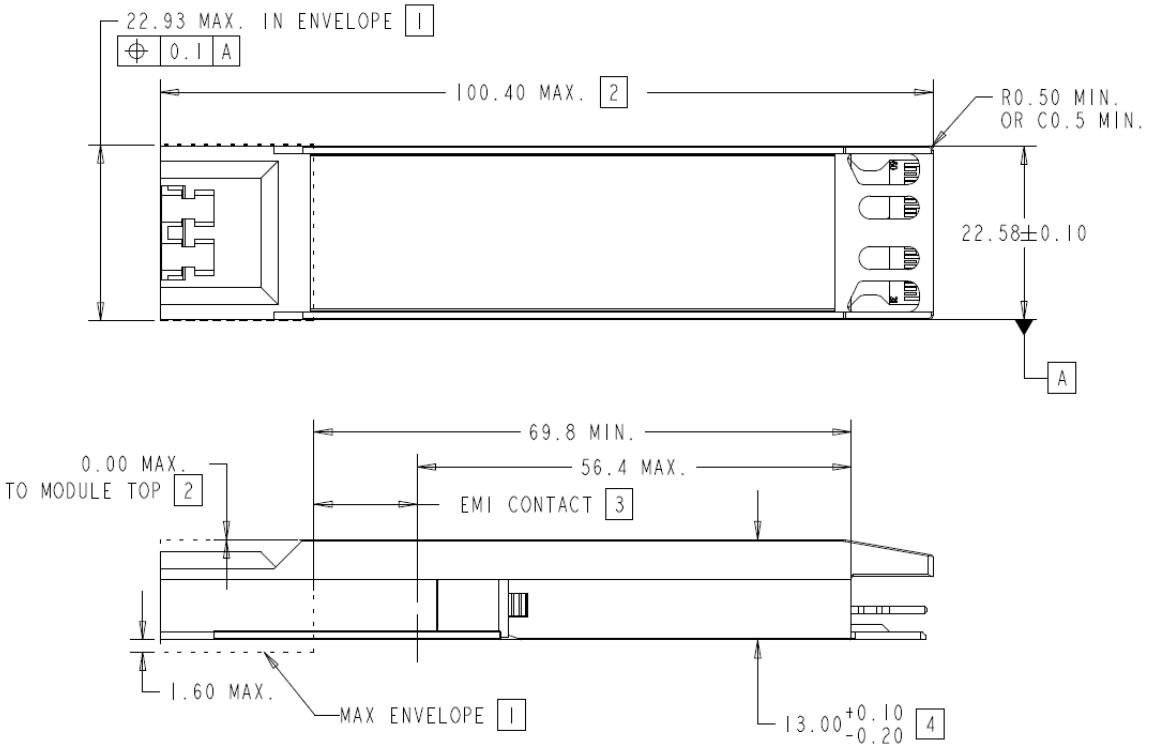
Figure 3-1: OSFP module with different connectors (Duplex LC, MPO, CS®, Copper)

In the module mechanical drawings included throughout this specification, the datum as defined in Table 3-1 shall apply.

Table 3-1: Descriptions of the module mechanical datum

Designator	Description	Figure
A	Width of Module	Figure 3-2
B	Forward stop of Module	Figure 3-2; also see Figure 3-8
C	Bottom surface of Module	Figure 3-2
D	Width of Module pc board	Figure 3-19
E	Signal pad leading edge of Module pc board	Figure 3-19
F	Top surface of Module pc board	Figure 3-19

Figure 3-2 shows the dimensions of the Standard OSFP module. Note that the module is shown with a typical latch release mechanism without a pull tab. Alternate latch release mechanisms are allowed. All dimensions in this specification are in millimeters (mm) unless otherwise noted.



NOTES:

1 FRONT OF THE MODULE, PULL TAB AND OTHER COMPONENTS CAN EXTEND 1.6MM MAX FROM THE BOTTOM OF THE MODULE AND CAN HAVE UP TO 22.93mm WIDTH IN THE MAX ENVELOPE SHOWN.

2 APPLIES TO THE TYPE 1 MODULE ONLY.

3 INDICATED SURFACES (ALL 4 SIDES) TO BE CONDUCTIVE FOR CONNECTION TO CHASSIS GROUND.

4 APPLIES FROM THE TOP OF THE MODULE TO THE BOTTOM OF THE MODULE, INSIDE THE CAGE.

Figure 3-2: OSFP overall dimensions

Figure 3-3 shows the total length and front height of Type 1, Type 2 and Type 3 OSFP modules. A Type 2 OSFP module provides maximum of 16mm additional length in front than a Type 1 module, and a Type 3 OSFP module provides maximum of 3.6mm additional height in the front than a Type 2 module. Type 2 and Type 3 module can provide additional space for various optical interface, as described in the section 10.3.
Type 3 OSFP module is not compatible with stacked cage in the section 5 and 6.

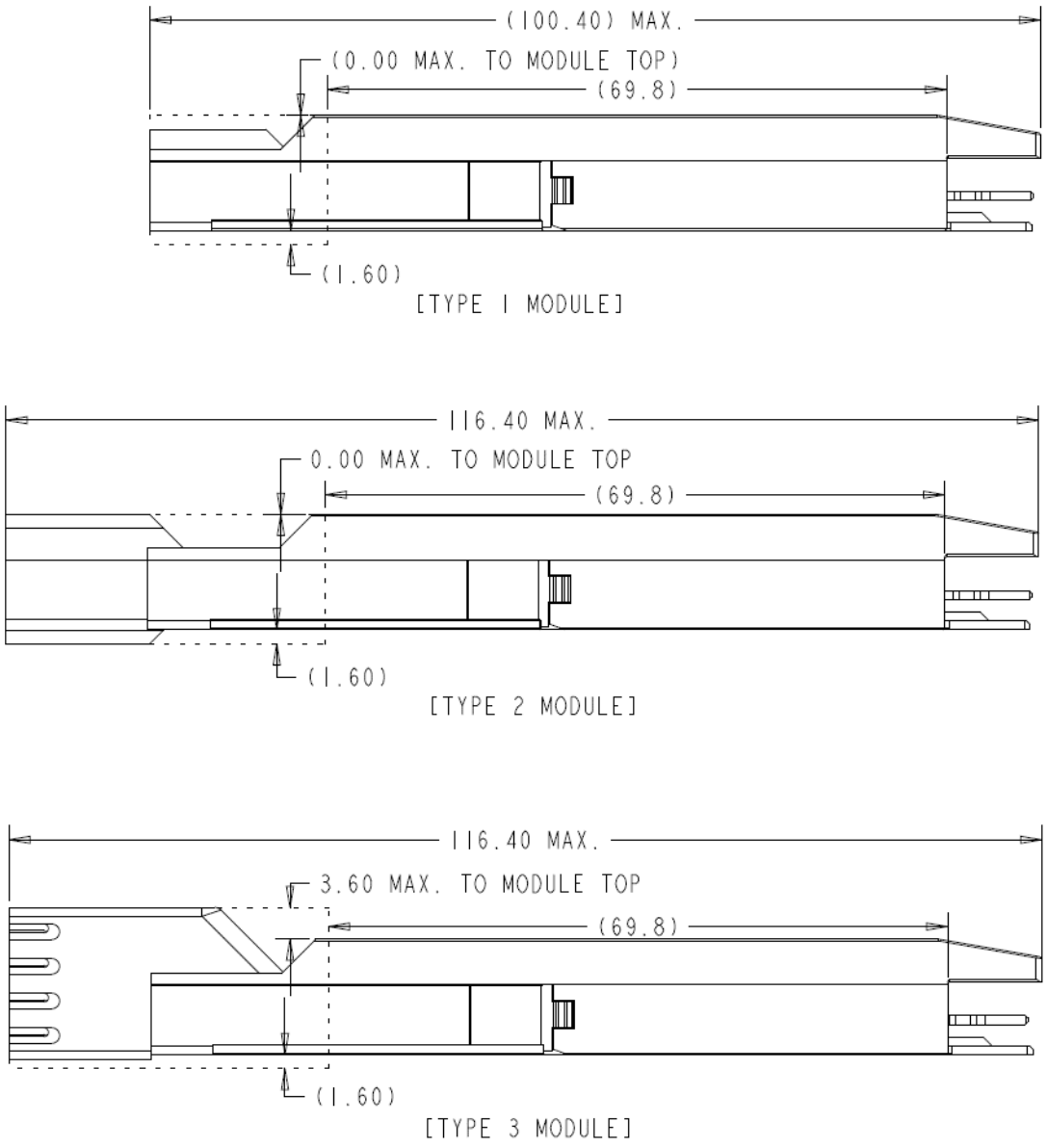


Figure 3-3: Size of module front, for Type 1, Type 2 and Type 3 OSFP

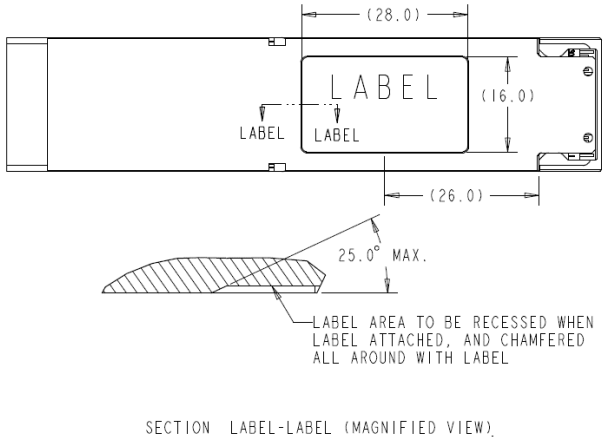


Figure 3-4: OSFP label reference location

Figure 3-4 shows the recommended label location. Figure 3-5 shows the corner radius of the module.

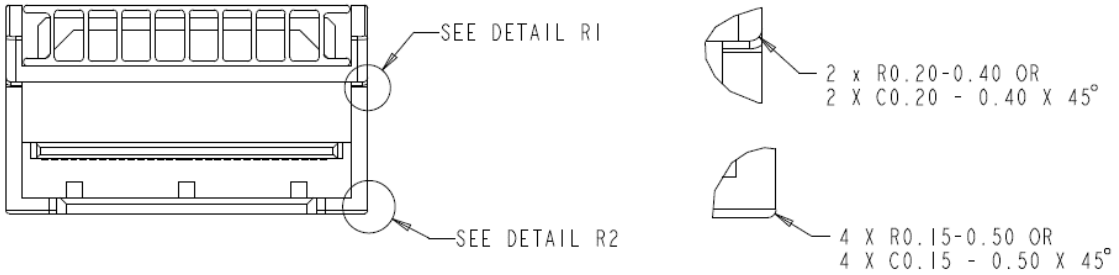


Figure 3-5: OSFP corner radius

3.2 OSFP Nose

To mate with an electrical connector located in the cage, an OSFP module shall have a protruded printed circuit board (PCB) with contact pads. A structure consisting of upper and lower lips forms a nose (i.e. back of the module) that serves as a guard to protect the PCB. Figure 3-6 through Figure 3-12 show the dimensional requirements of the nose, including the shape of the lip, connector mating area, forward stop, ventilation holes and location of the signal pads.

Figure 3-8 shows the location of the forward stop, consisting of the left and right vertical side walls of the bottom case of the module, which interact with features in the connector cage to stop the module when it is fully inserted. The vertical side walls shall extend at least 7.0 mm upward as measured from the bottom of the module for the forward stop feature.

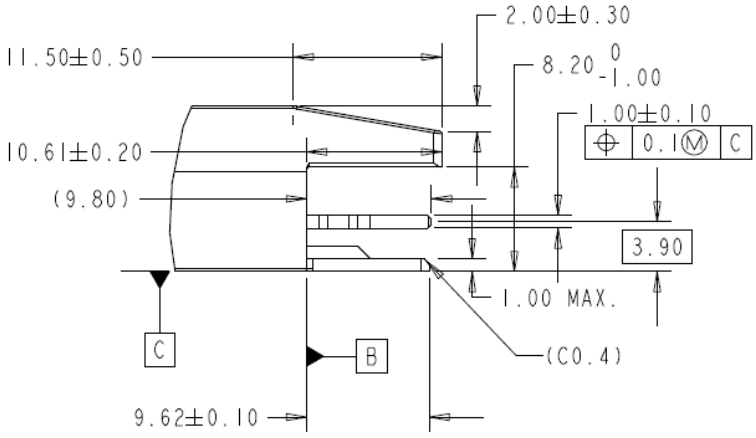


Figure 3-6: OSFP nose, side view

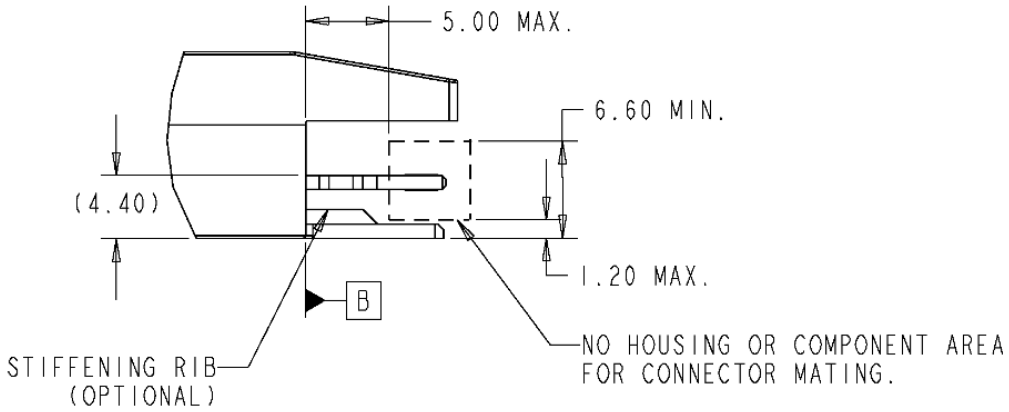


Figure 3-7: OSFP nose, side view, no component area

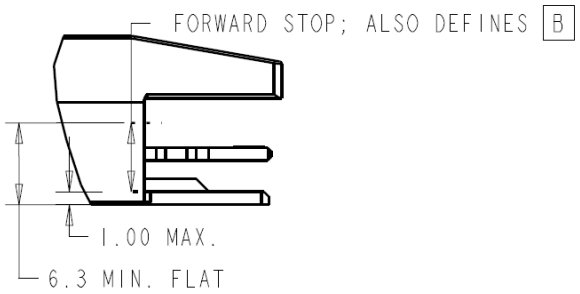


Figure 3-8: OSFP nose, side view, location of the forward stop

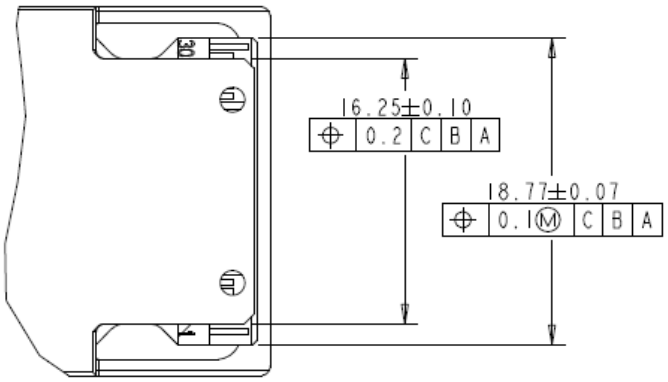


Figure 3-9: OSFP nose, bottom view

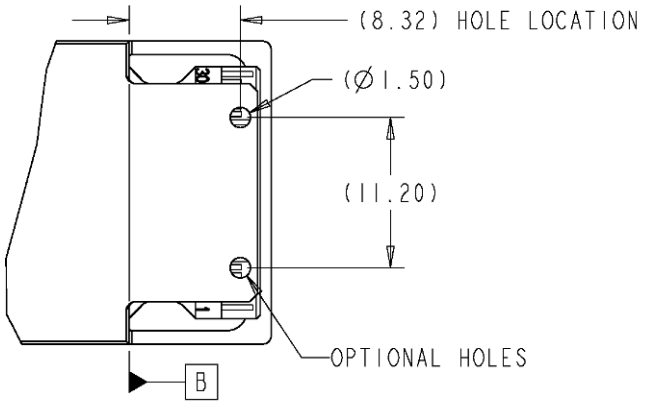


Figure 3-10: OSFP nose, bottom view, optional signal pad inspection holes

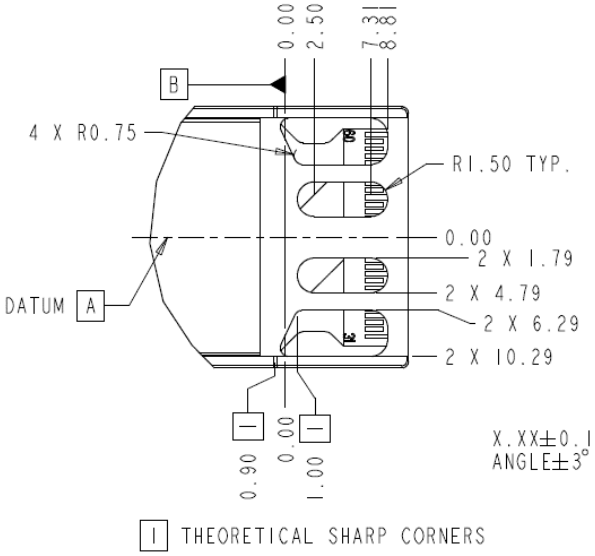


Figure 3-11: OSFP nose, top view: dimension for ventilation holes

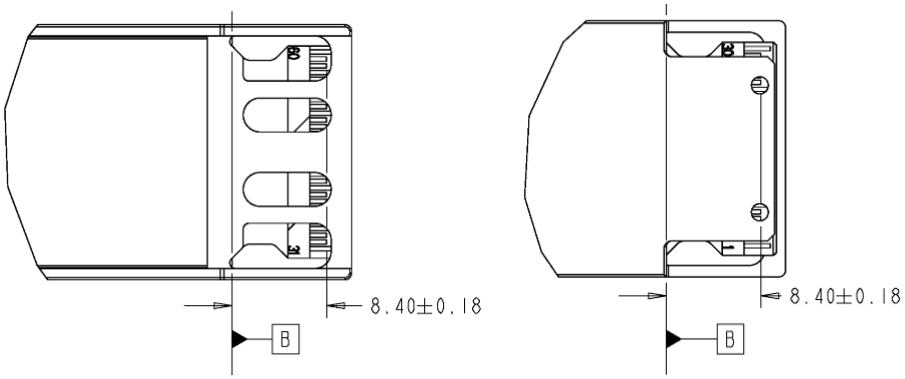


Figure 3-12: Signal pad location to module (left: top view, right: bottom view)

3.3 Heat Sink, Closed Top

In order to dissipate heat, the module allows for airflow along its length. Figure 3-13 shows requirements for the heat sink location in order to avoid collision with the keying feature in the cage and also ensure proper contact with ground and an optional thermal interface. Refer to Figure 4-11 for details of the key feature located in the cage.

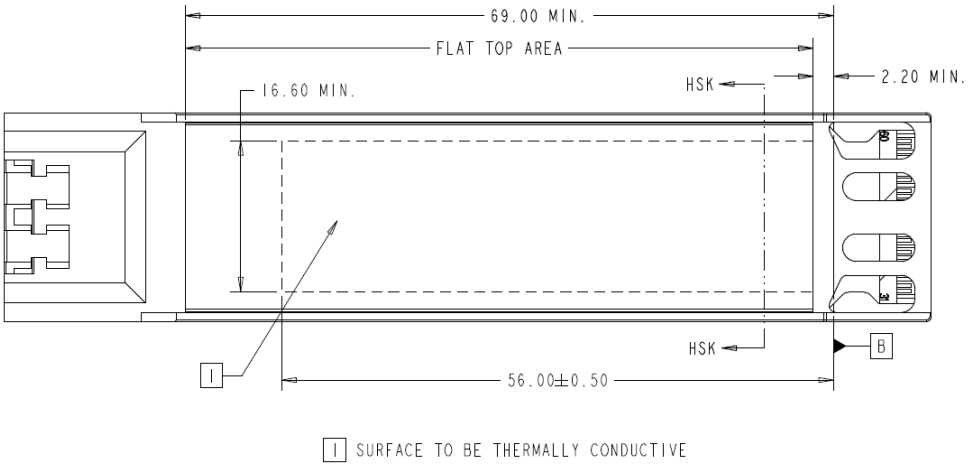


Figure 3-13: Heat sink, top view

The thermally conductive area in Figure 3-13 should have surface flatness and roughness as in Table 3-2. The area may contact with the riding heatsink, which depicted in the section 4.5.

Table 3-2: Surface flatness and roughness for the thermally conductive area

Module Power (Max.)	Surface Flatness	Surface Roughness
N/A	0.12mm or better	Ra 1.6μm or better
Recommended for module with more than 20W (Optional)	0.075mm or better	Ra 0.8μm or better

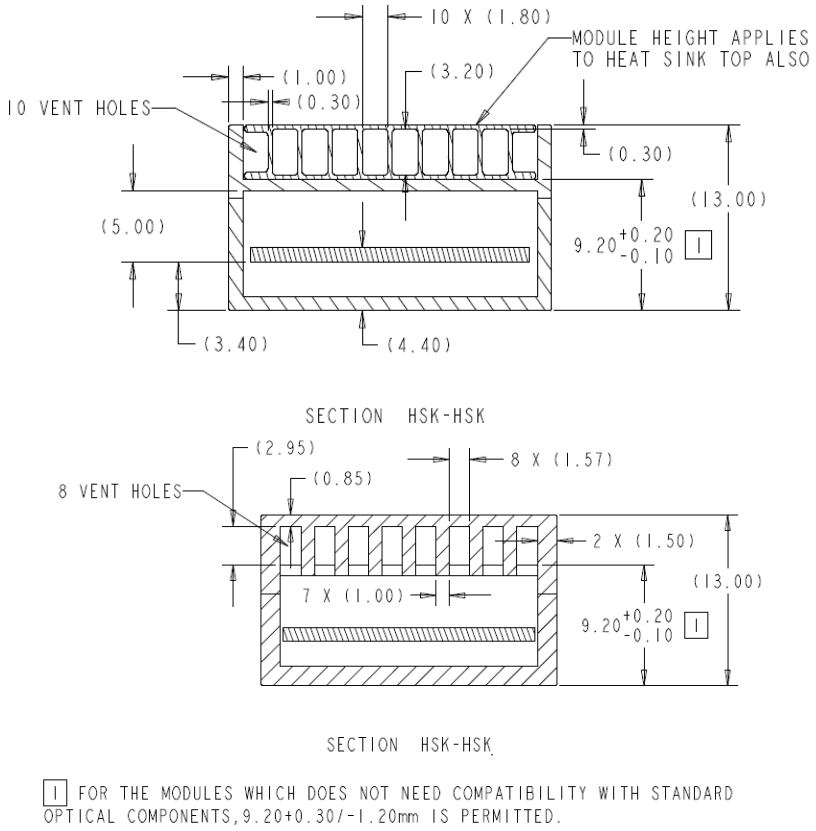


Figure 3-14: Examples of heat sink design (See Figure 3-13 for cross-section location)

Figure 3-14 presents two examples of heat sink design. Either may be considered for use. Alternate designs different from examples presented may also be used, but any heat sink design shall allow for an amount of airflow as defined in Section 8.2.

As shown in the Figure 3-15, top trailing edge of the closed top heatsink to have a minimum edge break to avoid riding heatsink damage.

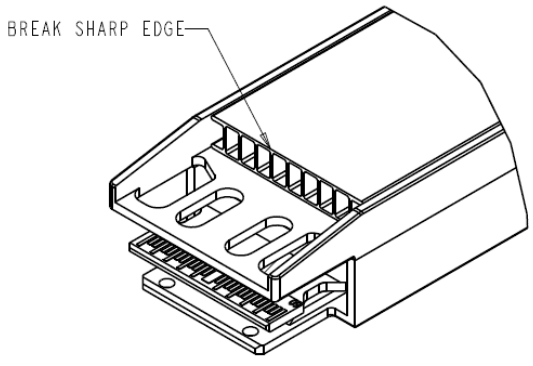


Figure 3-15: Flat top heatsink details, rear of plug

3.4 Heat Sink, Open Top

Modules which have a non-closed top, i.e. open top, are allowed only when the heat sink fins are designed to meet the dimensional requirements outlined in Figure 3-16 through Figure 3-18 in order to prevent EMI finger damage and to ensure proper EMI shielding. Height and length of the heat sink may differ from reference height presented, but still shall allow an amount of airflow as defined in Section 8.2.

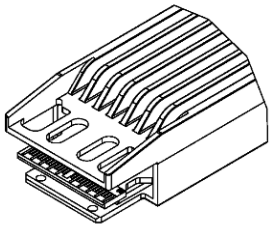


Figure 3-16: Open top heat sink (Isometric view)

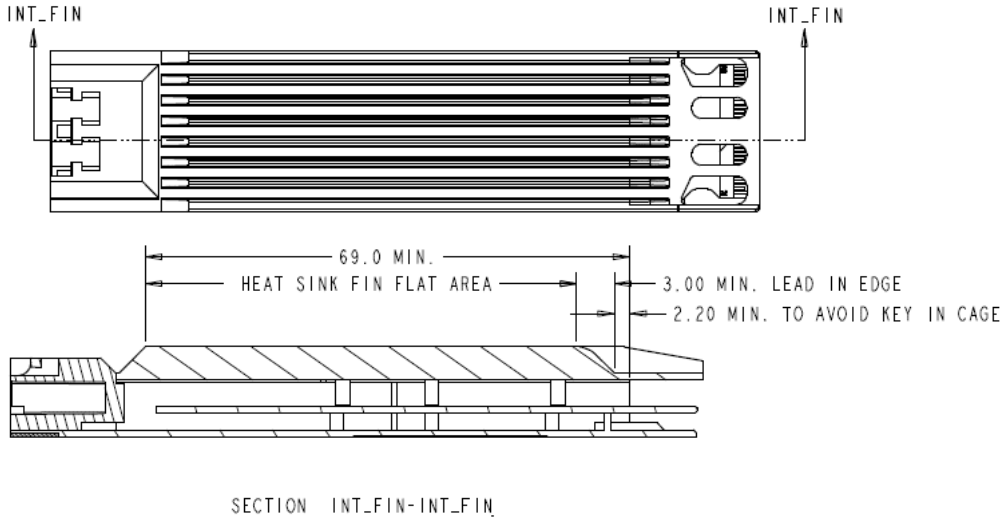


Figure 3-17: Heat sink location

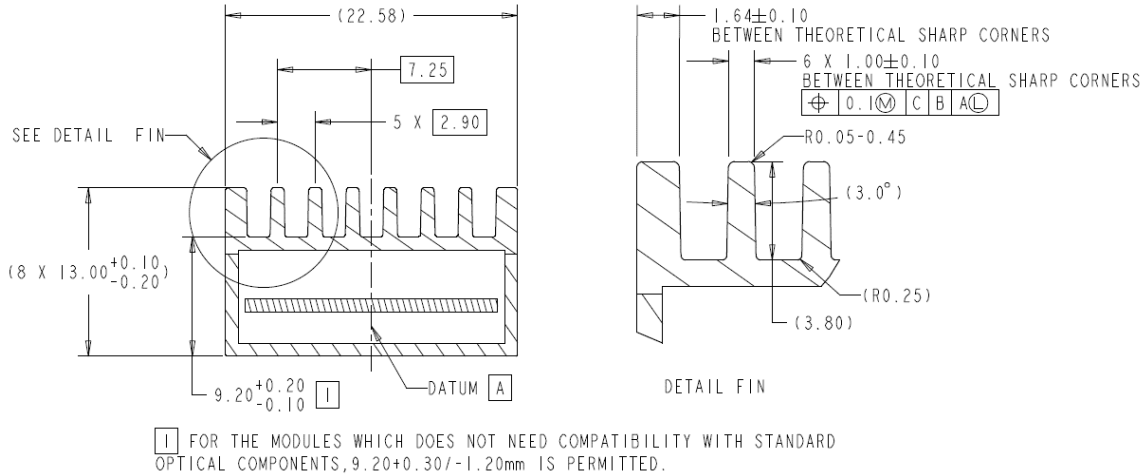


Figure 3-18: Heat sink fin pitch

The top and bottom internal EMI fingers are specified per this fin pitch, as depicted in Figure 4-8. It is possible to add airflow passages to the bottom of the module with this fin pitch for thermal management of high power modules.

3.5 Card-edge Design (Module Electrical Interface)

The OSFP module contains a PCB with contact pads (i.e. module PC board; paddle card) that mate with a connector as specified in Section 4.10 of this document. Critical dimensions for the contact pads are shown in Figure 3-19 through Figure 3-21. The contact pads on the PCB are designed for sequence mating during module insertion as follows:

- First mate: ground contacts
- Second mate: power contacts
- Third mate: signal contacts

During module removal, contact disconnects happen in reverse order of the above, e.g. signal contacts break first.

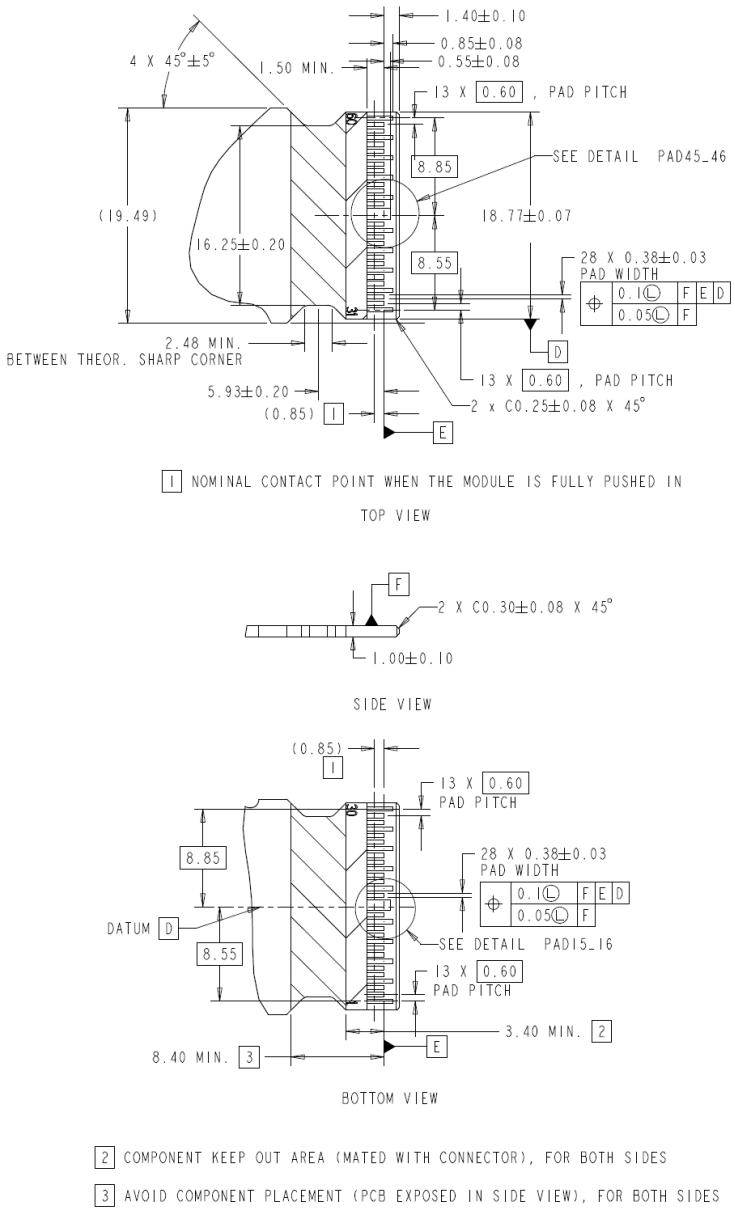


Figure 3-19: OSFP module pc board (card-edge)

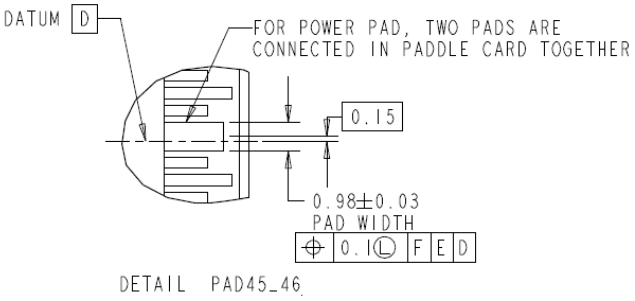


Figure 3-20: OSFP card-edge, detail of power pad (pads 45/46)

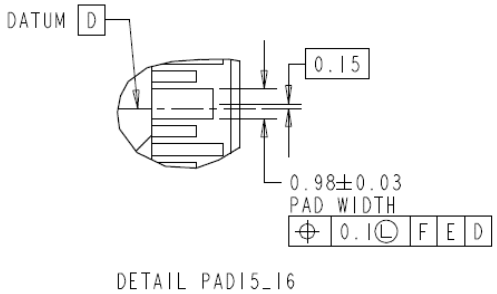


Figure 3-21: OSFP card-edge, detail of power pad (pads 15/16)

3.6 Contact Pad Plating Requirements

The contact pad plating shall meet the durability requirements of Section 7.1 and Section 7.2. The recommended plating specification is 0.762 µm minimum gold over 3.81 µm minimum nickel. Other plating systems are allowed provided they meet or exceed the requirements of Section 7.1 and 7.2.

3.7 Module Latch Feature

For latching, the module shall have latching pockets and a latch release mechanism at both sides as shown in Figure 3-22 to Figure 3-25. Dimensional details of the cage flap can be found in Figure 4-19 and Figure 4-20 .

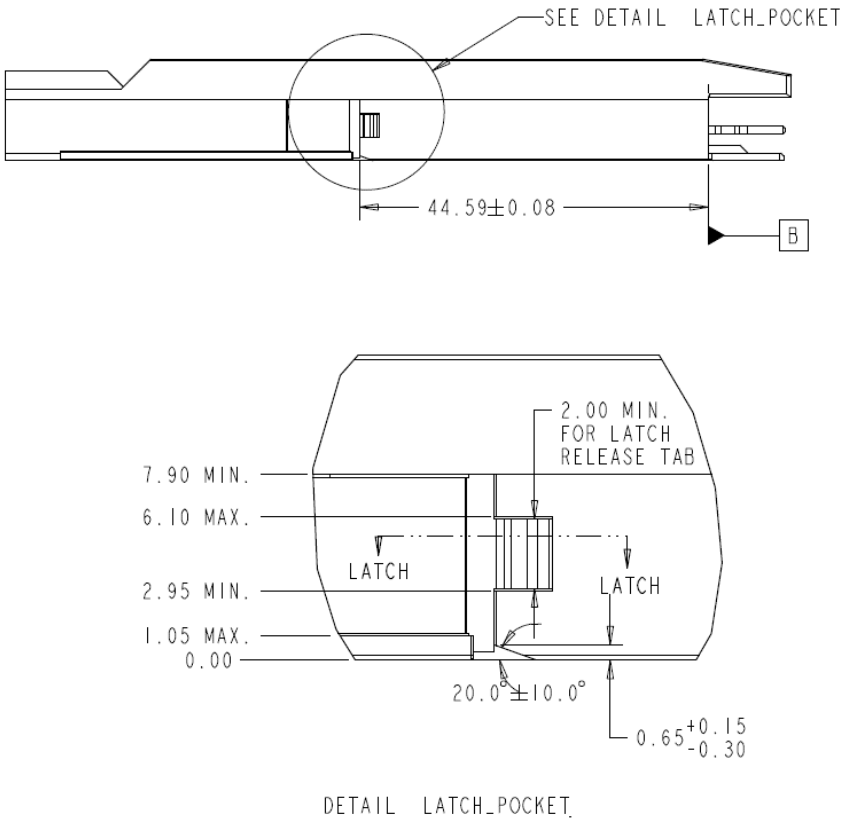


Figure 3-22: Latch pocket location

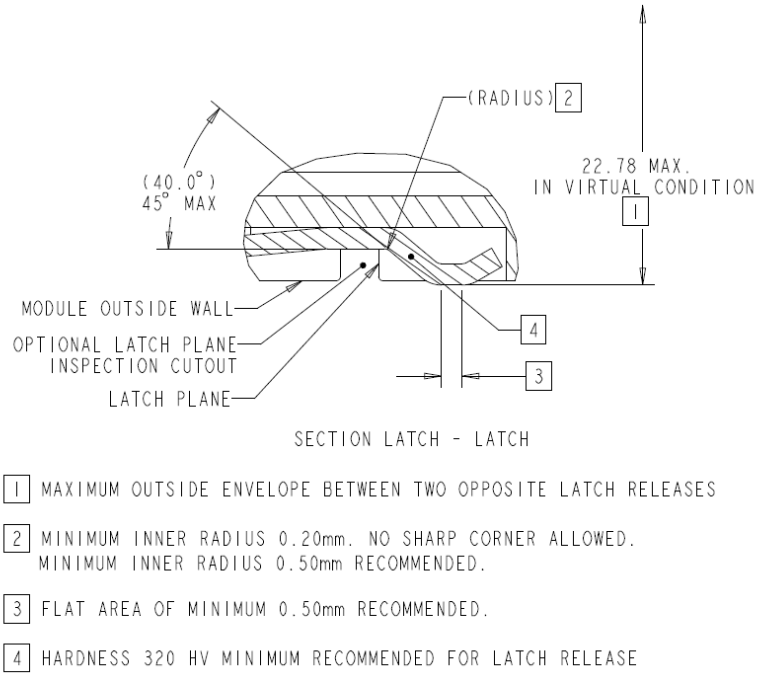


Figure 3-23: Latch release max width and latching pocket round

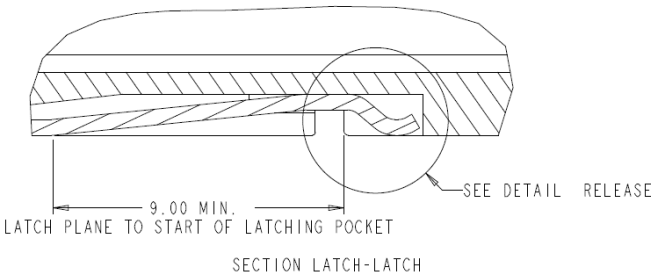


Figure 3-24: Latching pocket length

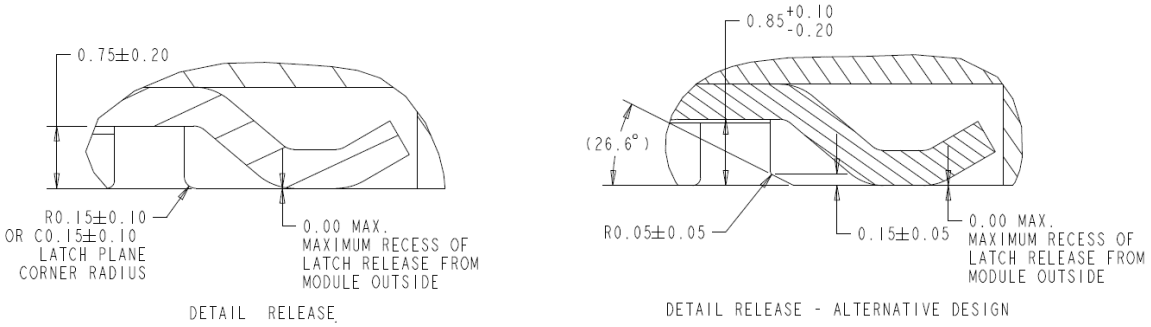


Figure 3-25: Latch plane corner radius and release details

In Figure 3-25, two reference designs are given. Different latch release design are allowed, as long as reliable latch release can be achieved.

3.8 Module Color Code

The module shall adhere to a color code by application of color to its pull-tab or other appropriate method. The color code to be applied is given in Table 3-3.

Table 3-3: OSFP color code

Product Type	Example PMD	Color	Pantone Code (Recommended)
OSFP copper cables	400G-CR8	Black	N/A
OSFP AOC Cables	400G-AOC	Grey	422U
OSFP 850nm solutions	400G-SR8, SR4.2	Beige	475U
OSFP 1310nm solutions for up to 500m	400G DR4	Yellow	107U
OSFP 1310nm solutions for up to 2km	400G FR4, FR8	Green	354C
OSFP 1310nm solutions for up to 10km	400G LR8	Blue	300U
OSFP 1310nm solutions for up to 40km	400G ER8	Red	1797U
OSFP 1550nm solutions for up to 80km	400G ZR8	White	N/A

3.9 Touch Temperature

Module surfaces outside of the cage must comply with applicable touch temperature requirements. If the temperature of the module case will exceed applicable short-term touch limits, then a means to prevent contact with the case during the handling of the module shall be provided. Refer to UL 62368-1 and NEBS GR-63.

4 Single Row Surface Mount Technology OSFP Connector and Its Cage: Mechanical Specification

In this section, the configuration of a single row SMT (Surface Mount Technology) connector and its cage are presented.

4.1 Overview

Figure 4-1 gives an overview of a 1x1 and 1x4 cage without modules installed. Figure 4-2 depicts a 1x1 cage with an OSFP module in the fully inserted position.

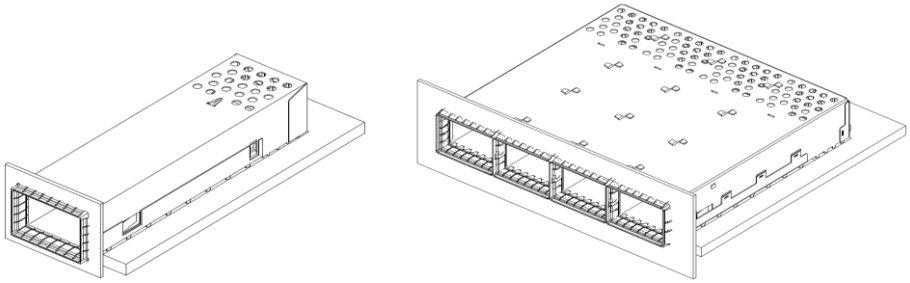


Figure 4-1: 1x1 and 1x4 cage, host PCB and panel

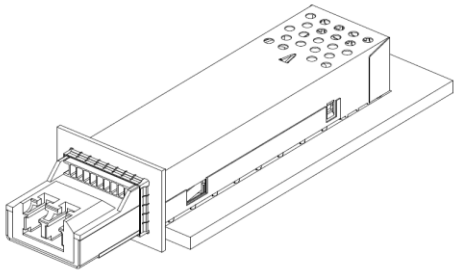


Figure 4-2: OSFP module in a 1x1 cage

In the cage and connector mechanical drawings included throughout this specification, the datum as defined in Table 4-1 shall apply. For datum of the module, see Table 3-1.

Table 4-1: Descriptions of the cage and connector mechanical datum

Designator	Description	Figure
G	Forward stop of Cage	Figure 4-3
H	Seating plane of Cage on host pc board	Figure 4-3
J	Width of inside of Cage	Figure 4-4
K	Connector guide post #1	Figure 4-6; Figure 4-23
L	Cage Pin #1	Figure 4-3
M	Top surface of host pc board	Figure 4-14
N	Host pc board through hole #1 to accept Connector guide post	Figure 4-14
P	Host pc board through hole #2 to accept Connector guide post	Figure 4-15
R	Host pc board through hole #1 to accept Cage Pin	Figure 4-15
S	Width of Connector	Figure 4-23
T	Front surface of Connector	Figure 4-23
U	Seating plane of Connector	Figure 4-23

4.2 Cage Dimensions and Positioning Pin

Figure 4-3 through Figure 4-5 shows cage datum, positioning pin, port size and cage height. In addition, Figure 4-6 shows nominal dimensions between the module and the cage when

the module is fully inserted. Note that the compliant pins in the cage are placed to support belly-to-belly applications. For ganged cages, some compliant pins shall be shorter to support the belly-to-belly application properly. Figure 4-7 shows the length of the compliant pins for a 1x4 cage. Figure 4-17 shows the host PCB board layout for a 1x4 cage.

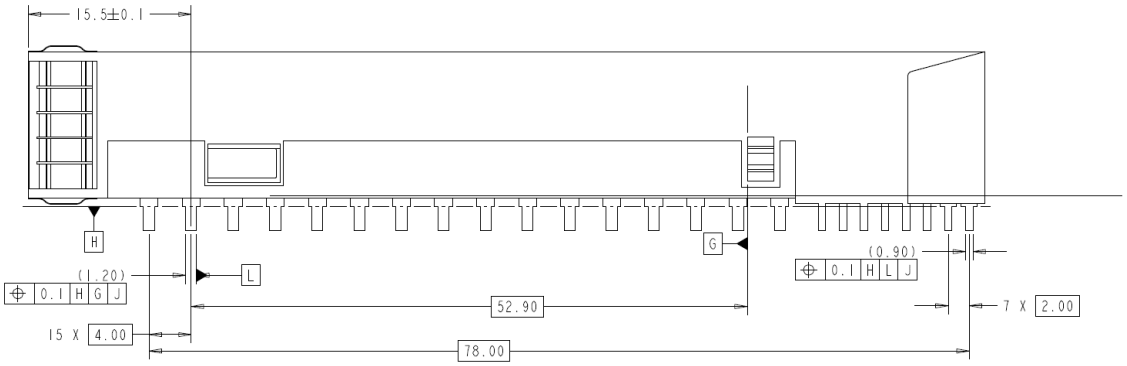


Figure 4-3: Cage positioning pins and forward stop

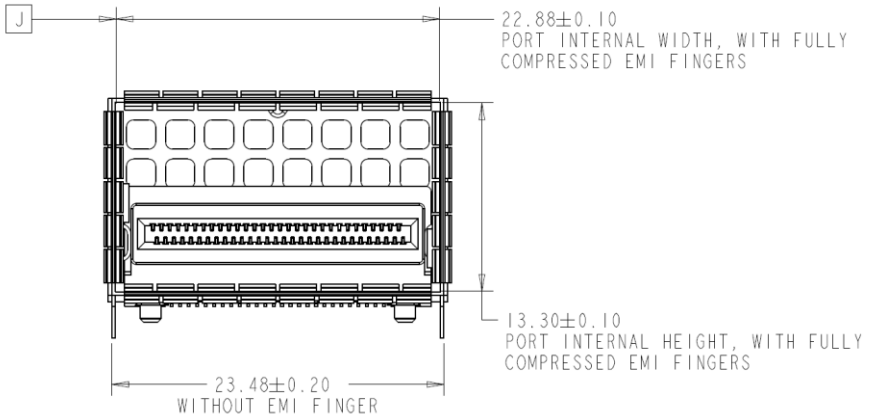


Figure 4-4: Port internal width and height

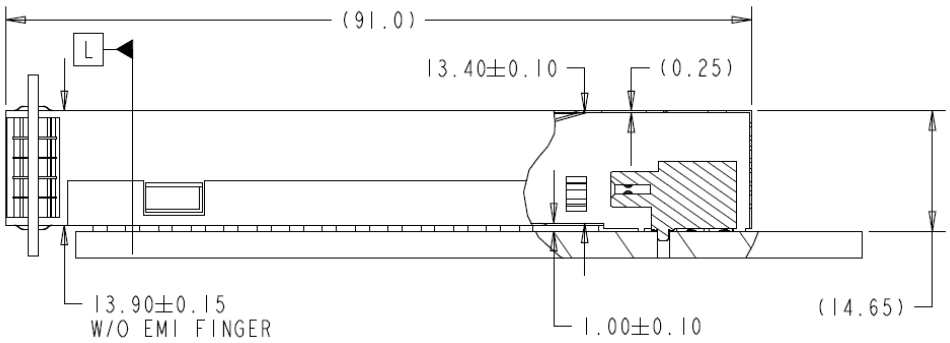
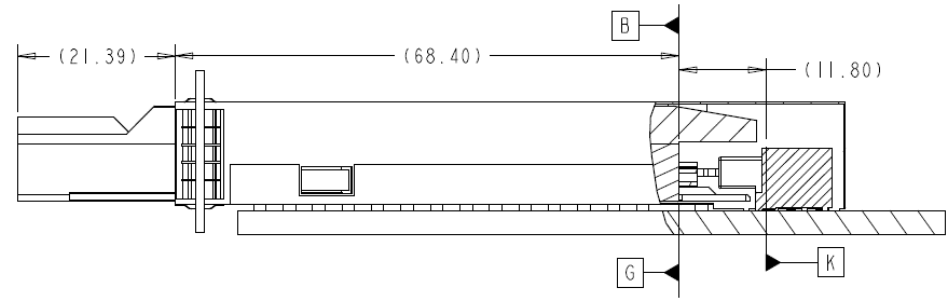


Figure 4-5: Side view of a 1x1 cage with vertical cage dimensions



DATUM B: MODULE FORWARD STOP
DATUM G: CAGE FORWARD STOP
DATUM K: CONNECTOR GUIDE POST

THIS FIGURE SHOWS THE DATUM ALIGNMENT BETWEEN CONNECTOR, CAGE AND MODULE AND ALSO SHOWS THE REFERENCE DIMENSION OF THE MODULE INSIDE CAGE, WHEN THE MODULE IS FULLY PUSHED IN.

Figure 4-6: Side view of a 1x1 cage with axial reference dimensions

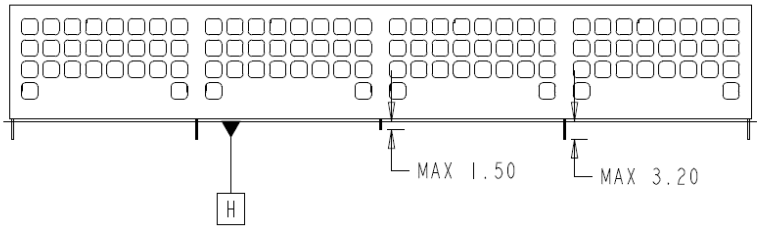


Figure 4-7: Length of the compliant pins into the board, for belly-to-belly application

4.3 EMI Finger Pitches

Figure 4-8 gives EMI finger dimensions to be used for the internal side of top and bottom EMI fingers. These pitches are designed such that the OSFP module as described in Section 3.4 is compatible. Fingers for the left, right, and outside of the cage shall be designed to ensure appropriate EMI shielding, but finger pitch is not specified. This EMI finger pitch specification shall be applied to the stacked SMT cage (Section 5) and stacked press-fit cage (Section 6).

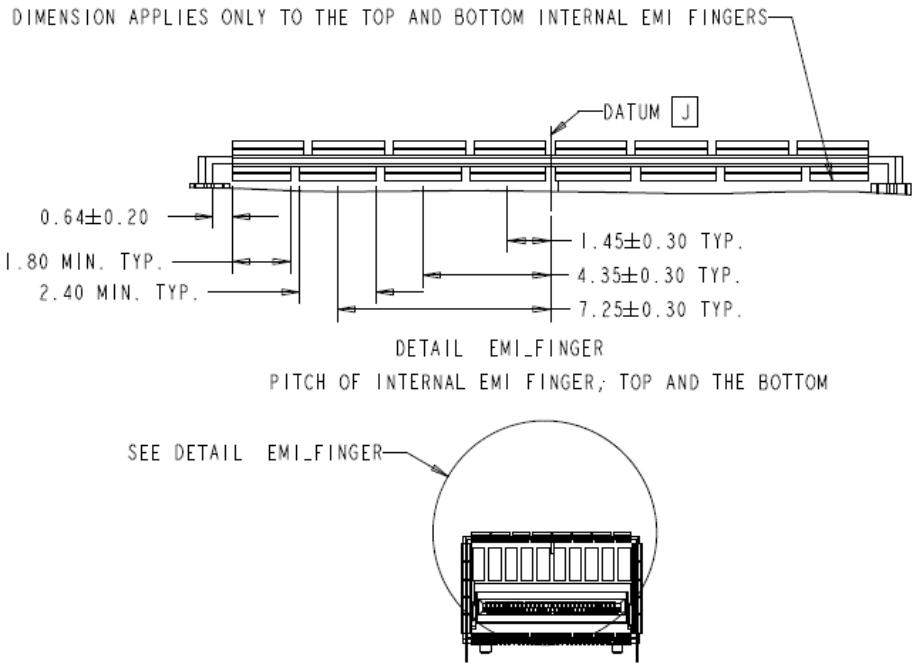


Figure 4-8: Internal EMI finger, top and bottom

4.4 Ventilation Hole, Key and Stop

Figure 4-9 shows the key and forward stop features. The keying feature will prevent the module from being inserted upside down.

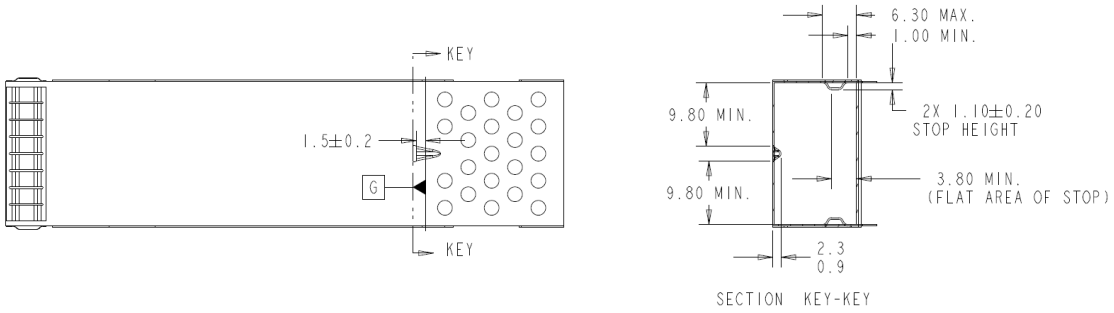


Figure 4-9: Key and stop

The cage should have ventilation holes to allow airflow. Refer to Figure 4-10 and Figure 4-11 for examples of ventilation hole details.

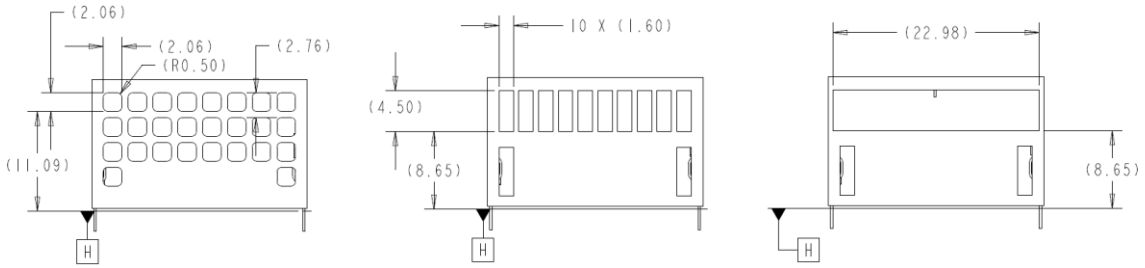


Figure 4-10: Rear ventilation holes, three example designs

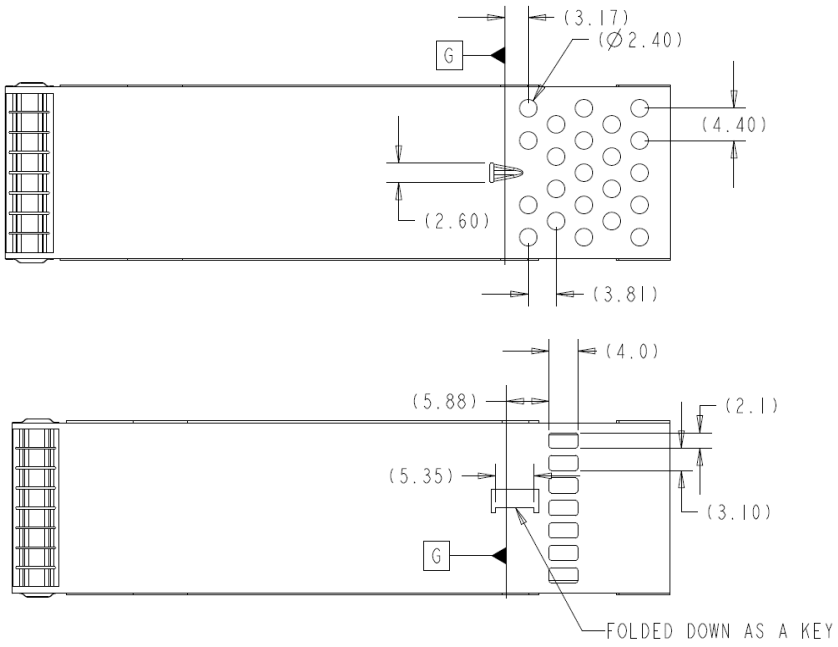


Figure 4-11: Top ventilation holes, two example designs

4.5 Riding Heatsink

An OSFP cage may have a riding heatsink. Figure 4-12 shows the cutout size of the cage for the riding heatsink. Figure 4-13 shows the reference design of the leading edge of a riding heatsink. The force which will be applied from the riding heat sink to an OSFP module shall not exceed 36N downward.

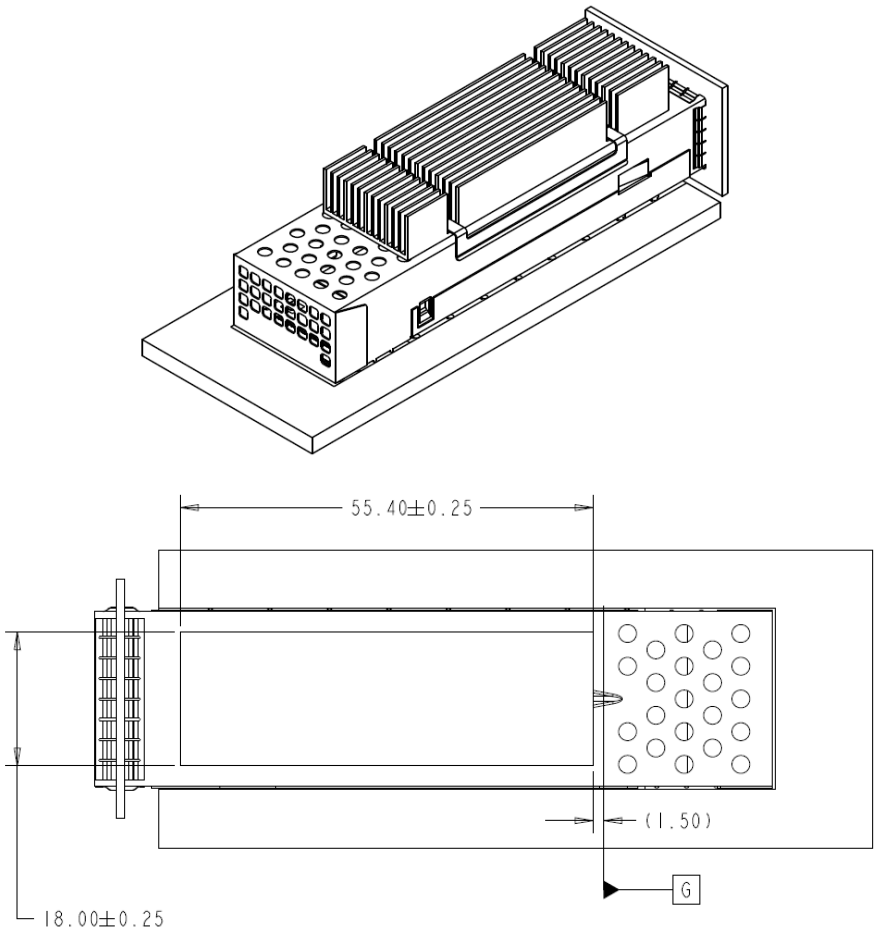


Figure 4-12: OSFP with a riding heatsink (above) and cutout on the cage for a riding heatsink in OSFP (bottom)

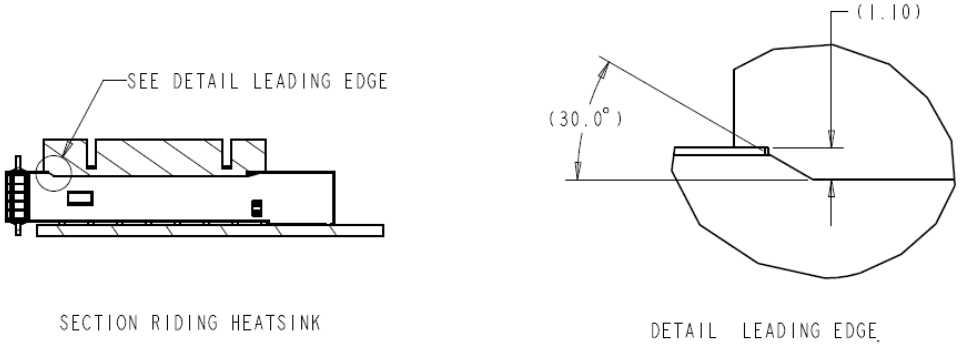


Figure 4-13: Heat sink leading edge, reference design

4.6 Host PCB Layout – 1x1 Cage

The host PCB layout pattern to accept a 1x1 cage is detailed in Figure 4-14 through Figure 4-16.

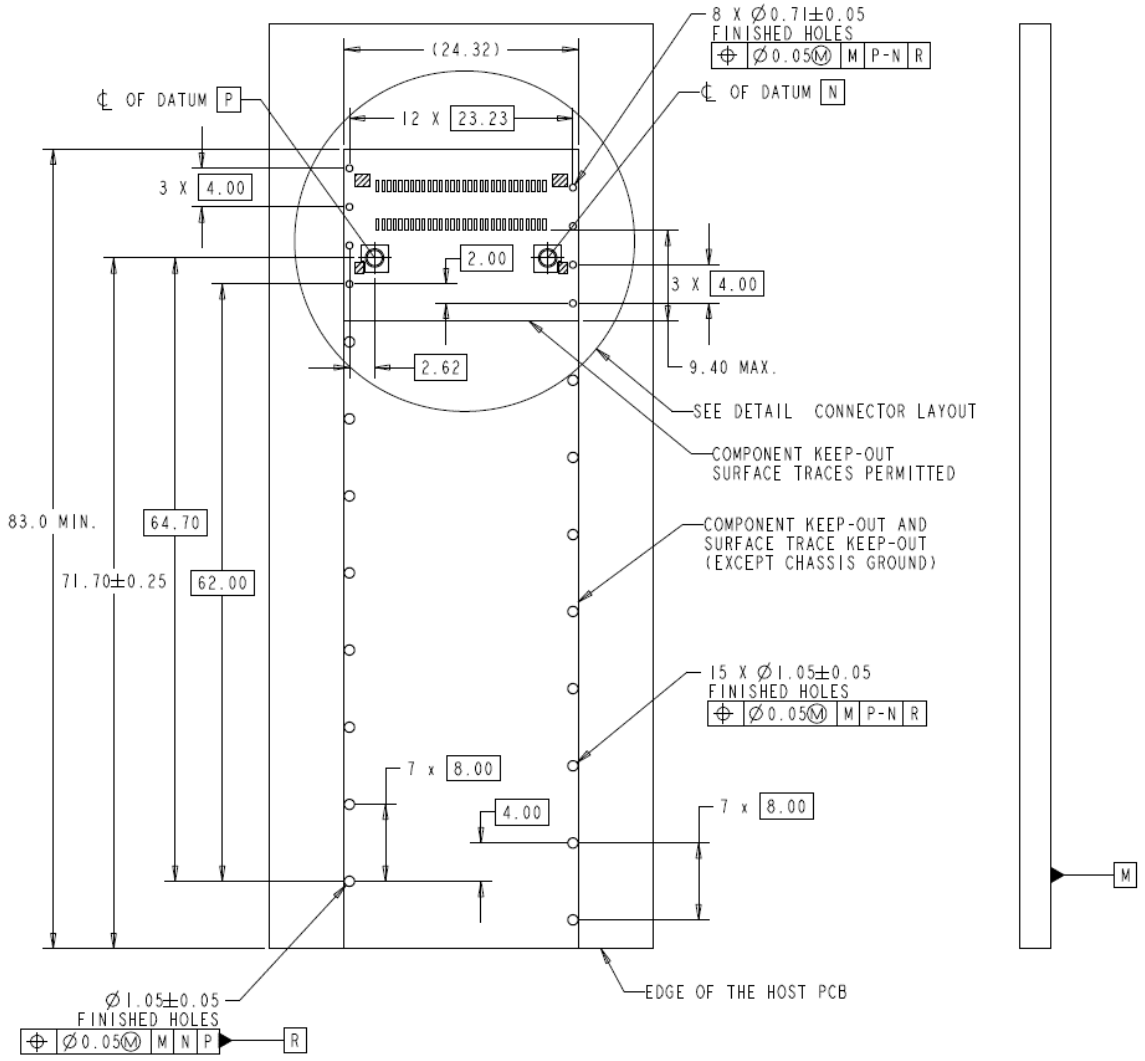


Figure 4-14: Host PCB layout for 1x1 cage

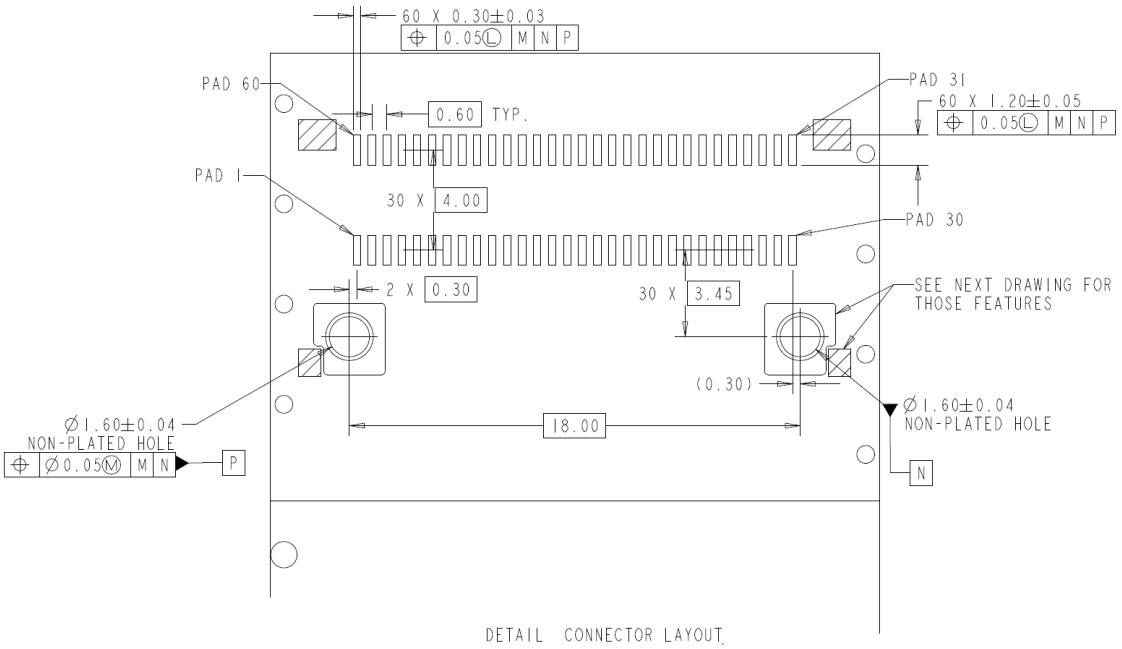


Figure 4-15: Host PCB layout, details

Figure 4-16 shows keep out areas and optional solder rings. The solder rings are for SMT belly-to-belly applications, thus applying solder to the area is optional. The keep out areas are there in order to prevent interference with the connector in Figure 4-23. The keep out areas should be kept in the layout in all cases regardless of whether solder is applied to the optional solder ring area.

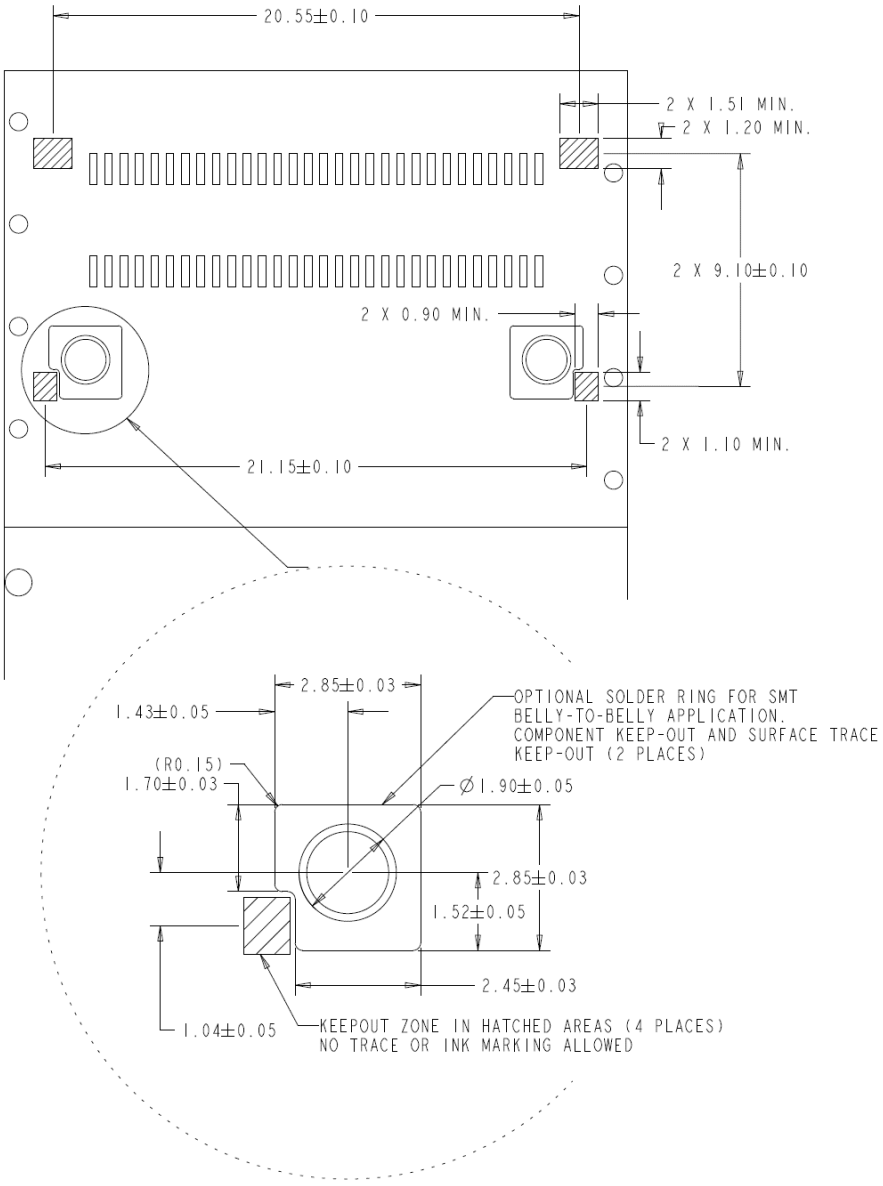


Figure 4-16: Solder ring for belly-to-belly application

4.7 Host PCB Layout – 1x4 Cage

For a 1x4 cage, the host PCB layout shall have a 23.23mm horizontal pitch from cage-to-cage as in Figure 4-17.

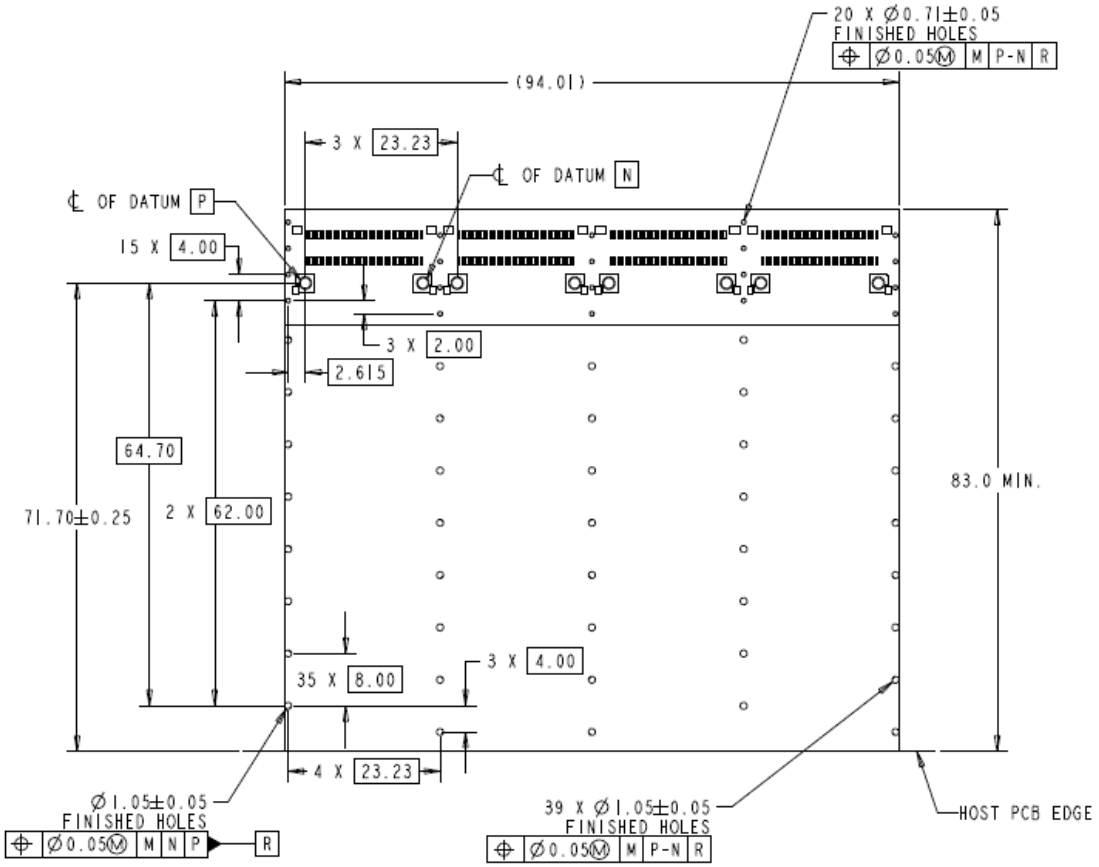


Figure 4-17: Host PCB layout for 1x4 cage

Figure 4-18 compares the host PCB layout between the 1x1, 1x2 and 1x4. The details of the 1x2 PCB layout are not given in this document.

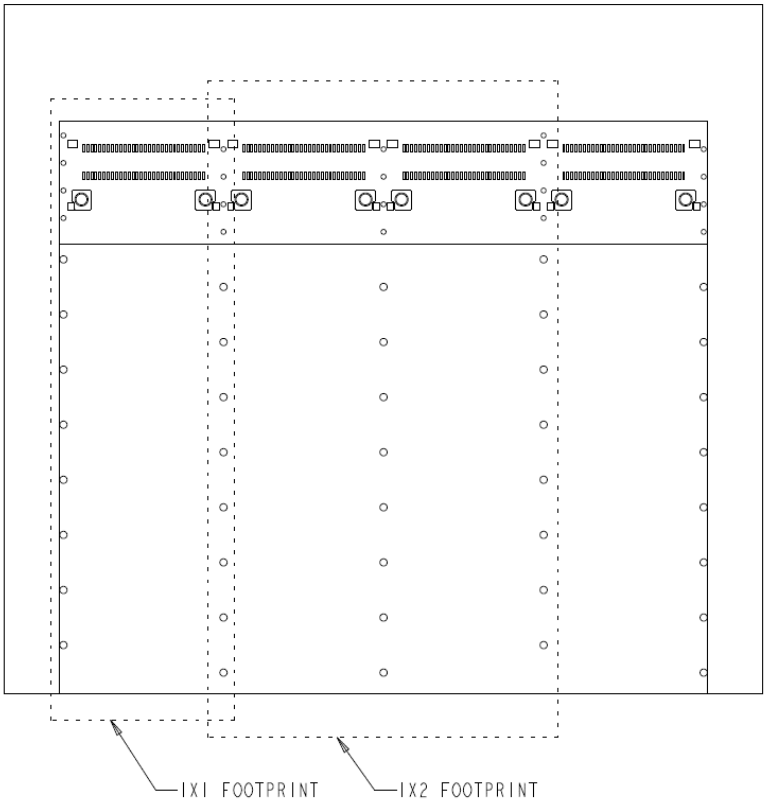


Figure 4-18: Comparison of host PCB layout between 1x1, 1x2 and 1x4

4.8 Latch Flaps in Cage

In the cage, flaps as shown in Figure 4-19 and Figure 4-20 shall be on both sides of the cage to latch the module into the cage. Flaps are shown in a 1x1 cage but can be applied

to a ganged cage such as a 1x4 cage or any 1xN cage. The dimension 44.80±0.08mm, cage latch to module stop, applies when the module is in mated condition.

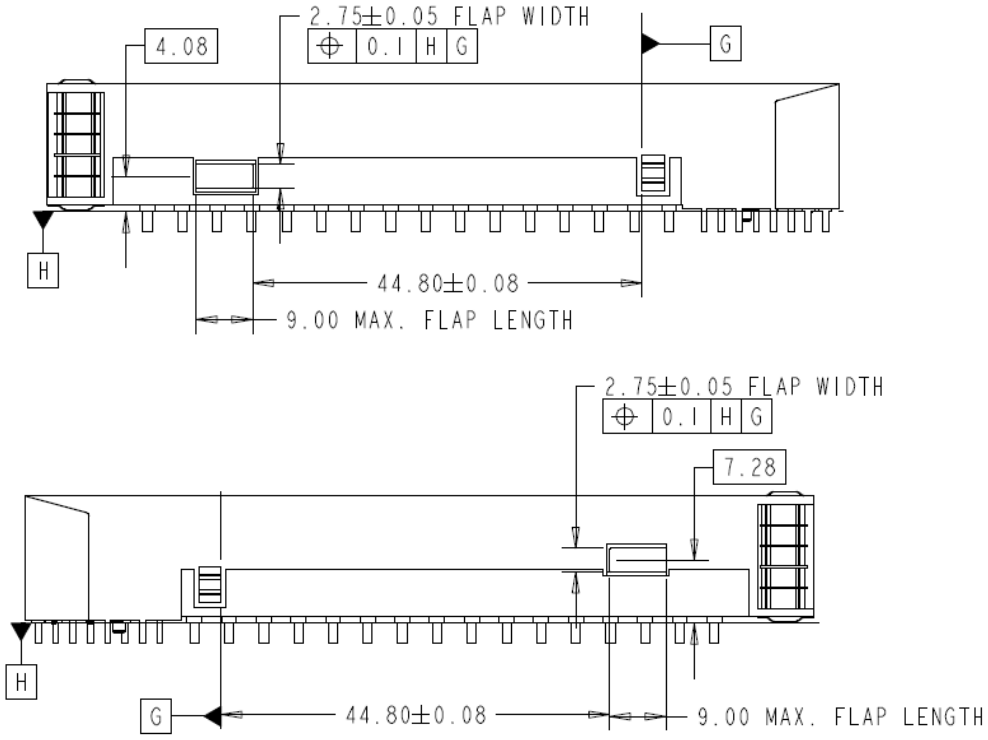


Figure 4-19: Latch feature, left and right side

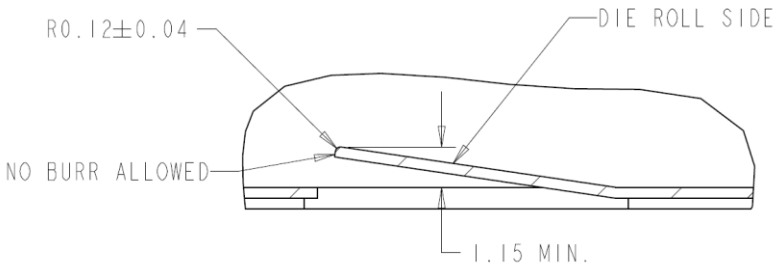


Figure 4-20: Latch flap, cross-sectional view from top

4.9 Bezel Panel Cut-Out

The EMI spring fingers of the cage shall make contact to the inside of the bezel panel cut out in order to make ground contact. Figure 4-21 and Figure 4-22 show recommended dimensions of the bezel panel cut-out. As the horizontal pitch of the cage is 23.23mm, the bezel cut out width of 1x2 shall be 47.51mm while the detailed design is not depicted here.

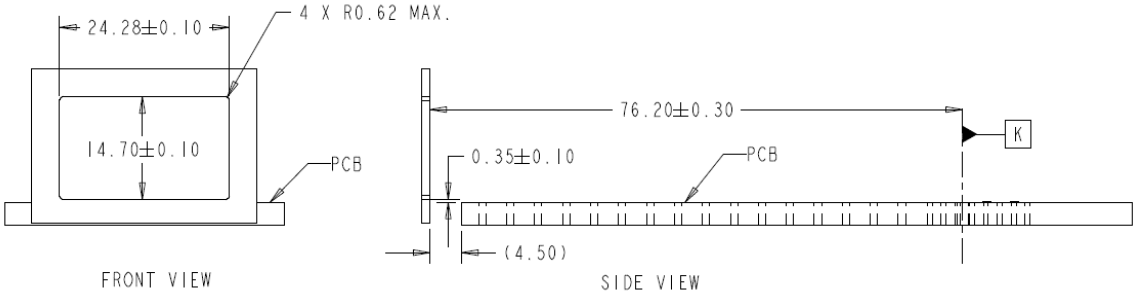


Figure 4-21: Bezel design and location for 1x1 cage

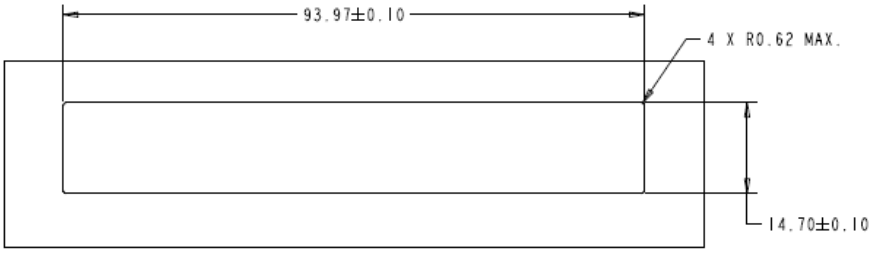


Figure 4-22: Bezel design for 1x4 cage

4.10 Single Row SMT Connector

The electrical connector shall have the following dimensions to properly receive the module as well as allowing for air to pass over the module to the outside. The tail direction of the connector is specified as shown.

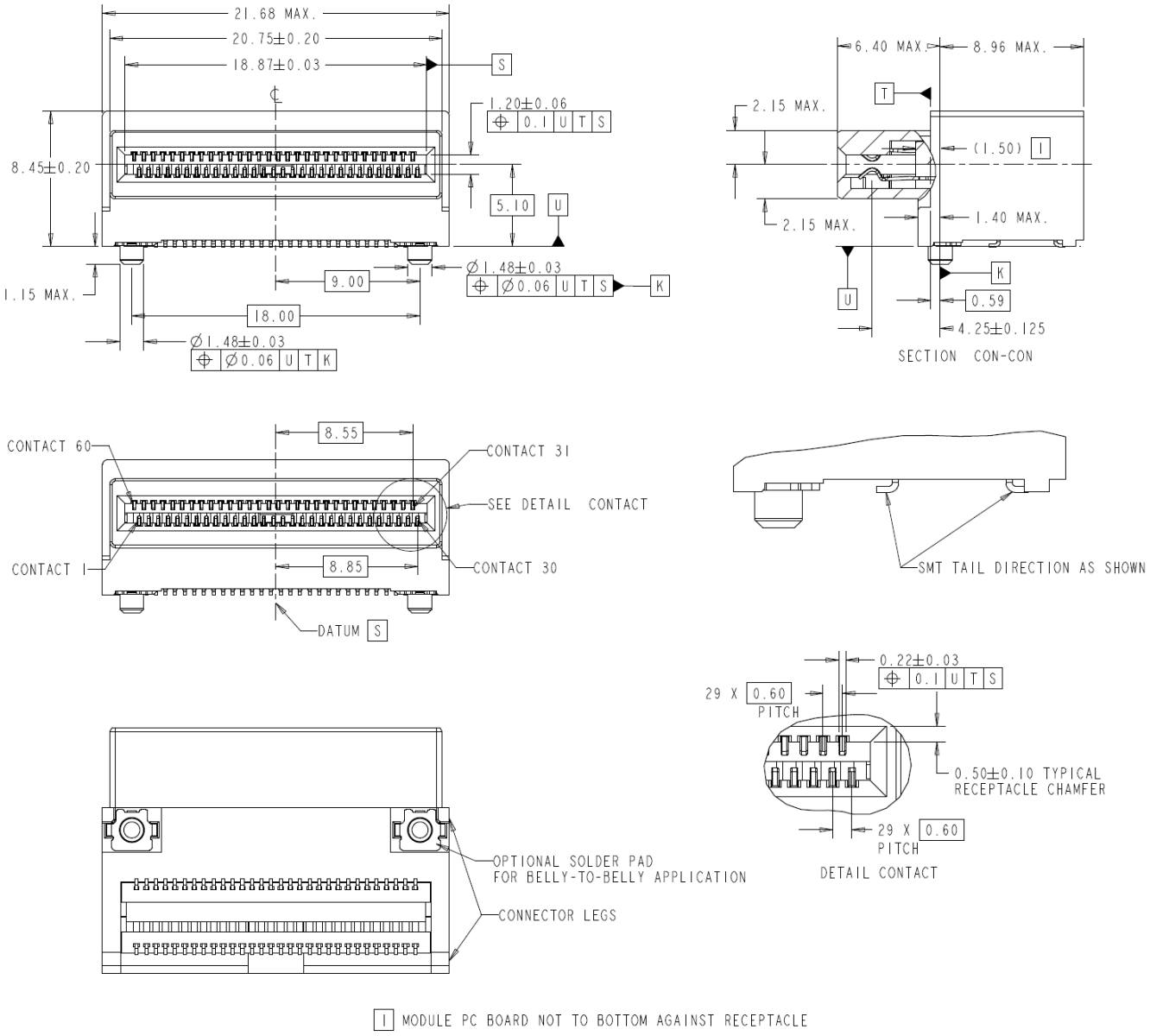


Figure 4-23: Surface mount connector

4.11 Blank Plug

Any unused or empty port of a cage shall have a blank plug. The blank plug shall serve to minimize EMI while at the same time allowing for a maximum airflow no more than that of a module. See Figure 4-24 for a recommended design. Blank plug shall be used on the stacked SMT (Section 5) and Stacked press-fit cage (Section 6).

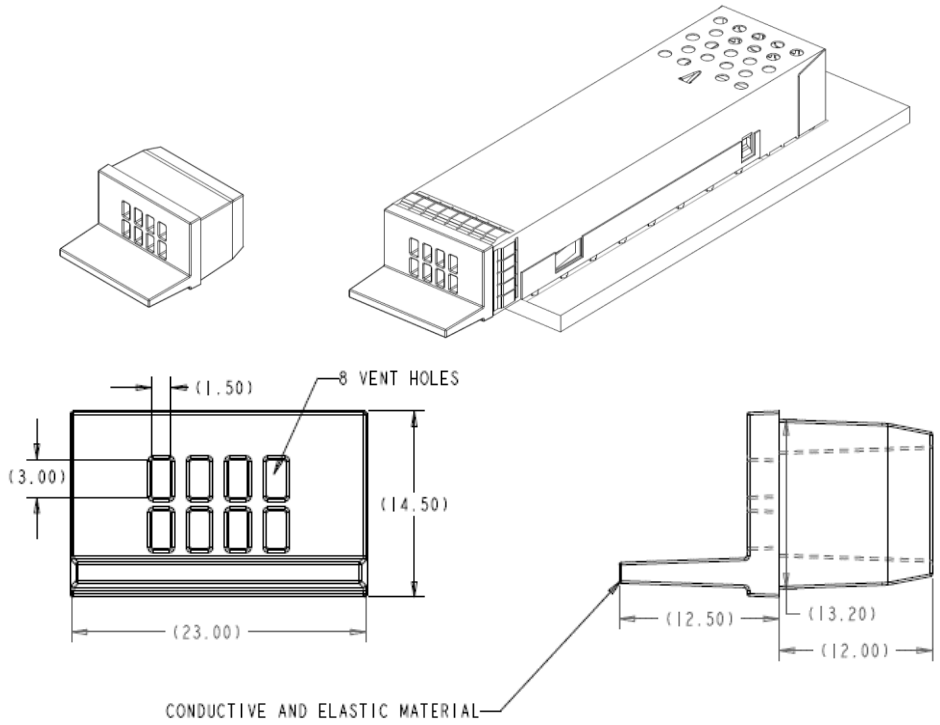


Figure 4-24: OSFP blank plug (reference design)

5 Stacked Surface Mount Technology Connector and Its Cage

In this section, the configuration of stacked SMT connector and cage are presented. Note that the stacked SMT connector and cage is compatible only with Type 1 and Type 2 OSFP modules, not with Type 3 OSFP module as in the Figure 3-3.

5.1 Overview

Figure 5-1 gives an overview of a 2x1 SMT connector, cage, host PCB and the panel.

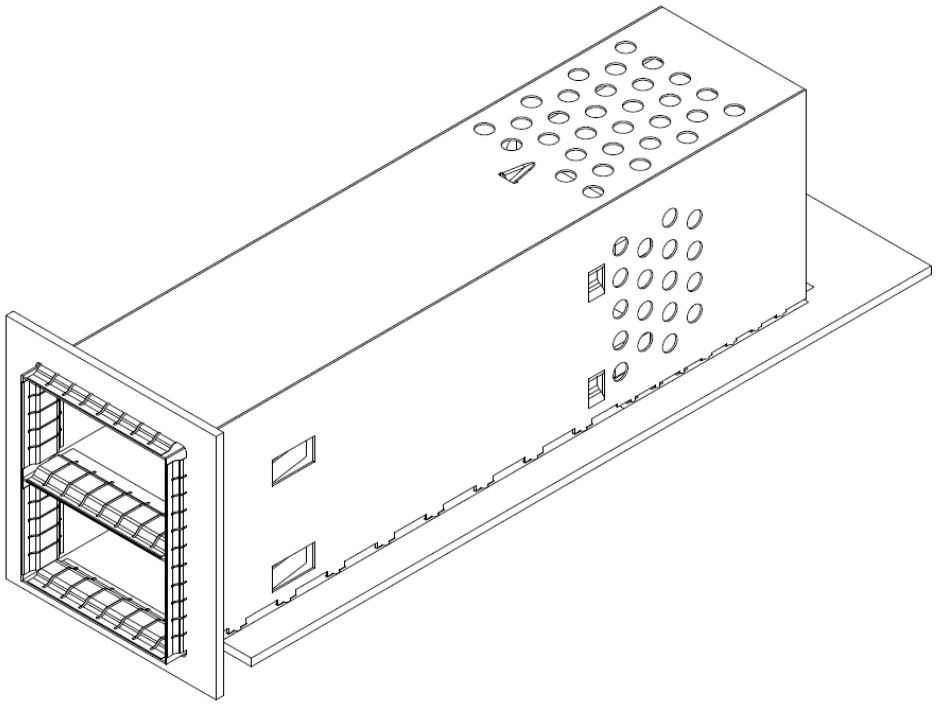


Figure 5-1: Stacked SMT 2x1 cage with host PCB and the panel

In the mechanical drawings of this section, the datum as defined in Table 5-1 shall apply. Note that the same designators are used for the corresponding features of the single row SMT connector and its cage, as in Table 4-1.

Table 5-1: Descriptions of the Stacked SMT cage and connector mechanical datum

Designator	Description	Figure
G	Forward stop of Cage	Figure 5-2
H	Seating plane of Cage on host pc board	Figure 5-2
J	Width of inside of Cage	Figure 5-3
K	Connector guide post #1	Figure 5-18
L	Cage Pin #1	Figure 5-2
M	Top surface of host pc board	Figure 5-9
N	Host pc board through hole #1 to accept Connector guide post	Figure 5-9
P	Host pc board through hole #2 to accept Connector guide post	Figure 5-9
R	Host pc board through hole #1 to accept Cage Pin	Figure 5-9
U	Seating plane of Connector	Figure 5-18

Latch, stop and keying features of the cage are not specified in the mechanical drawings in this section. For those features, the same specification as the single row SMT connector and its cage in section 4 shall apply.

5.2 Cage Dimensions and Positioning Pin

Figure 5-2 through Figure 5-4 show cage datum, positioning pin, port size, and cage height. Figure 5-5 shows that the middle row compliance pins in the 1x4 cage should be shorter than the others to support belly-to-belly applications.

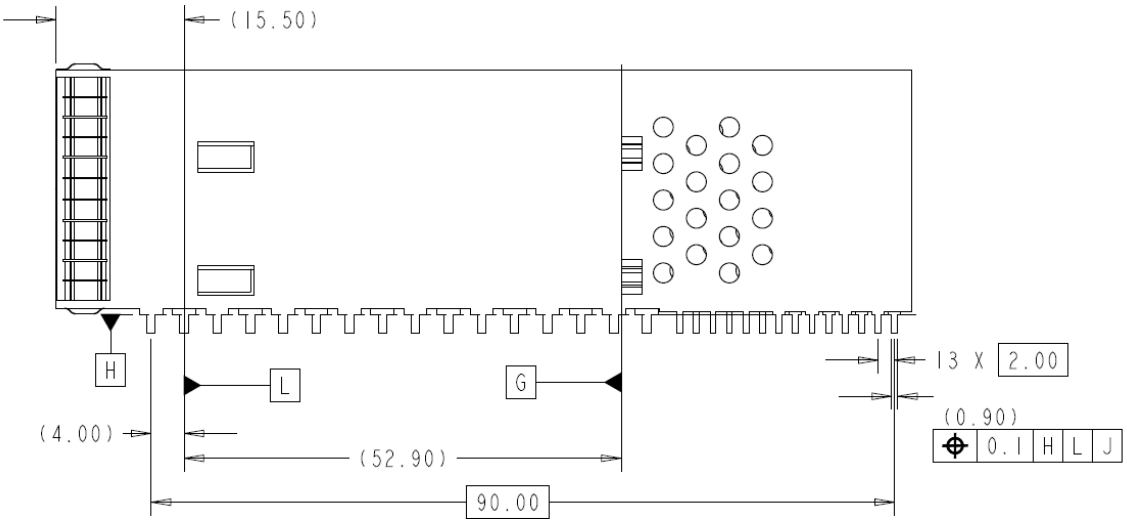


Figure 5-2: Cage positioning pins and forward stop

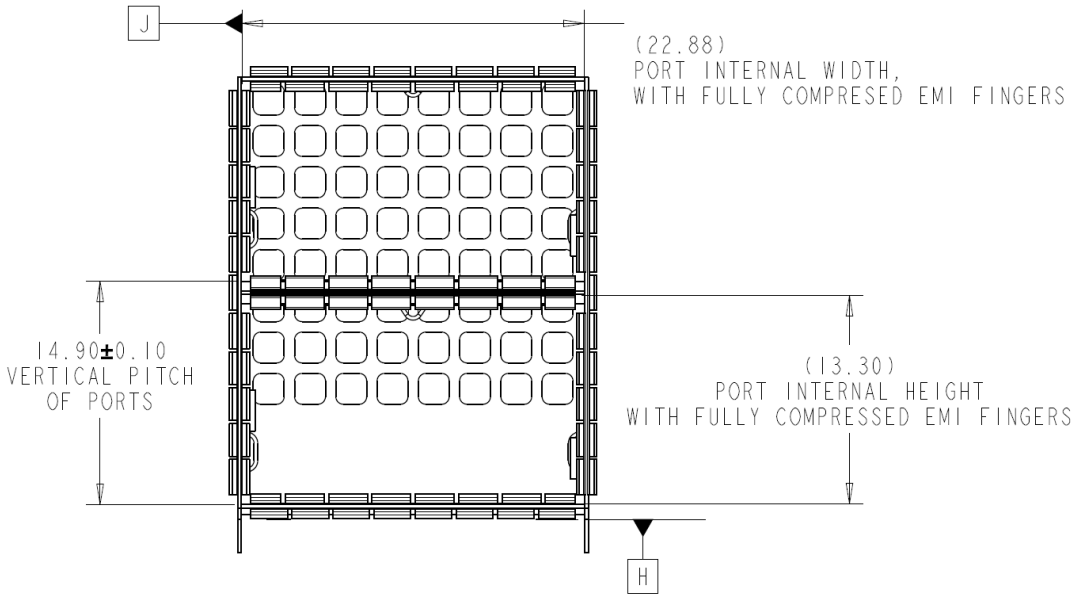


Figure 5-3: Port internal width, height and vertical pitch

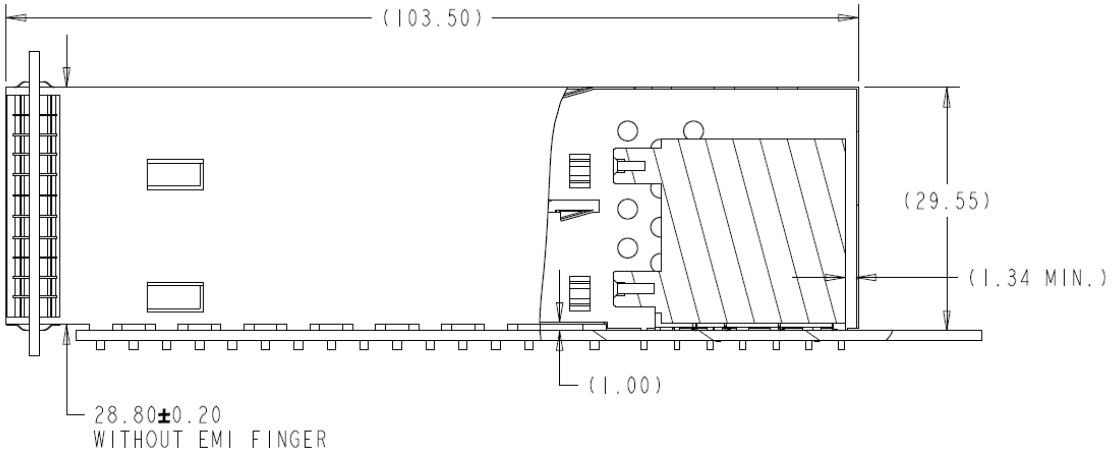


Figure 5-4: Side view of 2x1 cage with vertical cage dimensions

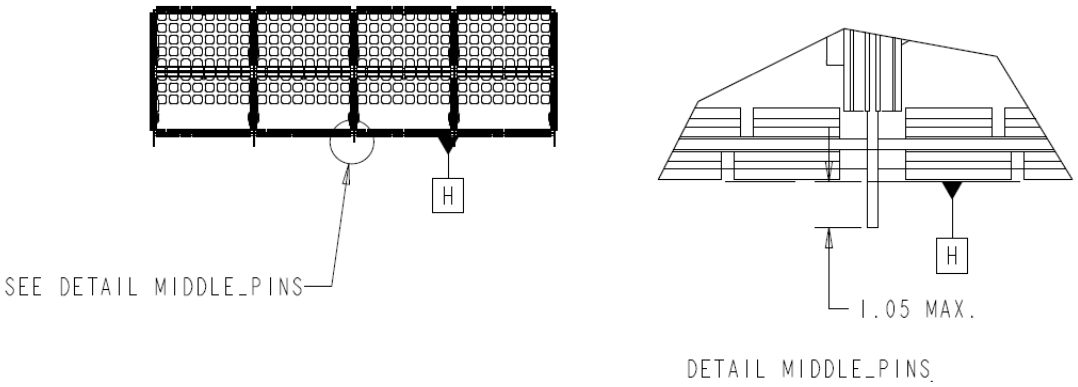


Figure 5-5: Length of the compliance pins at the middle, for belly-to-belly applications

5.3 Ventilation Holes

Cage should have ventilation holes to allow sufficient airflow. Figure 5-6, Figure 5-7 and Figure 5-8 show an example design.

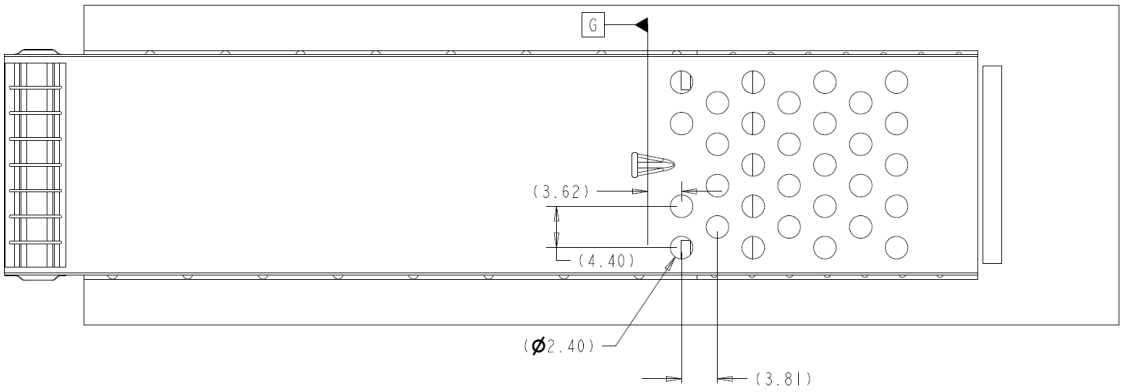


Figure 5-6: Top ventilation, example design

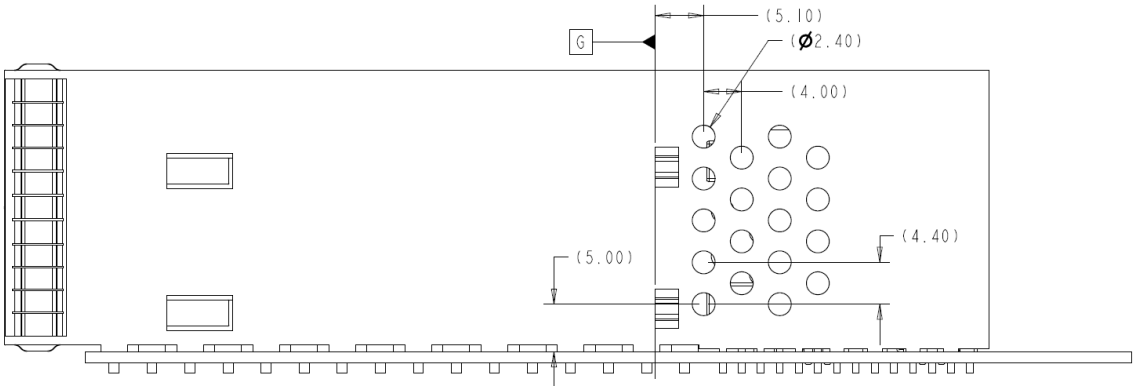


Figure 5-7: Side ventilation, example design

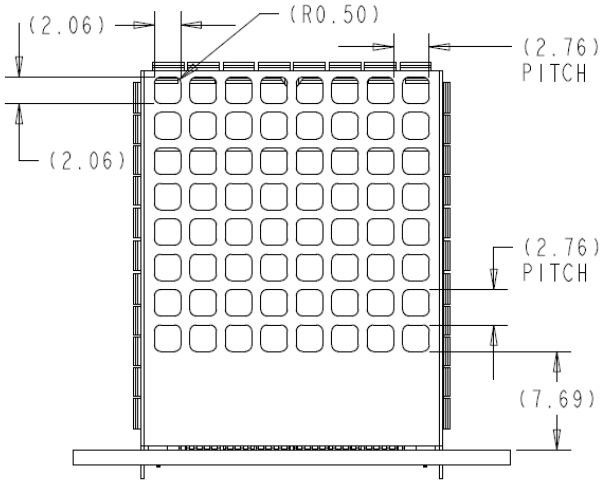


Figure 5-8: Rear ventilation, example design

5.4 Host PCB Layout – 2x1 Cage

The host PCB layout pattern for 2x1 SMT connector and cage are presented in this section. Note that pads 1 to 60 correspond to pins 1 to 60 of the OSFP in the lower port as in Figure 11-1, while pads 61 to 120 correspond to pins 1 to 60 of the OSFP in the upper port.

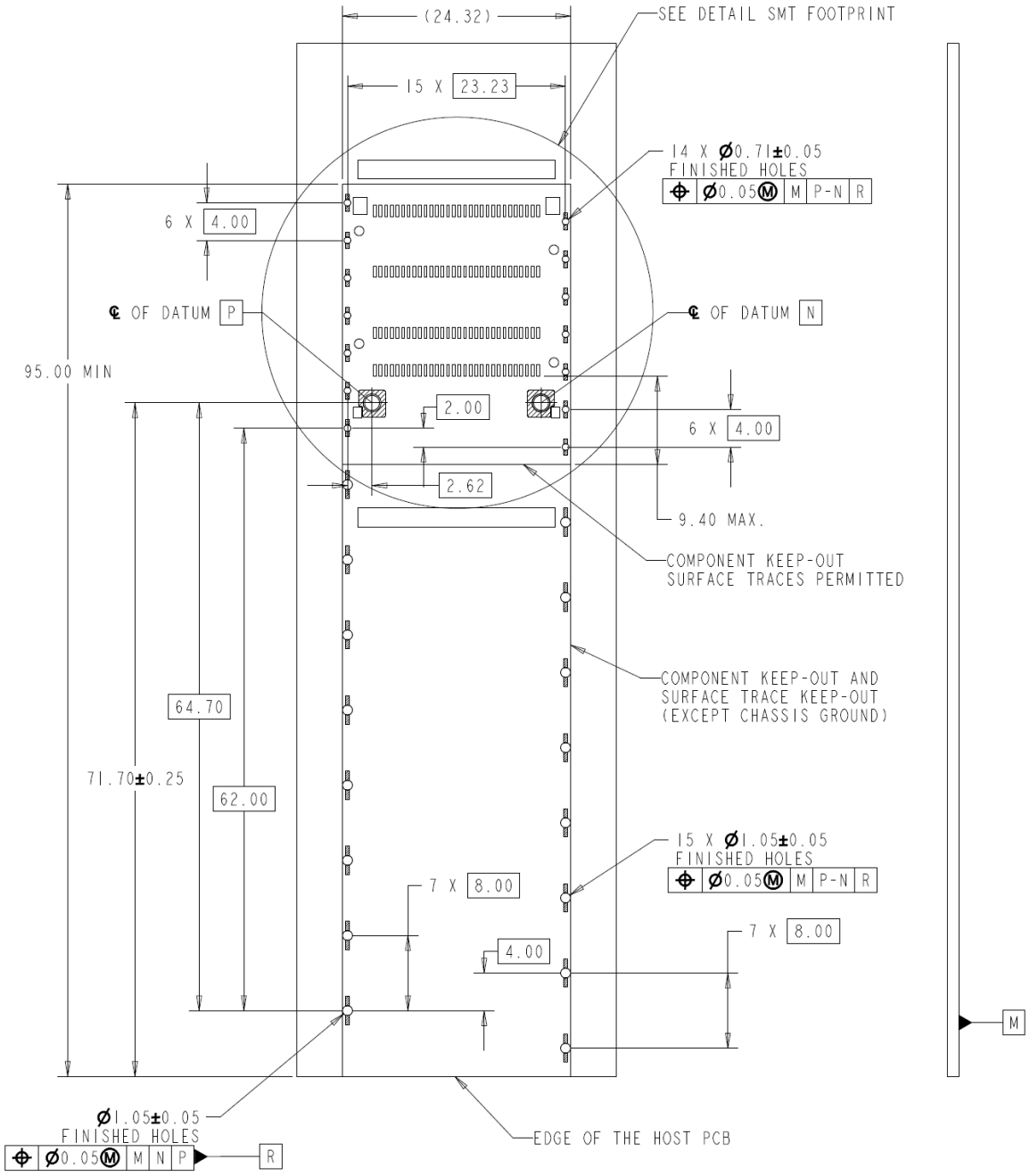


Figure 5-9: Host PCB Layout for 2x1 SMT cage

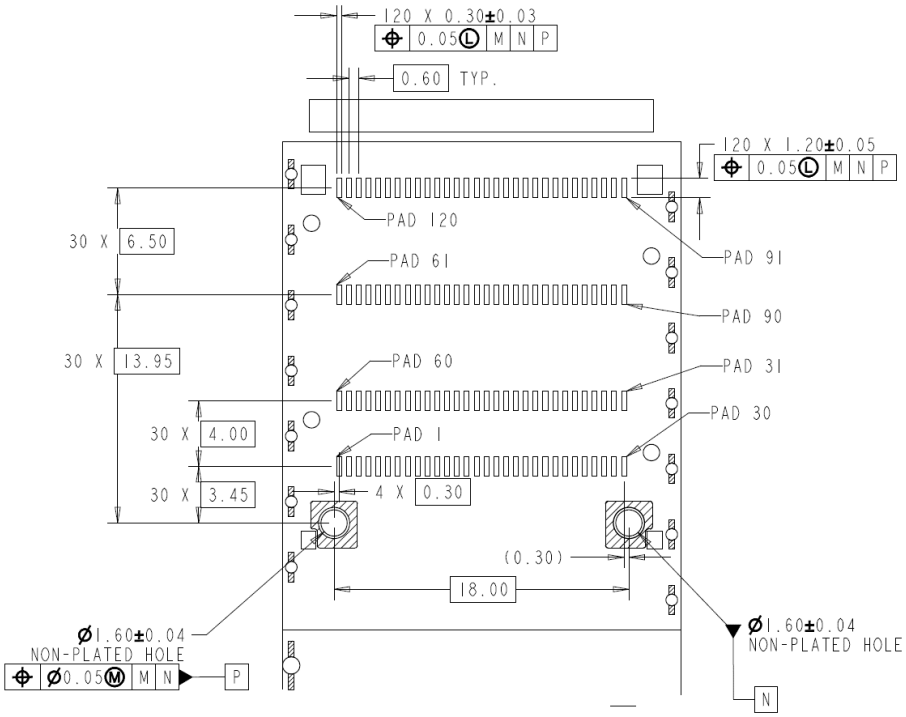


Figure 5-10: Host PCB layout, details

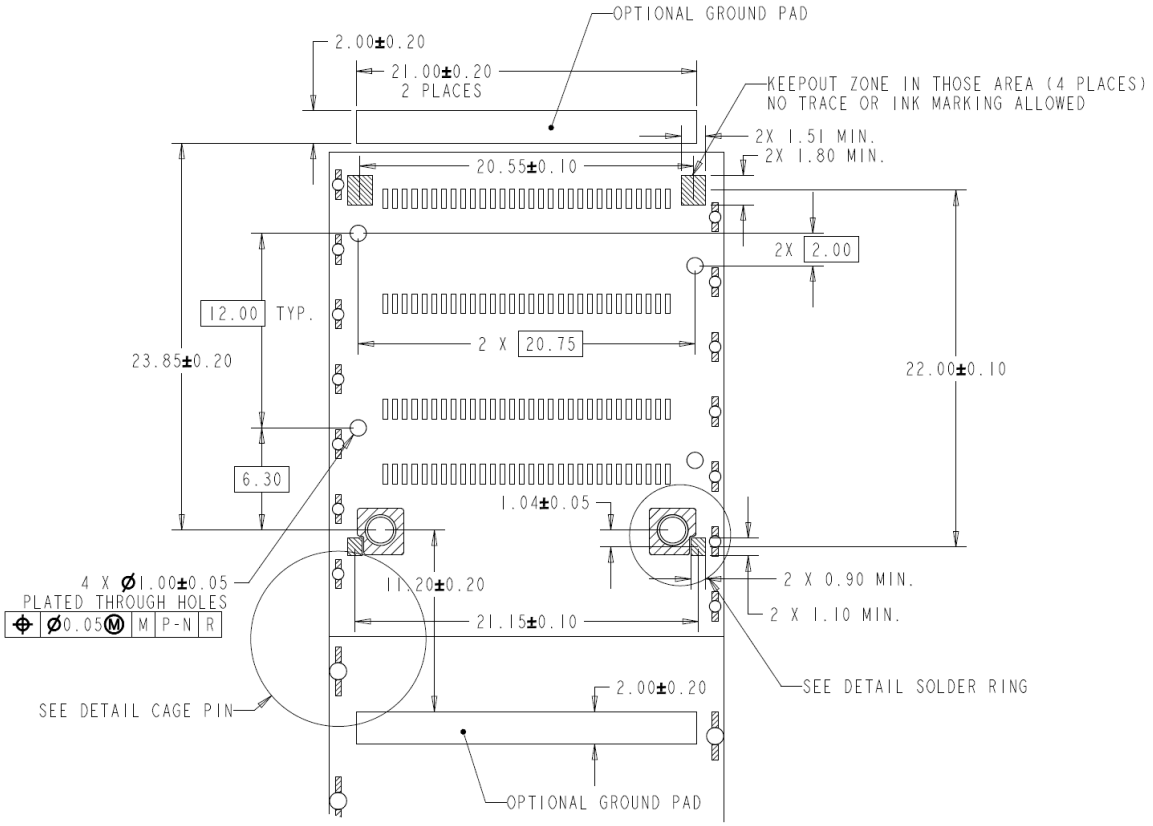


Figure 5-11: Layout for peg, retaining feature and ground pad

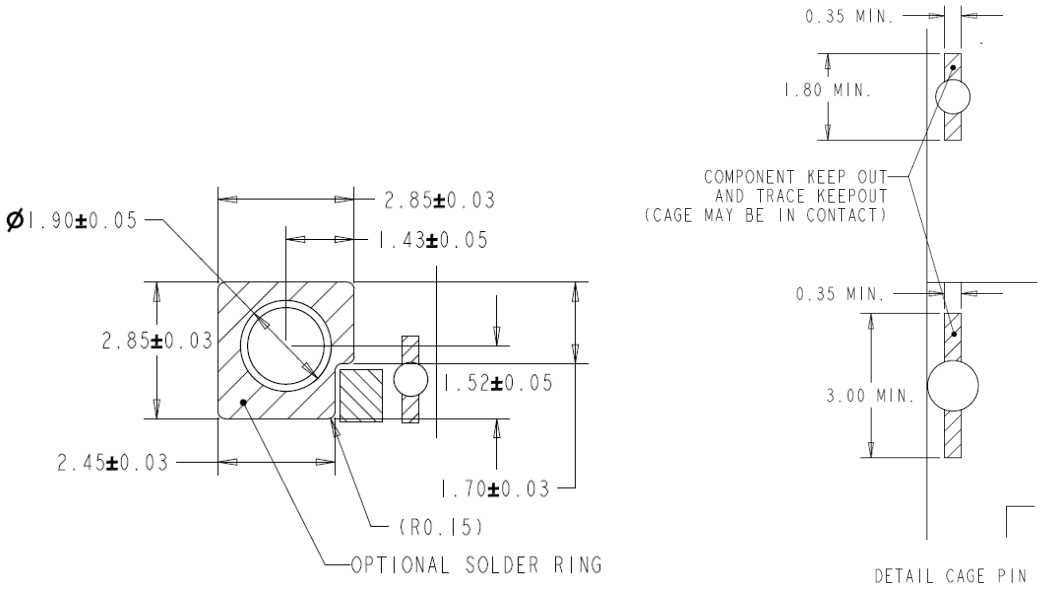


Figure 5-12*: Details of optional solder ring (left) and cage pin keepout (right)*

5.5 Host PCB Layout – 2x4 Cage

In this section, host PCB layout for the ganged cage is presented in a 2x4 cage host layout. Figure 5-14 shows the comparison of 2x1, 2x2 and 2x4, while the detailed layout specification of the 2x2 is not provided here.

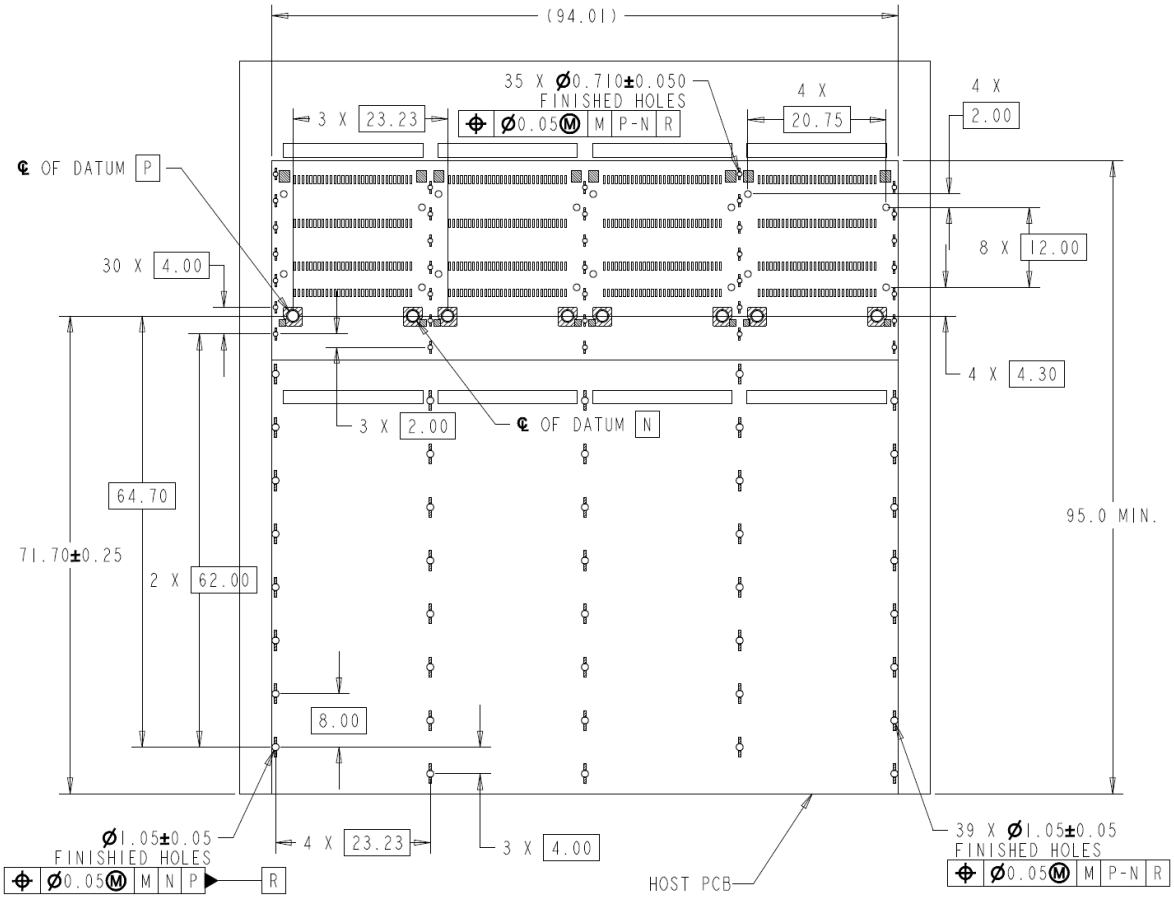


Figure 5-13: Host PCB layout for 2x4 cage

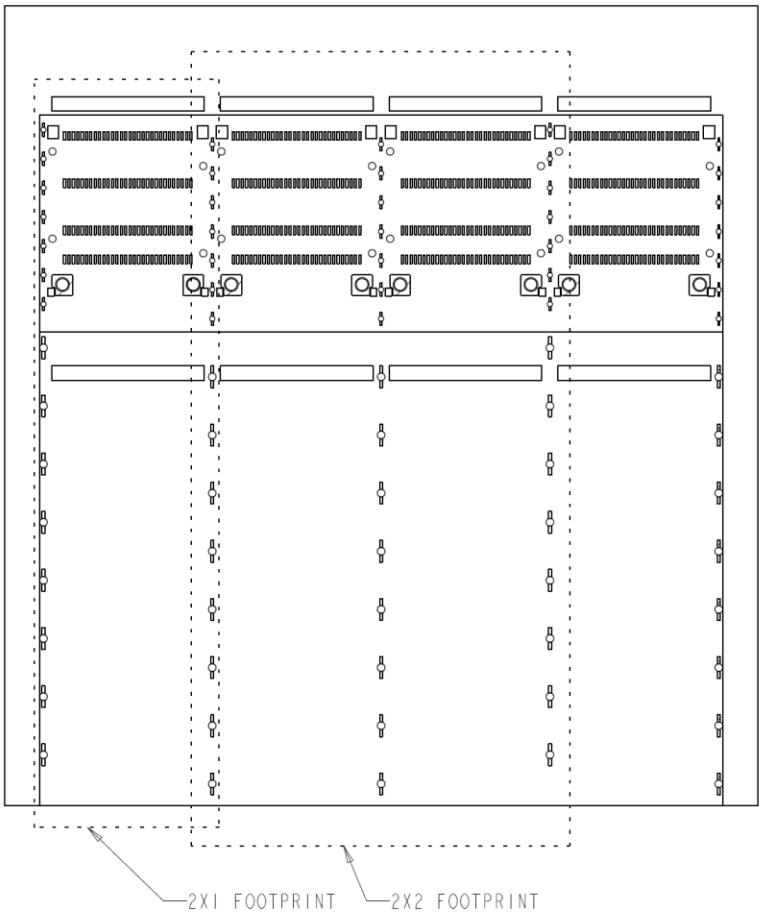


Figure 5-14: Comparison of SMT stacked 2x1, 2x2 and 2x4

5.6 PCB Thickness and Footprint for Belly-to-Belly Application

In this section, the minimum PCB thickness for the belly-to-belly application is shown, along with its host PCB layout. The cage and connector should be able to support a minimum PCB thickness as specified in Figure 5-15.

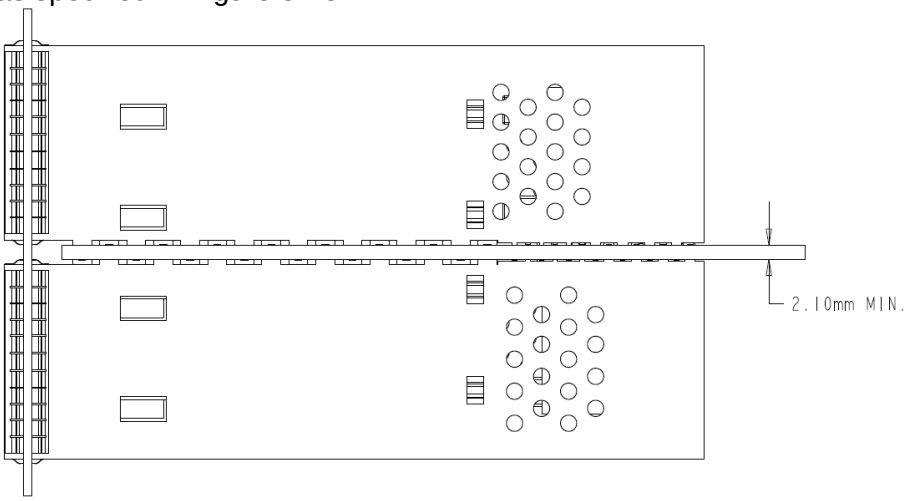


Figure 5-15: PCB thickness for belly-to-belly applications

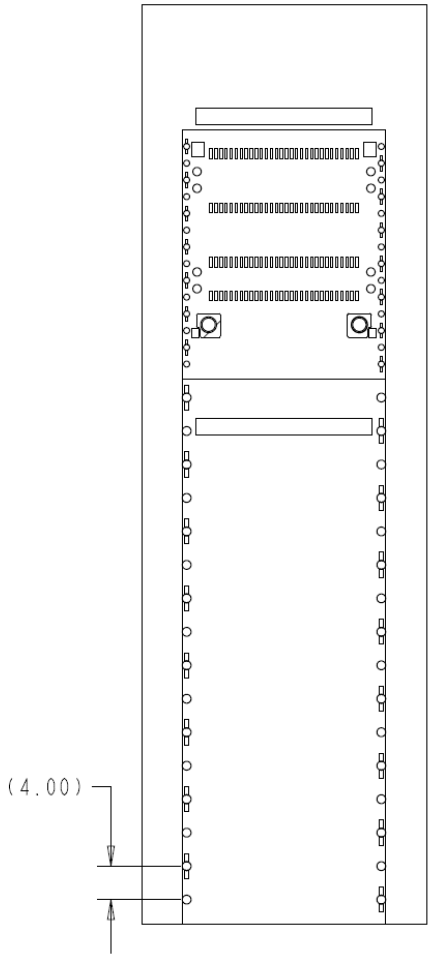


Figure 5-16: The host PCB layout for the 2x1 belly-to-belly applications

5.7 Stacked SMT Connector

Figure 5-17 to Figure 5-19 show the maximum mechanical envelope of the stacked SMT connector. Actual connector shape shall be smaller than this envelope. Figure 5-20 shows an example design, where the connector is optimized to provide better airflow to bottom row. For the contact and peg dimensions, specifications as defined in the section 4.9 for the single row SMT connector shall be applied.

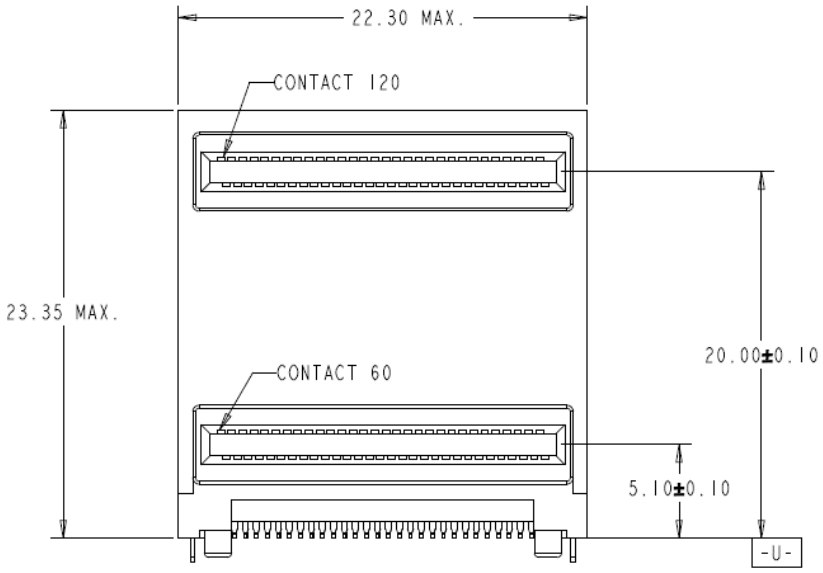


Figure 5-17: Stacked SMT connector, front view

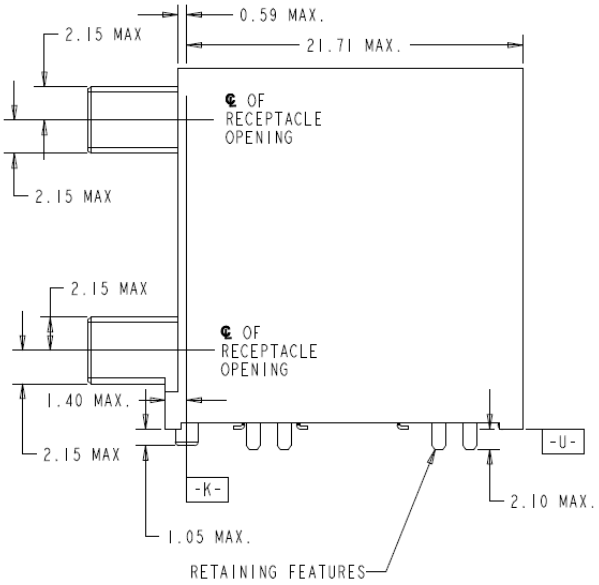


Figure 5-18: Stacked SMT connector, side view

For the retaining feature in Figure 5-18, the feature should be designed to allow proper retaining of the connector during and after soldering. The SMT tail direction shall be as defined in Figure 5-19.

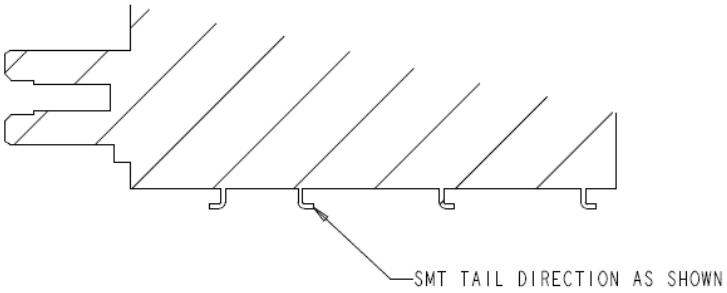


Figure 5-19: SMT tail direction

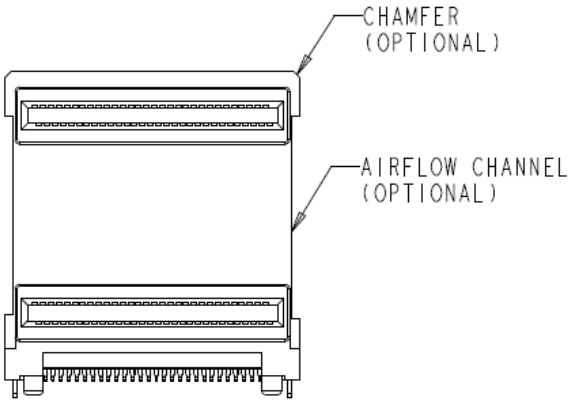


Figure 5-20: Example of actual connector design

5.8 Bezel Panel Cut-Out

In this section, the recommended shape for the bezel to make contact with the EMI finger of the cage is presented.

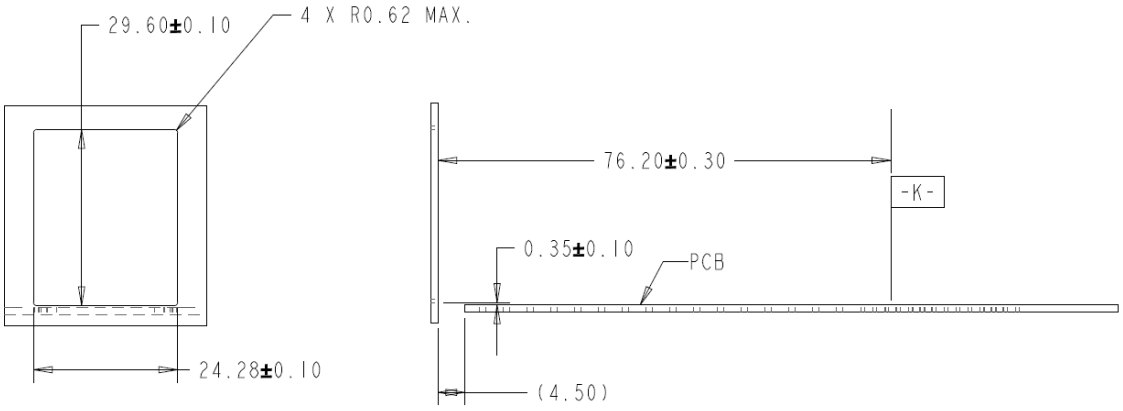


Figure 5-21: Bezel design and location for SMT 2x1 Cage

6 Press-fit Stacked OSFP Connector and cage Mechanical Specification

In this section, the press-fit stacked connector and cage for OSFP is described. Note that the stacked SMT connector and cage is compatible only with Type 1 or Type 2 OSFP modules, not with Type 3 OSFP module as in the Figure 3-3.

6.1 Overview

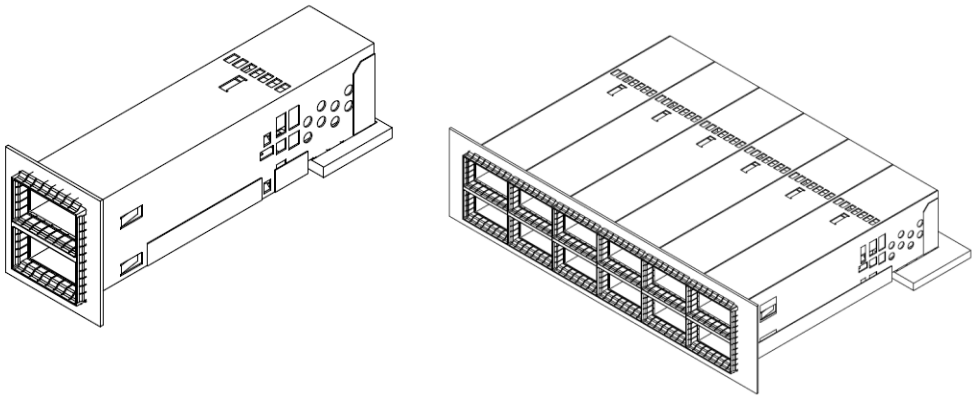


Figure 6-1: Overview of stacked cage, 2x1 and 2x6

In Figure 6-1, stacked cages of 2x1 and 2x6 are shown to demonstrate the stacked ganged cage. Both of the cages are shown with host PCB board and front panel.
For stacked cage, additional datum as defined in Table 6-1 shall apply.

Table 6-1: Descriptions of the module mechanical datum

Designator	Description	Figure
V	Centerline of the Connector Peg	Figure 6-15
Y	Rear Surface of the Connector	Figure 6-15

6.2 Cage Dimensions and Positioning Pin

Figure 6-2 shows the location of the cage positioning pins and the forward stop. Note that the host PCB have significant distance from the front of the cage. In Figure 6-3, the vertical pitch of the stacked cage is defined. To ensure sufficient strength of the cage compliant pins, two material thickness of 0.40mm and 0.25mm are used in the reference design of the cage. 0.40mm thickness is used where the cage compliant pins are used.
Figure 6-4 shows reference dimensions of the cage when assembled with host PCB and OSFP module.

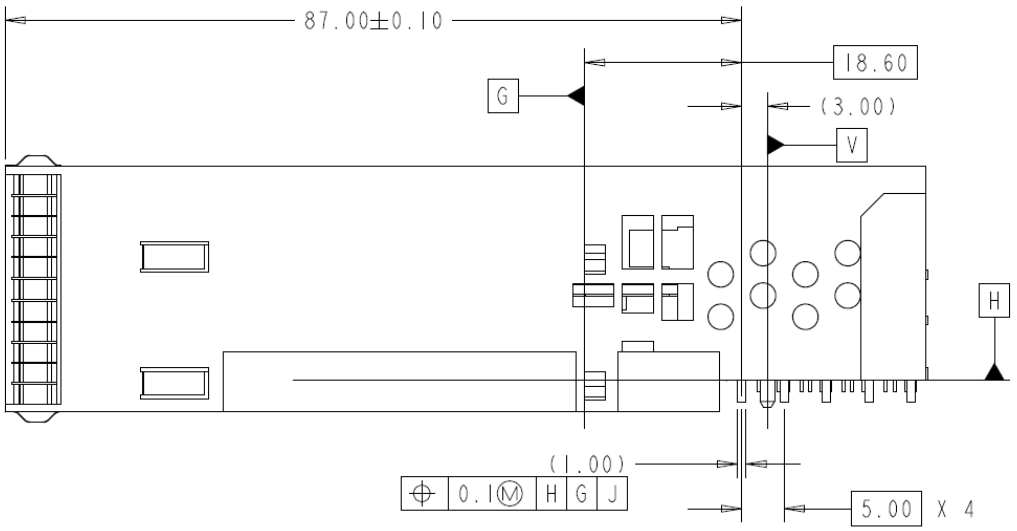


Figure 6-2: Stacked cage positioning pins and forward stop

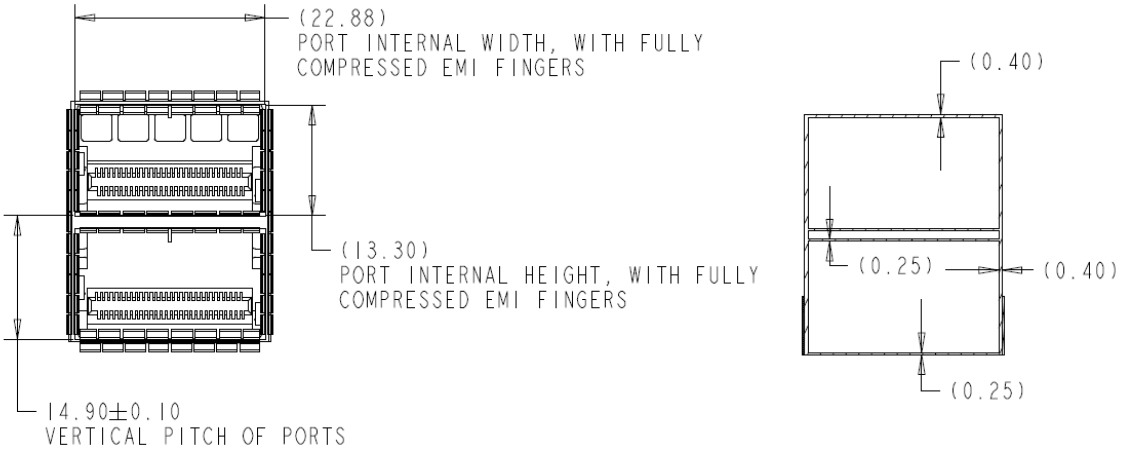


Figure 6-3: Stacked cage, port internal size, pitch and wall thickness

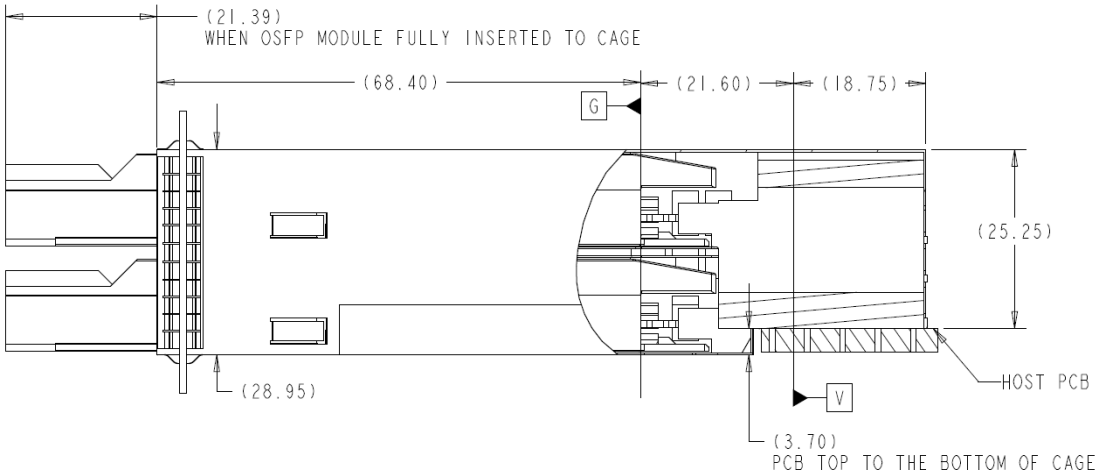


Figure 6-4: Cage with OSFP module, reference dimensions

6.3 Ventilation Holes

For proper cooling of the OSFP module in the stacked cage, the cage shall have appropriate ventilation holes. From Figure 6-5 to Figure 6-8, the ventilation holes required in the stacked

ganged cage are described. The vent holes are designed not only to help with airflow from front to back of the cage, but also to help with airflow between the top and bottom rows of the cage, airflow between neighboring ports and to the bottom of the cage.

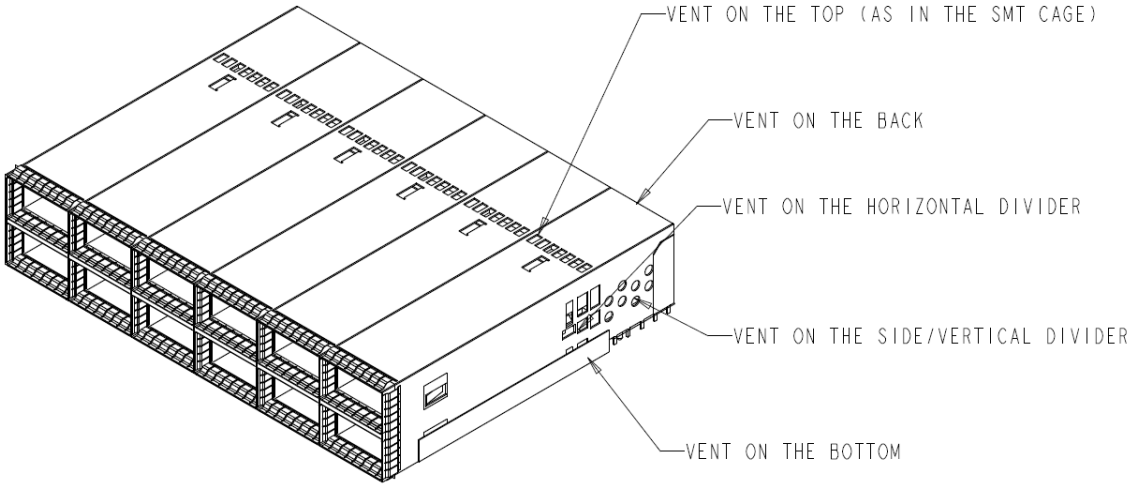


Figure 6-5: Overview of ventilation holes in the stacked cage

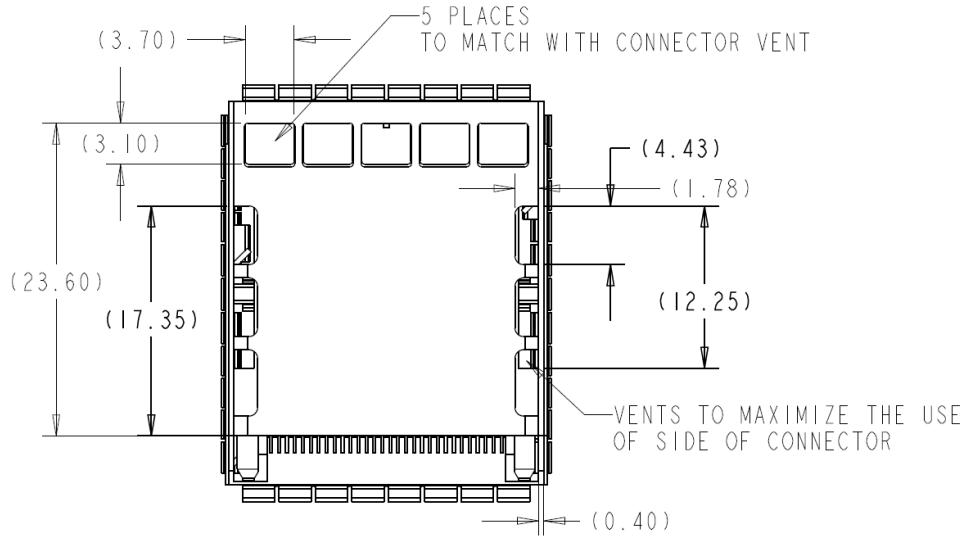


Figure 6-6: Ventilation holes at the back of the cage

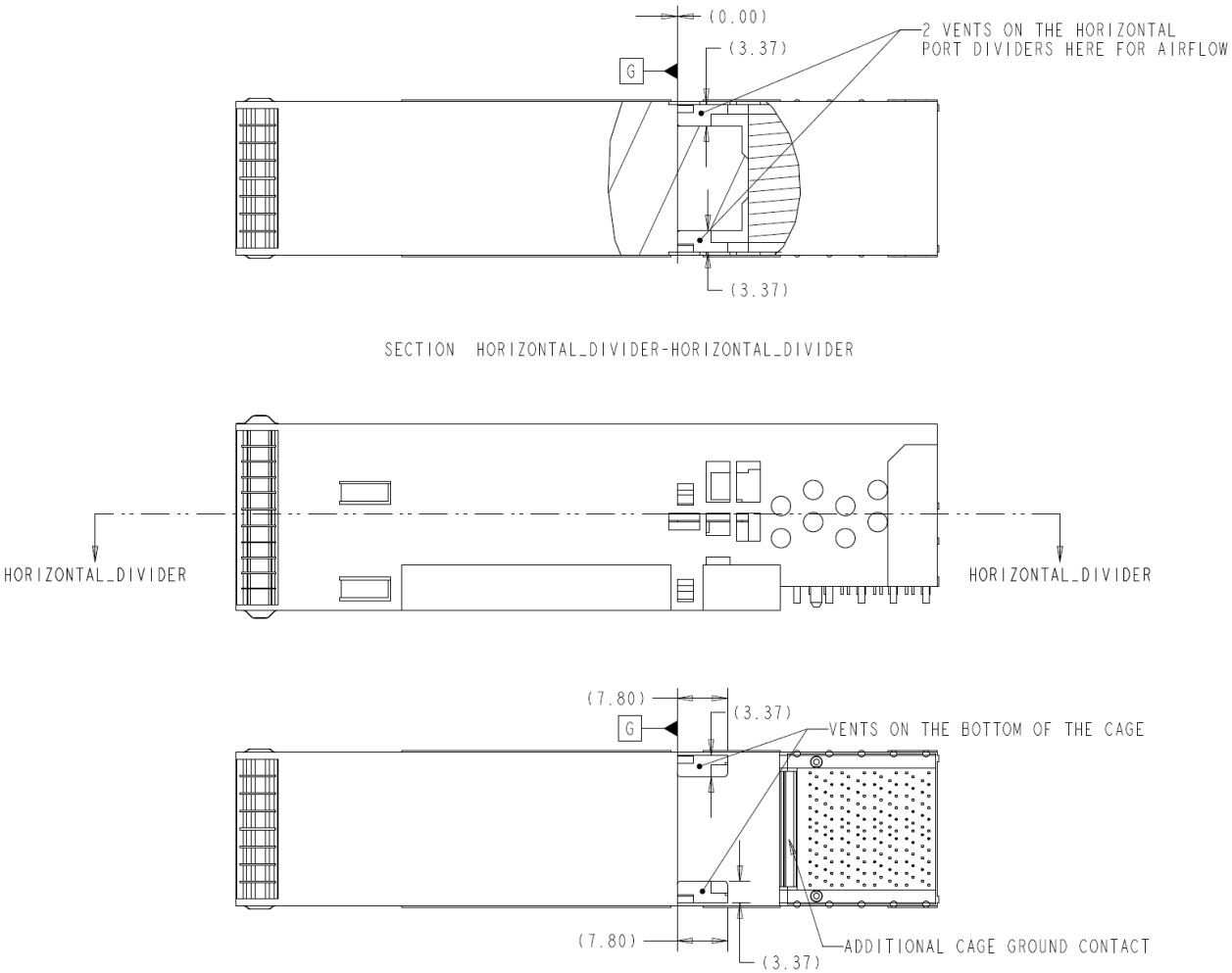


Figure 6-7: Ventilation holes in the horizontal divider and bottom

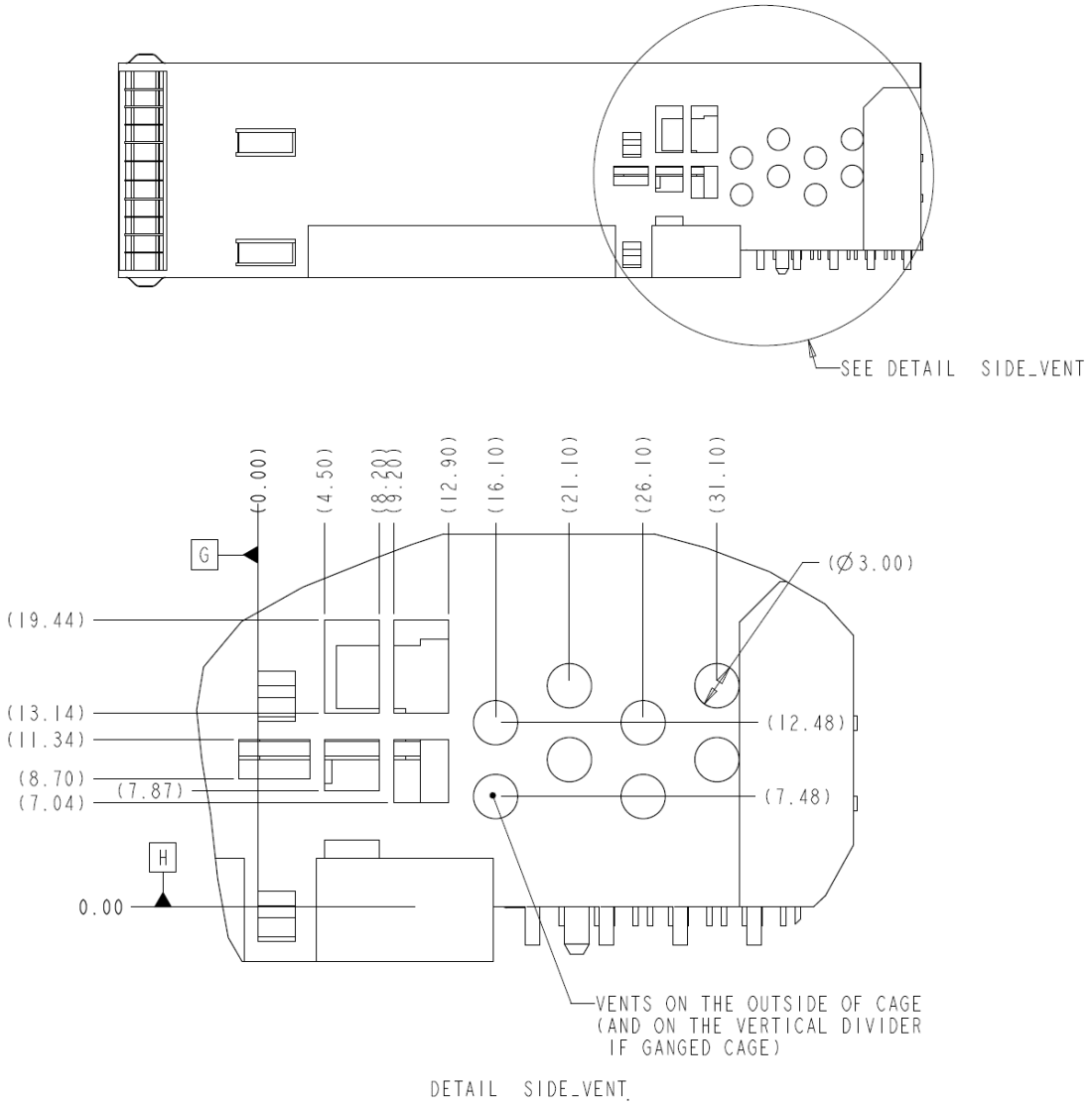


Figure 6-8: Ventilation holes in the side of the cage, and vertical divider

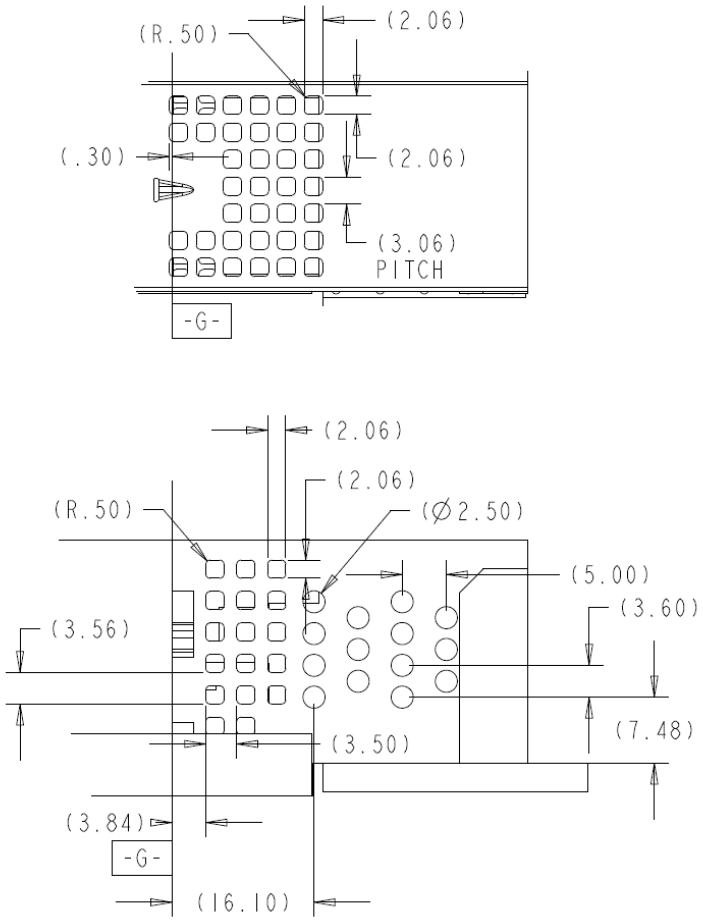
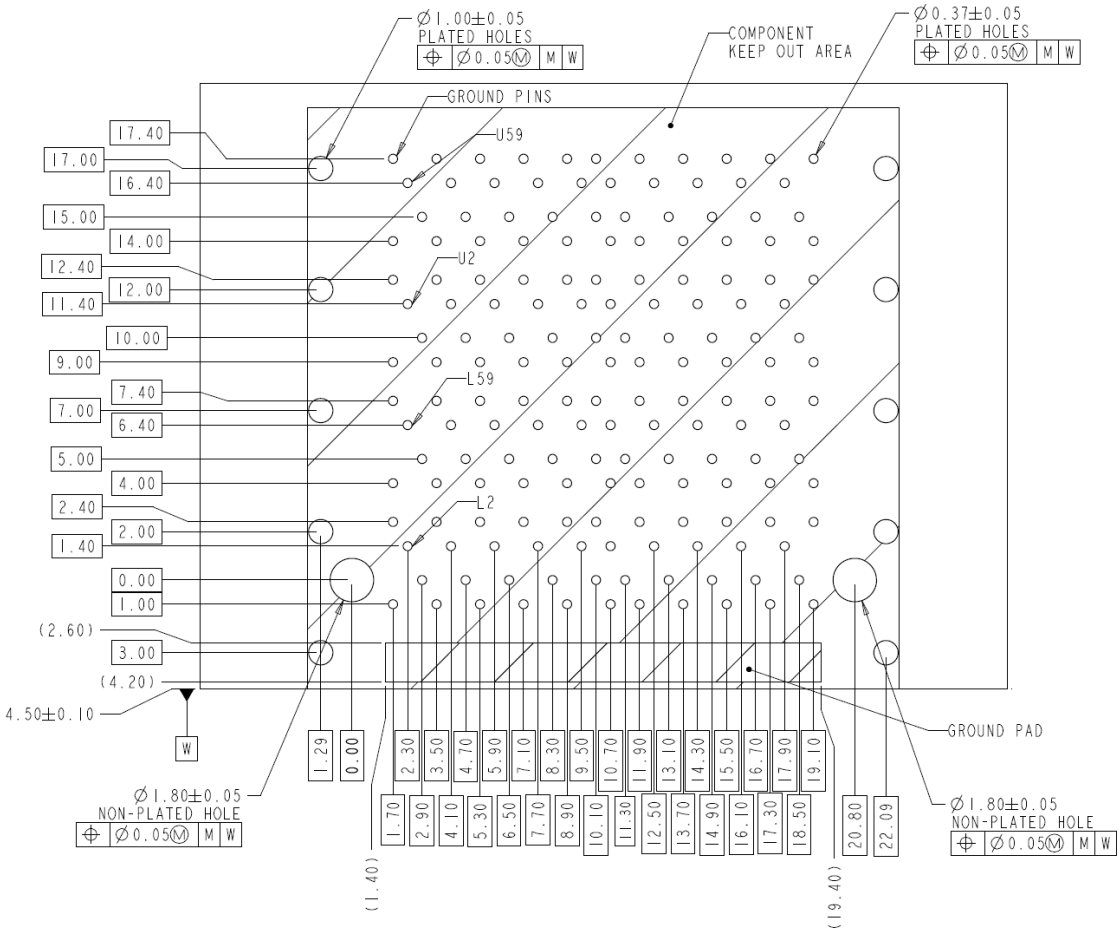


Figure 6-9: Ventilation holes in the top (above view) and side (bottom view) of the cage, alternative example

Rear ventilation pattern, Figure 6-6, is differ with stacked SMT cage in Figure 5-8 because the connector shapes are different. Figure 6-9 shows an alternative example design for top and side vent hole.

6.4 Host PCB Layout – 2x1 Cage



L2: PIN 2 OF THE LOWER PORT. U59: PIN 59 OF THE UPPER PORT.
SEE OSFP MODULE PIN OUT FOR PIN NUMBER CODE AND DETAIL FIGURE.

Figure 6-10: Host PCB layout for stacked connector

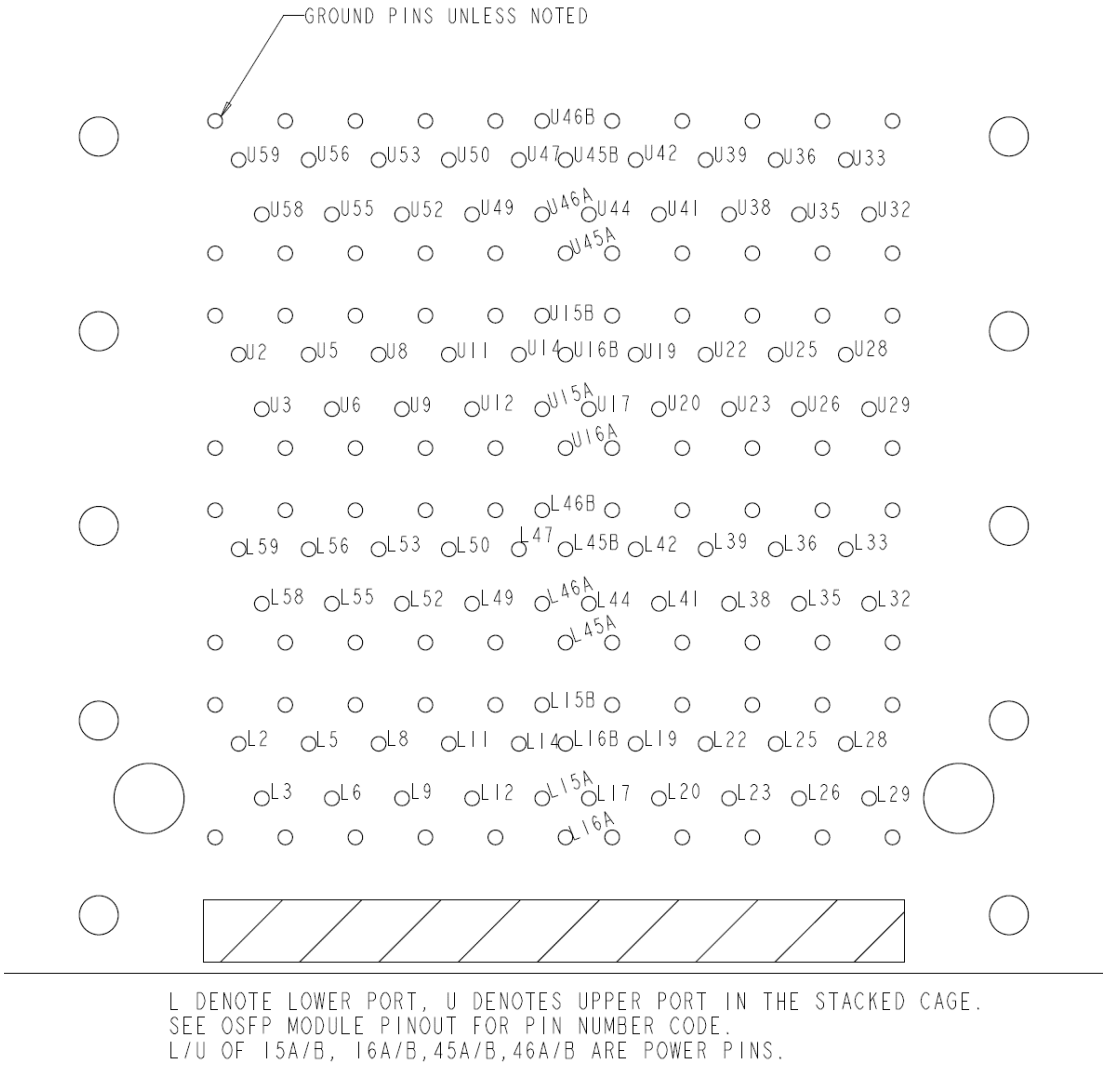


Figure 6-11: Host PCB pins for stacked connector

6.5 Host PCB Layout – Ganged Stacked Cage

As shown in the Figure 6-12, ganged stacked cages shall have a pitch of 23.38mm.

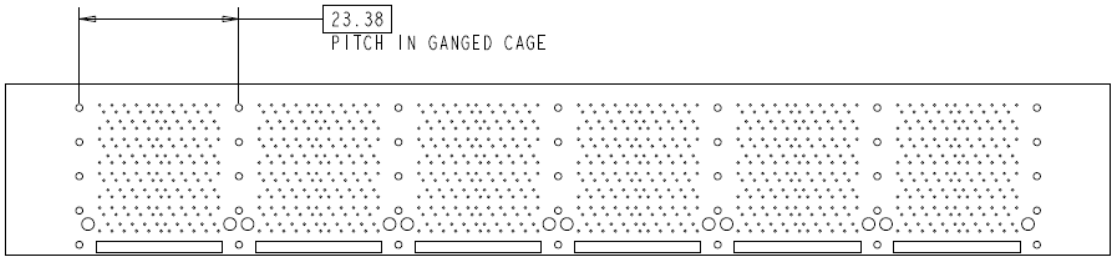


Figure 6-12: Host PCB layout for stacked ganged cage (shown with 2x6)

6.6 Bezel Panel Cut-out

Figure 6-13 shows the bezel cut out for a 2x1 cage. Figure 6-14 shows bezel cut out for a 2x6 cage.

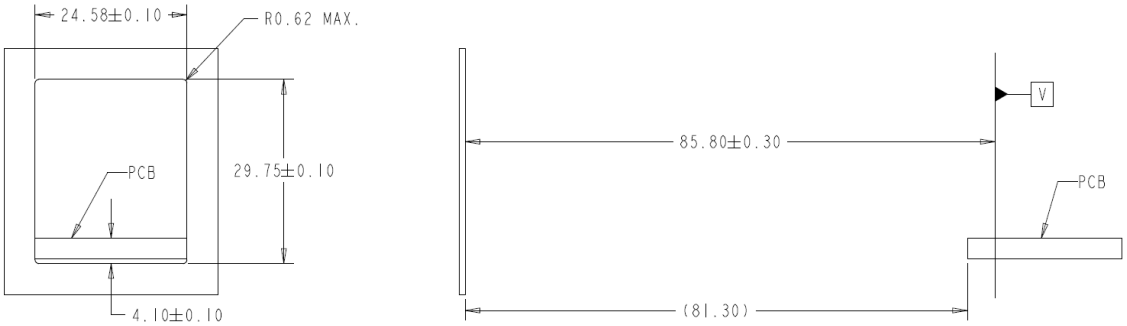


Figure 6-13: Bezel design and location for 2x1 cage

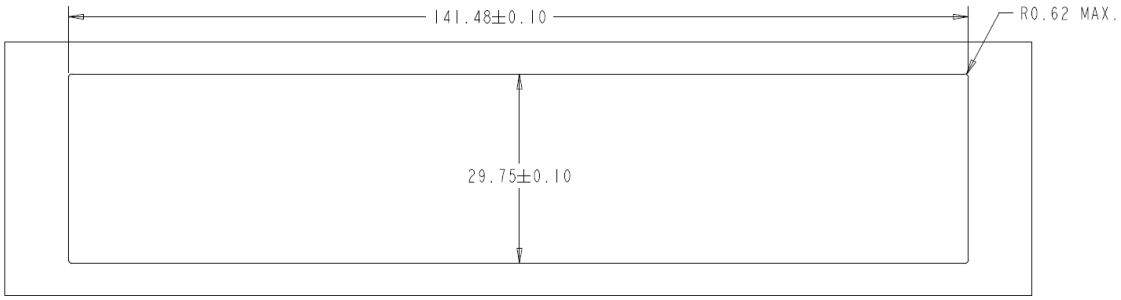


Figure 6-14: Bezel design for 2x6 cage

6.7 Electrical Connector for Stacked Cage (Press-fit)

The stacked electrical connector shall have the following dimensions to properly receive the module as well as allowing for air to pass over the module to the outside.

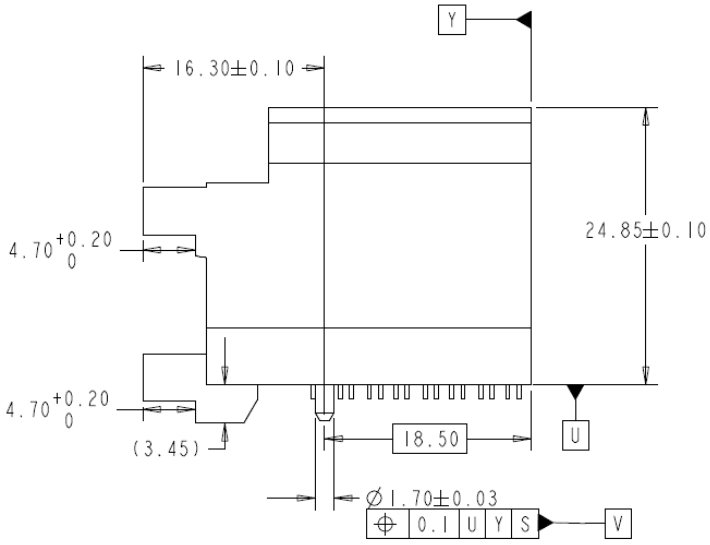


Figure 6-15: Stacked connector, side view

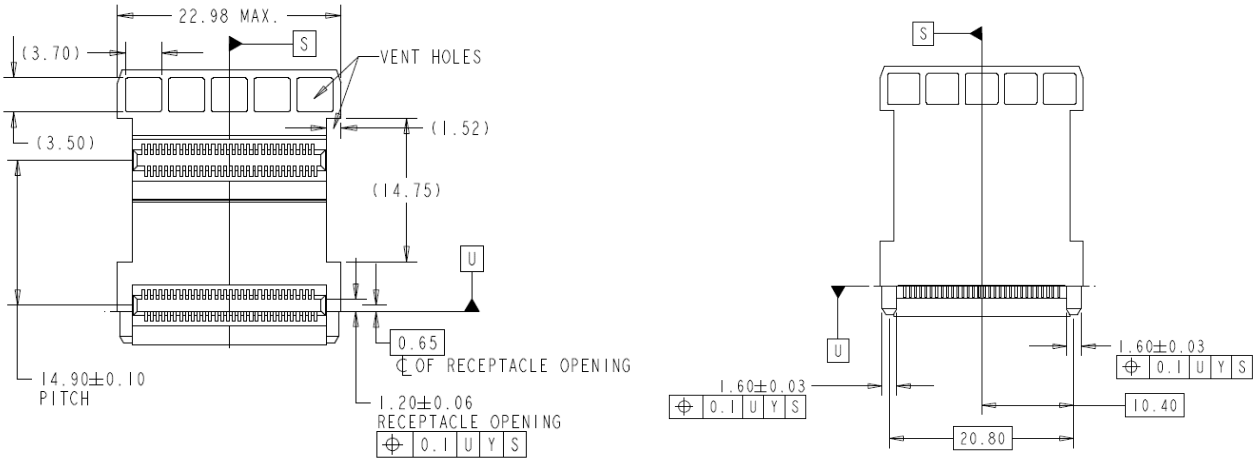


Figure 6-16: Stacked connector, front and back view

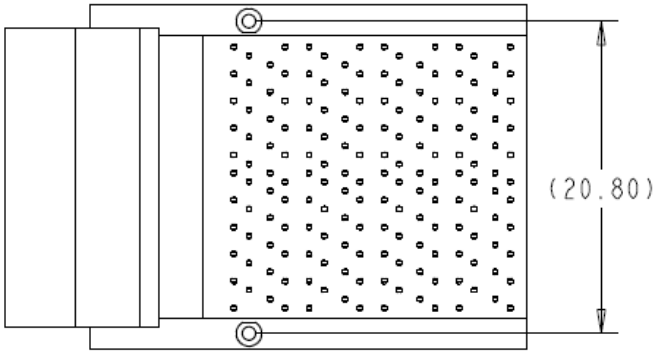


Figure 6-17: Stacked connector, bottom view

7 Plug-in and Removal of an OSFP Module

7.1 Insertion, Extraction, and Retention Forces for an OSFP Module

Table 7-1: Insertion, extraction, and retention forces for an OSFP module

Measurement	Minimum	Maximum	Units	Comments
OSFP Module Insertion	N/A	40 (55)	N	Module to be inserted into connector and cage with latch mechanism engaged. (55N if the cage have riding heatsink)
OSFP Module Extraction	N/A	30 (45)	N	Module to be removed from connector and cage with latching mechanism disengaged. (45N if the cage have riding heatsink)
OSFP Module Retention in Cage	125	N/A	N	No functional damage to module, connector, or cage with latching mechanism activated.

7.2 Durability

The required number of insertion and removal cycles as applicable to the OSFP module and its mating connector and cage are found in Table 7-2. The general requirement as applied to the values in the table is that no functional damage shall occur to the module, connector or cage.

Table 7-2: Durability

Insertion/Removal Cycles into Connector/Cage	Minimum (cycles)	Comments
Module Cycles	50	Number of cycles for an individual module, to be tested with cage, connector, and module; latches may be locked out during testing
Connector/Cage Cycles	100	Number of cycles for the connector and cage with multiple module, to be tested with cage, connector, and module; latches may be locked out during testing

8 Thermal Performance

8.1 OSFP Module Thermal Requirements

The OSFP module shall operate within one or more of the case temperature ranges defined in Table 8-1. The temperature ranges are applicable between 60m below sea level and 1800m above sea level.
The module supplier is responsible for defining a location in the module where the case temperature be measured or monitored. An internal component with the least thermal margin will be connected to this location.

Table 8-1: Temperature range classes

Class	Case Temperature
Standard	0 through 70°C
Reduced	20 through 60°C
Extended	-5 through 85°C
Industrial	-40 through 85°C
Custom	Custom temperature range. Module shall be able to post temperature range to host via management interface.

Table 8-1 defines case temperature only. For reference, touch temperature is controlled by regulatory requirements for handling and incidental contact defined section 3.9.

8.2 OSFP Connector Thermal Requirements

The OSFP connector is required to achieve the following thermal requirements while sustaining maximum power as defined in section 11.6.

Table 8-2: OSFP Connector Thermal Requirements

Parameter	Value
Life Expectancy	10 years
Maximum Ambient Temperature	65 °C
Maximum Temperature Rise of connector when all signal and power contacts energized simultaneously	30 °C

8.3 OSFP Module Airflow Impedance Curve

Figure 8-1 shows a typical airflow impedance range of an OSFP (module only) as measured along or through its heat sink. This typical range of airflow impedance can be used as a reference in an OSFP module's heat sink design and system design.

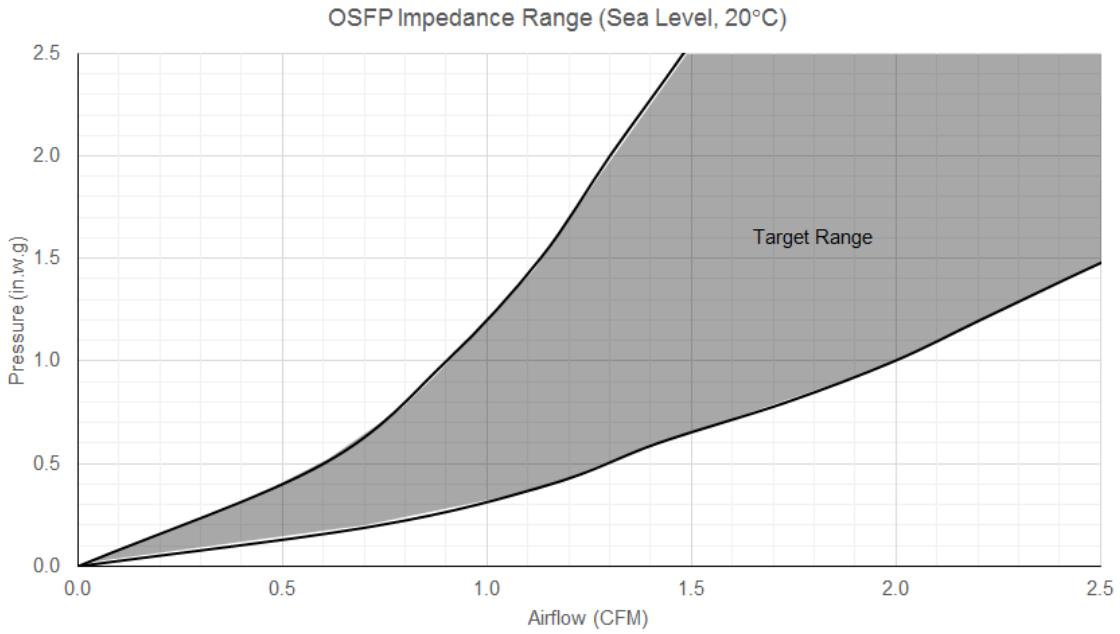


Figure 8-1: Target range of impediment to airflow of an OSFP module (20C, Sea Level)

8.4 Module Airflow Impedance Test Jig

The impedance range of Figure 8-1 was created using a jig as shown in Figure 8-2 and Figure 8-3. The jig is designed to support airflow along the heat sink as well as leakage around the module. The positive stop located within the jig reproduces the assembled condition within a host port. For a Type 2 module, it is normal for the front of the module to protrude beyond the jig opening. A Type 3 module may or may not extend beyond the jig opening.

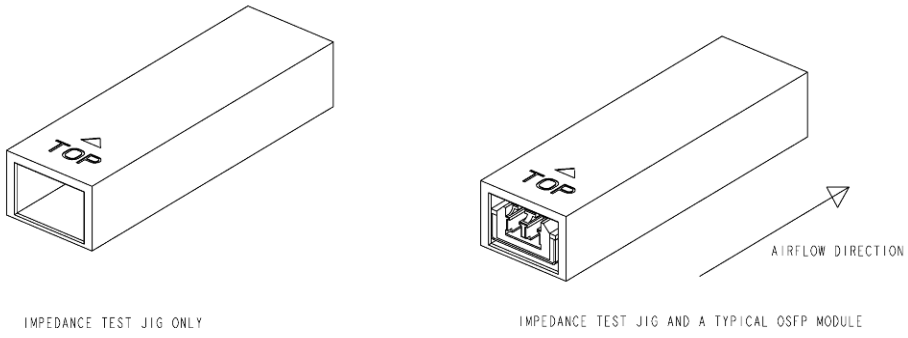


Figure 8-2: Impedance test setup for Type 1 and Type 2 OSFP module (Shown with Type 1)

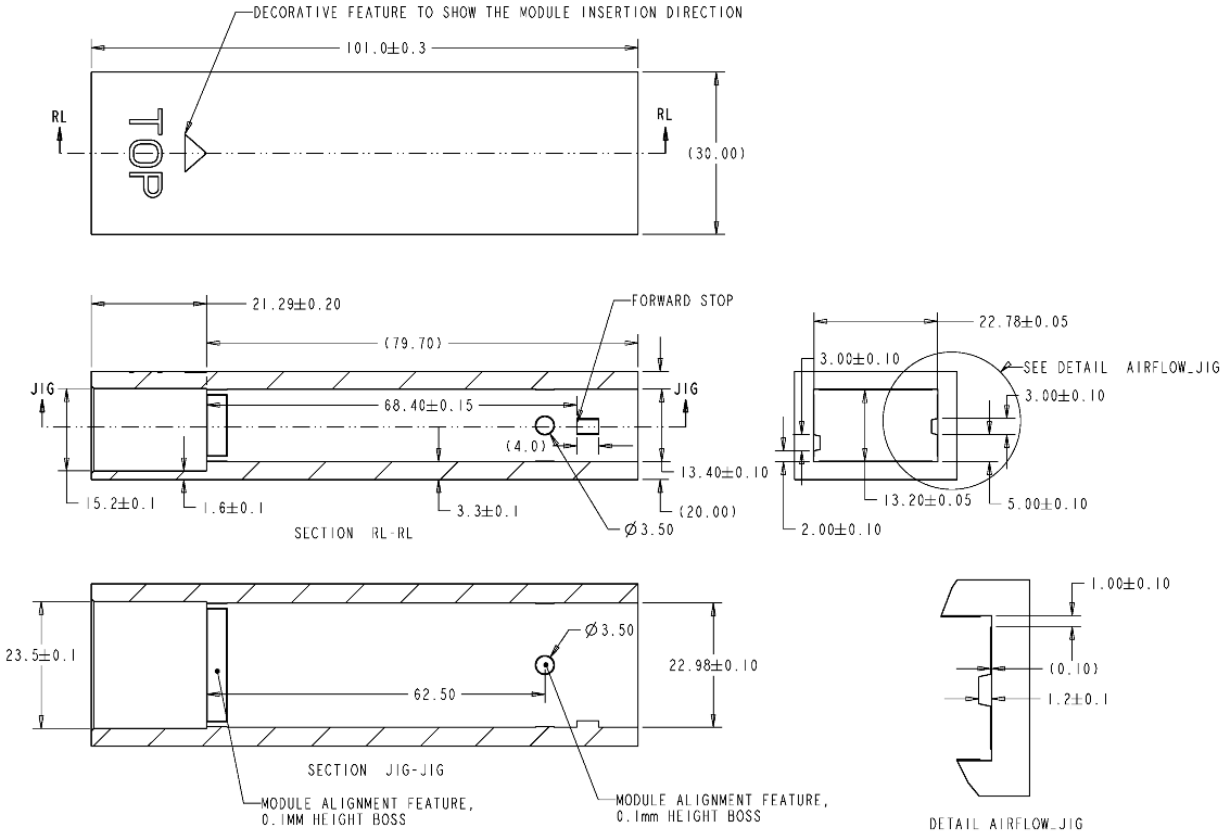


Figure 8-3: Impedance test jig for Type 1 and Type 2 OSFP

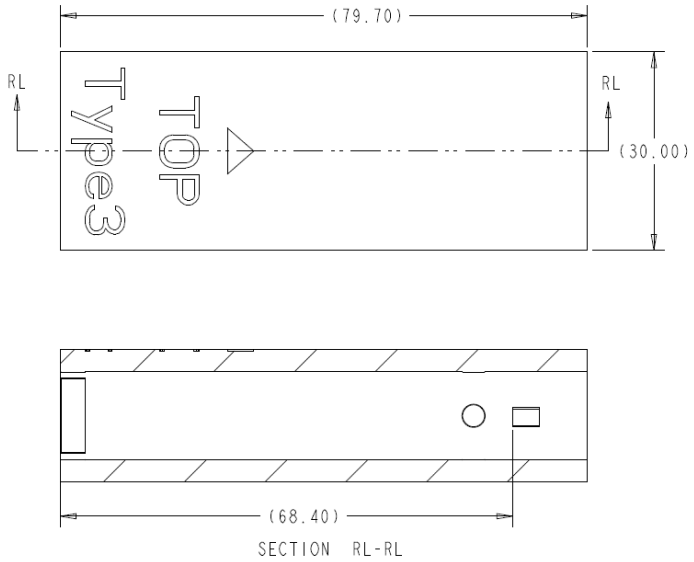


Figure 8-4: Impedance test jig for Type 3 OSFP

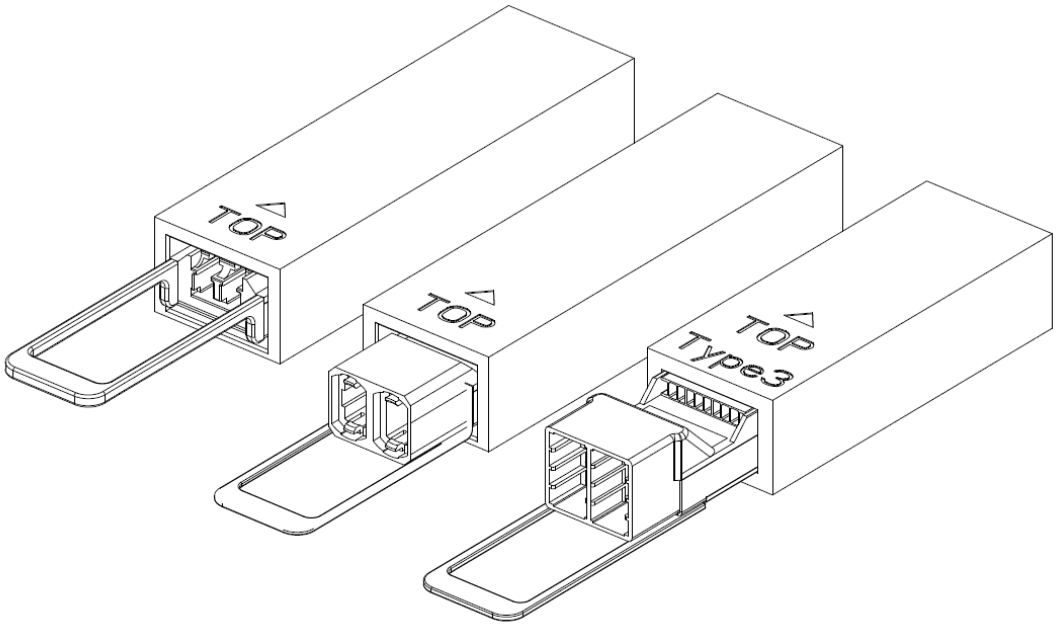


Figure 8-5: Impedance test setup for Type 1, Type 2 and Type 3 OSFP

9 OSFP Riding Heat Sink Module and Cage Mechanical Specification

9.1 Overview

OSFP Riding Heat Sink (OSFP-RHS) is a 9.5mm high pluggable module which does not have an integrated heat sink as shown in the Figure 9-1 and Figure 9-2. In place of OSFP's integrated heat sink, OSFP-RHS cage shall have a riding heat sink. To prevent insertion of OSFP-RHS into a standard OSFP cage, the shape and location of the positive stop has been changed. See Table 9-1 for a comparison between the OSFP-RHS and OSFP.

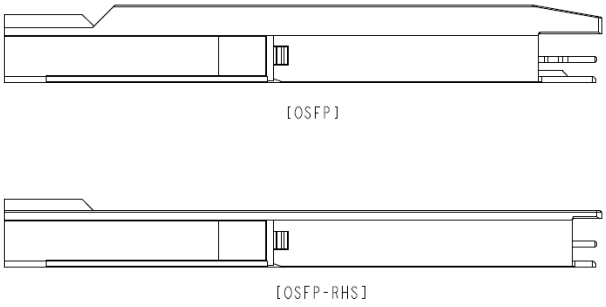


Figure 9-1: Side view of a typical OSFP (top) and a typical OSFP-RHS (bottom)

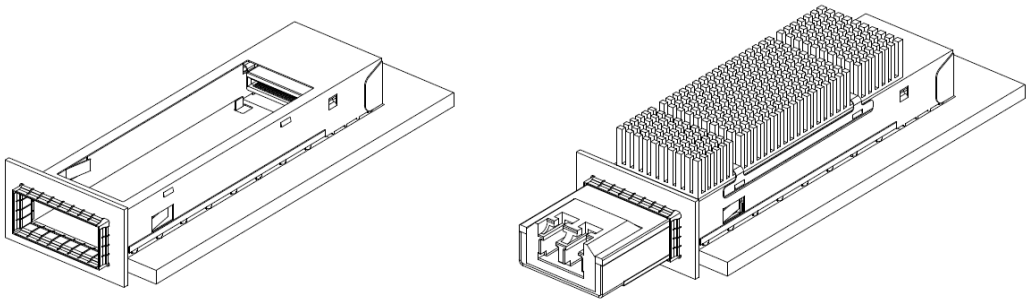


Figure 9-2: OSFP-RHS cage only (left) and OSFP-RHS cage with module and riding heat sink (right)

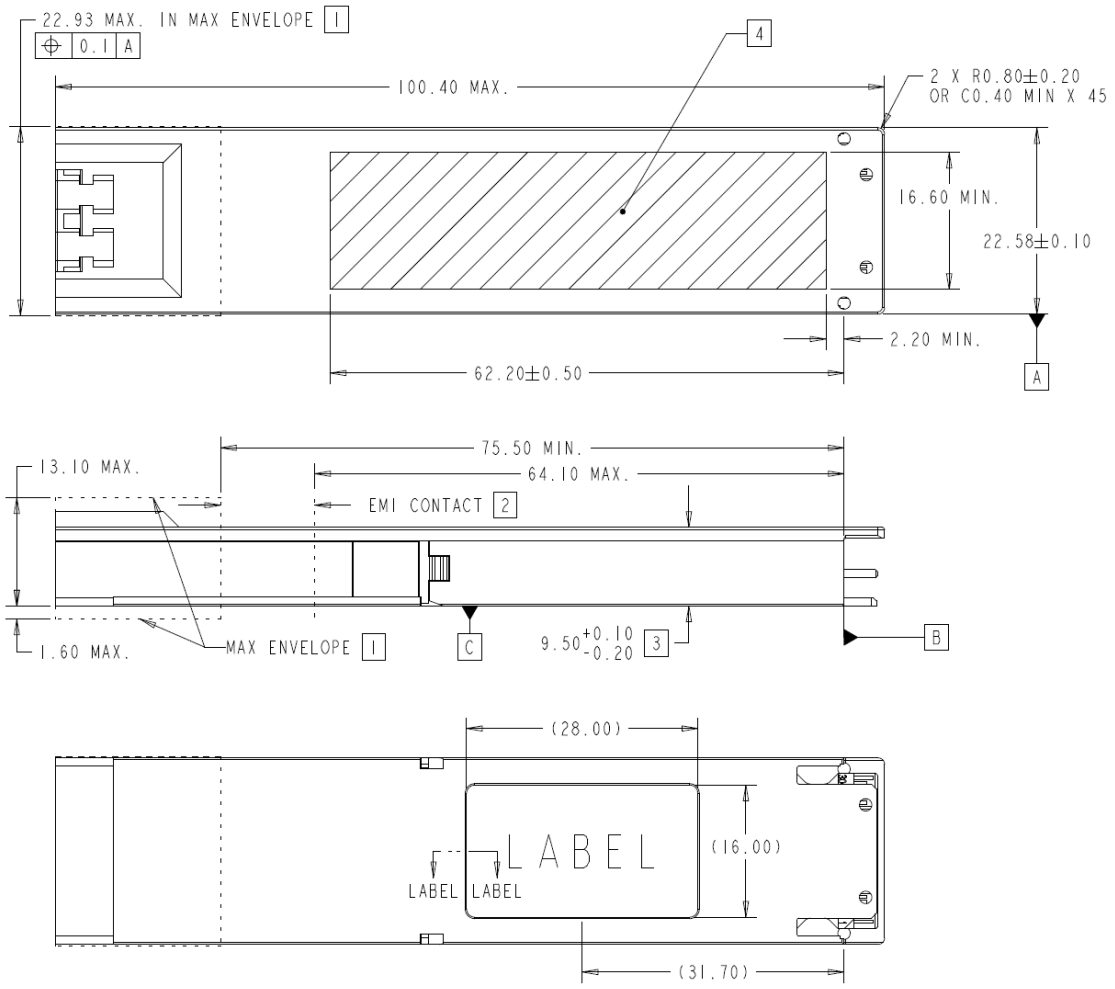
Table 9-1: Comparison of OSFP-RHS to OSFP

OSFP-RHS feature	Comment
Module	9.5mm height without heat sink and different positive stop; for the feature which is not explicitly specified for OSFP-RHS, same specification as of OSFP shall be applied.
Connector	Identical with Surface Mount Connector
Host PCB Board Layout	Identical with Surface Mount type
Cage	Port height/positive stop/bezel cutout is different with OSFP
Insertion/Extraction/Retention	No change; see Table 7-1
Durability	Identical with OSFP
Thermal Requirement	Identical with OSFP
Airflow Requirement	Not applicable (Section 8.2 is not applied)
Electrical and Management interface	Identical with OSFP

In the following sections, the dimensions of the OSFP-RHS will be defined.

9.2 OSFP-RHS Module Mechanical Specification

Figure 9-3 shows the overall dimension of an OSFP-RHS module from a top view. The reference datum definition is identical with Table 3-1, but note that the location of the datum B (forward stop of the module) is shifted 6mm to prevent an OSFP-RHS from being fully inserted into an OSFP cage as described in section 4 or 5.



NOTES:

1. FRONT OF THE MODULE, PULL TAB AND OTHER COMPONENTS CAN EXTEND 1.60mm MAX FROM THE BOTTOM AND 13.1mm MAX FROM THE BOTTOM WITH UP TO 22.93mm WIDTH IN THE MAX ENVELOPE SHOWN.
2. INDICATED SURFACES (ALL 4 SIDES) TO BE CONDUCTIVE FOR CONNECTION TO CHASSIS GROUND.
3. APPLIES FROM THE TOP OF THE MODULE TO THE BOTTOM OF THE MODULE, INSIDE THE CAGE.
4. SURFACE TO BE THERMALLY CONDUCTIVE. REFER SECTION 9.4 FOR FLATNESS AND ROUGHNESS REQUIREMENTS.

Figure 9-3: Overview of the OSFP-RHS and heat sink contact area

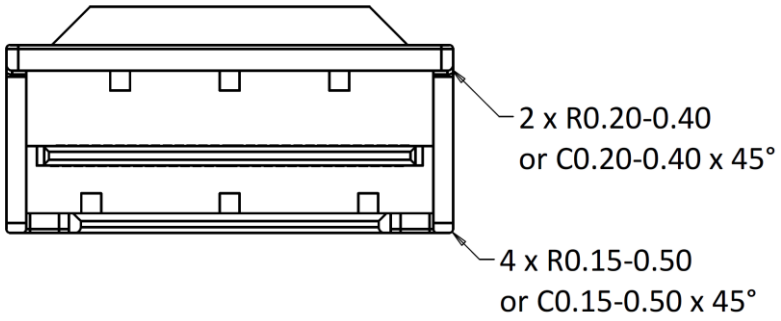


Figure 9-4: Corner radius of OSFP-RHS in back view

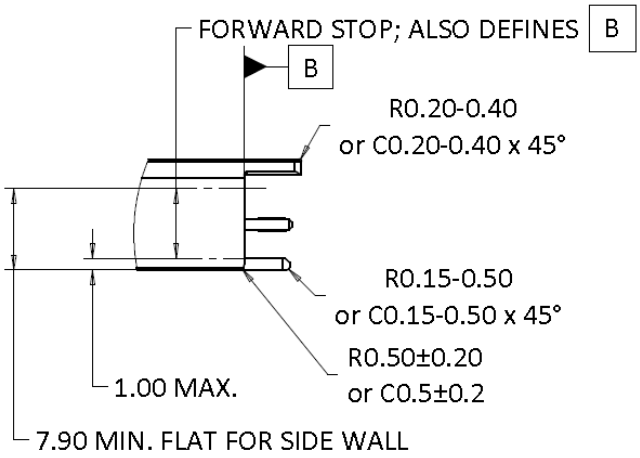


Figure 9-5: OSFP-RHS forward stop

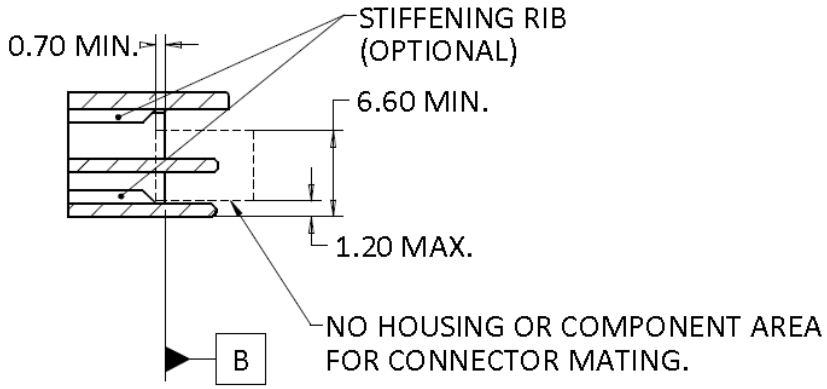


Figure 9-6: Connector keep out area in side view

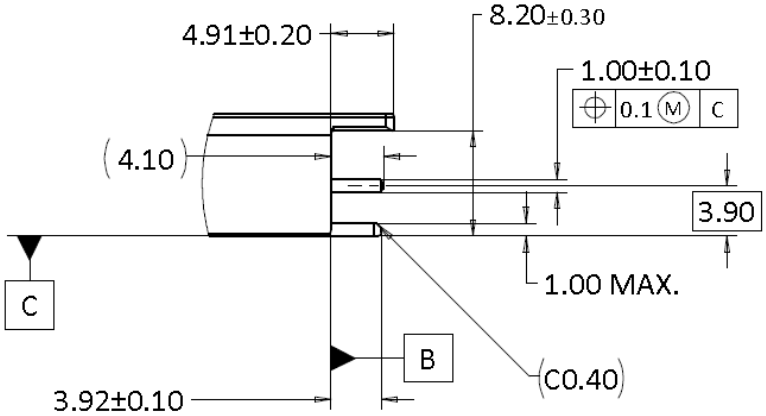


Figure 9-7: Nose of OSFP-RHS

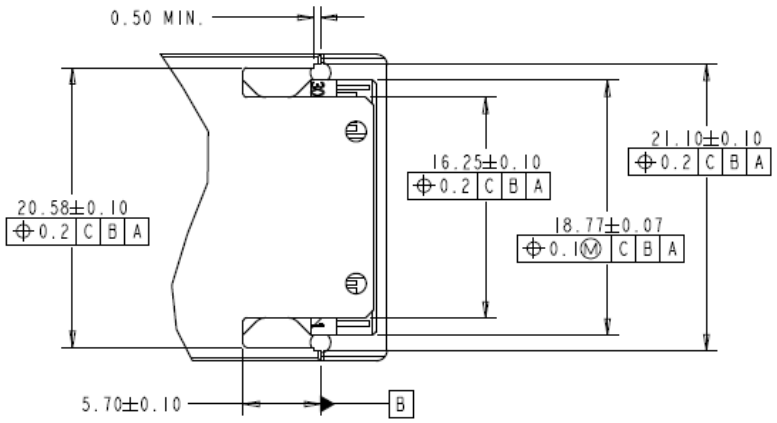


Figure 9-8: Paddle card position (bottom view of module) and module nose width

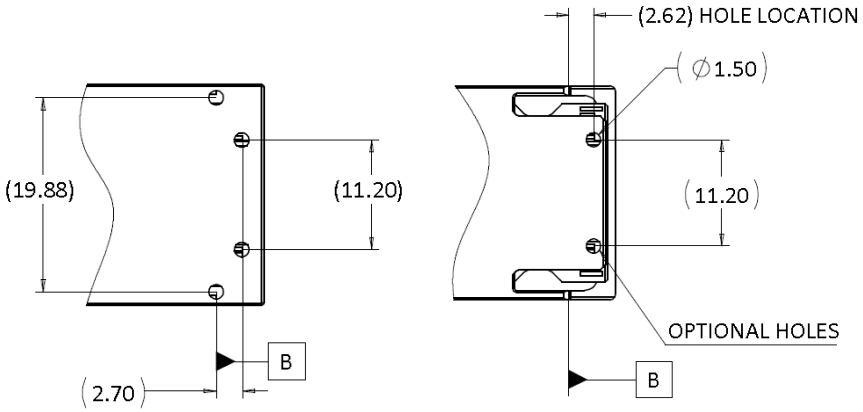


Figure 9-9: Location of inspection holes

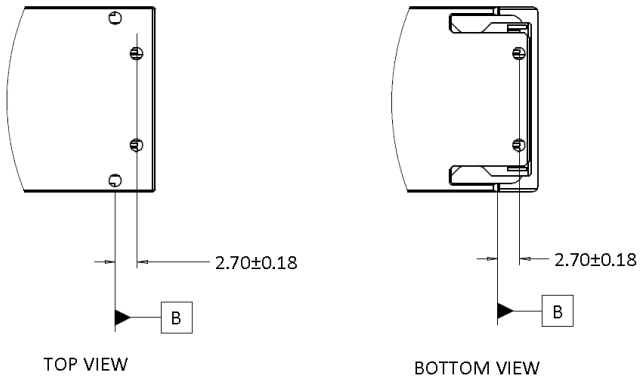


Figure 9-10: Signal pad location with respect to the forward stop

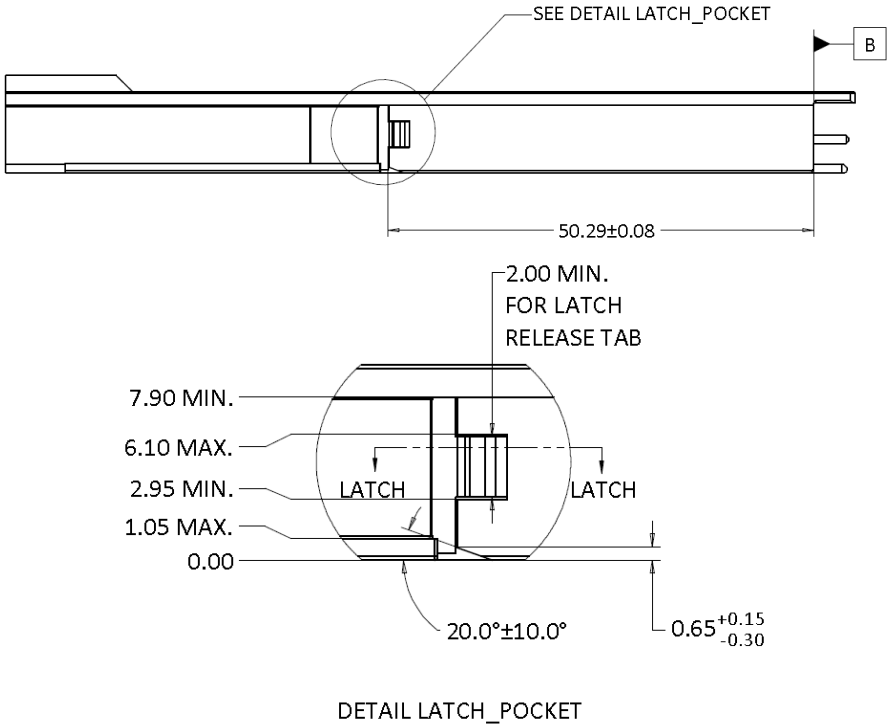


Figure 9-11: Latch pocket details of an OSFP-RHS (See section 3.7 for latch cross-section)

9.3 OSFP-RHS Paddle Card

Interface of the paddle card which mate with connector of an OSFP-RHS is identical with OSFP. Note that, as shown in the Figure 9-12, the shallow neck and the component place avoid area is not required in the OSFP-RHS. This is because the positive stop of the OSFP-RHS is shifted to the rear side of the module.

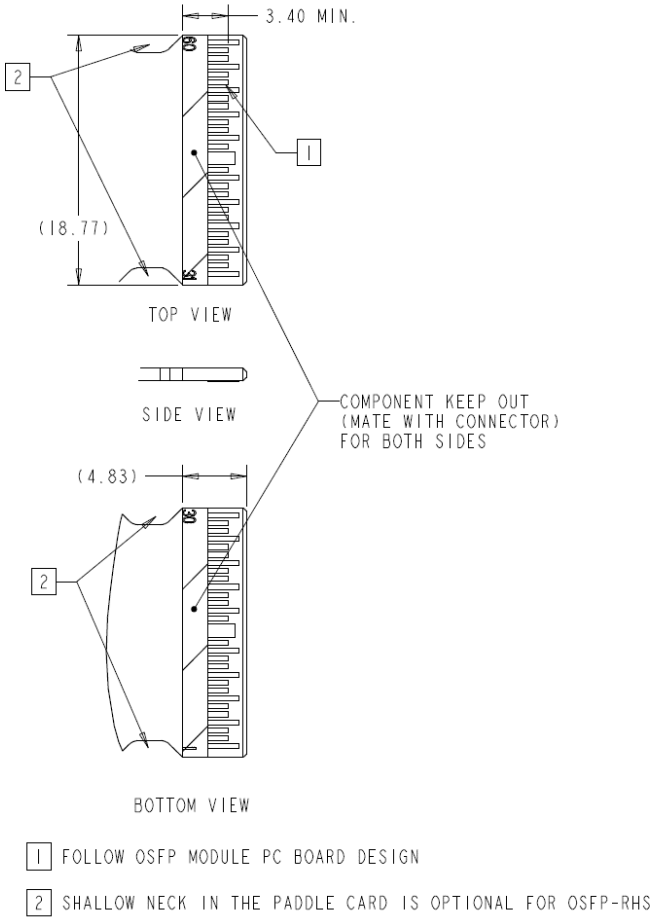


Figure 9-12: Paddle card of an OSFP-RHS

9.4 OSFP-RHS Thermal Interface Surface Requirements

The thermally conductive area of an OSFP-RHS, as in the Figure 9-3, shall be compliant with specifications in Table 9-2.

Table 9-2: Surface flatness and roughness of the thermally conductive area

OSFP-RHS Power (Max)	Surface Flatness	Surface Roughness
Equal or less than 5W	0.15mm or better	Ra 3.2μm or better
More than 5W	0.12mm or better	Ra 1.6μm or better
Recommended for module with more than 14W (Optional)	0.05mm or better	Ra 0.8μm or better

9.5 OSFP-RHS Cage Mechanical Specification

An OSFP-RHS cage has a lower height than an OSFP cage and makes use of a riding heat sink for cooling. The forward stop feature in an OSFP-RHS cage is shifted compared with an OSFP cage to match with an OSFP-RHS module. See Figure 9-13 to Figure 9-19 for the mechanical specification of the cage for OSFP-RHS. The host PCB foot print is identical with OSFP. Its latch feature is identical, except its geometrical reference (forward stop) has been moved.

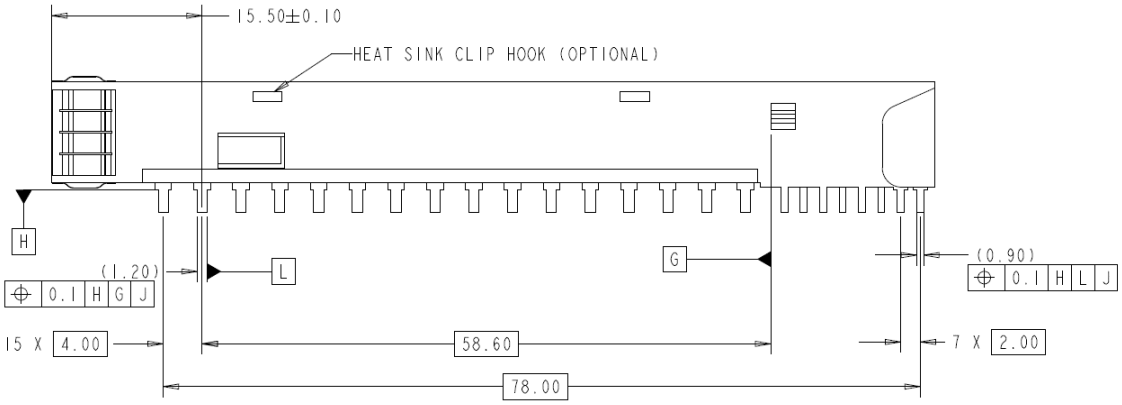


Figure 9-13: Cage positioning pins and forward stop

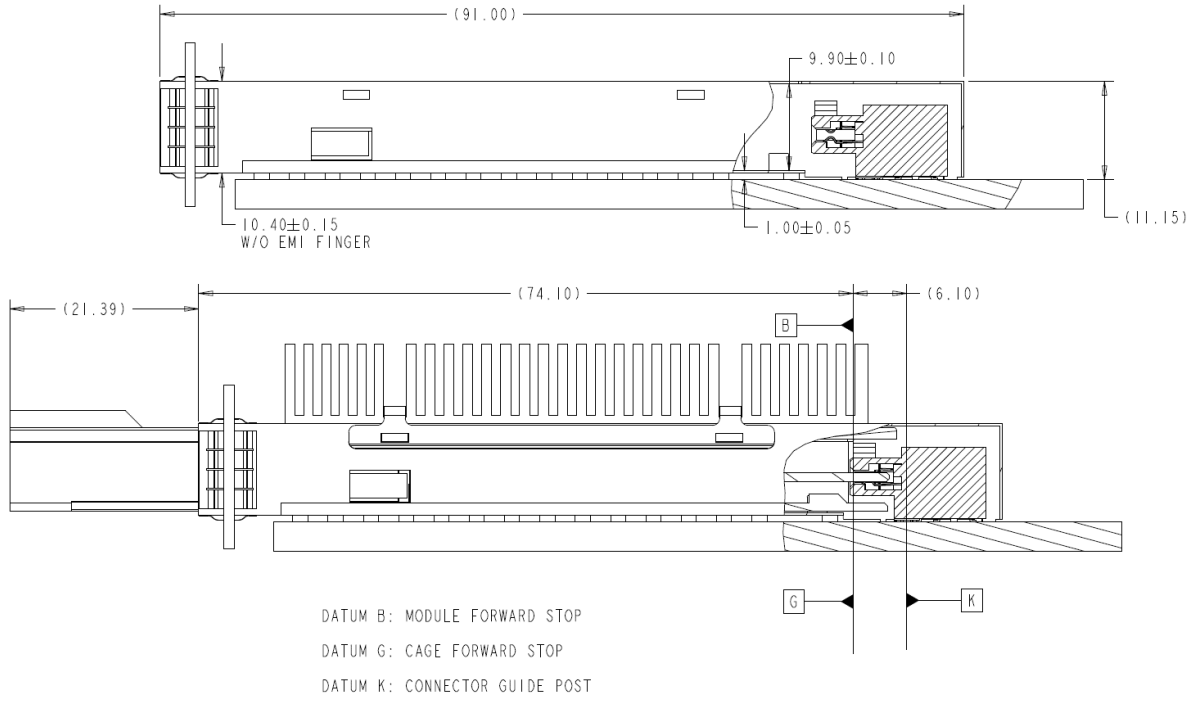


Figure 9-14: Side view of a 1x1 cage with vertical cage dimensions

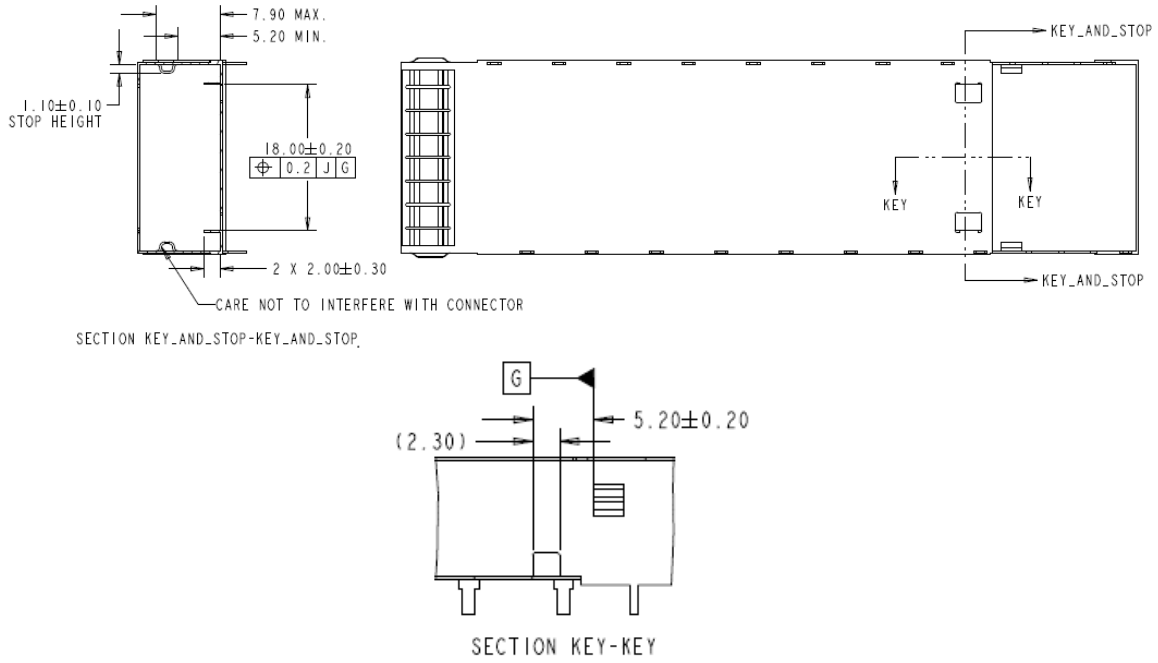


Figure 9-15: Keying feature in OSFP-RHS

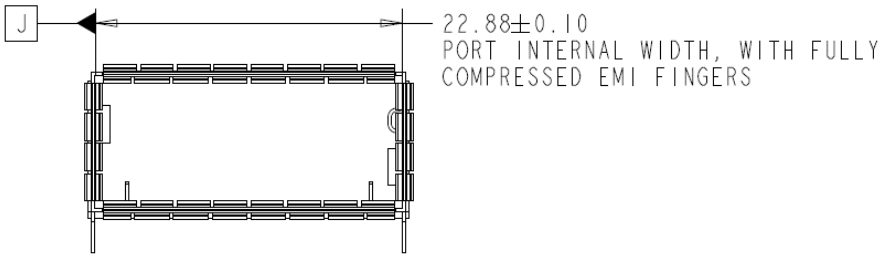


Figure 9-16: Internal width and centerline datum

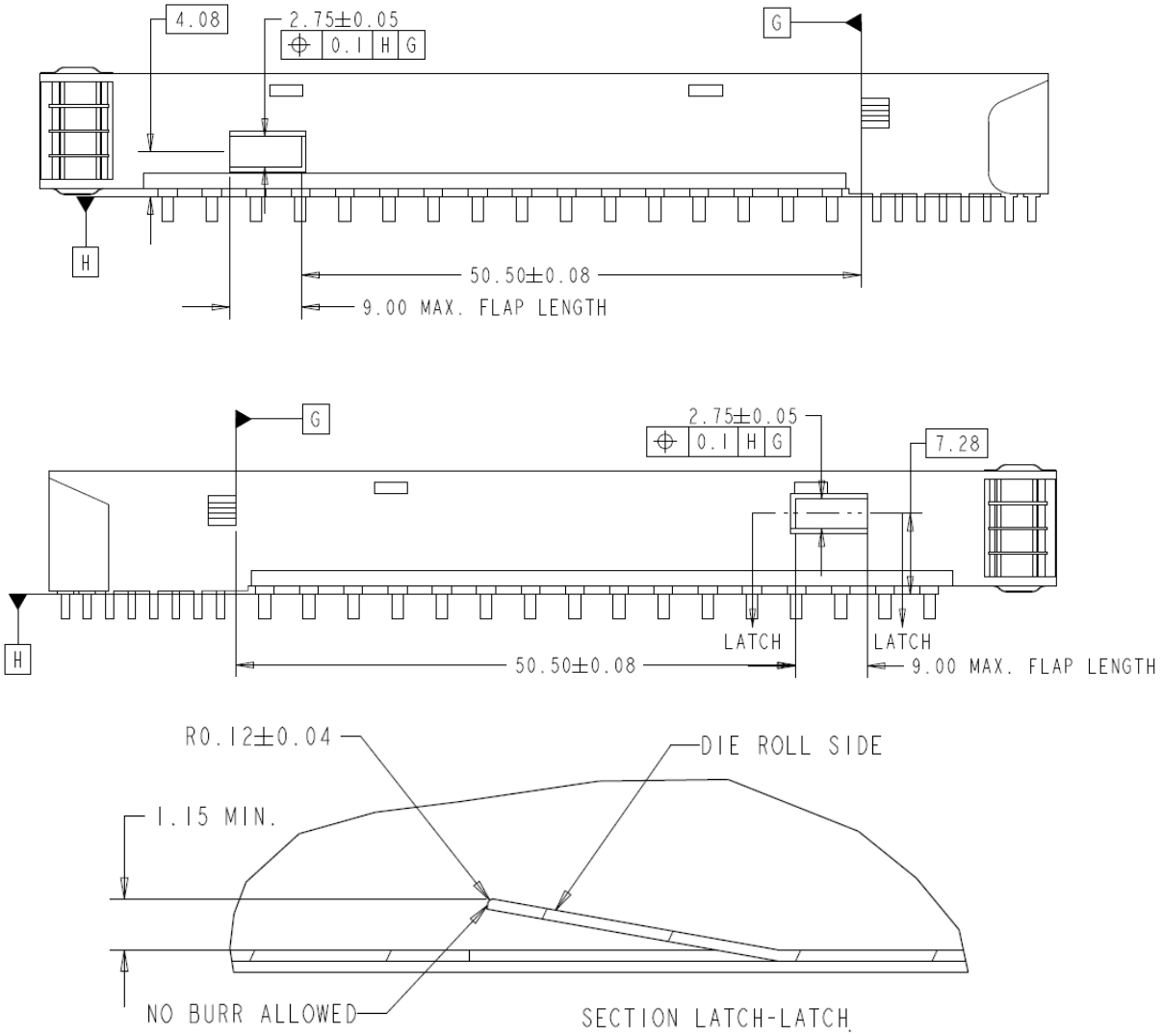


Figure 9-17: Latch feature for OSFP-RHS cage

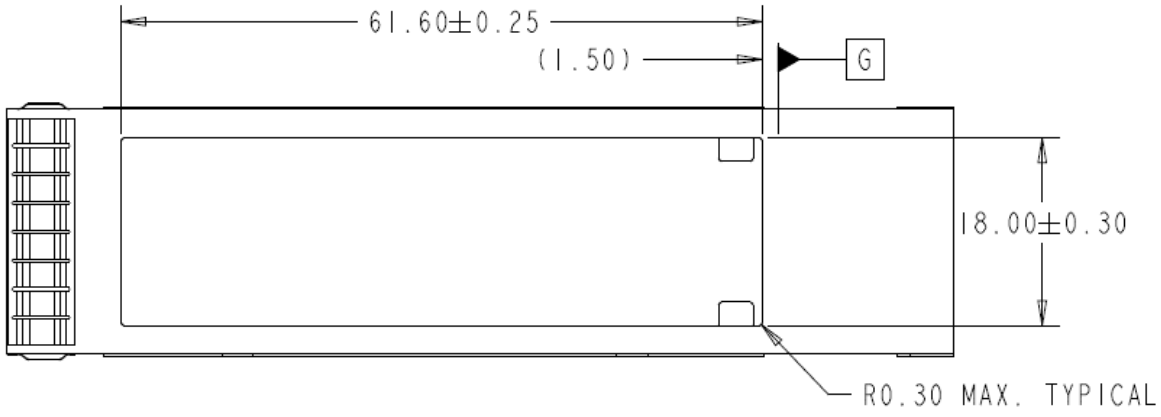


Figure 9-18: Cutout for a riding heat sink in the OSFP-RHS cage

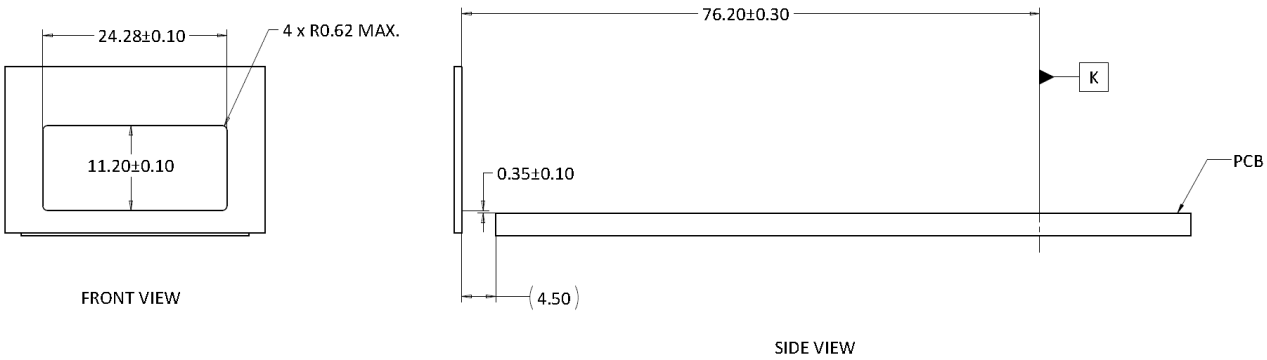


Figure 9-19: Bezel cutout for the OSFP-RHS cage

9.6 Maximum Heat Sink Down Force for an OSFP-RHS Cage

The cage should be designed so that the force which will be applied from the riding heat sink to an OSFP-RHS module shall not exceed 50N downward.

9.7 Custom Height OSFP-RHS

There may be a custom OSFP-RHS with height different than 9.5mm but otherwise having all other attributes of OSFP-RHS. Details of such custom height OSFP-RHS are not provided in this specification.

10 Optical PMD Block Diagrams

Below sub-sections illustrate block diagrams for a sampling of optical physical medium dependent sublayers (PMDs) that can be realized in an OSFP form factor. These block diagrams are meant to serve as guidelines for better understanding of the form factor and are by no means exhaustive.

10.1 400G PDM Block Diagrams

10.1.1 Optical PMD for parallel single mode fiber: 400G-DR4

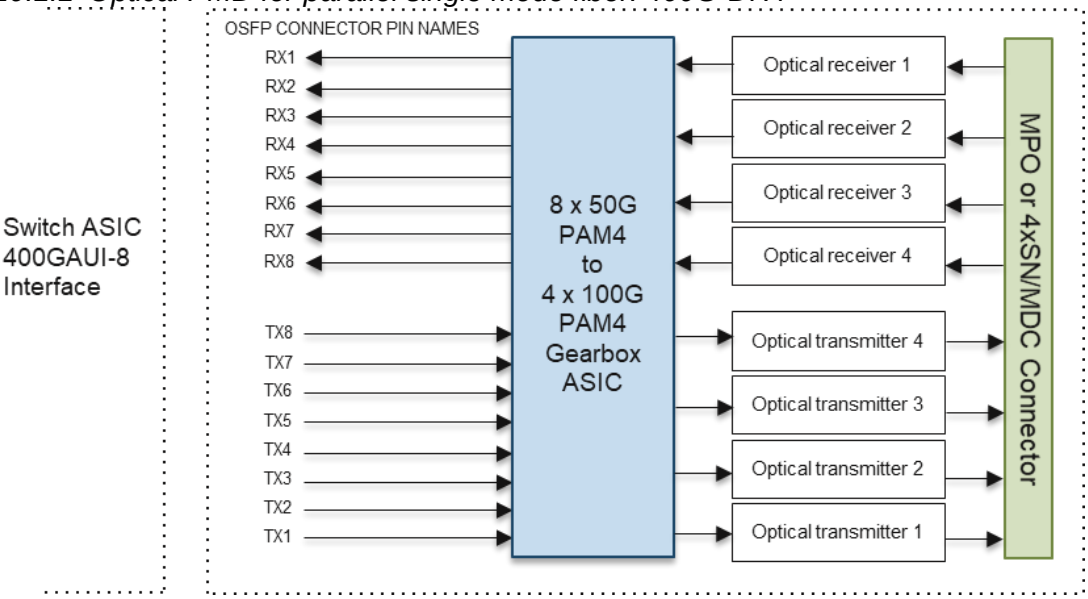


Figure 10-1: Block diagram for 400G-DR4

10.1.2 Optical PMD for parallel multi mode fiber: 400G-SR8

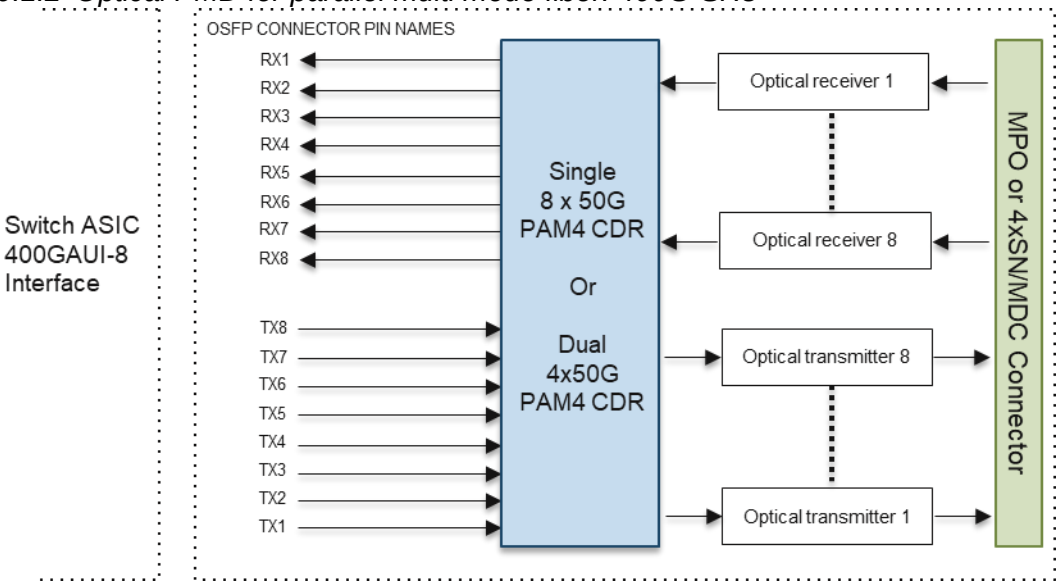


Figure 10-2: Block diagram for 400G-SR8

10.1.3 Optical PMD for parallel multi mode fiber: 400G-SR4.2

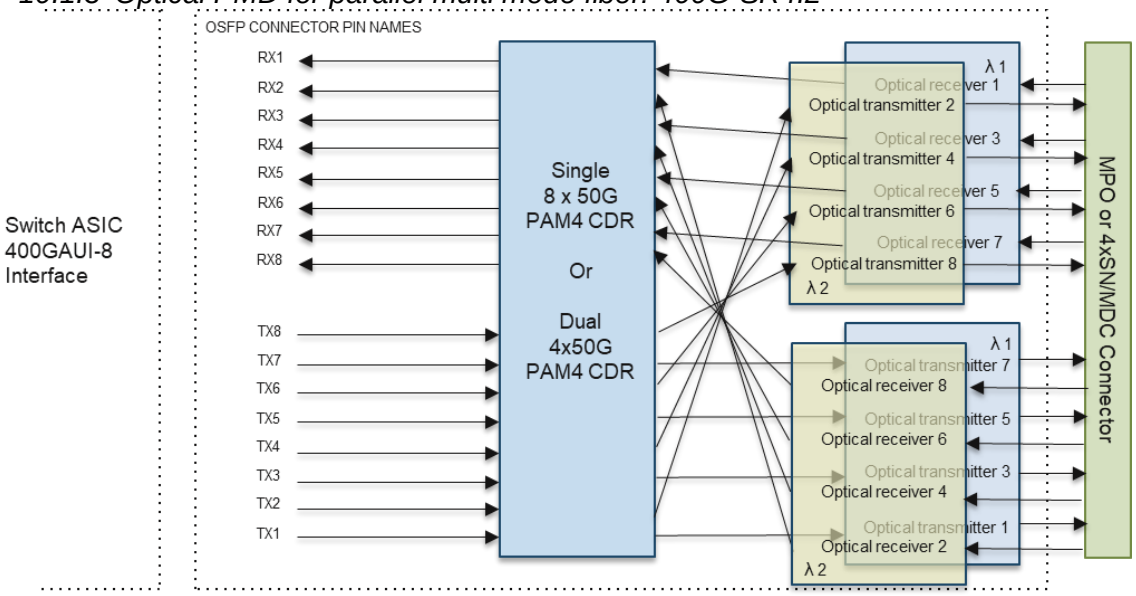


Figure 10-3: Block diagram for 400G-SR4.2

10.1.4 Optical PMD for duplex single mode fiber: 400G-FR4

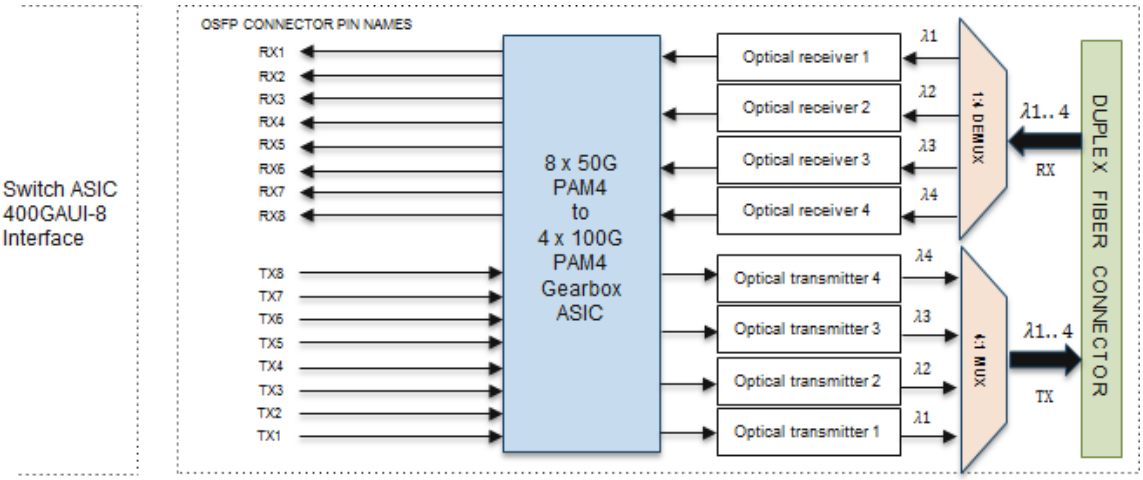


Figure 10-4: Block diagram for 400G-FR4

10.1.5 Optical PMD for duplex single mode fiber: 400G-FR8/LR8

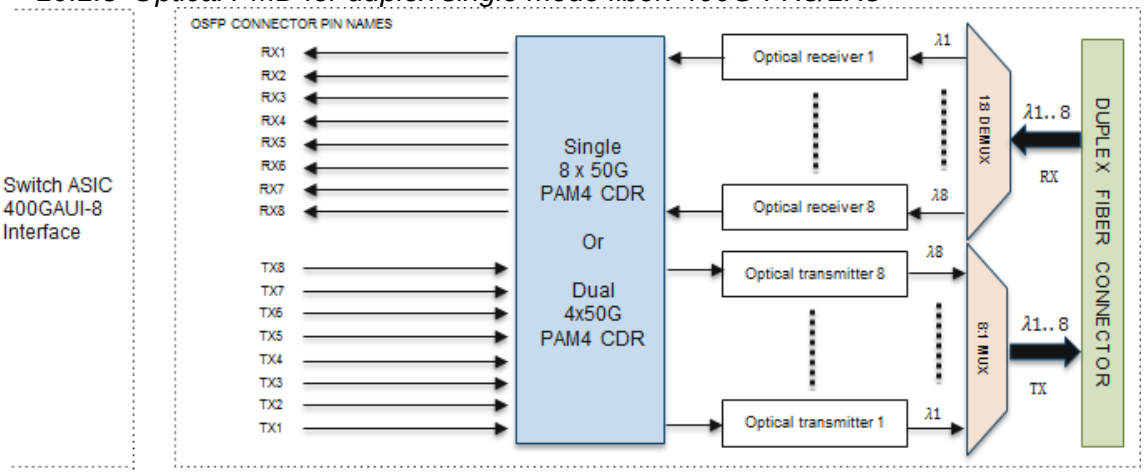


Figure 10-5: Block diagram for 400G-FR8/LR8

10.1.6 Optical PMD for dual duplex single mode fiber: 2x200G-2xFR4

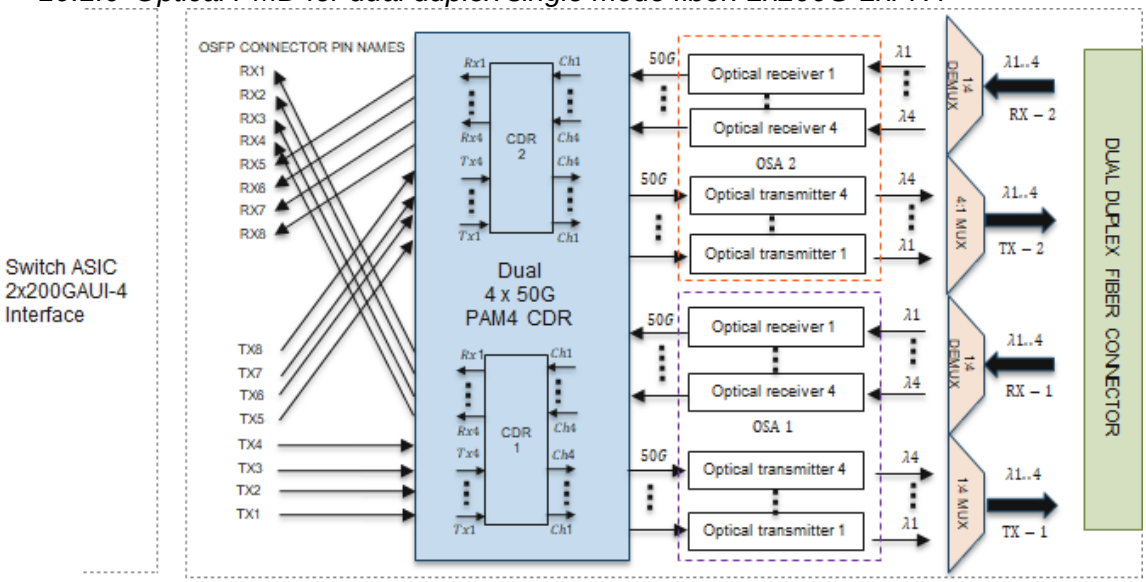


Figure 10-6: Block diagram for 2x200G-2xFR4

10.1.7 Optical PMD for dual duplex single mode fiber: 2x100G-2xCWDM4

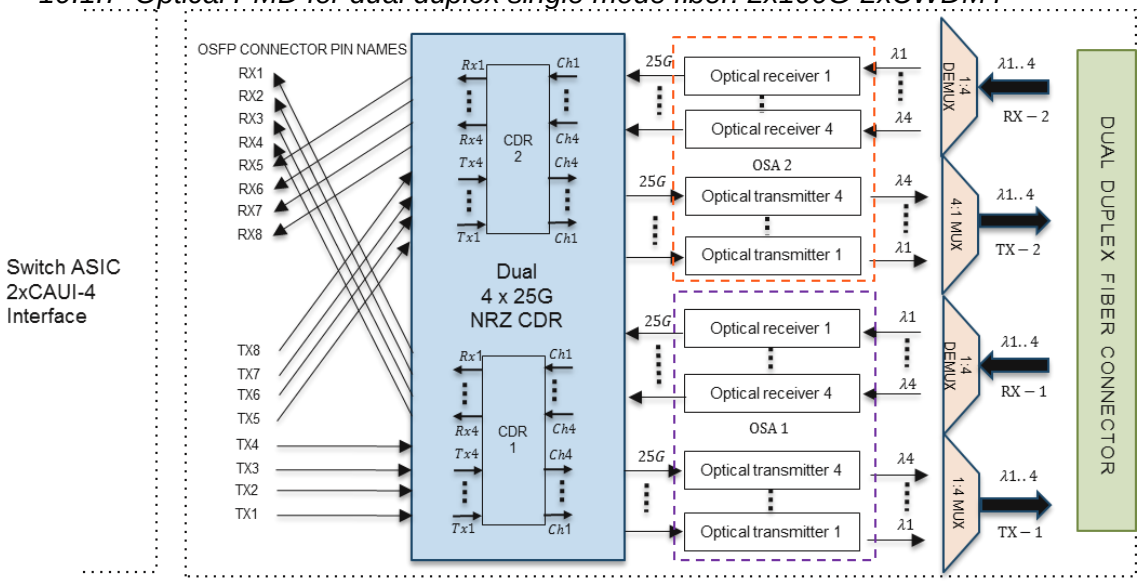


Figure 10-7: Block diagram for 2×100G-2xCWDM4

10.2 800G PMD Block Diagrams

10.2.1 Optical PMD for 1λ SMF solution: 800G DR8

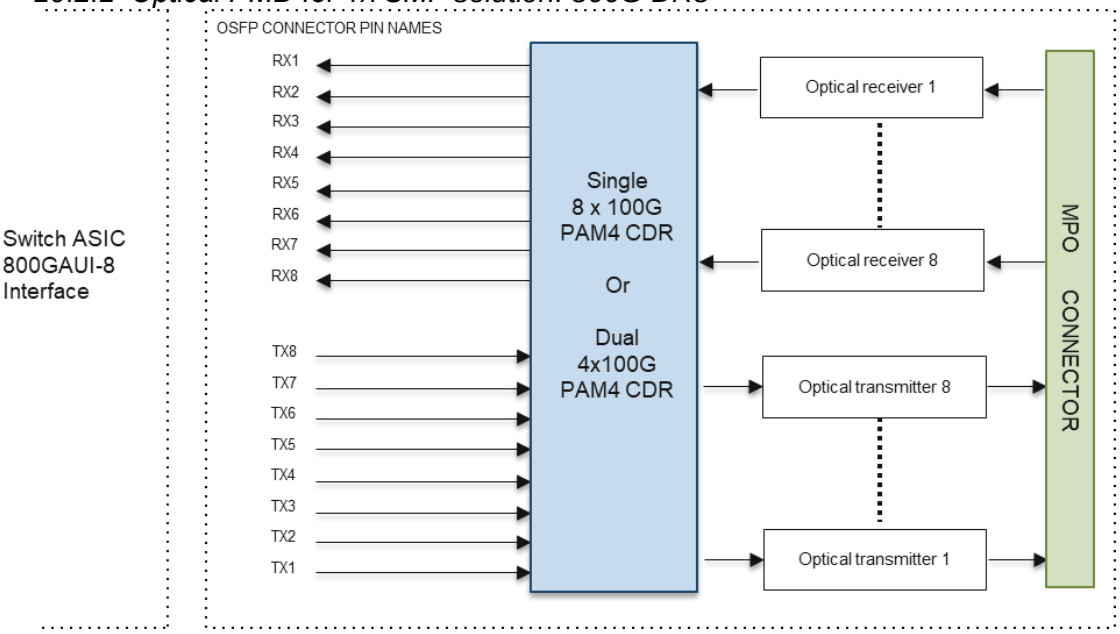


Figure 10-8: Block diagram for 800G OSFP optical PMD for parallel fiber, e.g. 800G DR8

10.2.2 Optical PMD for 2λ SMF/MMF solution: 800G BD4.2

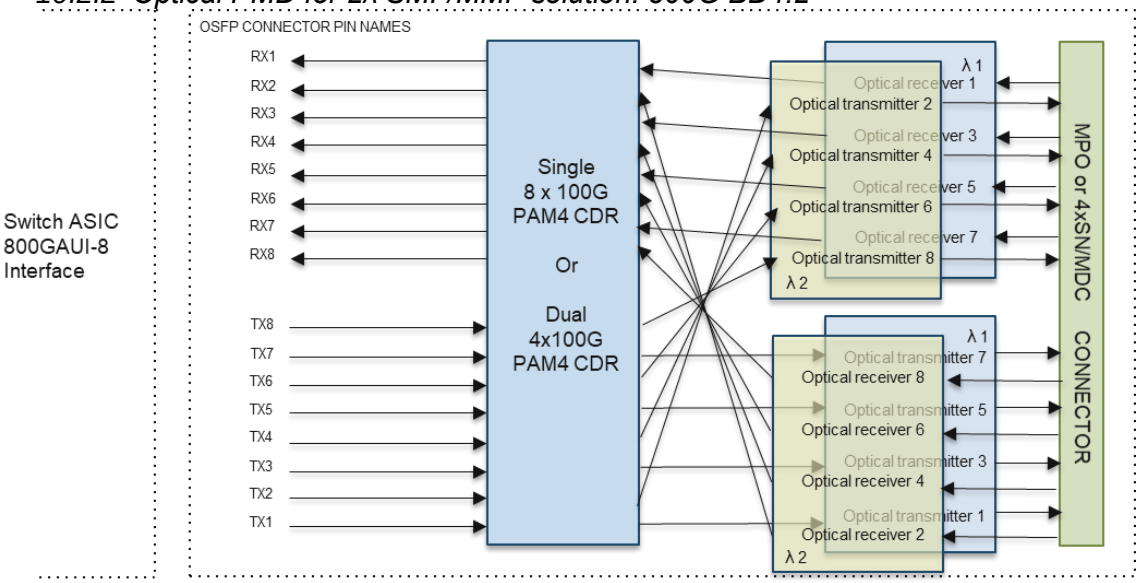


Figure 10-9: Block diagram for 800G-BD4.2

10.2.3 Optical PMD for 4λ SMF solution: 2xFR4

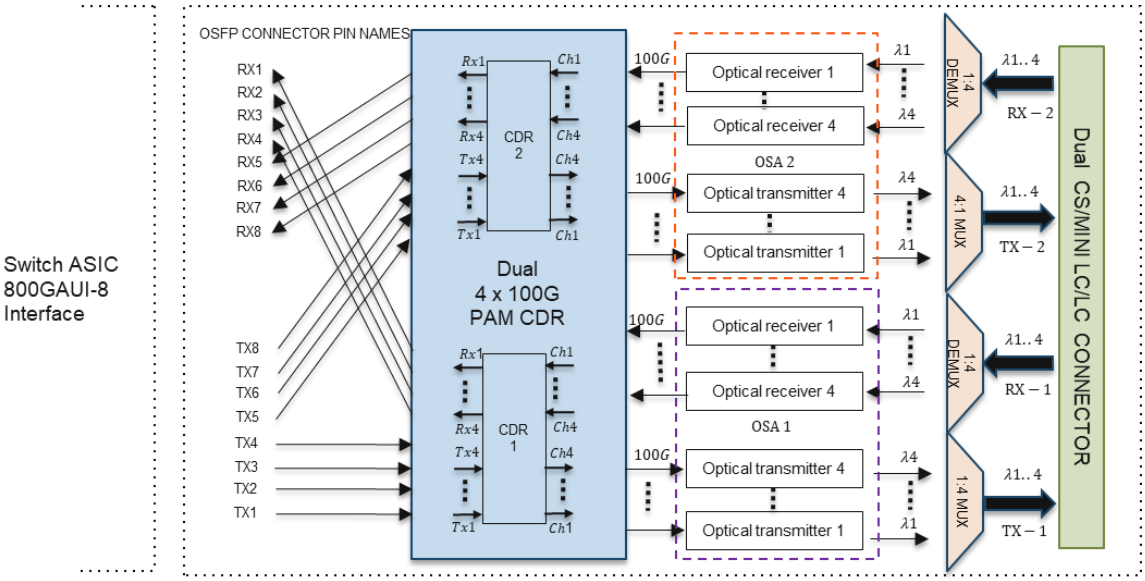


Figure 10-10: Block diagram for 2x400G FR4

10.2.4 Optical PMD for 4λ SMF solution: FR4

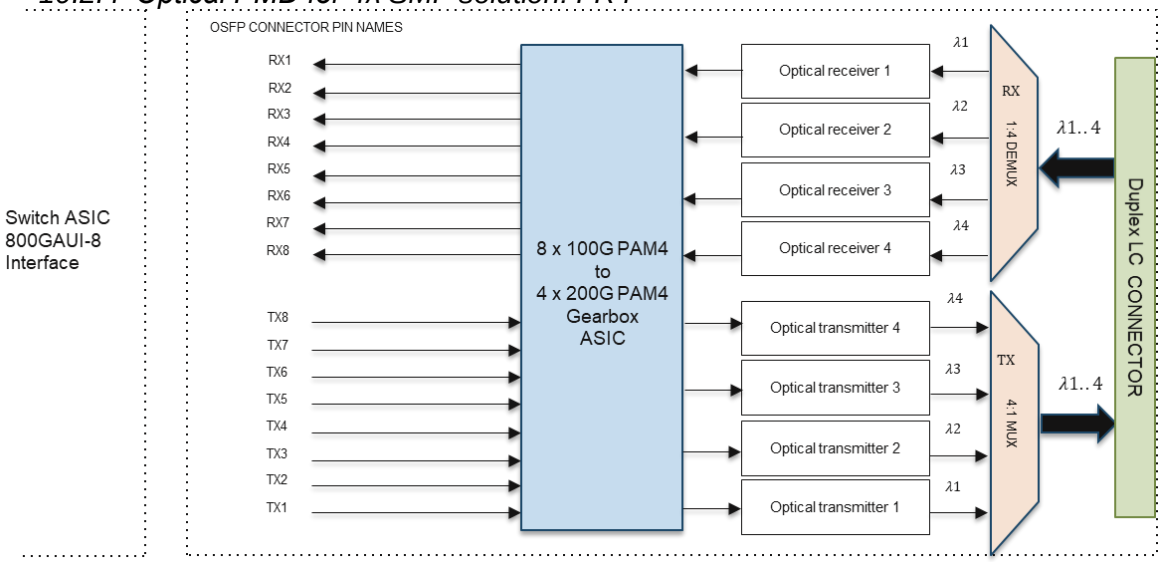


Figure 10-11: Block diagram for 800G OSFP optical PMD for duplex fiber, e.g. 800G FR4

10.2.5 Optical PMD for 8λ SMF solution: FR8/LR8

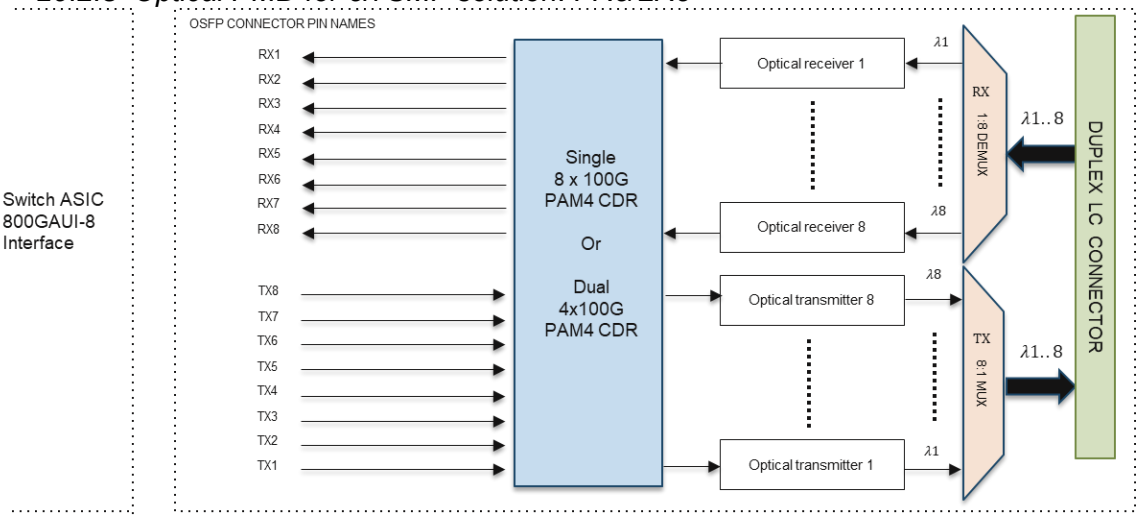


Figure 10-12: Block diagram for 800G OSFP optical PMD for duplex fiber, e.g. 800G, FR8/LR8

10.2.6 Optical PMD for 1λ MMF solution: 800G SR8

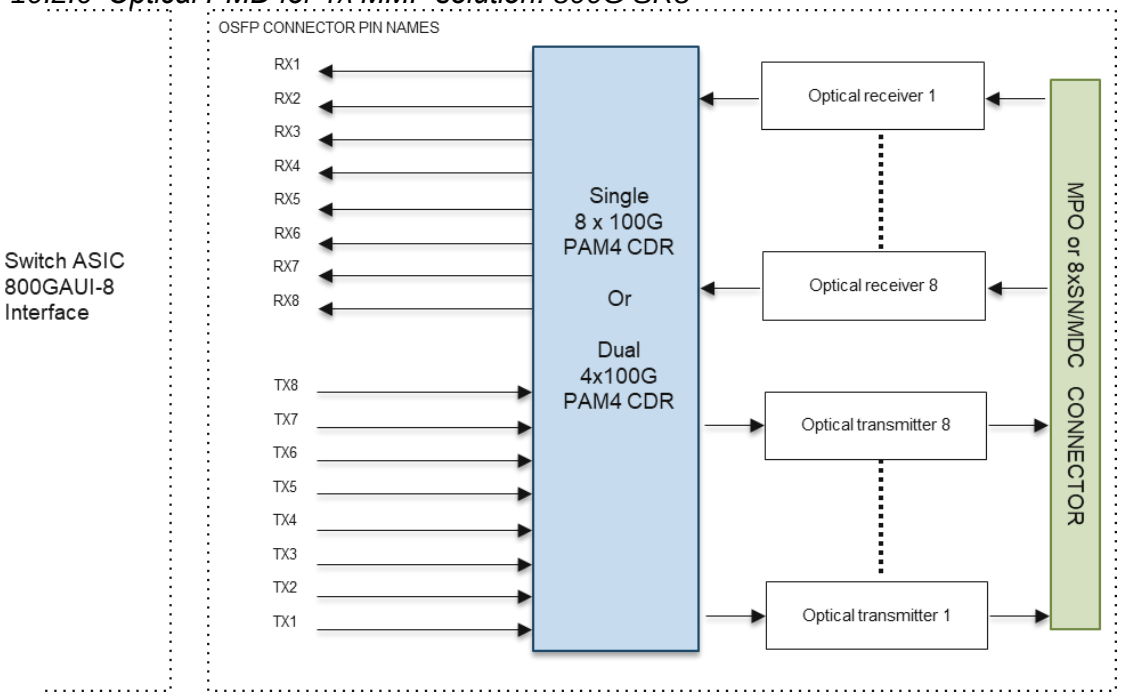


Figure 10-13: Block diagram for 800G OSFP optical PMD for parallel fiber, e.g. 800G SR8

10.2.7 Optical PMD for 4λ MMF solution : 2xSWDM4

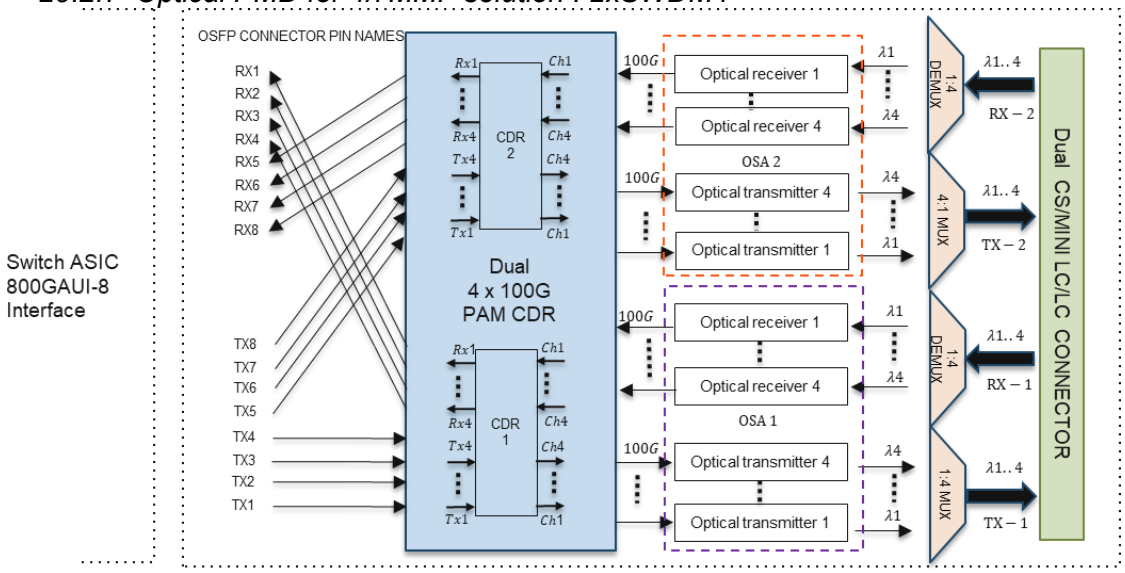


Figure 10-14: Block diagram for 2x400G SWDM4

10.3 OSFP Optical Interface

Optical interfaces that can be used for the OSFP modules are illustrated below. These interfaces are meant to be guideline. The centerline of the optical interface to be aligned with module centerline within 2mm.

10.3.1 Duplex LC Optical Interface

Figure 10-15 shows channel orientation of the optical connector when a duplex LC connector as in IEC 61754-20 is used in an OSFP module. The view is from the front of a typical OSFP module, but actual OSFP module design of the heat sink or height of the optical connector may be different from shown.

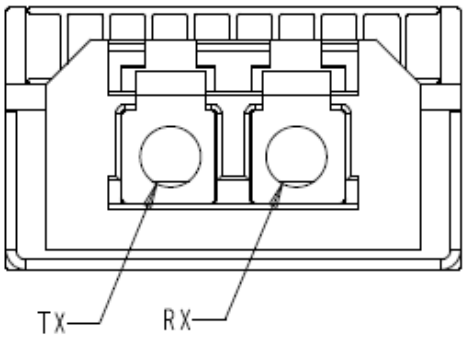
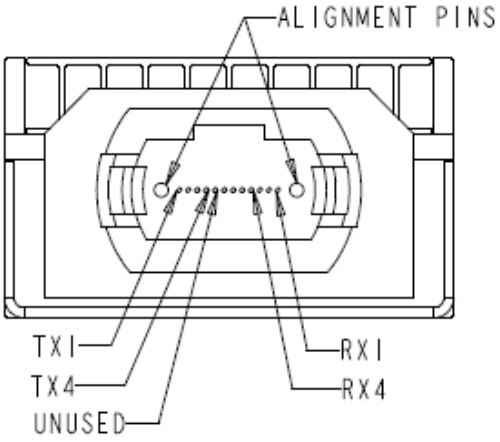


Figure 10-15: Optical receptacle and channel orientation for duplex LC connector

10.3.2 MPO-12 Optical Interface

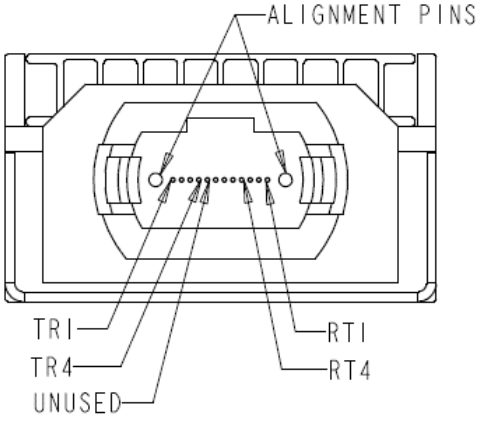
Figure 10-16 shows channel orientation of the optical connector when a male MPO-12 connector as in the IEC 61754-7-1 is used in an OSFP module for applications except 400G-SR4.2.




```
      Channels              Tx1 Tx2 Tx3 Tx4 x x x x Rx4 Rx3 Rx2 Rx1
(x: unused position)
```

Figure 10-16: Optical receptacle and channel orientation for MPO-12 connector

Figure 10-17 shows the channel orientation of the optical connector and signal lane mapping when a male MPO-12 connector is used in an OSFP module for 400G-SR4.2 application. There are two signals on two different wavelengths traveling on opposite directions inside each single fiber, as in the example shown in the section 10.1.3.



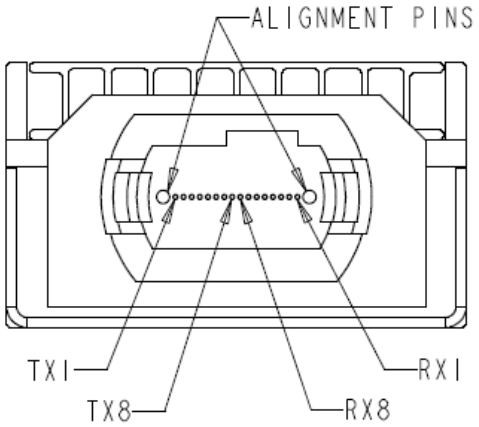
MPO Ferrule Names	TR1 TR2 TR3 TR4 x x x x RT4 RT3 RT2 RT1
Signal Names (λ1)	Tx1 Tx3 Tx5 Tx7 x x x x Rx7 Rx5 Rx3 Rx1
Signal Names (λ2)	Rx2 Rx4 Rx6 Rx8 x x x x Tx8 Tx6 Tx4 Tx2

Figure 10-17: Optical receptacle and channel orientation for MPO-12 for 400G-SR4.2

Fiber connectors that have the same footprint as the MPO connector, such as AirMT®, or 3M EBO-MP12/16, will use the same guideline for channel orientation as the MPO interface as in this section and 10.3.3, 10.3.4 and 10.3.11.

10.3.3 MPO-16 Optical Interface

Figure 10-18 shows channel orientation of the optical connector when a male MPO-16 connector as in the TIA-604-18 is used in an OSFP module.

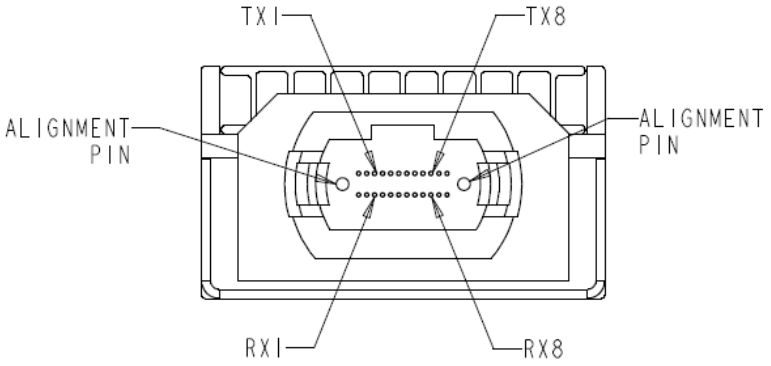


Channels	Tx1 Tx2 Tx3 Tx4 Tx5 Tx6 Tx7 Tx8 Rx8 Rx7 Rx6 Rx5 Rx4 Rx3 Rx2 Rx1

Figure 10-18: Optical receptacle and channel orientation for MPO-16 connector

10.3.4 MPO-12 Two Row Optical Interface

Figure 10-19 shows channel orientation of the optical connector when a male MPO-12 Two Row connector as in the TIA-604-18 is used in an OSFP module.



Channels	x	x	Tx1	Tx2	Tx3	Tx4	Tx5	Tx6	Tx7	Tx8	x	x
(x: unused position)	x	x	Rx1	Rx2	Rx3	Rx4	Rx5	Rx6	Rx7	Rx8	x	x

Figure 10-19: Optical receptacle and channel orientation for MPO-12 Two Row connector

10.3.5 MXC Optical Interface

Figure 10-20 shows channel orientation of a MXC connector with 16 fibers when it is used in the OSFP module.

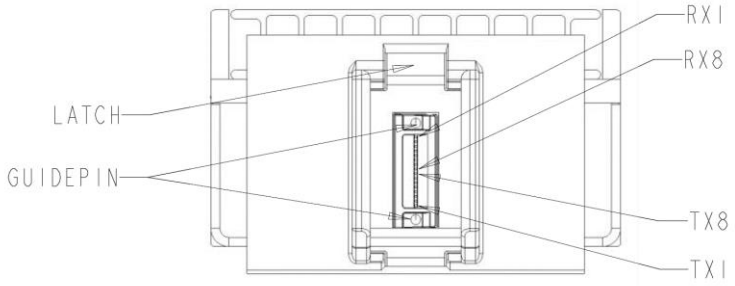


Figure 10-20: Optical receptacle and channel orientation for MXC connector

10.3.6 Dual Mini-LC Optical Interface

Figure *10-21* shows channel orientation of the optical connector when two Mini-LC connectors are used in side by side, consisting a dual mini-LC for an OSFP module.
Drawing below shows 11.35mm of pitch between the mini duplex LC connectors.
Note that the allowable size of the mating optical connector can be affected by the pitch of the ports on the module design and the optical connector design.

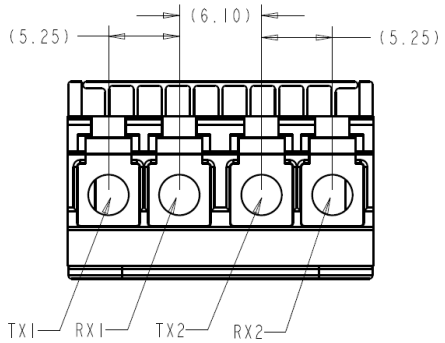


Figure 10-21*: Optical receptacle and channel orientation for Dual Mini-LC*

10.3.7 Dual Duplex LC Optical Interface

Figure 10-22 shows channel orientation of the optical connector when two duplex LC connectors are used as belly to belly, consisting of a dual duplex LC for an OSFP module.

Note that the allowable size of the mating optical connector can be affected by the pitch of the ports on the module design and the optical connector design. Figure 10-23 depicts the limitation of the size of the LC connector, if there is no interference with the latch release mechanism. This configuration might be implemented in a Type 2 OSFP, as depicted in the Figure 3-3 and Figure 10-22.

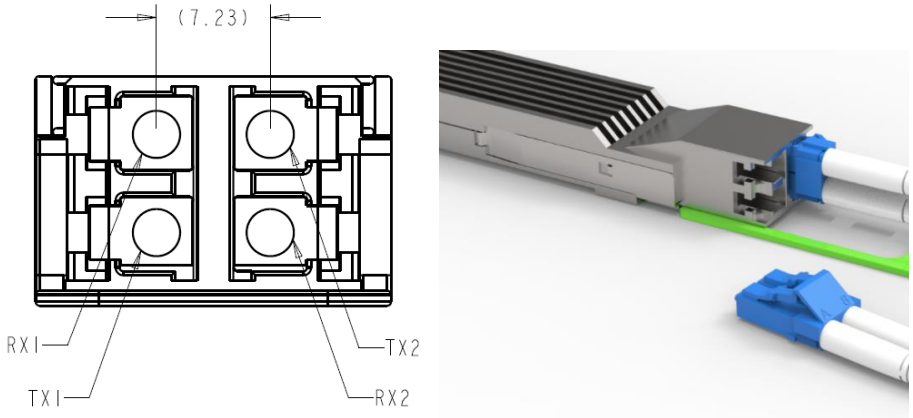


Figure 10-22: Optical receptacle and channel orientation for Dual LC, with an example

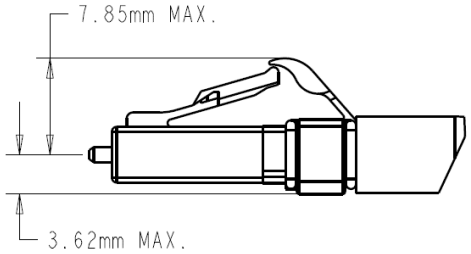


Figure 10-23: LC connector size requirement per given belly-to-belly pitch

10.3.8 Dual CS® Optical Interface

Figure 10-24 shows channel orientation of the optical connector when a dual CS® connector is used in an OSFP module. Receptacle 1 (Tx1, Rx1) and receptacle 2 (Tx2, Rx2) are connected with two separate independent duplex fiber cables.

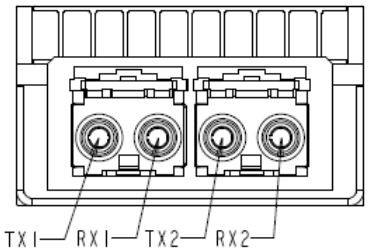
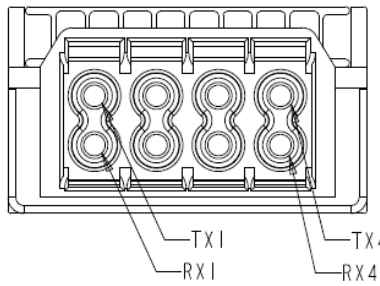


Figure 10-24: Optical receptacle and channel orientation for dual CS® connector

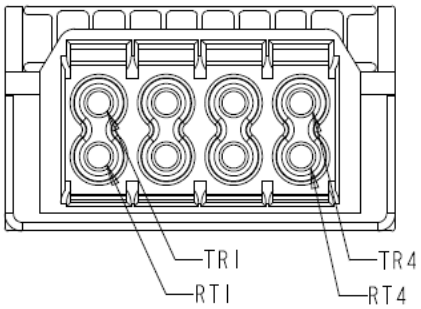
10.3.9 Quad MDC Optical Interface

Figure 10-25 shows channel orientation of the optical connector when a quad MDC connector is used in an OSFP module. Receptacle 1 (Tx1, Rx1), receptacle 2 (Tx2, Rx2), receptacle 3 (Tx3, Rx3), and receptacle 4 (Tx4, Rx4) are connected with four separate independent duplex fiber cables. Figure 10-26 shows for the 400G-SR4.2.



Channels	Tx1	Tx2	Tx3	Tx4
	Rx1	Rx2	Rx3	Rx4

Figure 10-25: Optical receptacle and channel orientation for quad MDC connector for 400G DR-4

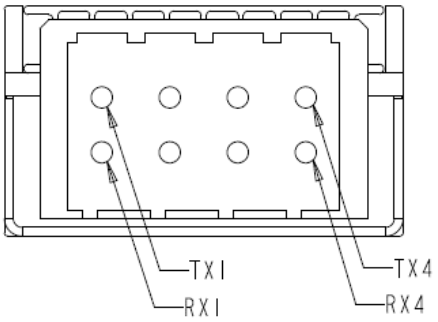


Quad MDC Ferrule Names	**TR1**	**TR2**	**TR3**	**TR4**
Signal Names (λ1)	Tx1	Tx3	Tx5	Tx7
Signal Names (λ2)	Rx2	Rx4	Rx6	Rx8
Quad MDC Ferrule Names	**RT1**	**RT2**	**RT3**	**RT4**
Signal Names (λ1)	Rx1	Rx3	Rx5	Rx7
Signal Names (λ2)	Tx2	Tx4	Tx6	Tx8

Figure 10-26: Optical receptacle and channel orientation for quad MDC connector for 400G-SR4.2

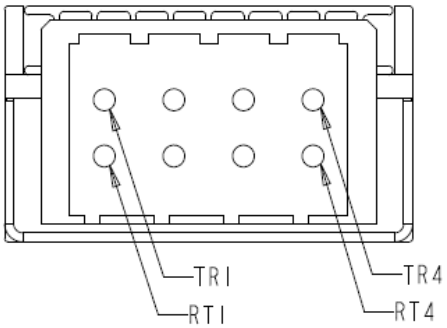
10.3.10 Quad SN® Optical Interface

Figure 10-27 and Figure 10-28 shows channel orientation of the optical connector when a quad SN® connector is used in an OSFP module. Receptacle 1 (Tx1, Rx1), receptacle 2 (Tx2, Rx2), receptacle 3 (Tx3, Rx3), and receptacle 4 (Tx4, Rx4) are connected with four separate independent duplex fiber cables.



Channels	Tx1	Tx2	Tx3	Tx4
	Rx1	Rx2	Rx3	Rx4

Figure 10-27: Optical receptacle and channel orientation for Quad SN® connector for 400G-DR4



Quad SN Ferrule Names	**TR1**	**TR2**	**TR3**	**TR4**
Signal Names (λ1)	Tx1	Tx3	Tx5	Tx7
Signal Names (λ2)	Rx2	Rx4	Rx6	Rx8
Quad SN Ferrule Names	**RT1**	**RT2**	**RT3**	**RT4**
Signal Names (λ1)	Rx1	Rx3	Rx5	Rx7
Signal Names (λ2)	Tx2	Tx4	Tx6	Tx8

Figure 10-28: Optical receptacle and channel orientation for Quad SN® connector for 400G SR4.2

10.3.11 Dual MPO Optical Interface

Figure 10-29 shows channel orientation of the optical connector when dual MPO-12 connectors are used in an OSFP module. MPO-12 connectors, which channel assignment within the connector to be as in the Figure 10-16, will be used as depicted in the figure. Note that the allowable size of the mating optical connector can be affected by the pitch of the ports on the module design and the optical connector design, as in the Figure 10-30. This configuration might be implemented in a Type 2 OSFP, as depicted in the Figure 3-3 and Figure 10-31.

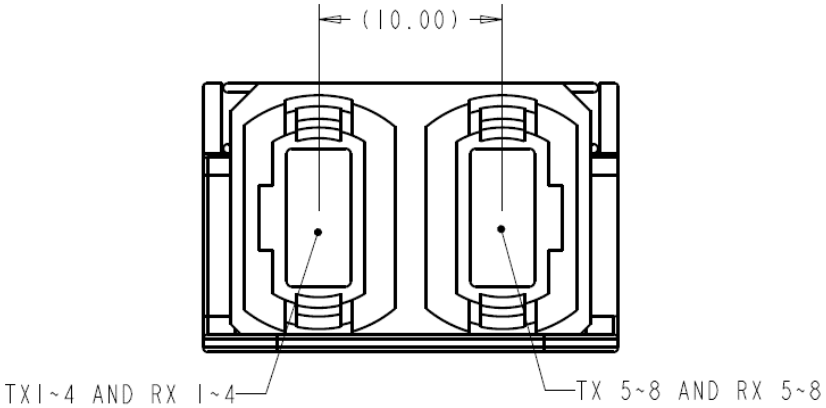


Figure 10-29: Optical receptacle and channel orientation for Dual MPO connector

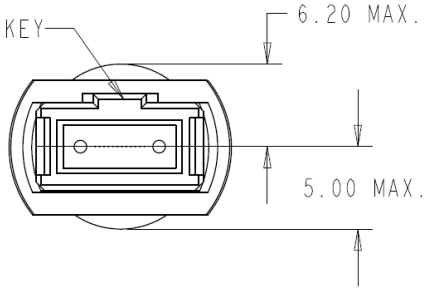


Figure 10-30: MPO connector size requirement per given belly-to-belly pitch

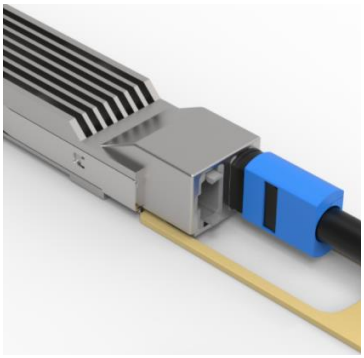


Figure 10-31: Example of an OSFP module with Dual MPO connector

10.3.12 Dual MXC Optical Interface

Figure 10-32 shows channel orientation of the optical connector when dual MXC connectors are used in an OSFP module. Connector 1 will be used for the first half of the channels of the module (TX1~4 and RX 1~4) while the Connector 2 will be used for the second half of the channels of the module (TX5~8 and RX 5~8). Figure 10-33 shows an example of OSFP with dual MXC connectors. This configuration might be implemented in a Type 2 OSFP, as depicted in the Figure 3-3.

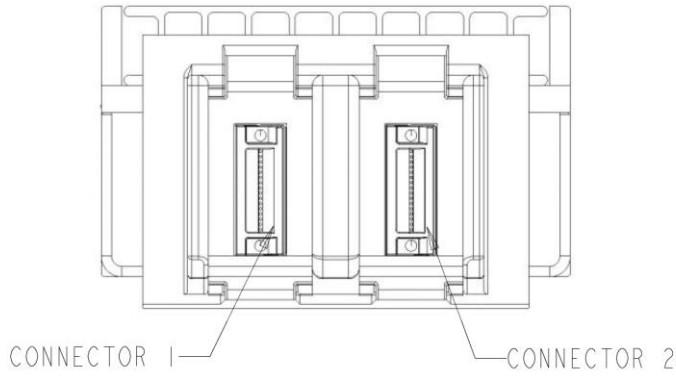


Figure 10-32: Optical receptacle and channel orientation for Dual MXC connector

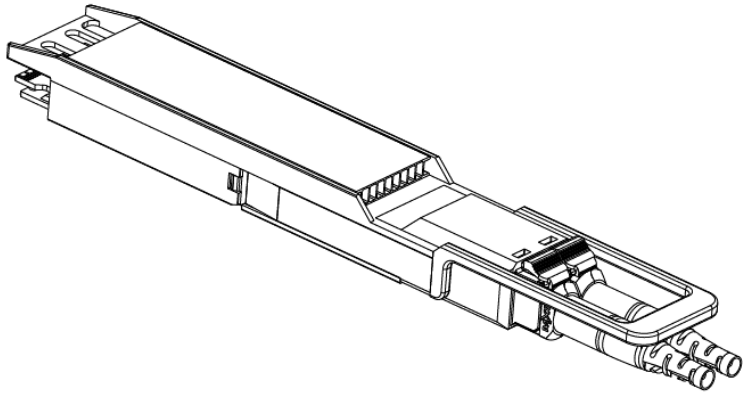


Figure 10-33: Example of an OSFP module with Dual MXC connector

10.3.13 8 x MDC Optical Interface

In addition to the section 10.3.9, 8 MDC connectors can be placed to an OSFP module as in the Figure 10-34. This configuration might be implemented in a Type 3 OSFP, as depicted in the Figure 3-3 and Figure 10-35.

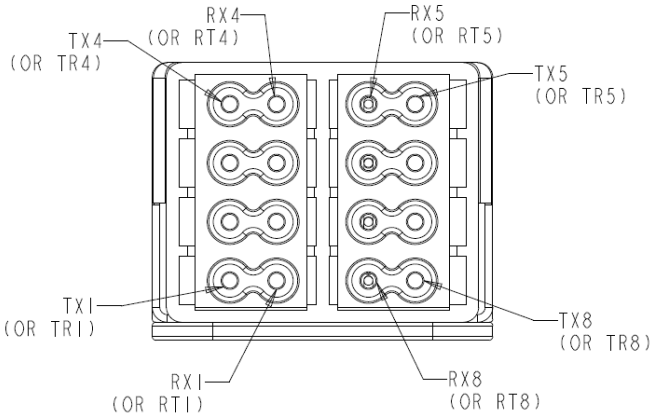


Figure 10-34: Optical receptacle and channel orientation for 8 x MDC connector

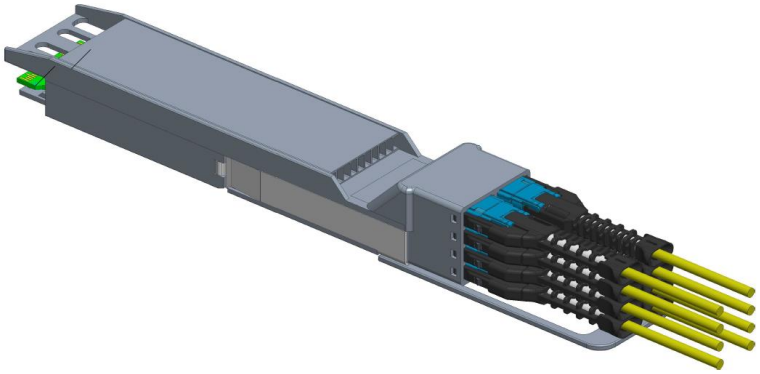


Figure 10-35: Example of a Type 3 OSFP with 8 x MDC connector

10.3.14 8 x SN® Optical Interface

In addition to the section 10.3.9, 8 SN® connectors can be placed to an OSFP module as in the Figure 10-36. This configuration might be implemented in a Type 3 OSFP, as depicted in the Figure 3-3.

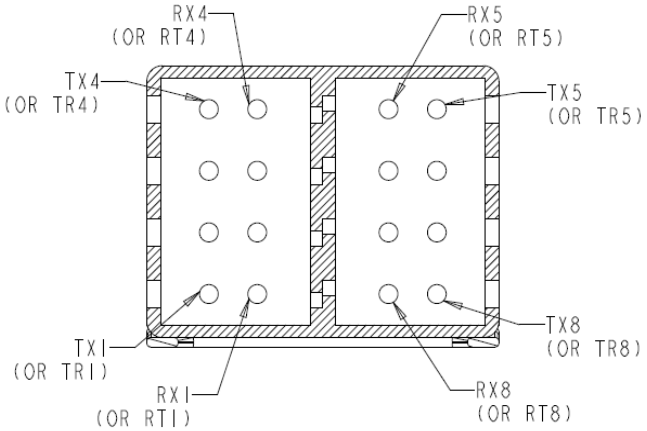


Figure 10-36: Optical receptacle and channel orientation for 8 x SN® connector

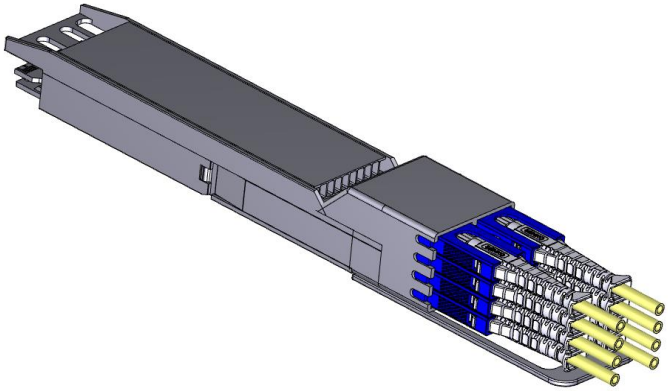


Figure 10-37: Example of a Type 3 module with 8 x SN® connector

11 Electrical Interface

11.1 Module Electrical Connector

The electrical interface of an OSFP module consists of a 60 contacts edge connector as illustrated by the diagram in Figure 11-1. It provides 16 contacts for 8 differential pairs of high-speed transmit signals, 16 contacts for 8 differential pairs of high-speed receive signals, 4 contacts for low-speed control signals, 4 contacts for power and 20 contacts for ground.

The edge connector pads have 3 different pad lengths to enable sequencing of the contacts to protect the module against electrostatic discharge (ESD) and provide reliable power up/power down sequencing for the module during insertion and removal. The ground pads are the longest for first contact, the power pads are the second longest for second contact and the signal pads are the third longest for final contact during insertion.

The chassis ground (case common) of the OSFP module shall be isolated from the module's circuit ground, GND, to provide the equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module. When an OSFP module is not installed, the signals to the connector within the unused cage should be disabled to minimize electromagnetic interference (EMI) emissions.

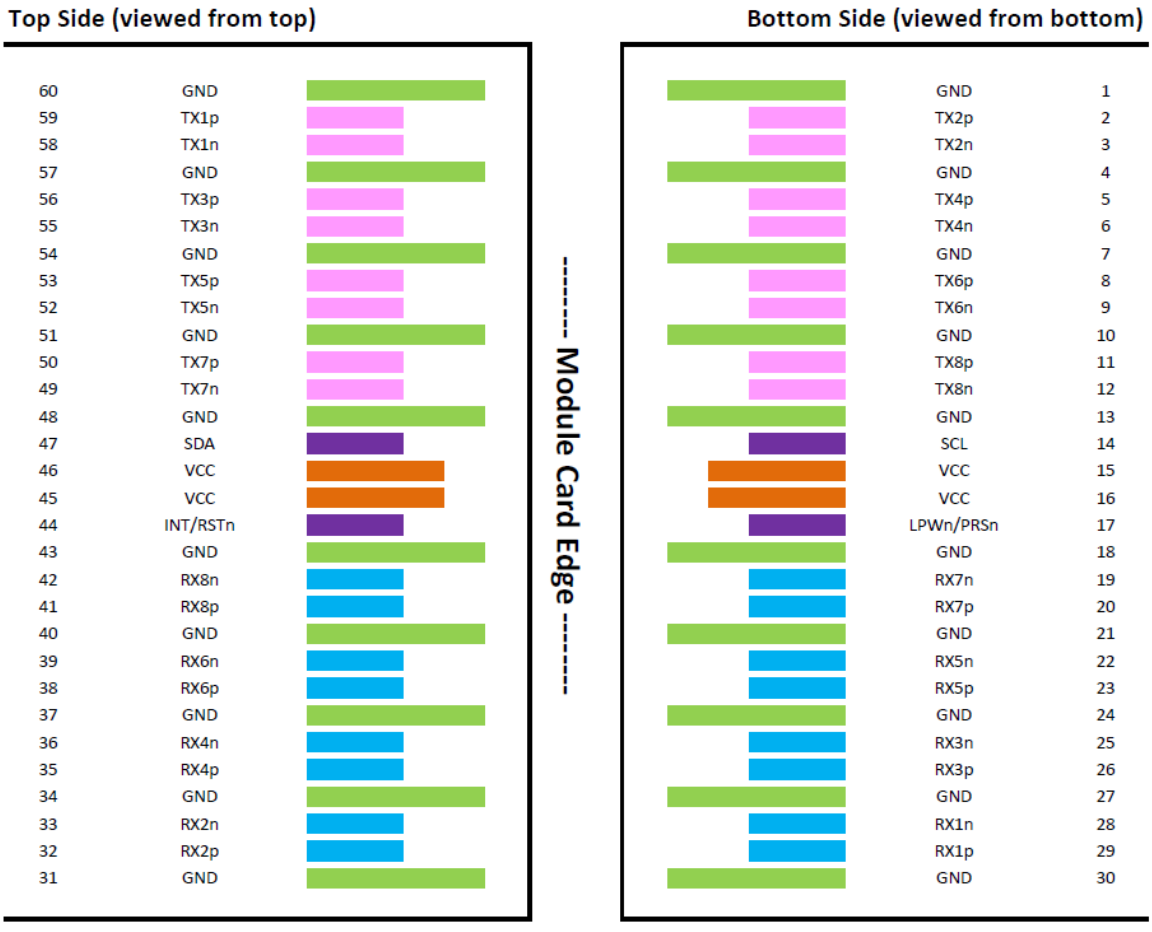


Figure 11-1: OSFP module pinout

11.2 Pin Descriptions

Table 11-1: OSFP module signal pin descriptions

Name	Direction	Description
TX[8:1]p	input	Transmit differential pairs from host to module.
TX[8:1]n	input	
RX[8:1]p	output	Receive differential pairs from module to host.
RX[8:1]n	output	
SCL	bidir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host.
SDA	bidir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.
LPWn/PRSn	bidir	Multi-level signal for low power control from host to module and module presence indication from module to host. This signal requires the circuit as described in Section 11.5.3
INT/RSTn	bidir	Multi-level signal for interrupt request from module to host and reset control from host to module. This signal requires the circuit as described in Section 11.5.2
VCC	power	3.3V power for module.
GND	ground	Module Ground. Logic and power return path.

11.3 Pin List

Table 11-2: OSFP connector pin list

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

11.4 High-Speed Signals

The high-speed signals consist of 8 transmit and 8 receive differential pairs identified as TX[8:1]p / TX[8:1]n and RX[8:1]p / RX[8:1]n. These signals can be operated in port configurations of either a single 8-lanes, dual 4-lanes, quad 2-lanes or 8 individual lanes depending on the capability of the host ASIC.

800GAUI-8 mode provides 8 differential lanes using 112G-PAM4 signaling operating at 53.125 GBaud. This results in 8 lanes of 100Gb/s for a total of 800Gb/s. This mode allows connection to PMD configurations of 1x800G, 2x400G, 4x200G or 8x100G.

400GAUI-8 mode provides 8 differential lanes using 56G-PAM4 signaling operating at 26.5625 GBaud. This results in 8 lanes of 50Gb/s for a total of 400Gb/s. This mode allows connection to PMD configurations of 1x400G, 2x200G, 4x100G or 8x50G.

Dual CAUI-4 mode provides 8 differential lanes using 25G-NRZ signaling operating at 25.78125 GBaud. This results in 8 lanes of 25Gb/s for a total of 200Gb/s. This mode allows connection to PMD configurations of 2x100G, 4x50G or 8x25G.

The high-speed signals follow the electrical specifications of IEEE802.3bs, IEEE802.3cd, IEEE802.3ck and CEI-56G-VSR-PAM as defined in OIF-CEI-04.0 for 400GAUI-8 mode and IEEE802.3bj, IEEE802.3bm for CAUI-4 mode.

The lane assignments in Table 11-3 shall be used for the different PMD configurations.

Table 11-3: High-speed signal lane mapping

(*L means Lane, L1 means Lane 1 in the port.)

PMD Configuration	Transmit and Receive Lane Assignments							
	L1	**L2**	**L3**	**L4**	**L5**	**L6**	**L7**	**L8**
1x800G (112G-PAM4) 1x400G (56G-PAM4)	Port 1							
2x400G (112G-PAM4) 2x200G (56G-PAM4) 2x100G (25G-NRZ)	Port 1				Port 2			
	L1*	L2	L3	L4	L1	L2	L3	L4
4x200G (112G-PAM4) 4x100G (56G-PAM4) 4x50G (25G-NRZ)	Port 1		Port 2		Port 3		Port 4	
	L1	L2	L1	L2	L1	L2	L1	L2
8x100G (112G-PAM4) 8x50G (56G-PAM4) 8x25G (25G-NRZ)	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8

11.5 Low-Speed Signals

There are 4 low-speed signals consisting of SCL, SDA, LPWn/PRSn and INT/RSTn. These signals are used for configuration and control of the module by the host. SCL and SDA use 3.3V LVCMOS levels and are bidirectional signals. LPWn/PRSn and INT/RSTn have additional circuitry on the host and module to enable multi-level bidirectional signaling.

11.5.1 SCL and SDA

SCL and SDA are a 2-wire serial interface between the host and module using the I^2C or I3C protocols. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3V on the host. The pull-up resistor value shall be 1k ohms to 4.7k ohms depending on capacitive load.

This 2-wire interface supports bus speeds:

- Required - I^2C Fast-mode (Fm) ≤ 400 kbit/s
- Optional - I^2C Fast-mode Plus (Fm+) ≤ 1 Mbit/s
- Optional - I3C Single Data Rate (SDR) ≤ 12.5 Mbit/s

The host shall default to using 100 kbit/s standard-mode I^2C when first accessing an unidentified module for backward compatibility. Once the module has been brought out of reset, the host can read the module's 2-wire interface speed register to determine the maximum supported speed the module allows. For an OSFP, the host may then use I^2C Fast-mode, I^2C Fast-mode Plus or I3C Single Data Rate, as indicated by the module. It is optional for the host to change the speed of the 2-wire interface but remaining at a low speed could lead to slow management transactions for modules that require frequent accesses.

SCL and SDA signals follow the electrical specifications of Fast-mode, and Fast-mode Plus as defined in the I^2C-bus specification or Single Data Rate mode as defined in the Specification for I3C.

11.5.2 INT/RSTn

INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module. The circuit shown in Figure 11-3 enables multi-level signaling to provide direct signal control in both directions. Reset is an active-low signal on the host which is translated to an active-low signal on the module. Interrupt is an active-high signal on the module which gets translated to an active-low signal on the host.

The INT/RSTn signal operates in 3 voltage zones to indicate the state of Reset for the module and Interrupt for the host. Figure 11-2 shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_INTn signal and the module uses a voltage reference at 1.25V to determine the state of the M_RSTn signal.

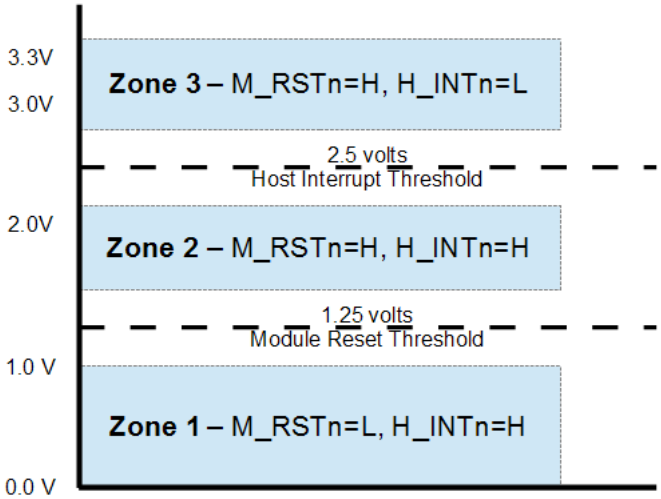


Figure 11-2: INT/RSTn voltage zones

- Zone 1 – Reset operation – Zone 1 is the state when the module is in reset and interrupt deasserted (M_RSTn=Low, H_INTn=High). The min/max voltages for Zone 1 are defined by parameters V_INT/RSTn_1 and V_INT/RSTn_2 in Table 11-4.
- Zone 2 – Normal operation – Zone 2 is the normal operating state with reset deasserted (M_RSTn=High) and interrupt deasserted (H_INTn=High). The min/max voltages for Zone 2 are defined by parameter V_INT/RSTn_3 in Table 11-4.

- Zone 3 – Interrupt operation – Zone 3 is the state for the module to assert interrupt and the module must also be out of reset (M_RSTn=High, H_INTn=Low). The min/max voltages for Zone 3 are defined by parameter V_INT/RSTn_4 in Table 11-4.

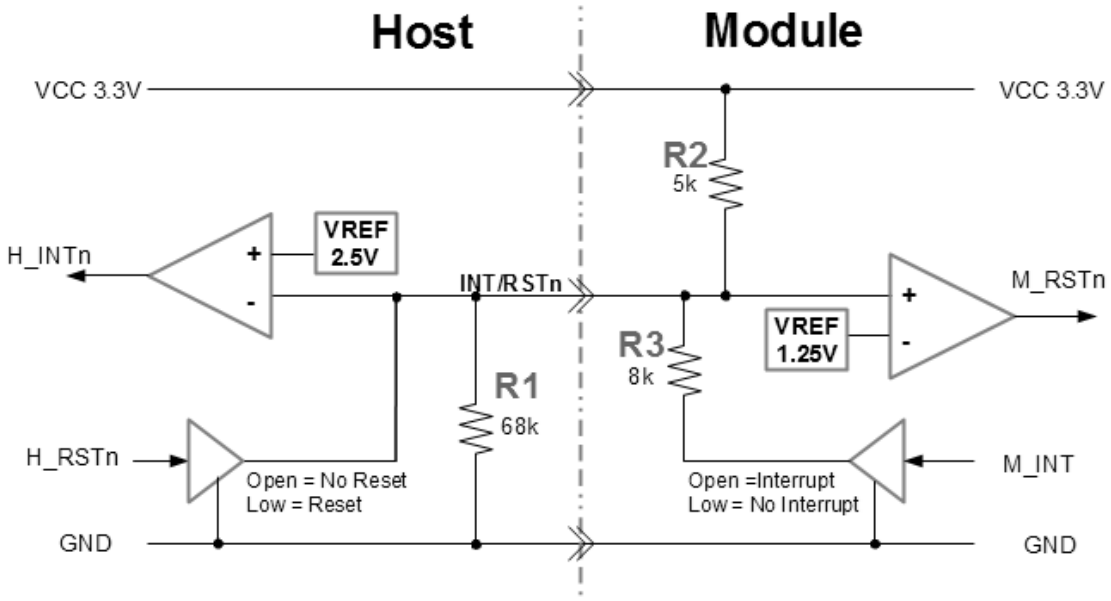


Figure 11-3: INT/RSTn circuit

Table 11-4: INT/RSTn circuit parameters

Parameter	Nominal	Min	Max	Units	Note
Host VCC	3.300	3.135	3.465	Volts	VCC voltage on the Host
H_Vref_INTn	2.500	2.475	2.525	Volts	Precision voltage reference for H_INTn
M_Vref_RSTn	1.250	1.238	1.263	Volts	Precision voltage reference for M_RSTn
R1	68k	66k	70k	Ohms	Recommend 68.1k ohms 1% resistor
R2	5k	4.9k	5.1k	Ohms	Recommend 4.99k ohms 1% resistor
R3	8k	7.8k	8.2k	Ohms	Recommend 8.06k ohms 1% resistor
V_INT/RSTn_1	0.000	0.000	1.000	Volts	INT/RSTn voltage for No Module
V_INT/RSTn_2	0.000	0.000	1.000	Volts	INT/RSTn voltage for Module installed, H_RSTn=Low
V_INT/RSTn_3	1.900	1.500	2.250	Volts	INT/RSTn voltage for Module installed, H_RSTn=High, M_INT=Low
V_INT/RSTn_4	3.000	2.750	3.465	Volts	INT/RSTn voltage for Module installed, H_RSTn=High, M_INT=High

11.5.3 LPWn/PRSn

LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present. The circuit shown in Figure 11-5 enables multi-level signaling to provide direct signal control in both directions. Low Power mode is an active-low signal on the host which gets converted to an active-low signal on the module. Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host.

The LPWn/PRSn signal operates in 3 voltage zones to indicate the state of Low Power mode for the module and Module Present for the host. Figure 11-4 shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_PRSn signal and the module uses a voltage reference at 1.25V to determine the state of the M_LPWn signal.

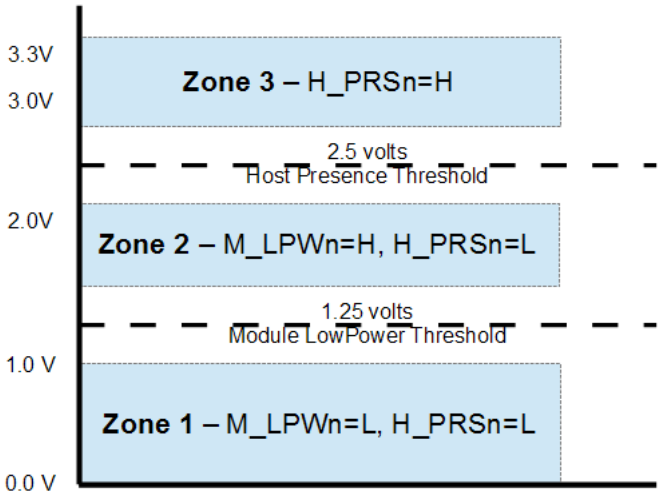


Figure 11-4: LPWn/PRSn voltage zones

- Zone 1 – Low Power mode – Zone 1 is the low power state and module is present (M_LPWn=Low, H_PRSn=Low). The min/max voltages for Zone 1 are defined by parameters V_LPWn/PRSn_1 in Table 11-5.
- Zone 2 – High Power mode – Zone 2 is the high power state and module is present (M_LPWn=High, H_PRSn=Low). The min/max voltages for Zone 2 are defined by parameters V_LPWn/PRSn_2 in Table 11-5.
- Zone 3 – Module Not Present – Zone 3 is the state for when the module is not present (H_PRSn=High). The min/max voltages for Zone 3 are defined by parameters V_LPWn/PRSn_3 in Table 11-5.

Module Removal – If the module is being unplugged and LPWn/PRSn loses contact, the pull-down resistor on the module shall assert Low Power mode on the module (M_LPWn=Low). The module is required to transition to low power (Power Class 1) and disable transmitters within the time specified by T_hplp in Table 11-7. This maximum transition time is to ensure the module is in Low Power mode before the power contacts lose connection to avoid potential damage from arcing.

The LPWn/PRSn signal is driven High or Open by the host for Low Power mode control. If logic is used to generate the High level then 3.3V LVCMOS is preferred.

For very low cost modules, such as DAC, the voltage comparator on the module may be omitted and the LPWn/PRSn pin shall in that case be tied to GND in the module. This type of module may only be used for low power mode (Power Class 1).

The module transmitters must be disabled when in Low Power mode. This ensures Power Class 1 and also provides a fast hardware shut down mechanism for applications such as redundancy switch-over. In addition, software controlled transmitter disable is provided by the TX Disable register via the I^2C interface.

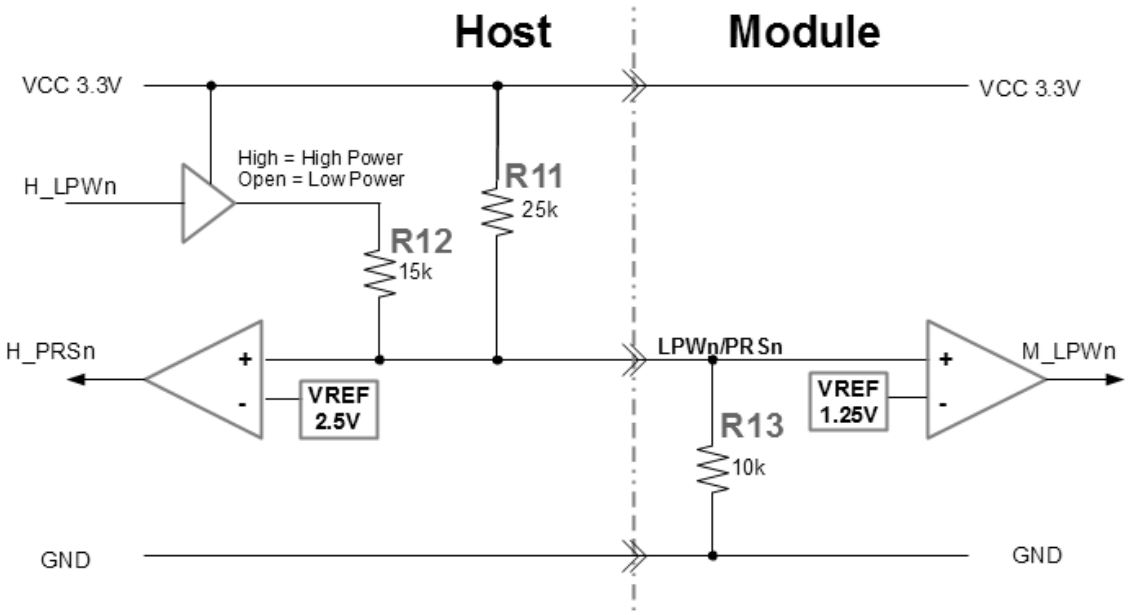


Figure 11-5: LPWn/PRSn circuit

Table 11-5: LPWn/PRSn circuit parameters

Parameter	Nominal	Min	Max	Units	Note
Host VCC	3.300	3.135	3.465	Volts	VCC voltage on the Host
H_Vref_PRSn	2.500	2.475	2.525	Volts	Precision voltage reference for H_PRSn
M_Vref_LPWn	1.250	1.238	1.263	Volts	Precision voltage reference for M_LPWn
R11	25k	24.5k	25.5k	Ohms	Recommend 24.9k ohms 1% resistor
R12	15k	14.7k	15.3k	Ohms	Recommend 15k ohms 1% resistor
R13	10k	9.8k	10.2k	Ohms	Recommend 10k ohms 1% resistor
V_LPWn/PRSn _1	0.950	0.000	1.100	Volts	LPWn/PRSn voltage for Module installed, H_LPWn=Low
V_LPWn/PRSn _2	1.700	1.400	2.250	Volts	LPWn/PRSn voltage for Module installed, H_LPWn=High
V_LPWn/PRSn_3	3.300	2.750	3.465	Volts	LPWn/PRSn voltage for No Module

11.5.4 Timing for control and status functions

The QSFP-DD specification should be followed for any timing of control and status functions that have not been defined in this specification.

11.5.5 OSFP module power up behavior

The OSFP module shall power up when system power is enabled or on module insertion or on VCC power enable to the module. Once powered, the module shall either wait in Low Power mode or enter High Power mode based on the state of the Reset signal, Low Power signal and ForceLowPwr bit of the module. The ForceLowPwr bit default is pre-programmed in the module by the manufacturer and typically would be set to 0. The host can change the ForceLowPwr bit after power up but it shall return to its pre-programmed default when the module is placed in reset or power cycled. The Reset and Low Power signals are described in sections 11.5.2 and 11.5.3. The ForceLowPwr bit is defined in the OSFP Management Interface Specification.

The table below shows the module power up state based on Low Power and ForceLowPwr. If LPWn=0 then the module shall go to low power mode and transmitters disabled. If ForceLowPwr=0 and LPWn=1 then the module shall immediately enable transmitters. If ForceLowPwr=1 and LPWn=1 then the module shall wait in Low Power mode until the host clears the ForceLowPwr bit for the module to enable transmitters.

Table 11-6: Power up behavior

Module State	ForceLowPwr = 0	ForceLowPwr = 1
Low Power asserted (LPWn = 0)	Low Power Mode (transmitters Disabled)	Low Power Mode (transmitters Disabled)
Low Power de-asserted (LPWn = 1)	Operational (transmitters Enabled*)	Low Power Mode (transmitters Disabled)

*The host may use the management interface to alter this default behavior

11.5.6 OSFP module reset behavior

Reset is a hardware signal from the INT/RSTn pin as defined in section 11.5.2. Asserting Reset overrides all other hardware and software controls and forces the module into the Reset state. This includes forcing Low Power mode and disabling transmitters.

11.6 Power

+3.3V power is delivered to the module via 4 power pins (VCC). These 4 power pins shall be connected together on the module and also together on the host. Each power pin allows up to 2.5 Amps for a total of 10.0 Amps. This enables a maximum power in excess of 30 Watts.

The specification of the module power is in accordance with methods defined by SFF-8679 Rev 1.7 section 5.5. There are 8 power classes defined as shown in Table 11-8. All modules in reset or the default low power mode must comply with Power Class 1. High power mode enables the module to draw power up to its advertised power class, and may be conditionally enabled by the host. The host may read the module power class register to know the power class of the module before or after enabling high power mode. The module shall not exceed the power class it identifies for itself.

Transition between low and high power mode is controlled by the M_RSTn (reset) signal, M_LPWn (low power mode) signal and ForceLowPwr bit. The module shall remain in or transition to low power mode when M_LPWn or M_RSTn are asserted or the ForceLowPwr bit is set. While in low power mode, active modules shall also disable transmitters. The module may transition to high power mode once M_RSTn and M_LPWn are deasserted and the ForceLowPwr bit is cleared.

The specifications of Table 11-7 and Table 11-8 are for the combined power of all 4 power pins. The measurement location for these specifications is at the OSFP connector VCC pins on the host board.

Table 11-7: OSFP power specification

Parameter	Symbol	Minimum	Nominal	Maximum	Units
Module power supply voltage including ripple, droop and noise below 100 kHz	Vcc_Module	3.135	3.300	3.465	V
Host power supply voltage including ripple, droop and noise below 100 kHz	Vcc_Host	3.201	3.300	3.465	V
Voltage drop across mated connector (Vcc_Host minus Vcc_Module)	Vcc_drop			66	mV
Total current for Vcc pins (1)	Icc_module			10.0	A
Host RMS noise output 10 Hz-10 MHz	e_{N_Host}			25	mV
Module RMS noise output 10 Hz - 10 MHz	e_{N_Mod}			15	mV
Module inrush - instantaneous peak duration	T_ip			50	µs
Module inrush - initialization time	T_init			500	ms
Inrush and Discharge Current (2)	I_didt			100	mA/µs
High power mode to Low power mode transition time from assertion of M_LPWn or M_RSTn or ForceLowPwr	T_hplp			200	µs

(1) Utilization of the maximum OSFP power rating requires thermal design and validation at the system level to ensure the maximum connector temperature is not exceeded. A recommended design practice is to heatsink the host board power pin pads with multiple vias to a thick copper power plane for conductive cooling.

(2) The specified Inrush and Discharge Current (I_didt) limit shall not be exceeded for all power transient events. This includes hot-plug, hot-unplug, power-up, power-down, initialization, low-power to high-power and high-power to low-power.

Table 11-8: OSFP power classes

Parameter	Symbol	Minimum	Nominal	Maximum	Units
Low Power Mode – M_LPWn or M_RSTn asserted or ForceLowPwr					
Power consumption	P_lp			2	W
Instantaneous peak current at hot plug	Icc_ip_lp			800	mA
Sustained peak current at hot plug	Icc_sp_lp			666	mA
Steady state current (1)	Icc_lp			637	mA
Power Class 1 module (high power mode)					
Power consumption	P_1			1.5	W
Instantaneous peak current at hot plug	Icc_ip_1			600	mA
Sustained peak current at hot plug	Icc_sp_1			500	mA
Steady state current (1)	Icc_1			478	mA
Power Class 2 module (high power mode)					
Power consumption	P_2			3.5	W
Instantaneous peak current at high power enable	Icc_ip_2			1400	mA
Sustained peak current at high power enable	Icc_sp_2			1167	mA
Steady state current (1)	Icc_2			1116	mA
Power Class 3 module (high power mode)					
Power consumption	P_3			7	W
Instantaneous peak current at high power enable	Icc_ip_3			2800	mA
Sustained peak current at high power enable	Icc_sp_3			2333	mA
Steady state current (1)	Icc_3			2233	mA
Power Class 4 module (high power mode)					
Power consumption	P_4			8	W
Instantaneous peak current at high power enable	Icc_ip_4			3200	mA
Sustained peak current at high power enable	Icc_sp_4			2666	mA
Steady state current (1)	Icc_4			2552	mA
Power Class 5 module (high power mode)					
Power consumption	P_5			10	W
Instantaneous peak current at high power enable	Icc_ip_5			4000	mA
Sustained peak current at high power enable	Icc_sp_5			3333	mA
Steady state current (1)	Icc_5			3190	mA
Power Class 6 module (high power mode)					
Power consumption	P_6			12	W
Instantaneous peak current at high power enable	Icc_ip_6			4800	mA
Sustained peak current at high power enable	Icc_sp_6			4000	mA
Steady state current (1)	Icc_6			3828	mA
Power Class 7 module (high power mode)					
Power consumption	P_7			14	W
Instantaneous peak current at high power enable	Icc_ip_7			5600	mA
Sustained peak current at high power enable	Icc_sp_7			4666	mA
Steady state current (1)	Icc_7			4466	mA
Power Class 8 module (high power mode)					
Power consumption	P_8 (2)			>14	W
Instantaneous peak current at high power enable	Icc_ip_8			P_8 * 400	mA
Sustained peak current at high power enable	Icc_sp_8			P_8 * 333	mA
Steady state current (1)	Icc_8			7600	mA

(1) Steady state current must not allow power consumption to exceed the specified maximum power for the selected power class.

(2) Power consumption P_8 is readable from the module Max Power register as defined in the Management Specification.

As a reference, the maximum power allowed in the previous revisions in the OSFP MSA are listed in Table 11-9.

Table 11-9: OSFP power summary per MSA revision

OSFP MSA Rev	Max Current	Max Power (at 3.3V nominal)
1.0	6 A	19.8 W
2.0	6.4 A	21.1 W
3.0	6.4 A	21.1 W
4.0	10 A	33.0 W

11.6.1 Power Filter

Figure 11-6 provides an example implementation for a 3.3V power filter on the host board. If an alternate circuit is used for power filtering then the same filter characteristics as this example filter shall be met.

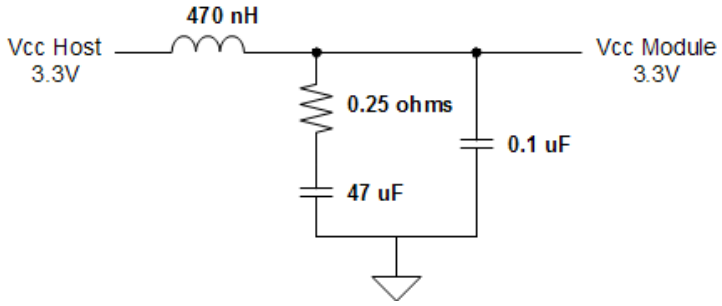


Figure 11-6: Host board power filter circuit

11.6.2 Power Electronic Circuit Breaker (optional)

For safety and protection of the host system, the power to each OSFP module may be protected by an electronic circuit breaker on the host board which is enabled with the H_PRSn signal such that power is only enabled when the module is fully engaged into the OSFP connector.

11.7 OSFP Host Board and Module Block Diagram

Figure 11-7 is an example block diagram of the host board's connections to the OSFP module.

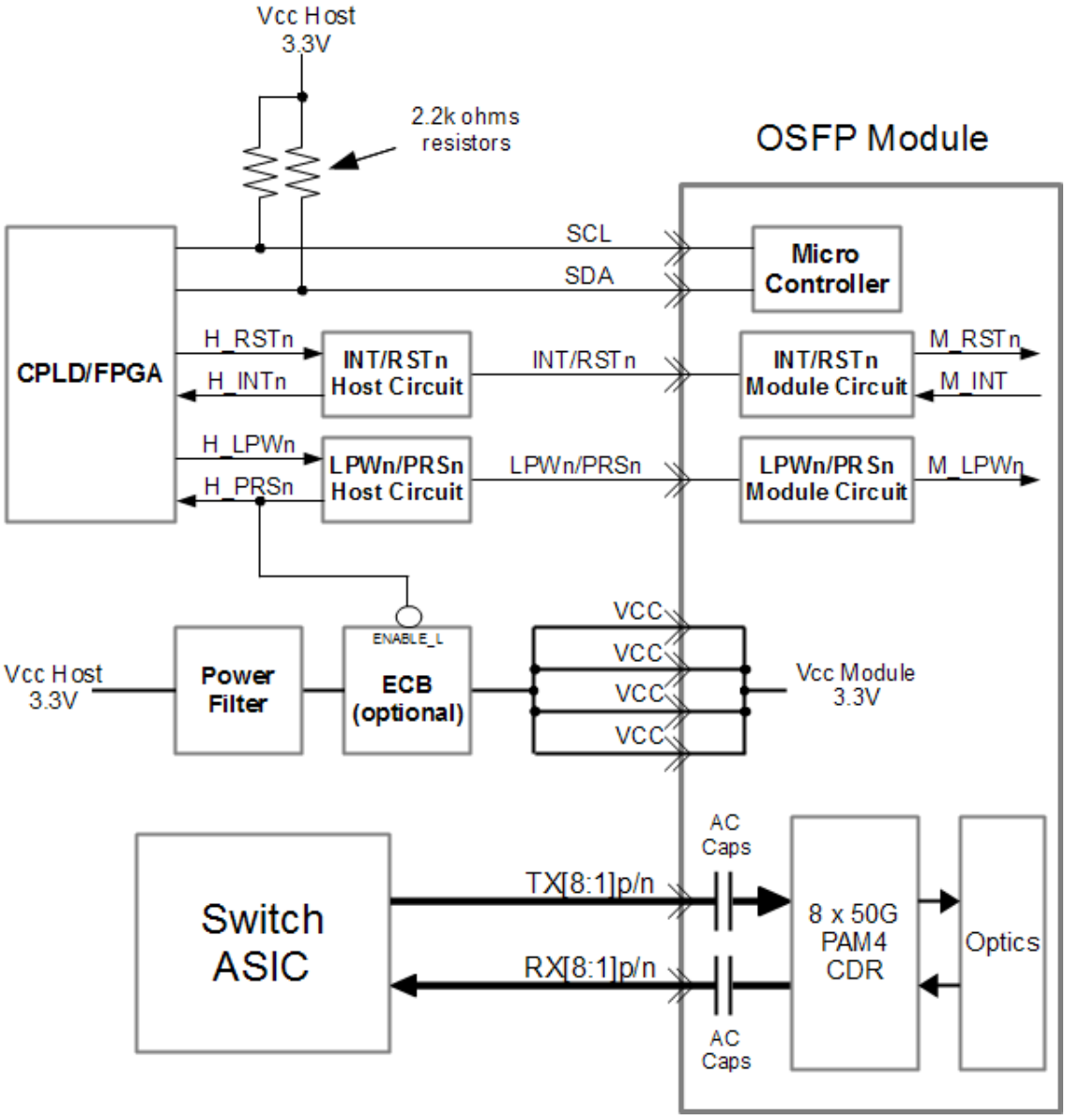


Figure 11-7: Host board and Module block diagram

11.8 Electrostatic Discharge (ESD)

Where ESD performance is not otherwise specified, the OSFP module shall meet ESD requirements given in EN61000-4-2, criterion B test specification when installed in a properly grounded cage and chassis. The units are subjected to 15kV air discharges during operation and 8kV direct contact discharges to the case.

The OSFP module and host high-speed signal, low-speed signal and power contacts shall withstand 1000 V electrostatic discharge based on Human Body Model per ANSI/ESDA/JEDEC JS-001.

Appendix A. OSFP Module LED (Informative)

A.1 LED Indicator and its Scheme

An OSFP module may have one or more LEDs at the front for use as a status indicator. In cases where a single LED is used for status indication of a multi-channel OSFP module, a green/yellow bi-color LED is recommended. In such case, the LED should light solid green when all channels of the module are operational and solid yellow when all channels are disabled. In cases where some channels are operational and some have fault conditions, a repeating pattern of LED flashing as outlined in Table A-1 is recommended.

Table A-1: Suggested OSFP LED signaling scheme for multiple channel modules

LED Status	Indication
On for 0.22 seconds	Green indicates channel 1 operational; Yellow indicates channel 1 is non-operational or disabled.
Off for 0.22 seconds	Pause until LED indicates status of next channel.
On for 0.22 seconds	Green indicates channel 2 operational; Yellow indicates channel 2 is non-operational or disabled.
Off for 0.22 seconds	Pause until LED indicates status of next channel.
…. Pattern repeats to final (*n*th) port	…
LED off for 1.76 seconds	Long pause for clear separation before pattern repeats from the beginning.

Appendix B. OSFP Pull Tab Length (Informative)

B.1 OSFP Pull Tab Length

An OSFP module may have a pull tab. Figure B-1 to B-3 show reference pull tab lengths with respect to the module positive stop. Note that this does not apply to passive copper cables.

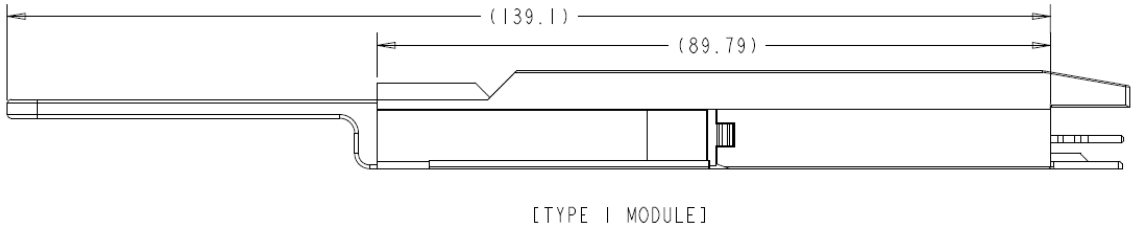


Figure B-1: Type 1 OSFP module lengths with pull tab

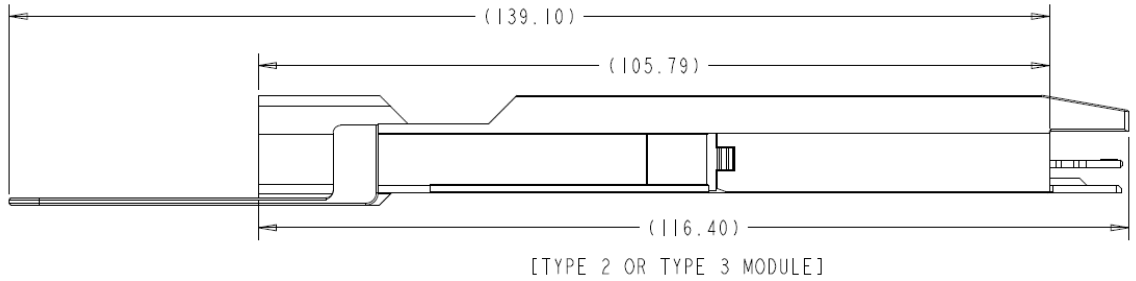


Figure B-2: Type 2 or Type 3 OSFP with pull tab

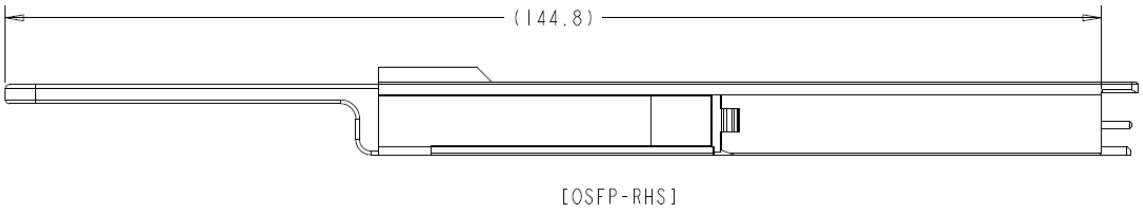


Figure B-3: OSFP-RHS module lengths with pull tab

Appendix C. OSFP with heatsink on the bottom

C.1 Bottom heatsink dimensions

The OSFP module is permitted to have an integrated heatsink on the bottom side for improved thermal control. Figure C-1 and Figure C-2 depict the OSFP module bottom side integrated heatsink design and fin placement. Figure C-3 provides the fin design details. The fin design and placement are consistent with the open top heatsink design specified in section 3.4, to comply with the EMI cage finger in Section 4.3.

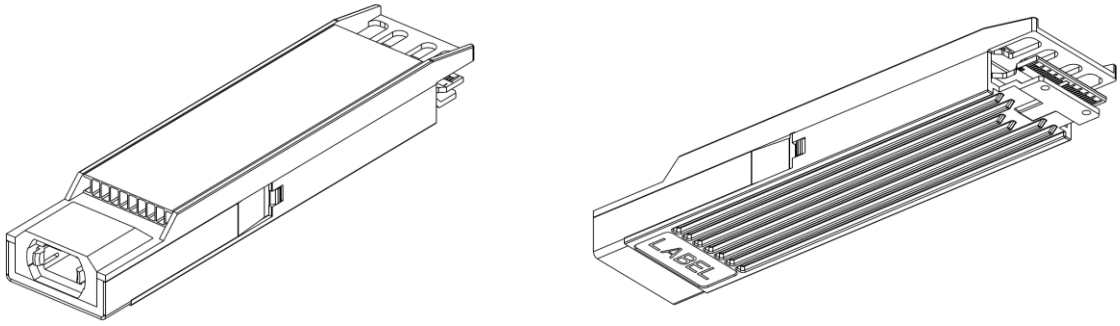


Figure C-1: OSFP module with bottom heatsink

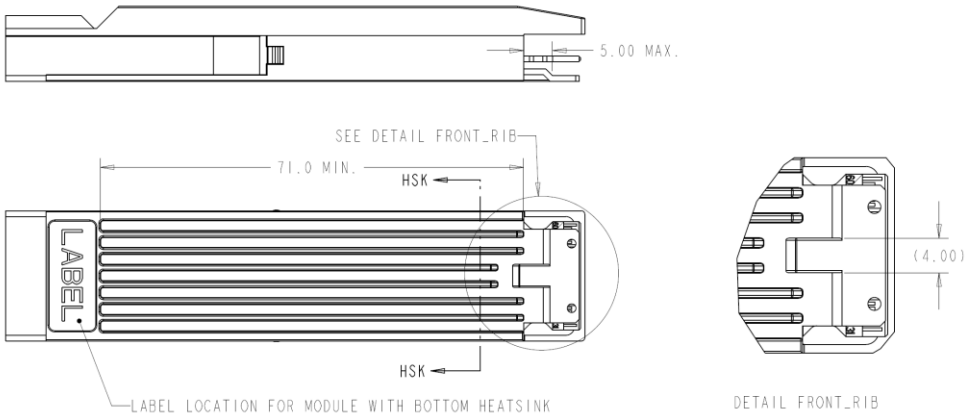


Figure C-2: OSFP with bottom heatsink, shape of the back

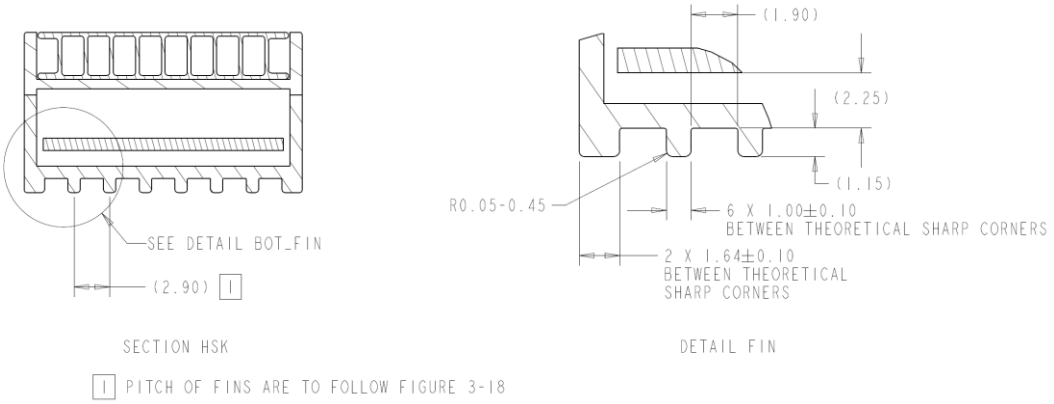


Figure C-3: Bottom heatsink fin pitch