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Coming of Age with the Transistor

By Sandip Tiwari

The transistor and its usage, semiconductors in general following in its wake, have been one of the greatest technological achievements of the human age. They are a social force through their daily use in computing, communications, transactions and in health. In this 75th anniversary celebration participation, I share here some of the lessons learned while coming of age with the transistor. The new and young entrants to the technological spectrum might find these vignettes amusing and perhaps useful.

Much has been written about the history and the future of the transistor. By the simple means of converting static energy into signal energy, it becomes a physical tool for logical transformations and communication, and even when not amplifying, it is an essential feedback tool for stability. It morphs into many forms and when it is together with other structures, it expands to new functions. With floating charge storage within it, it is a quasi-non-volatile memory, with a capacitor, it forms a fast and dense dynamic memory, and when paired with other transistors, it becomes a very fast static memory. The static random access memory even has the unusual fundamental characteristic of being self-aware. It stays in its state and a similar cross-coupled element is needed to change it or probe its state. The modern age is wrought by the techno-social changes from the invention, its evolution, and the new directions it has spun off: in pursuits related to intelligence/learning or physical well being that are unfolding, and many more that we cannot yet see.

Many have written about these transformations.

Speculation, imagining, and interactions of ideas are critical food of human evolution. Having been born in the decade following the

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Coming of Age with the Transistor

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Bell Laboratories demonstration and having grown with it, with a tinny-sounding seven-transistor radio made at the ripe age of 15 without access to a spectrum analyzer or an oscilloscope as the introduction, an education when learning transistors and their circuits were the rights of passage, and following the completion of the formal education, in IBM's research, and in academe, the transistor age has paralleled mine.

Instead of speculating specifics, it is useful to share some of the lessons of the journey drawn on this sampling of the different worlds. This article is a collection of musings of the physical and social learning from this transistor journey, what it speaks to for the future, and for the *judgments and choices that a young person must make in undertaking a journey in this technical world*.

See S. Y. Auyang, "Engineering-An endless frontier," Harvard, ISBN 0-674-01332-8 (2004) for a lucid discussion of technology through ages in the societal context.

Choose a direction while it is nascent: Engineers are creators of what does not exist. Engines of all types, water wheel, steam, electric, or combustion including those of the jets for transformation to mechanical form, all have had a fair period of research and early development of exponential growth and then a maturing linear long-life period before being substituted by a new invention. These Kondratiev cycles have invention-dependent time lengths. Electronics or more broadly optoelectronics as outgrowth of information energy inventions (the transistor, the solar cell, the semiconductor laser, and others) are no exception. For intellectual excitement over a period, the initial part is most interesting. The later part is interesting for the practically inclined, it is diffusive, and new unusual paths are its surprise pleasures. Electric vehicles are bringing a new period of vitality to old technologies of electric engines and batteries. Cars are now computing, sensing and communication engines on wheels. Autonomous motion is the semiconductor technology diffusing and being used in new avenues through the opening up of artificial intelligence, fast communications and multi-modal sensing platforms by the growth of integration.

Let curiosity drive the agenda: When one has solved a specific problem, it often ends with suggestions of other problems. Not always, and then one is at a loss for direction. The former becomes tiresome after a few years. While researching, many questions pop up, and one sets them aside. Letting them simmer and then froth up—a curiosity-driven pursuit—works wonders to setting up new satisfying directional agendas. While starting with compound semiconductor transistors, and their analog and digital circuits, it was not long before what happens in off-equilibrium conditions, or at nanoscale, to quantum and single electron and optoelectronic structures, and then transforming to issues of large scale: three-dimensional, adaptive, probabilistic, Bayesian, to neural became very fruitful venues. So, it is important to not let imaginary boundaries corral one. Developing the tools, carefully choosing available tools, and learning to shift keeps the development of the cocktail of skills alive and life interesting.

IBM and Bell Laboratories in the anti-trust era were quite open with their discoveries and direction. Not so anymore in modern times. Apple is a prime example.

Research in the real world needs to be surreptitious; timing and cleverness matters: The industrial and academic research environment is fluid in time. Bell Laboratories or IBM Research do not exist in the fervent form that they had for the forty plus years following the invention of the transistor. The idea of using semiconductors to replace vacuum tubes predates World War II, but the subject was kept in abeyance till the war effort ended. Industrial research is for the benefit of the company, but the research itself benefits from the sharing of learning, so there is an implicit tension of publication, research, and commercial pursuit. Timing matters, sometimes the industrial inventions are early and take a long time before use. Semiconductor lasers' pervasive use is one example. With transistors, we have CMOS. It appeared in Casio watches in the early 1970s making watches a few dollars a pop with the liquid crystal display. CMOS did not enter the mainstream of computing till the mid-80s. Cleverness matters. During that era, the IBM fabrication technology was three generations ahead of DEC (Digital Equipment Corporation), but the end products, where they competed, were similar in performance because of the higher-level design. DEC's pdp and alpha computers became the platforms for creation of UNIX and made it into university laboratories for training and usage by the next generation of technologists. When a company becomes large, it is reluctant to undercut a precious source of profit that is slowly being nibbled away by a new technology. To state that the industrial world is real is to imply that the academic world is not. Far from it. The same competition and pursuit of ideas, which requires funding, which supports the students, exists. If anything, there exists much close-to-the-chest-protectiveness, symbolism and eccentricity—some quite contrived—with numerous antinomies.

There are two classic antinomies that stand out. The first is that the faculty is the university, as ascribed to Isidor Rabi, in his response to Dwight Eisenhower, then the president of Columbia, stating that the faculty are employees of the university. The second is that students are "customers," versus that the university exists for the education of the students. Both of these contradictions stood out to me. It is the intellectual development of the students and exploratory research that is the object for a university. I found those early years of industrial research more academic and less tribal.

Growth sneaks up: As a subject area develops momentum, whether in the industry or in the academy, it is adiabatic enough for disconnections to develop even if an approach was working before. In industry it usually arises from do-not-rock-the-cash-cow syndrome or because the leadership has lost an understanding of the needs. In academia it is usually because there is a natural bias towards the smallest unit that one feels one belongs to. The new directions that a subject can be leading towards can be lost. The interesting problems are always at the boundaries. That is where interesting diffusion takes place from the developments of a subject area. Openness to ideas and directions, where one can explore new creations, is vital once one is past the basic research period. This requires making sure that the culture has plasticity and is evolving in resonance with the participants and the subject. This type of diversity came to the transistor world through the competition and the proliferation of start-up companies throughout history. Success of foundries, another example of growth sneaking up, has been incredibly useful to this later period's success since it has helped undercut the monoculture and given a lower cost possibility for implementing ideas in what is a capital-intensive semiconductor world.

With this broader context, some important themes related to the transistor and the coming period specifically.

Matthew's principle or effect is the preferential ascribing credit to one, the most known one, above all others who could lay claim. It comes from the book of Matthew 23:29. Matthew's principle is itself an example of Matthew's principle, an autological phrase.

Predictions are dangerous: As a graduate student in the late 1970s, a required reading were the technical papers by Hoeneisen and Mead [1] with 0.4 μm as the limit. There have been many other predictions of limits, by Meindl [2] of 0.20 μm, and even one by me [3] of about 10 nm. All these limits have been passed. They were not fundamental. They appeared since one constraint above all—a Mathew's principle fallacy—was given credence. The nature of research and development is that one has not accounted for the unknowns. An engineer looks at the limits as a challenge.

Learning from false forays is useful: Challenges exist to be overcome. Choices are made in the midst of incompleteness. A specific property looks appealing, yet devices and the systems are an assemblage of properties that need to come out just right. Examples of such forays have included attempts at using compound semiconductors for large-scale digital usage in early 1980s, which gave me my early career start. The difficulties of surfaces, the absence of good contacting approaches, voltage limits, absence of good circuits because of the limitations of devices, etc., all showed up in limiting what heterostructure field-effect or bipolar transistor could do digitally. The devices are still enormously useful for their high frequency and high speed, but only at limited integration scale and with difficulties of reproducibility. Condensed matter physics regularly springs intriguing and unusual properties in new or rediscovered systems. Inducing superconductivity or selective spin in semiconductors, nanotubes, graphene, ferroelectricity, metal-insulator transitions, exploiting single electron effects in logic and for memory have appeared in this world line. Each taught something. Superconductivity the issue of contacting interfaces and limiting voltages; spin the importance of selectivity, relaxation and signal-mode conversion; monolayers and nanotubes the problem of surfaces, contacts and the complete absence of reproducibility; ferroelectricity the issue of imprinting and reliability in the absence of a single-crystal medium; metal-insulator transitions of interfaces and contacts; and single-electron effects the impact of statistics of low numbers. Some of these constraints were clear at the very beginning, nevertheless understanding the behavior was important. The learning led to limited but powerful uses elsewhere exploiting a specific property, and was a learning to be kept in the brain's archive for later reuse. They taught something new. The SiGe heterobipolar transistor [4] was a result of such a learning. Strain became useful in improving desired properties. Single-electron effects provide one of the most sensitive ways to make precision measurements of fields and charges, and the charge storage in defects rather than nanocrystals is the basis for the enormously useful non-volatile archival memories that have become ubiquitous. While the direction of using reconfigurability around defective elements in large-scale circuits did not work, the learning of the distributions became the source for probabilistic approach of computation in the inexact and Bayesian direction.

Wrong may be right, Right may be wrong: This right-wrong apparition conundrum is quite pervasive in technology. New technology developments in time can overcome practical limitations. A classic example is chemical-polishing for planarization. With the older feel for the very messy grit-based polishing and surface preparation of semiconductor wafers, the prognosis for planarizing multi-material surfaces looked poor. The incredible device structures with buried structures such as trench capacitors, three-dimensional integrated systems, silicon-on-insulator, the multi-decade layered field-programmable gate arrays, and the

3d NAND flash are all examples of chemical-polishing technology's success. In the 1980s, the phrase "silicon succeeds because of SiO_2" was popular. Low interface state density, stability, reliability, scaling, process technology, polysilicon gates, reproducible threshold voltages, were directly or indirectly linked to the oxide. Today, the most advanced device structures have high permittivity materials with ionicity and softness built in with the SiO_2 interface layer keeping mobility reasonable, metal silicides gates, and other changes abound. SiO_2 is only in the background.

Statics and dynamics are different: As the scaling era ended, it was inevitable that numerous new ideas floated. Some examples are in the false-forays discussion. But, one specific one connected to understanding ideas—not just of the transistors—is the difference between static and dynamic behavior. The dynamic behavior, because of the digital circuit usage at speeds well below fundamental limits, is often mistaken for quasi-static behavior. The fallacy of the consequences glares when static analysis is used to project dynamics. There are quite a few examples from the transistor age. Low barrier Schottky contacts to replace doped contacts of transistors is one. As a diode, one has access to the electrochemical potential to both sides of the interface through the contacts. Carriers can flood in and out of the semiconductor so dielectric relaxation defines this flow of a Schottky junction. In a transistor, there is an intervening channel of opposite polarity and insulator region. A change from off to on state means that an insulator and a low carrier and charge density region exists in between. Fields are largely terminating at the electrodes in the starting of the dynamic change from the off state. The injection of carriers is now rate limited in a very different way, and the dynamic resistance of $(k_B T/e)/I$ is subject to the actual current I, which is vanishing, and only starts becoming significant once electrons jump across and through the barrier to the channel to change its electrochemical potential. A large time-constant exists. Static and dynamic behavior is different. A different version of this same problem is when impact ionization is to be used to improve subthreshold slope. Impact ionization takes time to build up and needs space for the carriers to acquire the energy. This is the phenomenon of dead time and space known from the days of Impatt diodes, an early microwave generating two-terminal device. Here again, static and dynamic behavior are very different. A very different version of this static-dynamic issue is the use of ferroelectricity in the floating region of the gate. Hysteresis curves are static curves, where relaxation processes are allowed to complete during a change. By constraining—a clamping—one can unfold the negative slope behavior. This is similar to the voltage- or current-driven unveiling of tunnel diode characteristics. One shows hysteresis, the other a negative slope. In the case of a device, with no clamping, and sudden change in bias conditions, one now has the dynamic effect of the propagation of the domains whose end result the hysteresis curve describes. The dynamic behavior is entirely different from the static behavior.

Poisson and Gaussian are different: The transistor usage shows the consequences of the law of small and large numbers and central-limit theorem in a variety of ways with consequential effects that show up both in logic usage and in memories. As transistor dimension decreases, with low averages of dopants, the threshold voltage distributions become skewed Gaussian as the Poisson effect of dopants has a position-levered consequence. This same consequence is important for the two-dimensional effects near the junctions. Poisson consequence of dopants is particularly acute in random-walk memories such as dynamic random access or floating storage of flash. For the dynamic case, the appearance of a potential perturbation by a site that can trap an electron in the close vicinity of the transistor leads to a large change in the *sub-atto-ampere* current flowing through the transistor. This leads to serious variable retention. Dynamic memories have to be refreshed far more often to compensate for this leakage in the very few cells subject to this Poisson effect. In the case of floating storage structures, which are meant to be non-volatile, this implies one has to take out the structure's entire row and column. Such Poisson effects are inevitably going to increase with small devices.

Both dynamic and floating storage memories, one clearly volatile, the other quasi-non-volatile, are memories that are based on pinching off of charge leakage. The former by a transistor, the latter by the insulating dielectric barriers. They are not naturally stable such as the bistable static random access memory or magnetic or spin-torque memory, which have two clearly defined attractor states confined by a barrier. The leakage of current is a random walk. Electron flow of the transistor is being constricted in the former. Electron flow from the trapped state is being constricted in the latter.

Thermodynamics rules; Energy, speed and power: The mix of small dimensions and numbers and large densities and numbers and a healthy curated assembly of these properties together makes the semiconductor world very thermodynamics centric [5]. Noise and fluctuations—thermodynamics of what is programmed into the substrate, the signal, and the surrounding world—set the lower limits of operation in determinisitic approaches. The probabilistic distribution functions arising thermodynamically do the same in probabilistic approaches. In all these cases the entropy determines the rate at which faults, errors and variabilities will appear both at the transistor scale as well as the integrated system scale. So, Rent's rule, fault tolerance, power, energy, time, hierarchy of the design are all connected.

It is here that the difficulties with the emphasis on one property above all shows up. Herbert Simon [6] has an interesting parable to illustrate the importance of hierarchy. Hora and Tempus are two watchmakers. Both made watches with a thousand little individual parts. Tempus made his

watches by putting all the parts together in one go, but if interrupted, for example, by the phone, he had to reassemble it from all these one thousand parts. The more the customers liked the watch, the more they called, the more Tempus fell behind. Hora's watches were also just as good. But he made them using a hierarchy of subassemblies. The first group of subassemblies used ten parts each. Then ten such subassemblies were used to build a bigger subassembly, and so on. Proud competitors in the beginning, Tempus ended up working for Hora. If there is a one-in-a-hundred chance of being interrupted during the assembling process, Tempus, on average, had to spend four thousand times more time than Hora to assemble a watch. He had to start all over again from the beginning. Hora had to do this only part of the way. Hierarchy made Hora's success at this rudimentary complex system possible. The hierarchy of this node-connection assemblage leads to the Janus effect of Arthur Koestler [7]. Nodes of the hierarchy are like the Roman god, whose one face is toward the dependent part and the other toward the apex. This link and proliferation of these links with their unusual properties are crucial to the emergent properties of the whole.

Thermodynamics places constraints via the confluence of energy, entropy, and errors. The complex system consists of a large number of hierarchical subassemblies. Reduction in errors requires large reduction in entropy. This demands energy. But, such a reduction process requires the use of more energy. Heat arises. To be sustainable—avoiding overheating, even as energy flow keeps the system working—requires high-energy efficiency, limits to the amount of energy transformed, and keeping a lid on errors. Having to deploy so much energy at each step makes the system enormously energy hungry. The giant turbines that convert energies to electric form—the mechanical motion of the blades to the flow of current across voltages—need to be incredibly efficient so that only a few percent—if that—of that energy is lost to the volume. And a turbine is not really that complex a system. Computation and communication have not yet learned this lesson and it shows up powerfully in the neural-network kingdom.

Nature has found its own clever way around this problem. Consider the complex biological machine that is the human. The building or replacement processes occur individually in very small volumes—nanoscale—and are happening in parallel at Avogadro number scale. All this transcription, messaging, protein and cell generation, and so on, requires energy and nature works around the error problem by introducing mechanisms for self-repair. Very low energy (10–100 $k_B T$, the $k_B T$ being a good measure of the order of energy in a thermal motion) breaks and forms these bonds. Errors scale exponentially with these pre-factors. At 10 $k_B T$ energy, one in 100,000 building steps, for example, for each unzipping and copying step, will have an error, so errors must be detected, the building machine must step back to the previous known good state and rebuild that bond, a bit like that phone call to Tempus and Hora, but causing Hora to restart only from an intermediate state. Nature manages to do this pretty well. The human body recycles a body weight of ATP (adenosine triphosphate)—the molecule for energy transformation—every day so that chemical synthesis, nerve impulse propagation, and muscle contraction can happen. Checking and repairing made this complexity under energy constraint possible. So, all the work on reconfigurability and using error-prone parts, which von Neumann [8] started with, may yet come back. Although, so far in neural network implementations, we have largely demonstrated unreliability from reliable components.

Naming matters: There exists a culture in engineering where the naming of inventions or new techniques is an art in itself. In compound semiconductors, MODFET or SDHT didn't work out, HFET and HEMT did. DELTA FET [9] as a name is lost in history and FINFET rules, with tri-gate transistor struggling behind. I failed with inexact computing [10] as a nom de guerre. Approximate computing was how that subject track followed the early work. Not many recognize an interesting high current effect in double heterostructure bipolar transistors since the paper just titled it as a new effect [11]. But, nanocrystal memory [12] stuck. A good name attracts attention, and in turn, progress in that subject area. Sometimes the naming is a success by being a means to obfuscation as is the case with the node naming. They have nothing to do with the actual channel length that rate limits the transport, but a means to halo building.

Much has been written about Walter Shockley and his personality, for example, in M. Riordon and L. Hoddeson, "Crystal Fire: The Birth of the Information Age," W. W. Norton, New York, ISBN 0-393-04124-7 (1997), and in F. Seitz and N. G. Einspruch, "Electronic Genie: The Tangled History of Silicon," University of Illinois Press, Chicago, ISBN 0-252-02383-8 (1998). The junction transistor was a month's work after the first invention driven by the personality, and a cascade of offshoots started from his Shockley Semiconductors. A harsh personality still had a large impact. Bardeen left the group and moved to University of Illinois and achieved a second Nobel prize. Successes all around.

People matter, hard work matters: Good ideas come as a spark in an environment where many discussions and thoughts are being exchanged with critical technical assessment based on the current state of learning, which is by itself incomplete. This requires a variety of technical viewpoints and perspectives, interesting personalities, personalities often with attitudes, different cultures and evolving cultures. Being surrounded by brilliant people provides one an opportunity to learn and in turn create. Quite often some of the people may be brilliant, albeit very self-centered, and one needs to figure out ways to live with such folks too. But people who shuffle things

from here to there and from there to here should be avoided at all costs. The hard work should be towards something learned and created, and not just heat of the first law of thermodynamics.

Biography

Sandip Tiwari, a native of India, was educated starting in Physics before moving to Electrical Engineering, attending IIT Kanpur, RPI, and Cornell, and after working at IBM Research, joined Cornell in 1999. He has been a visiting faculty at Michigan, Columbia, Harvard, Stanford, TUM, University of Orsay, and ETH, the founding editor-in-chief of Transactions on Nanotechnology and authored the popular Electroscience textbook series of Oxford University Press. He is the Charles N. Mellowes Professor in Engineering Emeritus and Visiting Distinguished Professor at IIT Kanpur. He was director of USA's National Nanotechnology Infrastructure Network until 2012.

His research has spanned the engineering and science of semiconductor electronics and optics, and has been honored with the Cledo Brunetti Award of the Institution of Electronic and Electrical Engineers (IEEE), the Distinguished Alumnus Award from IIT Kanpur, the Young Scientist Award from Institute of Physics, and the Fellowships of American Physical Society and IEEE. Particularly joyful to him is discovering scientific explanations, uncovering new phenomena, inventing new devices and technologies, and moving in directions that are of broader societal use. His current research interests are in the challenging questions that arise when connecting large scales, such as those of massively integrated electronic systems, a complex system, to small scales, such as those of small devices and structures that come about from the use of nanoscale, bringing together knowledge from engineering and physical and computing sciences. His personal passion is satyagraha, in bringing critical and broad thinking skills and of openness to the young through education, and as a global citizen in the phenomenology that pervades the world.

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From Invention of the Transistor to VLSI to Ubiquitous Computing

Yuan Taur

Transistors as Amplifiers

The word "transistor" came from "transfer resistor". A transistor is a 3-terminal device with the 3rd terminal (the transfer electrode) modulating the current between terminals 1 and 2 (the resistor). It was developed as a solid-state, i.e., semiconductor, replacement of the bulky and power-consuming vacuum tubes for amplifying small input signals in telecommunication. While 1947 is generally regarded as the year the transistor was invented, the concept of the transistor was conceived nearly a hundred years ago in a 1926 patent filing on FET (Field-Effect Transistor). What was discovered in 1947 was actually a

bipolar transistor, which operates through the injection of minority carriers in a forward-biased p-n junction. As such, there is a steady-state current flow in all bipolar transistors in the on state. An FET, on the other hand, is a two-dimensional device with the current flow perpendicular to the field applied from the transfer electrode. In that respect, there can be negligible current flow from the transfer electrode in the on state. In particular, a MOSFET (Metal-Oxide-Semiconductor FET) is turned on by producing a field in the semiconductor (between terminals 1 and 2) through an insulator (or vacuum), hence has no steady-state current in the transfer terminal. However, a MOSFET is more challenging to build because the presence of surface states would hinder the effect of the transfer electrode. Only until 1960, more than 30 years after its invention, was the first MOSFET realized. Today, MOSFETs have grown to be the main constituent of the VLSI (Very Large Scale Integration) microchips through its application in digital computation.

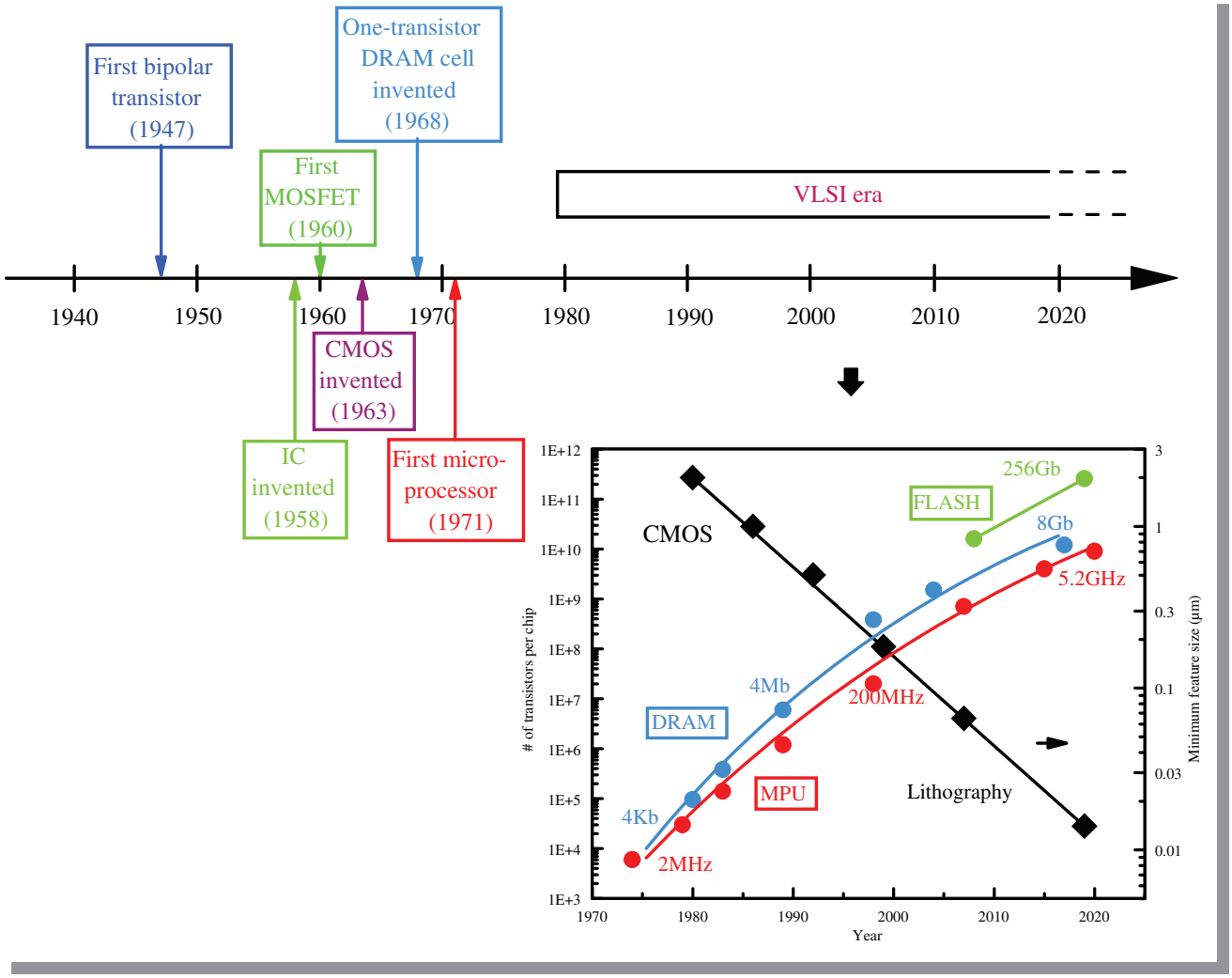
Digital Computation

During the same time period of the transistor invention, digital computation has become the mainstream approach to computing systems. The first general-purpose electronic digital computer was constructed in 1946 using vacuum tubes as the active logic elements. In the late 1950s, semiconductor transistors replaced vacuum tubes in digital systems because of their smaller size and lower power consumption. The late 1960s and '70s witnessed further dramatic advances in computer hardware, fueled by several key breakthrough inventions. The first was the fabrication of the integrated circuit (IC), a tiny silicon chip containing hundreds of transistors, diodes, and resistors. This microcircuit made possible the production of electronic systems with higher operating speeds, capacity, and reliability at a significantly lower cost. Another key milestone in the VLSI evolution is the invention of the one-transistor DRAM (Dynamic Random Access Memory) cell. It utilizes circuit techniques to refresh and maintain the charge stored on a reverse-biased p-n junction. A third key milestone is the invention of the CMOS (Complementary-MOS) circuit. It consists of n-channel and p-channel MOSFETs connected in parallel at the input and in series at the output such that there is no steady-state conducting path between the power supply terminals. Although CMOS occupies a larger area and has a longer delay time as the input signal has to turn on/off two MOSFETs, it becomes the key constituent of logic circuits because of its negligible standby power consumption. Note that while a bipolar transistor makes a better amplifier due to its high voltage gains, a complementary bipolar circuit does not have the same low power feature as CMOS because there is always power dissipation in the turned-on bipolar transistors. CMOS had a humble beginning, with its initial application in battery-operated wrist watches and hand-held calculators. Both are low-speed devices.

LSI and VLSI

The development of large-scale integration (LSI) enabled hardware manufacturers to pack thousands of transistors and other related components on a single silicon chip about the size of a baby's fingernail. Such microcircuitry yielded two devices that revolutionized computer technology. The first of these was the microprocessor unit (MPU), which is an integrated circuit that contains all the arithmetic, logic, and control circuitry of a central processing unit. Its production resulted in the development of microcomputers, systems no larger than portable television sets yet with substantial computing power. The other important device to emerge from LSI circuitry was the semiconductor memory (DRAM). This compact storage device is well suited for use as the main memory in minicomputers and microcomputers, particularly those designed for high-speed applications. Such compact electronics led in the late 1970s to the development of the personal computer, a digital computer that was small and inexpensive enough to be used by ordinary consumers. By the beginning of the 1980s, integrated circuitry had advanced to very-large-scale integration (VLSI). This design and manufacturing technology significantly increased the circuit density of microprocessor, memory, and support chips—i.e., those that serve to interface microprocessors with input-output devices. By the 1990s, some VLSI circuits contained more than 3 million transistors on a silicon chip less than 0.3 square inches (2 square cm) in area. The use of personal computers grew through the 1980s and '90s. When MOSFETs are made smaller, the density increases and they switch faster with lower power dissipation. By the late 1990s, all mainframe computers were made in CMOS technology. Today's microchips contain 10 billion to 1 trillion transistors, with an MPU clock frequency reaching 5 GHz. In the meantime, floating gate MOSFETs, produced since the 1980s as nonvolatile memory arrays, have become inexpensive enough to replace magnetic tapes and laser disks as the portable storage units.

Standard bulk MOSFETs can be scaled to a gate length of 20 nm or so, which requires a body doping reaching its limits. To go beyond that, the VLSI industry turned to double-gate MOSFETs with no doping requirements. The concept of double-gate MOSFETs was introduced in a patent filing as early as 1935. However, they cannot be fabricated using the conventional planar IC technology, especially with the source-drain regions self-aligned to both gates. A version of the double gate MOSFET was fabricated in 1989, which was later given the name FinFET. The manufacturing of FinFET into VLSI products was accomplished in 2012 by applying a sub-lithographic patterning technique patented in 1980. This extended the gate length from 20 nm to potentially 10 nm. It will be extremely difficult to further push the gate length to 5 nm, as that would require the fin thickness to approach atomic dimensions below 2 nm. Because of the



Evolution of semiconductor devices and circuits and of the circuit performances

limitation to gate length, the clock frequency of MPU has largely saturated at 5 GHz. Instead of pushing the performance of uniprocessors, the industry turned to parallelism with multiple CPUs on a chip to enhance the processor throughput. Another limiting factor is the chip power which becomes a serious issue since the thermal voltage, kT/q, is fixed. The consequence is that the operating voltage of VLSI chips cannot be reduced much below 1 V. One future direction of the IC industry is 3D integration, with which the circuit density increases linearly with the number of active layers.

Ubiquitous Computing

The spread of the World Wide Web in the 1990s brought millions of users onto the Internet, the worldwide computer network, and by 2019 about 4.5 billion people, more than half the world's population, had Internet access. Computers became smaller and faster and were ubiquitous in the early 21st century in smartphones and later tablet computers. Other examples include smart cars, CMOS cameras, GPS road guidance systems, etc. The invention of the transistor 75 years ago has brought unprecedented growth to the semiconductor industry, with an enormous impact on how people work and live.

Biography

Yuan Taur is a Distinguished Professor at the Department of Electrical and Computer Engineering, University of California, San Diego. Prior to UCSD, he has been with IBM T. J. Watson Research Center from 1981 to 2001. He has served as the Editor-in-Chief of *IEEE Electron Device Letters* from 1999 to 2011. He received IEEE Electron Devices Society's J. J. Ebers Award in 2012 "for contributions to the advancement of several generations of CMOS process technologies." He coauthored a book with Tak H. Ning, "Fundamentals of Modern VLSI Devices," published by Cambridge University Press, 1st ed. 1998, 2nd ed. 2009, 3rd ed. 2022.

A REVIEW OF THE 68TH IEEE INTERNATIONAL ELECTRON DEVICES MEETING

BY SRABANTI CHOWDHURY, IEDM 2022 PUBLICITY CHAIR
AND JUNGWOO JOH, IEDM 2022 PUBLICITY CO-CHAIR

EDITED BY DANIEL TOMASZEWSKI, EDS NEWSLETTER EDITOR-IN-CHIEF
AND MANOJ SAXENA, EDS NEWSLETTER ASSOCIATE EDITOR-IN-CHIEF

For nearly seven decades, the annual IEEE International Electron Devices Meeting (IEDM) conference (www.ieee-IEDM.org), sponsored by the IEEE Electron Devices Society, has been the world's largest, most influential forum where the world's best and brightest electronics technologists go to learn about the latest breakthroughs in semiconductor and electron device technologies, design, manufacturing, physics, and modeling. The conference scope encompasses devices in silicon, compound and organic semiconductors as well as emerging material systems for nanometer-scale CMOS transistors, advanced memories, displays, sensors, MEMS devices, novel quantum and nano-scale devices, optoelectronics, neuromorphic solutions, devices for energy harvesting, and high-speed devices, to name some only. The technical programs of IEDM include presentations, panels, focus sessions, tutorials, short courses, and other events reporting and promoting achievements in the area of electron devices.

The 68th annual IEEE-IEDM was held in-person on 3–7 December 2022 at the Hilton San Francisco Union Square Hotel. The on-demand access to recorded presentations after the event was also provided. More than 1771 people registered for the Conference, including 1442 attending in person and 329 with on-demand access.

To outline a position of this year's Conference, Srabanti Chowdhury, IEEE IEDM 2022 Publicity Chair, and Associate Professor of Electrical Engineering at Stanford University said "Our conference began just a few years after the transistor was invented, in recognition of its revolutionary potential. The breakthroughs described at the IEEE IEDM every year since then have pushed transistors and related technologies forward, enabling the ongoing digital transformation of society. That is why our theme this year is: **The 75th Anniversary of the Transistor and the Next Transformative Devices to Address Global Challenges**." Jungwoo Joh, IEEE IEDM 2022 Publicity Vice Chair and Process Development Manager at Texas Instruments underlined a leading role of the Conference: "In a way, the broad reach, interdisciplinary nature and technical depth of the topics that are featured at the IEEE IEDM serve as a kind of crystal ball showing where the industry is headed. This year will be no different, with an anticipated technical program of more than 220 presentations, plus many educational opportunities, supplier exhibits, award presentations and other events highlighting the industry's best work." Srabanti Chowdhury continued: "The semiconductor industry has a higher profile in the world right now than perhaps at any other point in its history, and that makes the developments to be reported at the IEDM this year that much more impactful, because they will ultimately lead to products that make our lives better. In terms of the technical trends which are evident in this year's program, many of the accepted papers indicate a strong and growing interest in the use of 2D material systems for advanced, extremely scaled devices. I also would like to point out that this is the first time in the IEDM's long and storied history that the top three spots on the IEDM Executive Committee are held by women: Barbara DeSalvo of Meta Platforms is our General Chair; Dina Triyoso of TEL Technology Center America is our Technical Program Chair; and Kirsten Moselund of Paul Scherrer Institute/EPFL is our Technical Program Vice Chair." Jungwoo Joh added: "This year's technical program features presentations that explore the state-of-the-art in essentially every important semiconductor-related technology. A theme that runs through many of them is the need to deal with electrothermal considerations in extremely scaled devices, because thermal management goes hand-in-hand with reliability and performance."

The above statements of the IEDM 2022 Publicity Chairs reflected the list of the IEDM 2022 Technical Subcommittees covering an extremely broad scope of topics:

- Advanced Logic Technology (ALT)
- Emerging Device and Compute Technology (EDT)
- Memory Technology (MT)
- Microwave, Millimeter Wave and Analog Technology (MAT)
- Modeling and Simulation (MS)
- Optoelectronics, Displays and Imaging Systems (ODI)
- Power Devices and Systems (PDS)
- Reliability of Systems and Devices (RSD)
- Sensors, MEMS and Bioelectronics (SMB)

The key points of the IEDM 2022 are reported below.

Tutorials

Six Tutorials were carried out on 3 December by experts in the field to bridge the gap between textbook-level knowledge and leading-edge current research, and to introduce attendees to new fields of interest. 658 people (507 in-person) attended the following Tutorials:

- *FEOL Reliability: From Essentials to Advanced and Emerging Devices and Circuits*, by Ben Kaczer (IMEC); content: description of the the main degradation mechanisms occurring in present-day and future Field-Effect Transistors (FETs), such as Nanosheets and Forksheets, including SILC, TDDB, BTI, RTN and HCD
- *Fabrication and Three-Dimensional Integration Technologies*, by Qiangfei Xia (Univ. Massachusetts); content: 3D integration solutions, including the chiplet approach and monolithic integration techniques and perspectives on challenges and opportunities in the fabrication and 3D integration
- *Resistive Memories-Based Concepts for Neuromorphic Computing*, by Elisa Vianello (CEA-Leti); content: Approaches for implementing neuromorphic/in-memory computing with unreliable devices, going from relatively conventional approaches to radical new ideas exploiting also device imperfections
- *The Era of Advanced Packaging and Hybrid Bonding*, by Sitaram Arkalgud (Tokyo Electron); content: Evolution of packaging for microelectronics to increased chip-to-chip bandwidth, lower power consumption, improved reliability, and the integration of different materials and technologies in a package
- *Innovations and Technologies for 2nm CMOS and Beyond*, by Tenko Yamashita (IBM); content: Recent CMOS scaling research activities and progress from the semiconductor industry, challenges and potential solutions of VTFET and stacked FET as the next CMOS architecture
- *Integrating Microfluidics and Electronic Chips: Technologies for In Vitro and In Vivo Clinical Diagnostics*, by Carlotta Guiducci (EPFL); content: System-level approach to the design of a new generation of clinical diagnostic systems considering the peculiar challenges for the manufacturability and integration on the silicon of microfluidic systems for sample preparation, segregation and separation.

Short Courses

Two Short Courses were carried out in parallel on 4 December that offered the attendees the opportunity to learn about important areas and developments, and to network with global experts. 828 people (647 in-person) attended each of the following Short Courses:

- *High-Performance Technologies for Datacenter and Graphics to Enable Zetta-Scale Computing*, organized by Ruth Brain (Intel), with the following presentations:
  - *Future of High-Performance Computing,* by Wilfred Gomes (Intel)
  - *Energy-Efficient CMOS Scaling*, by Daewon Ha (Samsung)
  - *Novel Logic Devices for Energy-Efficient Computing*, by Iuliana Radu (TSMC)
  - *Heterogeneous Integration and Chiplet Packaging*, by Subu Iyer (UCLA)
  - *Process Architectures To Improve Power Delivery*, by Geert Hellings (IMEC)
  - *Optical Interconnects*, by Vladimir Stojanovic (UC Berkeley)
- *Next-Generation High-Speed Memory*, organized by Yih Wang (TSMC), with the following presentations:
  - *High-Speed Memory for Future HPC and AI: Architecture to System Design*, by John Wuu (AMD)
  - *High-Speed SRAMs for Future HPC and AI*, by Hidehiro Fujiwara (TSMC)
  - *Next-Generation DRAM for HPC and AI*, by Kyomin Sohn (Samsung)
  - *Future Prospects of In- and Near-Memory Computing*, by Naveen Verma (Princeton)
  - *High-Speed Emerging Memories for AI and HPC*, by Shimeng Yu (Georgia Tech)
  - *3D Technologies for Memory-Compute Integration*, by Geert Van der Plas (IMEC)

Plenary Talks

On 5 December, the regular part of IEDM started with three Plenary Talks:

- ***Celebrating 75 years of transistor innovation by looking ahead to the next set of great innovation opportunities*** by Anne Kelleher, Executive Vice President/General Manager of Technology Development, Intel
- ***Expanding Human Potential through Imaging and Sensing Technologies*** by Yusuke Oike, General Manager, Sony Semiconductor Solutions
- ***Enabling full fault tolerant quantum computing with silicon based VLSI technologies*** by Maud Vinet, Quantum Hardware Program Manager, CEA-Leti

Regular/Focus Sessions

The Plenary Talks session was followed by 37 sessions (including the plenary one) with presentations of more than 223 papers accepted by 9 Technical Subcommittees and grouped in corresponding tracks. Among the sessions, five special Focus Sessions on the following topics were held:

- ***Advanced Heterogeneous Integration: Chiplets and System-in-Packaging*** (5 December)
  This Focus Session was motivated by the fact that leading-edge integrated circuits have become so complex that it's difficult to add new features and achieve higher performance. Heterogeneous integration—where separately manufactured chips and chiplets (sub-processing units) are assembled into a single package in various ways—is an alternative. Components having different functions can be built and optimized using the most appropriate technologies, and then combined into a unified circuit. Many aspects of this important topic were discussed by the industry experts in the following presentations:
  - *Advanced System-in-Package Enabled by Wafer-Level Heterogeneous Integration of Chiplets*, by S. Bhattacharya et al, A*Star
  - *Heterogeneous and Chiplet Integration Using Organic Interposer*, by S-P. Jeng et al, TSMC
  - *Advanced Packaging Technology Platforms for Chiplets and Heterogeneous Integration*, by L. Cao, ASE
  - *Advanced Substrate Packaging Technologies for Enabling Heterogeneous Integration (HI) Applications*, by G. Duan et al, Intel
  - *Hybrid Substrates for Chiplet Design and Heterogeneous Integration Packaging*, by J. Lau et al, Unimicron Technology
  - *Advanced Package FAB Solutions (APFS) for Chiplet Integration*, by S.W. Yoon, Samsung.
- ***Quantum Information and Sensing*** (6 December)
  This Focus Session discussed the fundamental work taking place to make various types of quantum sensors possible. Quantum sensing is the idea that sensors based on quantum phenomena (e.g. entanglement, coherence, tunneling, etc.) could be used to measure physical, electrical, magnetic, light and other quantities in ways that aren't possible otherwise. The following presentations were made during the Session:
  - *Spin Qubits in Silicon FinFET Devices*, by S. Paredes et al, IBM/Univ. Basel
  - *Rare Earth-Based Solid-State Qubit Platforms*, by S. Guha et al, Univ. Chicago/Argonne National Laboratory/MIT
  - *Josephson Parametric Amplifiers for Rapid, High-Fidelity Measurement of Solid-State Qubits*, by S. Shankar, Univ. Texas at Austin
  - *Towards Topological Superconducting Qubits*, by J. Shabani et al, New York Univ.
  - *Potential of Diamond Solid-State Quantum Sensors*, by M. Hatano et al, Tokyo Institute of Technology
  - *Hybrid-Magnon Quantum Devices: Strategies and Approaches*, by A. Hoffmann, Univ. Illinois Urbana-Champaign
- ***DNA Digital Data Storage, Transistor-Based DNA Sequencing, and Bio-Computing*** (6 December)
  This Focus Session featured papers at the intersection of computer science and biology. Some explored the intriguing possibility of using DNA molecules as a potential data storage medium, because of DNA's extremely high density. Others described experimental nano-scale biosensors and related devices, which may lead to novel life-science technologies:
  - *Advances in Electronic Nano-Biosensors and New Frontiers in Bioengineering*, by R. Bashir et al, Univ. Illinois Urbana-Champaign/Gachon Univ./Korea Univ./Univ. California Irvine/Univ. Texas Austin
  - *Single-Molecule Field-Effect Transistors: Carbon Nanotube Devices for Temporally Encoded Biosensing*, by K. Shepard et al, Columbia Univ.
  - *Wafer-Scale Biologically Sensitive Carbon Nanotube FETs: from Fabrication to Clinical Applications*, by Z, Zhang et al, Peking University
  - *The Nanopore-FET as a High-Throughput Barcode Molecule Reader for Single-Molecule Omics and Read-Out of DNA Digital Data Storage*, by P. Van Dorpe et al, IMEC/KU Leuven
  - *DNA Storage: Synthesis and Sequencing Semiconductor Technologies*, by D. Lavenier, Univ. Rennes
  - *Bacterial Nanopores Open the Future of Data Storage*, by M. Dal Peraro et al, EPFL
  - *System Design Considerations for Automated Digital Data Storage in DNA*, by C. Takahashi, Univ. Washington
- ***Special Topics in Non-Von Neumann Computing*** (6 December)
  This Focus Session explored various ways to get around the main limitation of a so-called von Neumann architecture of most of the computers. In this architecture named after computer pioneer John von Neumann, a processor stores and fetches data from separate memory circuits, accessed with various input/output interfaces. With today's much faster processing speeds and denser chips, the inability of a processor to access memory quickly enough and at low power is becoming a serious limitation. The following works were presented during the Session:
  - *Training-to-Learn with Memristive Devices*, by E. Neftci et al, Peter Grunberg Institute
  - *Energy-Efficient Activity-Driven Computing Architectures for Edge Intelligence*, by S.-C. Liu et al, Univ. Zurich

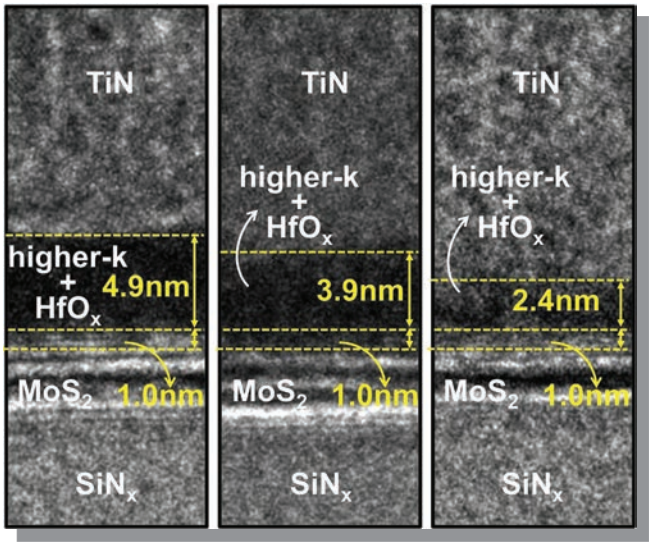
- *Multistable Neuromorphic Computing: Controlling Attractor Switches Using Waveforms*, by J. Chang et al, Univ. Texas at Austin
- *Life is Probabilistic—Why Should All Our Computers Be Deterministic? Computing with p-Bits: Ising Solvers and Beyond*, by B. Behin-Aein et al, Ludwig Computing
- *Ferroelectric FET Configurable Memory Arrays and Their Applications*, by S. X. Hu et al, Notre Dame/ De La Salle Univ. /Univ. South Florida
- *Scalable In-Memory Computing Architectures for Sparse Matrix Multiplication*, by J. Kendall et al, Rain Neuromorphics/Univ. Florida/Sandia National Laboratory
- *Subthreshold Operation of SONOS Analog Memory to Enable Accurate Low-Power Neural Network Inference*, by S. Agrawal et al, Infineon/Sandia National Labs
- *Analog Compute-in-Memory For AI Edge Inference*, by D. Fick, Mythic

- ***Emerging Implantable-Device Technology*** (7 December)
  This Focus Session was devoted to advanced electronic technologies for new and improved implantable medical devices used for monitoring and predicting brain activity and for other related purposes. An important aspect of these technologies is ensuring a biodegradation of the resulting devices after use. The following works were presented during the Session:
  - *Optogenetic Neural Probes: Fiberless, High-Density, Artifact-Free Neuromodulation*, by E. Yoon, Univ. Michigan
  - *Soft Wireless Optogenetic and Hybrid Implants for Advanced Neural Interfacing*, by J-W Jeong, KAIST
  - *Bilayer-Nanomesh Transparent Neuroelectrodes on 10μm-Thick PDMS*, by J. Ryu et al, Dartmouth College/Northeastern Univ.
  - *Biodegradable Implantable Microsystems*, by J. Brugger et al, EPFL
  - *The Future of Holistic Neural Interfaces: 2D Materials, Neuromorphic Computing, and Computational Co-Design*, by D. Kuzum et al, Univ. California San Diego
  - *Channels, Layout and Size Scalability of Implantable CMOS-Based Multielectrode Array Probes*, by L. Berdondini et al, Italian Institute of Technology
  - *Increasing the Lifetime of Implantable Neural Devices*, by S. Negi et al, Blackrock NeuroTech/ Univ. Texas Dallas
  - *A Transient, Closed-Loop Network of Wireless, Body-Integrated Devices for Autonomous Electrotherapy*, by J. Rogers, Northwestern Univ.

Below, we briefly present selected papers that, in our opinion, are of a very high scientific quality and are relevant for further developments in the related areas.

CMOS Scaling: 2D Devices

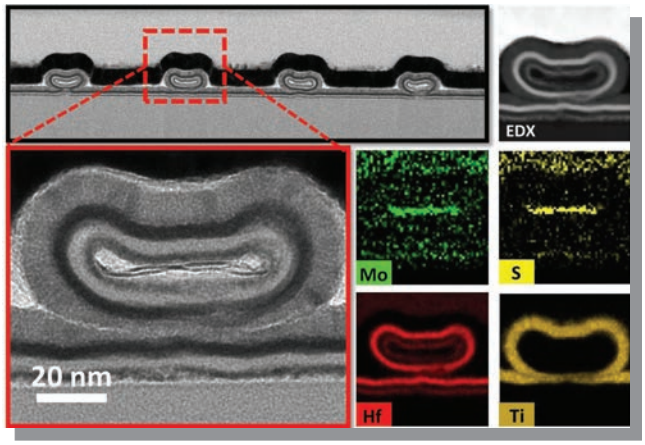
Nearly Ideal Subthreshold Swing with 2D MoS2: Monolayer transition metal dichalcogenides (TMDs) are so-called 2D materials because they are ultra-thin, just one layer of atoms thick. Since transistors are built from layers of materials, the use of monolayer TMDs can potentially lead to smaller devices. However, a key drawback is that it's quite difficult to deposit pinhole-free dielectric layers, or insulators, onto them. That makes it challenging to incorporate them into the stack of materials which forms a transistor gate. In the **paper #7.4**, a TSMC-led team described how they integrated hafnium-based dielectrics (formed by atomic layer deposition) with the monolayer TMD material MoS_2, to build a top-gated nFET with a physical dielectric thickness of 3.4 nm and an electrically equivalent oxide thickness (EOT) of ~1 nm. A so-called subthreshold swing (SS) is key in MOSFET transistors, because the lower the SS, the less current leaks through the device when it's turned off. The devices the researchers built had a nearly ideal SS of <70 mV/dec. In the paper, the key process parameters and their impacts were given in detail.



TEM images of TiN/higher-k + HfO_x/conformal interfacial dielectric (1.0 nm)/1L-MoS_2 top gate nFETs, where t_{HfOx}=0.9 nm, $t_{higher\text{-}k}$ is (a) 4 nm, (b) 3 nm and (c) 1.5 nm, respectively. **(Paper #7.4, "*Nearly Ideal Subthreshold Swing in Monolayer MoS_2 Top-Gate nFETs with Scaled EOT of 1 nm*," T-E Lee and Y-C Su et al, TSMC/NYCU/NARLabs)**

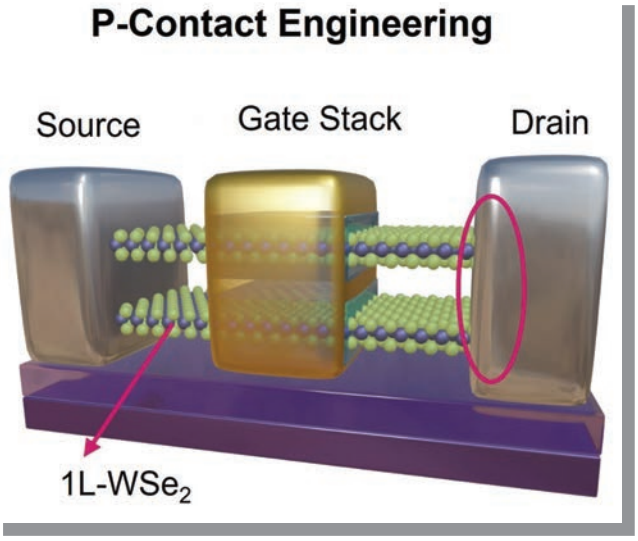
First 2D GAA Device: Silicon nanosheet transistors are considered the most promising candidate for next-generation device architectures because they offer improved electrostatic control, relatively high drive current and the feasibility of implementing devices with variable widths. Currently, gate-length scaling and high electrostatic control come from thinning down the Si channel, but in the future extreme gate-length scaling could be enabled by using monolayer transition metal dichalcogenides (TMDs).

While silicon nanosheets integrated with monolayer TMD as the channel material are promising, both the performance of such devices and their potential fabrication processes still need to be explored. In the **paper #34.5**, a TSMC-led team described a possible integration flow for 2D monolayer TMD-channel devices, and addressed critical challenges in stacked 2D sheet architectures. They used these insights to build the first-ever monolayer MoS_2 nanosheet FET in a gate-all-around (GAA) configuration. At a gate length of 40nm, the transistor exhibited an impressive I_{ON} ~410 μA/μm at V_{DS} = 1V, achieved with a monolayer channel ~0.7 nm thin. The FET had a large I_{ON}/I_{OFF}>1E8, and positive V_{TH} ~1.4 V with nearly zero DIBL. The researchers said higher drive current could be achieved by stacking multiple channel layers.



TEM cross section of monolayer MoS_2, nanosheet device with gate stack fully wrapped around the channel, and corresponding EDX elemental mapping (right bottom). **(Paper #34.5, "*First Demonstration of GAA Monolayer-MoS_2 Nanosheet nFET with 410 μA/μm I_D at 1V V_D at 40nm Gate Length*," Y-Y. Chung et al, TSMC/NYCU/NARLabs)**

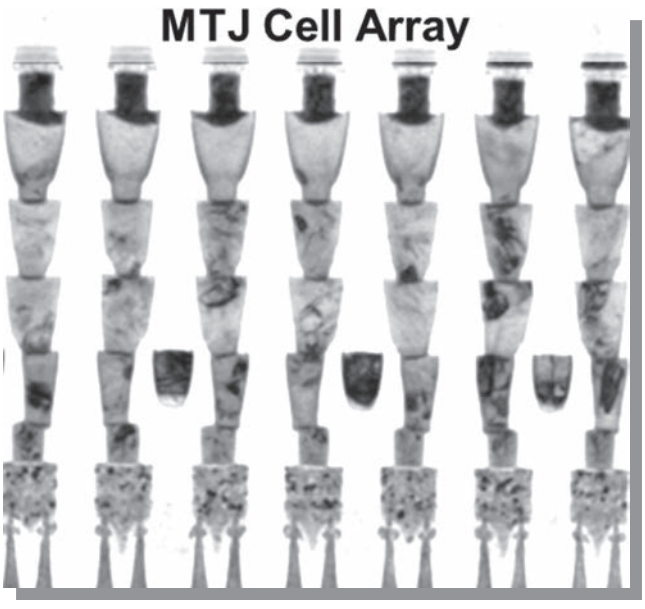
Low-Resistance p-Type Contacts to 2D Materials: Making low-resistance metal contacts to 2D materials is a bottleneck to their practical use in CMOS transistors. Progress has been made with n-type contacts for use with nFETs, but low-resistance p-type contacts for use with pFETs are more challenging because of the electro-thermodynamic conditions that arise between p-type metals and 2D materials. These conditions create an energy mismatch called the Schottky barrier: the greater the Schottky barrier height, the greater the resistance to current flow. In the **paper #28.1**, a TSMC-led team conducted computational computer modeling and simulation studies to investigate various materials for use as p-type contacts to the 2D material WSe_2. As a result of these studies, they identified two new strategies as realistic pathways to achieving Schottky barrier-free (i.e., ohmic) low-resistance p-type contacts: van der Waals metallic contacts using a material like 1T-T_iS_2, and bulk semi metallic contacts using various materials, of which $Co_3Sn_2S_2$ was identified as exceptionally good, with a theoretical contact resistance as low as 20 Ω·μm. Physical experiments were performed to further evaluate it.



Schematic of a monolayer WSe_2 nanosheet transistor. **(Paper #28.1, "*Computational Screening and Multiscale Simulation of Barrier-Free Contacts for 2D Semiconductor pFETs*," N. Yang et al, TSMC/Penn State Univ./Univ. Florida/Tohoku Univ./Rice Univ./Texas A&M Univ.)**

Memory Technology

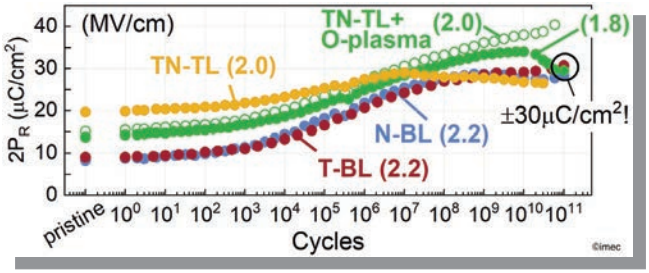
World's Smallest, Most Energy-Efficient MRAM: At present, non-volatile random access memory (nvRAM) only serves niche markets, but there is growing interest in it as a low-leakage working memory solution (e.g., for cache memory)



A cross-sectional TEM of an eMRAM bit-cell array embedded in a 14nm logic platform. **(Paper #10.7, *"World-Most Energy-Efficient MRAM Technology for Non-Volatile RAM Applications,"* T.Y. Lee et al, Samsung)**

for emerging applications that rely on massive data collection and analysis, like Artificial Intelligence of Things (AIoT) and edge AI computing applications. Lowering total power consumption is critical in these applications. In the **paper #10.7**, Samsung researchers described the smallest, most energy-efficient standalone nvRAM memory ever reported. Based on a 28-nm embedded MRAM technology, it demonstrated best-in-class write energy (25 pJ/bit), along with active power requirements of just 14 mW (read)/27 mW (write) at a 54 MB/s data rate. It also featured the smallest package dimensions to date (30 mm^2 at 16 Mb), and essentially unlimited endurance (>1E14 cycles). A key part of the device's architecture is a magnetic tunnel junction (MTJ); scaling the MTJ down to the 14-nm FinFET node resulted in a 33% improvement in area scaling and 2.6x faster read times, which demonstrates the technology's potential to serve as a low-leakage working memory.

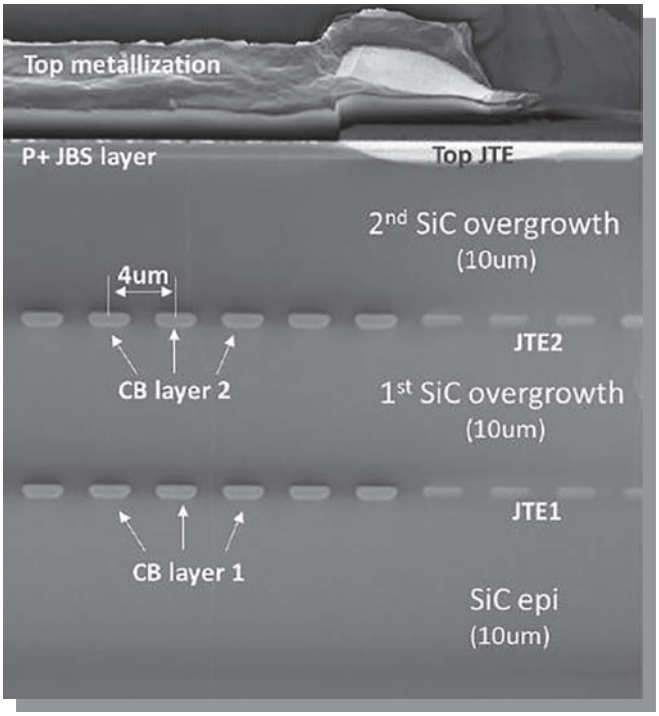
Superior Ferroelectric Performance: As electronic systems become more sophisticated, the industry is searching for RAM with fast access time (<10 ns), high endurance (>10^{14} cycles) and reasonably good data retention in transient power conditions such as when a system shifts into "sleep" mode. One transistor-one capacitor (1T-1C) structures based on ferroelectric (FE) materials are an active area of research. (FE materials have a polarization which can be reversed by the application of an electric field; these polarization states can represent the "0" and "1" values which are the basis of digital data.) In particular, hafnium zirconate (HZO) is being intensively studied due to its compatibility with CMOS processing and its suitability for scaling below 10 nm. In the **paper #6.4**, an IMEC-led team used materials engineering techniques to significantly improve the ferroelectric performance of HZO. They fabricated both bilayer and trilayer HZO capacitors using either a 1 nm TiO_2 seed layer and/or a 2 nm Nb_2O_5 cap layer, and TiN top and bottom electrodes. Depending on the chemical precursors used, the trilayer devices showed either a significantly improved endurance of up to 10^{11} cycles, or record-high data retention (i.e., "remnant polarization," or $2P_R$) = 66.5 μC/cm^2 after 3 x 10^6 cycles at 3 MV/cm.



The demonstrated endurance of capacitors made with different chemical precursors over 10^{11} cycles may make them promising for practical use. **(Paper #6.4, "*High Performance La-doped HZO-based Ferroelectric Capacitors by Interfacial Engineering*," M. I. Popovici and J. Bizindavyi et al, IMEC/ASM/KU Leuven)**

Power Devices

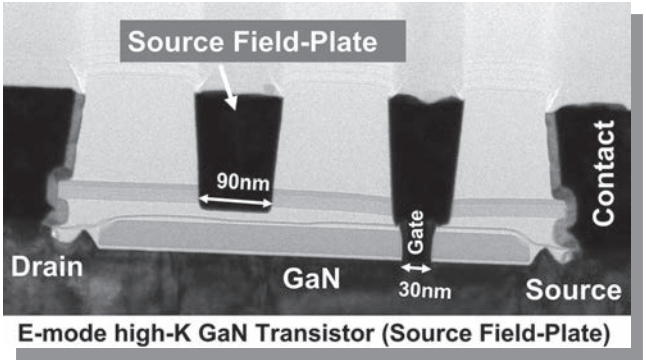
Ultra-High Voltage Superjunction SiC Devices: Semiconductors like power MOSFETs, IGBTs and SiC switches/diodes are the basis of the electric motor drives and power conversion systems used in marine, rail, energy and other large-scale applications. Because of the switching and conduction losses of these semiconductors, these systems are limited to low switching frequencies. If they could operate at higher frequencies, then smaller, more efficient, higher-voltage and less costly systems could be developed for such applications. In the **paper #9.1**, a team led by General Electric researchers reported on SiC superjunction MOSFETs and diodes formed by a very high energy (MeV) ion implantation technology, resulting in devices with specific on-resistance below the SiC unipolar, or theoretical, limit, resulting in lower losses. The researchers demonstrated the technology by building 2 kV SiC superjunction PiN diodes and 3.8 kV SiC superjunction JBS (junction barrier Schottky) diodes. The devices represent a scalable path toward future realization of 3-20 kV switches for power electronics applications.



SEM cross sectional view (right) of 3.3 kV SiC Charge-Balanced (CB) JBS diodes. **(Paper #9.1, "*Scalable Ultrahigh Voltage SiC Superjunction Device Technologies for Power Electronics Applications*," R. Ghandi et al, GE/RPI)**

Record f_{max} for 40 V GaN-on-Si: As the power density requirements of servers, graphics platforms and other high-performance systems continue to rise, new power-delivery solutions are needed for higher efficiency and density, and to support the faster data rates required by evolving applications. Gallium nitride (GaN) is promising

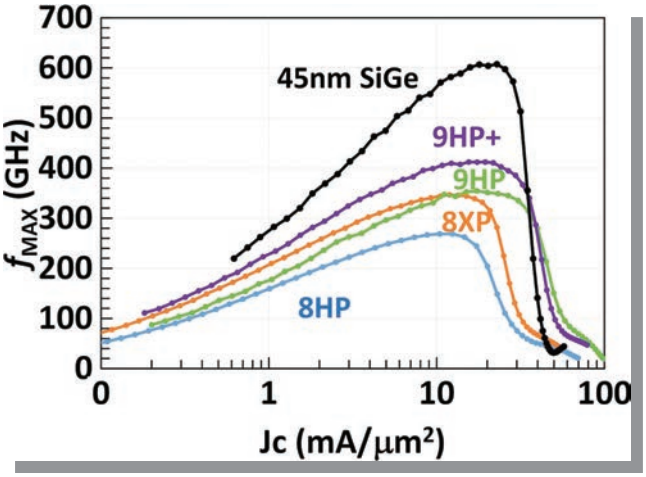
for its ability to operate at higher voltages and frequencies than silicon, and with lower losses. Last year at IEDM, Intel described a highly scaled, high-performance, enhancement-mode high-k GaN-on-Si NMOS FinFET built on a 300mm Si platform, and integrated with Si PMOS FinFET technology. It had a then-record f_t/f_{max} of 300/400 GHz for a 300 mm GaN-on-Si device. At IEDM 2022, in the **paper #35.1**, Intel researchers discussed how they scaled the technology (30 nm channel length) and extended its performance by integrating a submicron-length field plate to manage the electrical field within the device. They achieved an operating voltage of 40 V, and an f_{max} of 680 GHz (f_t = 130 GHz), a record for a 300 mm GaN-on-Si device.



TEM micrograph of source field-plated E-mode high-k gate dielectric GaN NMOS transistor. **(Paper #35.1, "*Scaled Submicron Field-Plated Enhancement-Mode High-K Gallium Nitride Transistors on 300 mm Si(111) Wafer with Power FoM ($R_{ON}xQ_{GG}$) of 3.1 mohm-nC at 40V and F_t/F_{max} of 130/680 GHz,*" H.W. Then et al, Intel)**

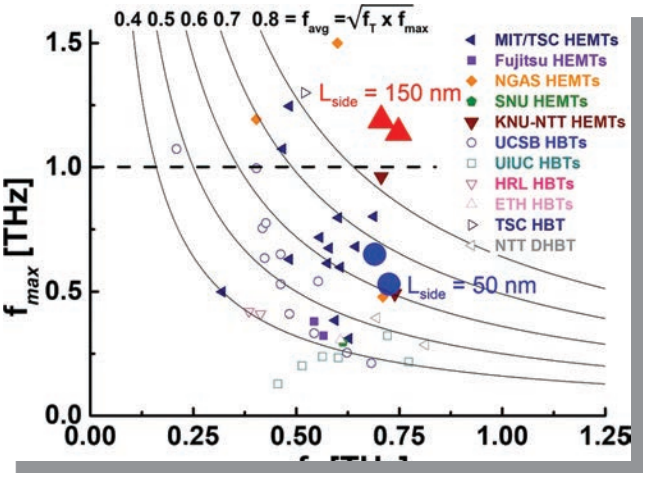
High-Speed Devices

Speed Record for BiCMOS: In the **paper #11.6**, GlobalFoundries researchers discussed SiGe heterojunction bipolar transistors (HBTs) integrated into a 45nm BiCMOS process. They achieved the highest reported f_{max} (oscillation frequency) ever reported for an HBT in any silicon-on-insulator technology. In a ring oscillator test circuit, the gate delay per stage was 1.76ps, also a speed record for a BiCMOS device. Cascode power cell measurements (i.e., amplifier measurements) showed >18 dB of gain at 100 GHz. The technology monolithically integrates SiGe HBTs, high-speed CMOS and low-loss passive devices on a single platform, and is promising for high-frequency applications such as 5G/6G communications, satellite communications, sub-THz sensing and automotive radar, among others.



f_{max} vs J_C at V_{CB} = 0.3V of SiGe HBTs for different generations of high performance BiCMOS technologies at GlobalFoundries. **(Paper #11.6, "*415/610GHz f_T/f_{MAX} SiGe HBTs Integrated in a 45nm PDSOI BiCMOS Process,*" V. Jain et al, GlobalFoundries)**

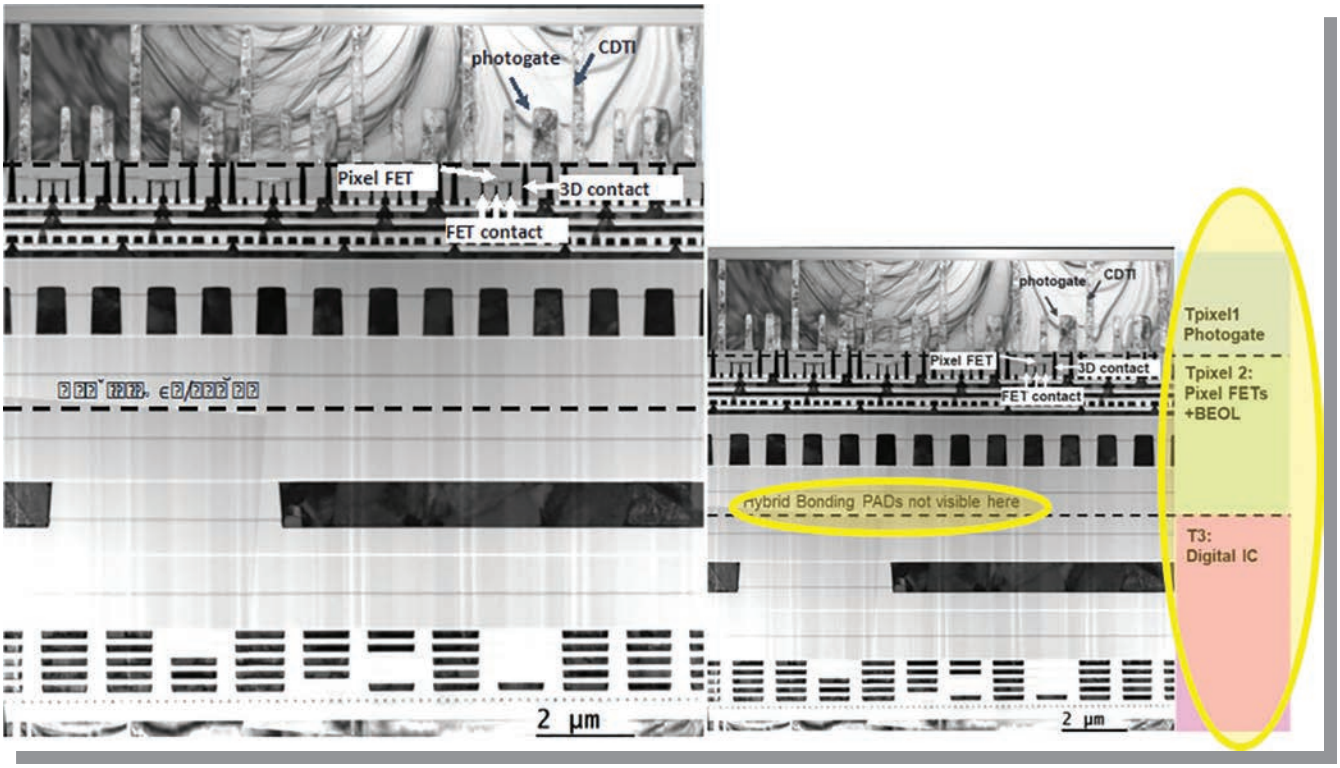
Speed Record for InGaAs Quantum-Well HEMTs: Evolving millimeter-wave wireless communication technologies such as 6G will require higher operating frequencies (~300 GHz, with data rates approaching 0.1 Tbps) than are possible today. To achieve this performance, researchers are investigating devices made of InGaAs and other III-V materials (from those two columns in the periodic table of elements), which are faster than silicon devices. In the **paper #11.4** a team led by researchers from Korea's Kyungpook National University reported on 20 nm-gate-length InGaAs transistors with f_{max} = 1.1 THz and f_t = 0.75 THz, the best balance of f_{max} and f_t in any transistor technology, and the highest f_t in any FET technology. Key to this performance was a DIBL value of 60 mV/V. (DIBL is a parasitic effect that potentially can lead to a transistor that turns on prematurely.) At the IEDM, the researchers described the device DC characterization and physical modeling studies, the scaling behavior of these devices, and options for further improvement in f_{max}.



Benchmark of f_{max} vs. f_T for the devices in this work, in comparison to those of other reports. **(Paper #11.4, "*Terahertz $In_{0.8}Ga_{0.2}As$ Quantum-Well HEMTs Toward 6G Applications,*" W-S Park and H-B Jo et al, Kyungpook National Univ./Univ. of Ulsan/QSI Co./NTT Corp.)**

Advances in Imaging & Sensing

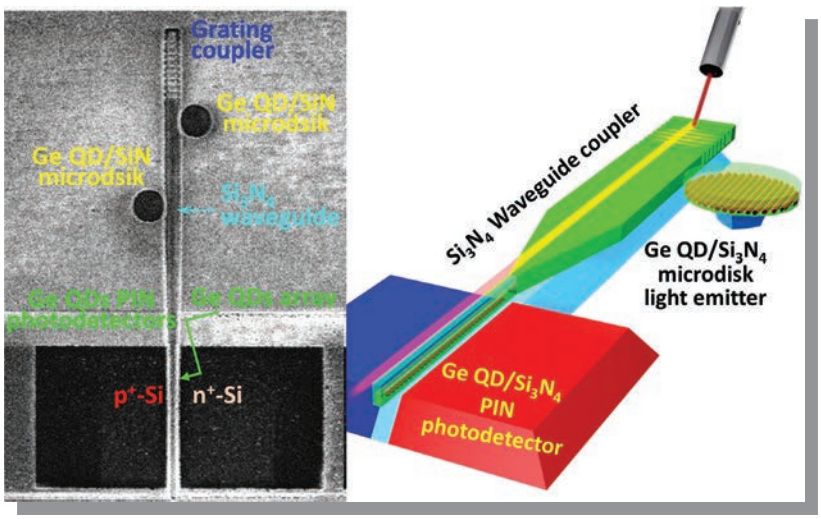
Toward Ultra-Miniaturized Pixels: In the **paper #37.4**, an ST-Microelectronics-led team described an innovative 3-tier back-side CMOS image sensor. It features a two-layer



TEM cross-section of the three-tier backside CMOS image sensor. **(Paper #37.4, *"3-Tier BSI CIS with 3D Sequential & Hybrid Bonding Enabling a1.4um pitch,106dB HDR Flicker Free Pixel,"* F. Guyader et al, STMicroelectronics/CEA-Leti/Univ. Grenoble Alpes)**

sequential integration stack of the photogate and pixel layers, hybrid-bonded to a logic circuitry layer, with no alignment issues. The sequential stacking of the photogate and pixel transistor layers resulted in a flicker-free, high dynamic range (106 dB) pixel with 1.4 µm pitch. The pixel transistor's thin-film SOI architecture offers advantages in terms of scalability and performance compared to its bulk counterpart, opening the possibility for future ultra-miniaturized pixels that can be integrated into complex SoC architectures.

Ge Photodiodes Embedded in Silicon: Photonic integrated circuits use light to transmit and process signals. A key goal is to monolithically integrate them with standard CMOS technology, both for improved performance and power-efficiency in high-performance computing applications, and also to expand on-chip sensing and quantum computing functionality. Silicon itself isn't ideal for photonics because it has a high refractive index. Germanium (Ge), though, can be strained to become pseudo-direct bandgap in operation, giving it properties such as luminescence. Using a combination of lithographic patterning and self-assembled growth, researchers from Taiwan's National Yang Ming Chiao Tung University (NYCU) described in the **paper #19.2** how they embedded strained Ge quantum dot nanostructures within cavities in silicon, where the principle of quantum confinement enhanced their luminescence. The process enabled the monolithic integration of Ge light emitters and PIN photodetectors with



*Schematic diagram and SEM micrograph showing the monolithic integration of Si3N4 wave guided Ge QD/Si3N4 µdisk light emitters and PIN photodetectors.(***Paper #19.2, *"Monolithic Integration of Top Si3N4-Waveguided Germanium Quantum-Dots Microdisk Light Emitters and PIN Photodetectors for On-chip Ultrafine Sensing,"* C-H. Lin et al, NYCU***)***

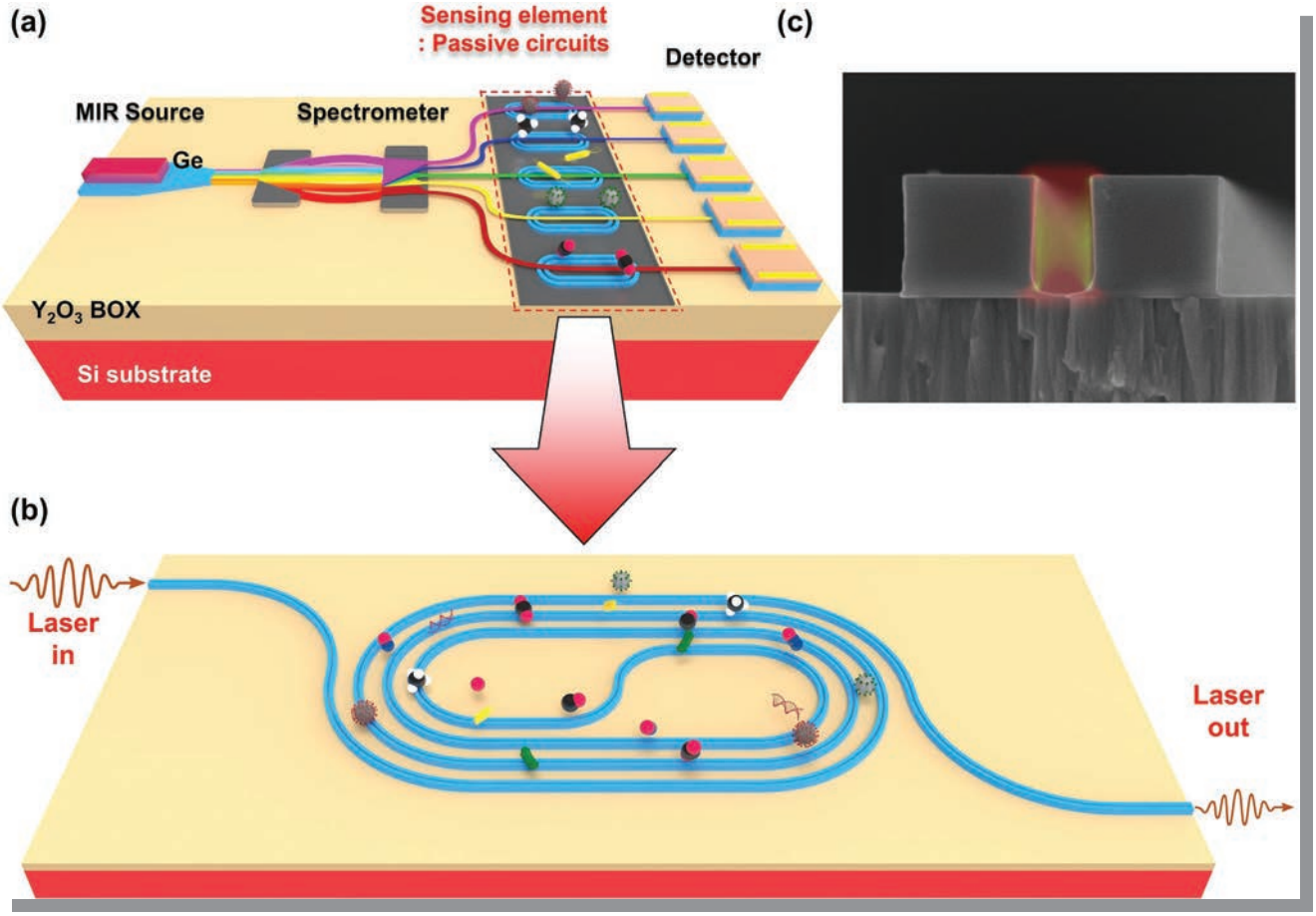
top waveguide-coupled Si_3N_4/SiO_2/Ge structures using standard Si processing. Photodiode dark current of 0.1 pA/μm and >95% coupling efficiency from SiN waveguides to the Ge photodiodes was demonstrated.

Ge-Based Optical Sensor: Germanium is of growing interest for photodetection, and a **paper #24.1** from the Korea Advanced Institute of Science and Technology (KAIST) described its use in a novel spectroscopy device. The mid-infrared range of the light spectrum (MIR, 2-15 μm) is increasingly used for optical sensing in applications such as environmental monitoring, defense, security, and biochemical sensing, because various biochemicals (gases, bacteria, viruses) have unique MIR absorption profiles. By vibrationally exciting their intermolecular bonds, MIR technologies have become effective methods for quantitative analysis. However, silicon photonics platforms based on SOI technology can't cover the entire MIR spectrum. Instead, KAIST researchers built a Ge-on-insulator (Ge-OI) gas sensor for biochemical sensing in the MIR range that demonstrated superior performance (low loss of 1.88 dB/cm), high optical confinement (a factor of 44.3% in the sensing region), and impressive sensitivity and limit-of-detection (0.0885%/ppm and 8.5 ppm, respectively).

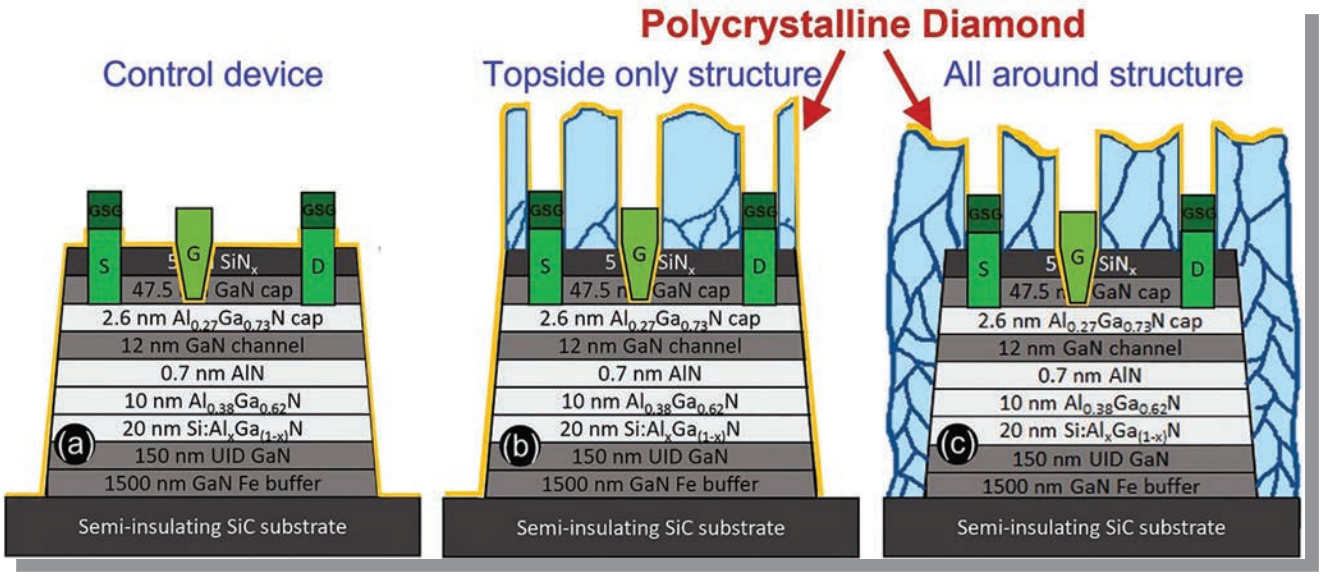
The Growing Importance of Thermal Management

Heat reduces the performance and reliability of electronic devices, and effective thermal management is becoming more important than ever as devices shrink. Papers at IEDM 2022 will address the issue from many different perspectives. Here are two noteworthy examples:

All-Around Diamond Films Spread Heat: GaN-based devices have great potential as solid-state power amplifiers for high-frequency applications such as 5G and beyond, given their higher power density at any operating frequency versus other materials. But with high output power density comes significant device self-heating,



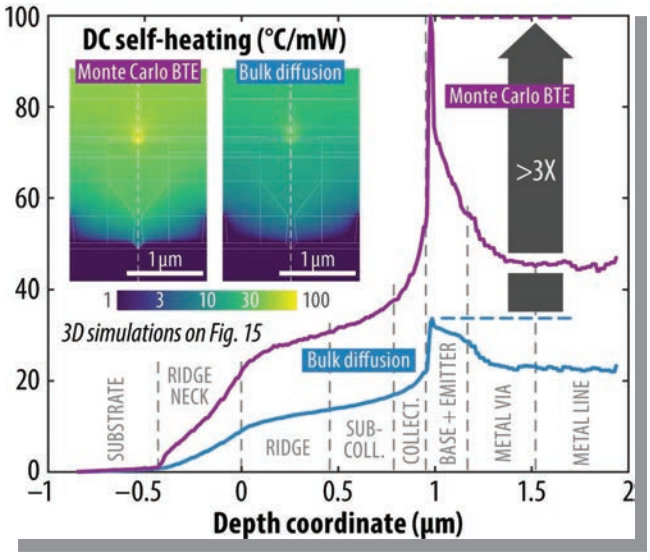
(a) Schematic of the MIR integrated optical sensing platform based on the GeOI with the componenets of the MIR source, spectrometer, and detector arrays. (b) Proposed slot waveguide with a spiral structure as a sensing element in the intergrated on-chip sensor for detecting biochemical such as gas, virus, bacteria, and etc. (c) Cross-sectional view of the slot waveguide with a highly localized field in the narrow gap for a strong light-matter interaction. **(Paper #24.1, "*Biochemical* Spectroscopy *Based on Germanium-on-Insulator Platform for Mid-Infrared Optical Sensor*," J. Lim et al, KAIST)**



Schematic image of (a) the control device without diamond (b) topside-only diamond integration and (c) all-around diamond integration. In topside-only integration, diamond is present only on the active device area and in all-around integration, diamond is present on active device area, MESA sidewalls and SiC substrate. **(Paper #30.8, "*Novel All-Around Diamond Integration with GaN HEMTs Demonstrating Highly Efficient Device Cooling*," R. Soman et al, Stanford Univ./Univ. Bristol/UC Santa Barbara/Georgia Inst. of Technology/Univ. Maryland)**

severely limiting RF performance and reliability, especially for ultra-scaled devices. Package-level heat removal isn't always adequate. Diamond is an excellent thermal conductor. In the **paper #30.8**, a Stanford-led team reported using polycrystalline diamond films as heat spreaders to facilitate hot spot removal at the device level. A novel polymer-assisted seeding technique enabled them to completely surround GaN HEMTs with isotropic thin-film CVD-grown diamond, providing complete sidewall coverage and minimizing total thermal resistance to the substrate. They used three different characterization techniques to monitor the devices' channel temperatures, and found that GaN HEMTs with 500 nm all-around diamond had lower peak and average channel temperatures versus control devices without diamond. Peak temperatures were 98 ± 19°C lower at 9.5 W/mm DC power. They also had a more uniform temperature profile and fewer hot spots along the gate electrode.

GaN and InP RF Devices Run 30%–70% Hotter Than Thought: Self-heating in RF devices is especially concerning given the substantial power requirements of RF circuits. Heat transfer in RF devices has always been diffusive in nature, accomplished via conduction as electrons or phonons flow through the bulk material and transfer thermal energy to other particles they encounter. Diffusion can be analyzed effectively with commercial modeling software. But as devices shrink, their feature sizes are becoming equivalent to the average distances electrons and phonons travel before they reach another particle, providing less of an opportunity to diffuse heat. Conventional computer models can't take this into account, and so estimates of transistor self-heating are becoming increasingly inaccurate as devices shrink. In the **paper #15.3** an IMEC-led team reported development of a new thermal modeling framework that does take it into account. Based on Monte Carlo simulations (a statistical averaging technique), they modeled heat flows in GaN and InPh RF devices, and found transistor-level peak temperatures in RF devices rose by 30%–70% more than thought. They



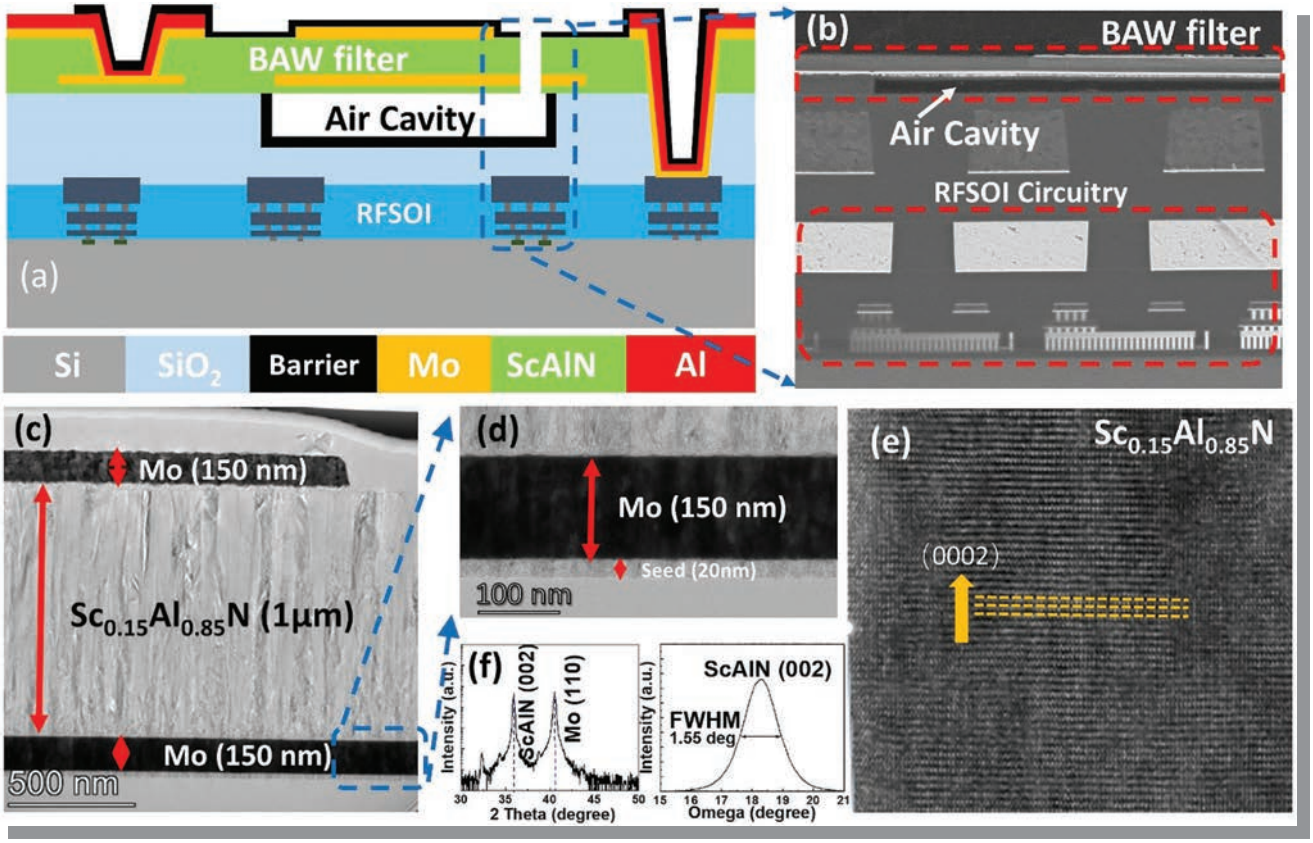
The impact of non-diffusive thermal transport effects in InP nanoridge HBTs. **(Paper #15.3, "*Thermal Modelling of GaN & InP RF Devices with Intrinsic Account for Nanoscale Transport Effects*," B. Vermeersch et al, IMEC/Vrije Universiteit Brussel)**

performed experiments with GaN-on-Si HEMT-based RF amplifiers to validate the models.

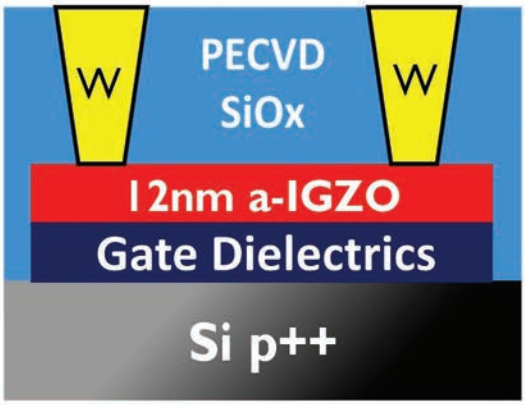
Noteworthy Papers on Diverse Topics

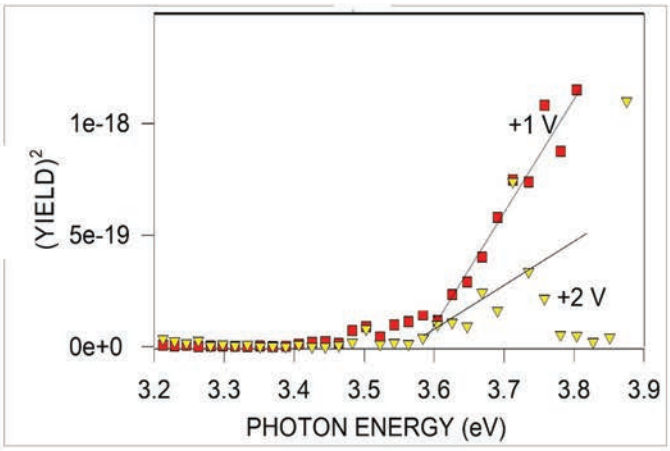
Integrated BAW Filters and RF Switches: RF acoustic filtering is essential for smartphone front-end modules to improve receiver sensitivity, reduce transmitter power consumption, and handle the increasing number of frequency bands which must coexist (e.g., Wi-Fi, GPS, LTE, 5G). There are about 100 RF acoustic filters in today's high-end smartphones, with bulk acoustic wave (BAW) filters produced by MEMS processes dominating the high-band frequencies. However, as the number of frequency bands increases, it becomes more challenging to package >100 chip-scale packaged filters inside a compact module. Also, system-level performance and cost are greatly impacted by increased losses from the wire routing on the numerous printed circuit boards. A potential solution is to monolithically integrate the BAW filters with front-end circuitries vertically on the same chip, instead of connecting them side-by-side through I/O interconnections. In the **paper #16.2**, researchers from Singapore's Agency for Science, Technology, and Research (A*Star) described a development of a 200mm wafer-level 3D monolithic integration process to do this. The first-of-its-kind process integrates scandium aluminum nitride (ScAlN)-based BAW filters with RF SOI switches. The integrated switched filter demonstrated impressive performance for such a small device: Operating at 2.5 GHz, it achieved an insertion loss of <3.6 dB and bandwidth of >120 MHz within a compact area of <1mm^2.

Understanding Charge-Trapping in IGZO TFTs: In recent years, IGZO (indium gallium zinc oxide) has become the focus of intensive research for back-end-of-line (BEOL) and DRAM applications. While most studies have shown IGZO-based devices can meet performance requirements, what's been missing is an in-depth understanding of the fundamental physical mechanisms that limit IGZO device reliability at industry-relevant gate-dielectric thicknesses (EOT) and operating conditions. Characterizing the interface traps, or degradation mechanisms, within the material is fundamental to that understanding. In the **paper #30.1**, an IMEC-led team reported that they developed a new light-assisted spectroscopy method to study charge-trapping in IGZO thin-film transistors (TFTs). It enabled



(a) Schematic of the cross-section of $Sc_{0.15}Al_{0.85}N$-based BAW filter on RFSOI wafer. (b) SEM cross-sectional image of the fabricated monolithic integration wafer. (c) TEM image of the cross-section of BAW stack. (d) TEM image showing the bottom Mo with smooth surface and 20nm seed layer. (e) HRTEM of the $Sc_{0.15}Al_{0.85}N$ layer showing good crystallization with (0002) orientation. (f) Theta 2 theta scan of Mo/$Sc_{0.15}Al_{0.85}N$ stack and rocking curve of $Sc_{0.15}Al_{0.85}N$. **(Paper #16.2, "*3D Monolithic Integration of ScAlN-based GHz MEMS Acoustic Filters on 200mm RFSOI Wafer*," Y. Zhang and X. Wang et al, A*Star)**





Device	1	2	3	4
Dielectric/EOT	SiO_x/10nm	AlO_x/4.8nm	AlO_x/3.3nm	HfO_x/2.8nm
IGZO Deposition Composition	From single 1:1:1 ratio target at 0% O_2 and 300°C 40%In: 40%Ga: 20%Zn		Co-sputtered from 3 monoxide targets at 10% O_2 and RT 38%In: 36%Ga: 26%Zn	
$t_{ch\text{-}IGZO}$	12nm			
V_{fb}(25°C)	-0.403	-0.363	-0.468	-0.417
V_{th}(25°C, @I_D=1e-8A)	-0.021	-0.235	-0.230	-0.240

Summary of devices used in this work: back-gated IGZOTFTs with different gate-dielectrics and IGZO channel deposition/composition are investigated; (top-right) internal photoemission (IPE) shows an IGZO-bandgap (Eg) of ~3.5eV. **(Paper #30.1, "*Characterizing and Modelling of the BTI Reliability in IGZO-TFT using Light-assisted I-V Spectroscopy*," Z. Wu et al, IMEC/KU Leuven)**

them to model the current-voltage (I-V) characteristics of IGZO TFTs under various temperatures and illumination conditions, which provided an understanding of degradation mechanisms and revealed the complex interaction between the gate dielectrics and the IGZO channel. The method may be used with other wide bandgap materials such as GaN and SiC one day as well.

We hope that the above brief description of the selected works illustrates well a very rich program of IEDM 2022. We also hope that it will also foster you, the EDS Newsletter readers, to contribute to the next IEDM edition in December 2023. Finally, we would like to add that in addition to the strictly technical program, two events were carried out during IEDM 2022, i.e. the Luncheon and Evening Panel Session, both on 6 December. During the career-focused luncheon, two industry and scientific leaders talked about their personal experiences in the context of career growth. They were Myung-hee Na, Vice President of SK Hynix's Revolutionary Technology Center, and Lisa Rutherford, Director of Research Science at Meta Reality Labs Research. The evening panel sessions are a tradition of the IEDM conference. They are an interactive forum where experts give their views on important industry topics, and audience participation is encouraged to foster an open and vigorous exchange of ideas. This year's panel was moderated by Stefan De Gendt, Scientific Director at IMEC, and Suman Datta, Professor at Georgia Institute of Technology. The panelists were: Serge Biesemans (IMEC), Anton DeVilliers (TEL), Tahir Ghani (Intel), David Gundlach (NIST), Gosia Jurczak (LAM), Seok-Hee Lee (former CEO SK hynix), Nirmal Ramaswamy (Micron), Heike Riel (IBM). The Session catchword "*75 Years of Transistor Technology—(No) Time for Retirement?*" triggered an entertaining and insightful evening panel discussion on the importance and future of the vanishingly small and yet irreplaceable technology initiated 75 years ago by landmark inventions made by Walter Brattain, John Bardeen (1947 - the point-contact transistor) and William Shockley (1948 - the junction transistor).

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We are looking forward to meeting you at IEDM 2023!

Chronology of Silicon-based Image Sensor Development

Yoshiaki Daimon Hagiwara, IEEE Life Fellow
Sojo University, Kumamoto-city, Japan

Introduction

The article presents key steps of development of silicon-based image sensors. The author's intention has been to present them chronologically. However, since different aspects of the sensor design are discussed, some contents have been duplicated. Hopefully, they do not obscure the overall picture of the image sensor development.

The P+P doping variation in the base region of a bipolar transistor was first proposed by Herbert Kroemer in 1953 to realize the drift-field transistor for high frequency operations as shown in Fig. 1. The forward biased emitter-base junction injects electrons from the electron fog in the emitter into the base. There, the minority carriers swiftly migrate towards the collector thanks to the electric field induced by the P+P doping variation in the base region. Properly shaped doping profiles became later an indispensable building block of silicon image sensors.

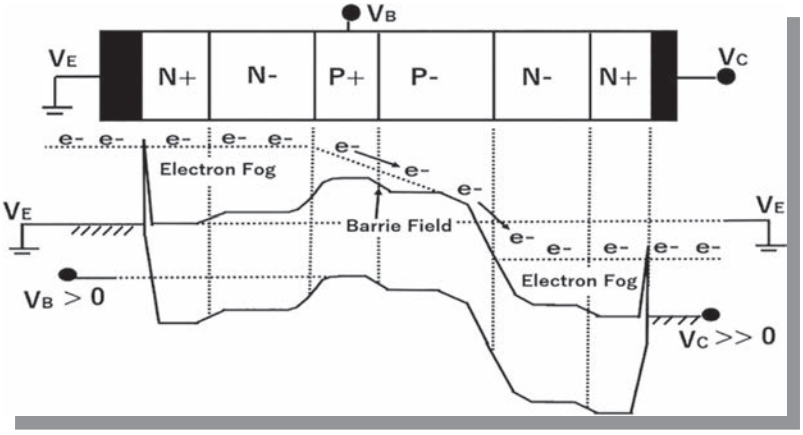

Figure 1. The drift-field transistor for high frequency operations, invented by Herbert Kroemer in 1953

In 1970, the CCD image sensor was invented that provided a complete charge transfer capability without image lag. The CCD image sensors were next intensively studied and refined [1-5]. However, the MOS photo capacitor used in the CCD image sensor employed metallic electrodes that impeded transmission of the short-wave blue light.

In 1975, three double and triple junction pinned photodiodes (PPDs) were invented and patented [7-9]. Reproductions of figures in the Japanese Patent Applications of (a) the N+N-P+NP-P triple junction PPD (JPA1975-127646), (b) the N+N-P+N double junction PPD (JPA1975-127647) and (c) the PNP double junction PPD (JPA1975-134985) are shown in Fig. 2. All of them behave as photo junction-capacitors and have the CCD-like complete charge transfer capability, no image lag feature with in-pixel vertical overflow drain (VOD) structure for the anti-blooming function, and the electronically adjustable exposure time for fast moving action pictures. Potential distributions shown in Fig. 2 clearly illustrate the mentioned above importance of doping profiles in those devices. Devices (a) and (b) both have in-pixel MOS capacitor buffer

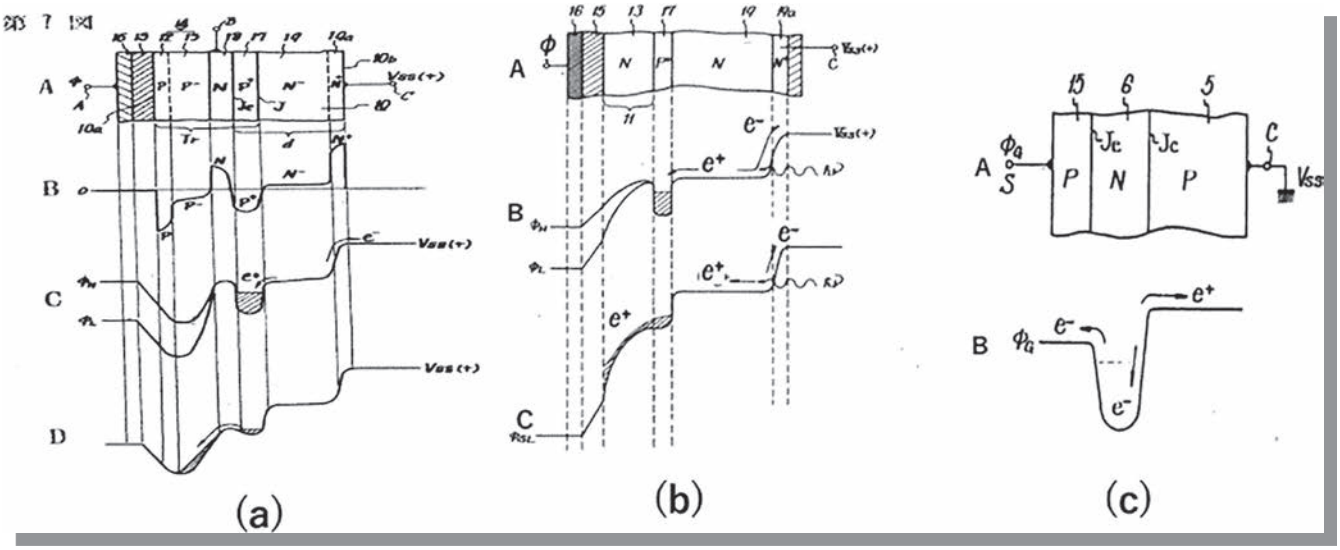

Figure 2. Reproductions from the Japanese Patent Applications of (a) the N+N-P+NP-P triple junction PPD, (b) the N+N-P+N double junction PPD, and (c) the PNP double junction PPD

memory for realization of the global shutter function in the CMOS imagers.

Short-wave blue light with the photon energy higher than 1.1 eV is absorbed in the vicinity of the silicon surface and cannot penetrate deep into the silicon crystal. Therefore, in order to guide the short wave blue light into the deep bulk semiconductor region, wide bandgap semiconductors are generally used, instead of silicon, for high-performance solar cells. However, the problem is that the PN junction barrier potential in the PN junction depletion region cannot be formed at the semiconductor surface because the strong barrier electric field in the depletion region invites the undesired surface dark current. This problem was solved in 1975 for image sensor applications by using the pinned surface P+P doping variation to enhance the short wave blue light sensitivity in the P+PNPN triple junction type pinned photodiode [7-9] which preserves the CCD-like complete charge transfer capability without image lag in the blue light transmission. The pinned surface P+P doping variation effect was used in this device, creating the surface band bending of kT ln(P+/P) to separate the photo electron and hole pairs generated by short wave blue light effectively at the silicon surface.

A 128-bit analog CCD delay line [12] was developed and reported at the SSDM 1977 conference in Tokyo. It used the PNP junction PPDs with the complete charge transfer capability and the unique directionality resulting from the narrow-channel transfer gates for the virtual charge transfer operation (Fig. 3).

In 1978, a frame transfer (FT) CCD area image sensor was reported at the SSDM 1978 conference [13]. That image sensor used the same PPDs with a very low dark current, the complete charge transfer capability and the no image lag feature, as proved by a spectral response and signal output waveforms (Fig. 4). Fig. 4a shows a pinned-surface and buried-storage PNP junction type photodiode. Fig. 4b shows the spectral response of the imager with short-wave blue light sensitivity. Fig. 4c shows the output signal at no illumination showing very low surface dark current level. Fig. 4d shows the output signal waveform with input light, showing the no image lag feature. The hole accumulation region providing the surface pinning is formed by the adjacent heavily doped channel stops obtained using the high energy ion implantation followed by the lamp anneal step, invented and developed by Kazuo Nishiyama at Sony. Many other companies, including Kodak and NEC apparently used either the LOCOS isolation technology or the shallow trench isolation (STI) technology since they are standardized processes widely used for the digital CMOS LSI chips. However, the LOCOS and STI processes induce the extra thermal stress and the undesired crystal damage, degrading the chip yield and reliability. Therefore, since 1978 Sony has used neither LOCOS nor STI in the image sensor productions. The image sensor reported at the SSDM 1978 conference [13] was the world's first PNP double junction PPD.

Fig. 5 shows different variants of photodiodes. Fig. 5a shows again the PNP double junction PPD developed by Sony in 1978. Fig. 5b shows the PPD defined and presented by the Semiconductor History Museum of Japan. Both photodiodes have the adjacent heavily doped P+ channel stop regions formed by the deep high energy ion implantation and without the use of LOCOS or STI isolation. For a comparison, Fig. 5c shows the buried photodiode developed by NEC [17], Fig. 5d shows the PPD developed

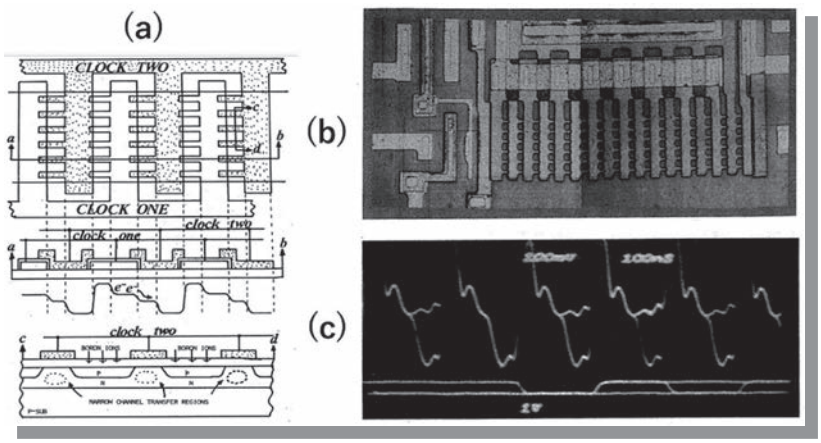

Figure 3. (a) Top and cross-sectional views with the PPD type SiO_2-exposed light-receiving windows; (b) the chip photograph at both ends of the two-phase narrow-channel CCD analog delay line; (c) the output waveform showing the complete charge transfer capability without image lag

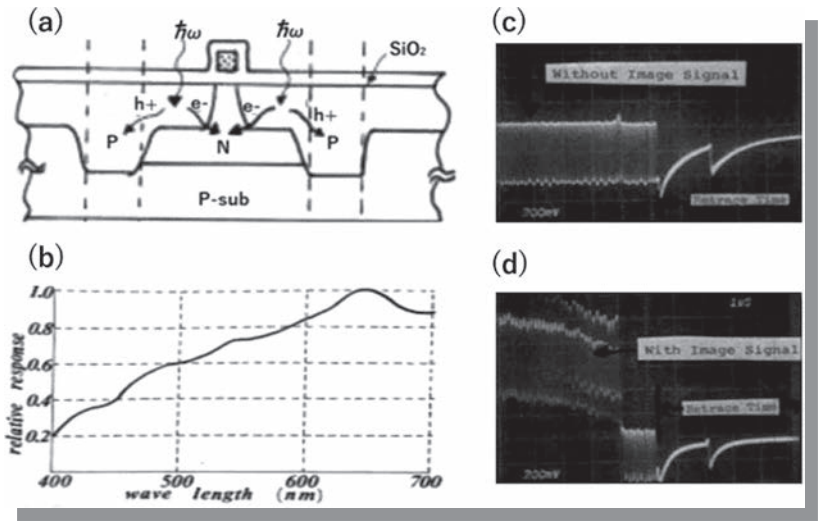

Figure 4. (a) Pinned-surface and buried-storage PNP photodiode; (b) spectral response of the blue-light sensitive imager; output signal (c) without (d) with illumination

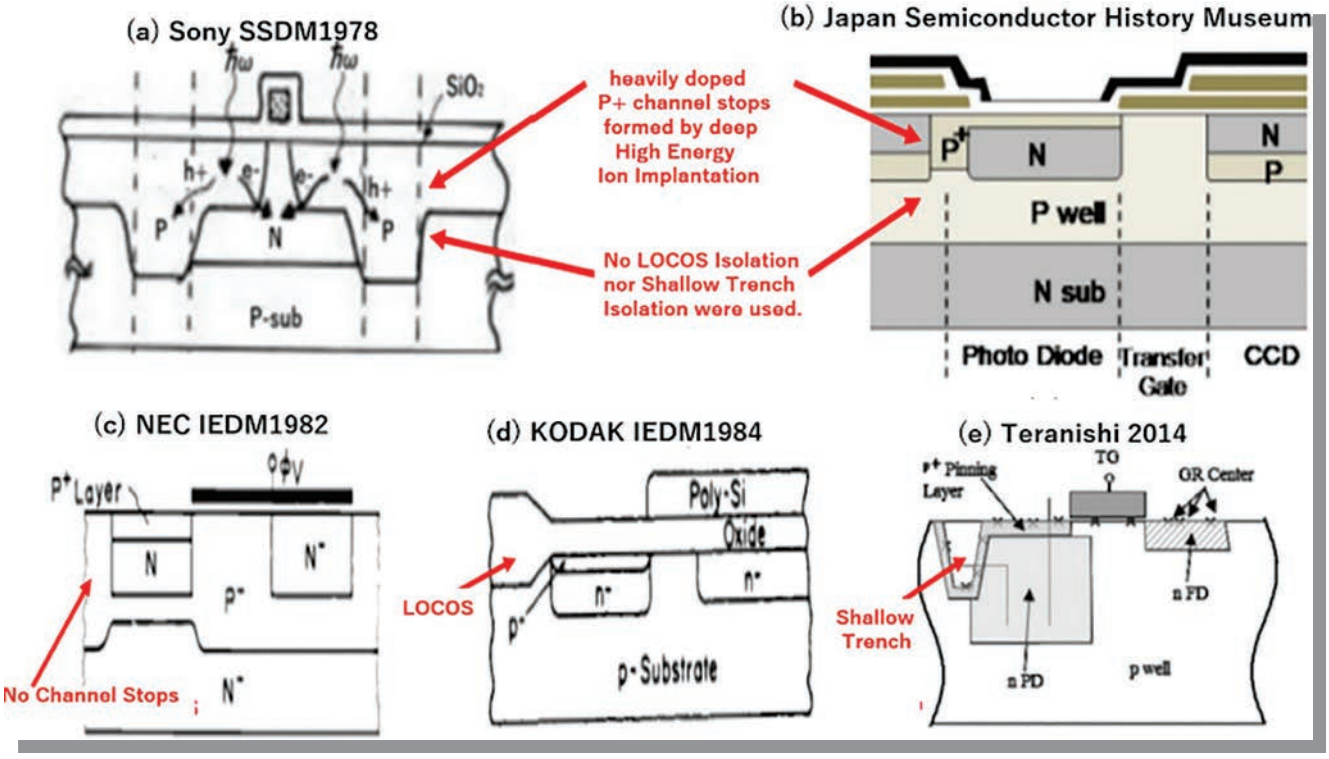

Figure 5. (a) PNP double junction PPD developed by Hagiwara team at Sony in 1978; (b) PPD defined and shown by Semiconductor History Museum of Japan, (c) NEC buried photodiode [17], (d) Kodak PPD [18], (e) PPD reported by Teranishi [25,26]

by Kodak [18] and Fig. 5e shows another conventional pinned photodiode reported by Teranishi [25-26].

A subsequent review paper [21] in 1996 revisited the 1975 invention [9] and the SSDM 1978 paper [13], and explained that it was essentially the invention of both the virtual-phase CCD with the built-in narrow-channel type directionality and the no-image-lag feature, which became the basis of Sony's so-called "Hole Accumulation Diode," (HAD) with the anti-blooming function capability and with the low thermal and crystal stress.

The image sensors include not only detection diodes but also control circuitries. Bipolar transistor and thyristor are switching devices using the base region as a gating-switch while the double and triple pinned photodiodes use the in-pixel clocked overflow-drain (OFD) to realize the anti-blooming, the global shutter function and the electronic shutter function, by controlling the light exposure time with a complicated external clocking sequence according to the TV scanning system.

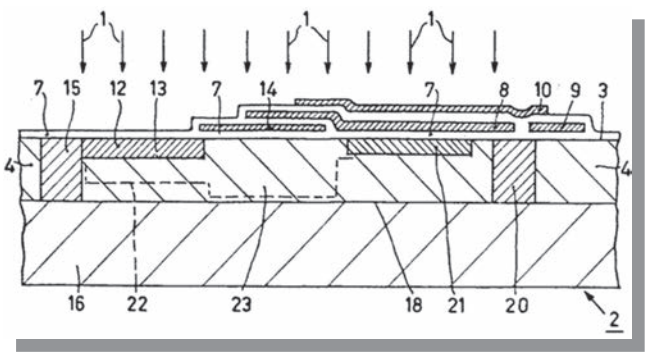

Figure 6. The double junction type buried photodiode image sensor reproduced from Netherland Patent Application NPA [6]

The world's first Double Junction-type Buried Photodiode

As it has been mentioned above, the MOS photo capacitor used in a CCD image sensor employs metallic electrodes which impede the short-wave blue light transmission. Philips solved this problem in 1975 using the first double junction type buried photodiode [6]. In Fig. 6 from the NPA7506795 patent, a dashed potential profile (12) is drawn to show an empty potential well of a complete charge transfer. No image lag feature was expected in this design. However, in reality the surface P region is connected to the high resistivity substrate (16) by a resistive region (15). Evidently, the surface region (13) may have a large RC delay time constant, introducing a serious image lag problem. Thus, the surface region (13) potential is not completely pinned and is floating with a RC delay-time, inviting time-lag and image-lag problems. Therefore, by definition such a structure cannot be considered to be a pinned photodiode.

The world's first Triple Junction-type Pinned Buried Photodiode

The double junction buried photodiode without the metallic electrode has a fair light-sensitivity. More detailed surface doping engineering is required to enhance the short-wave

blue-light sensitivity of such a device. This problem was solved by using the pinned surface P+P doping profile in the PNPN triple junction type PPD [7], which preserves the CCD-like complete charge transfer capability without image lag in the blue-light transmission. By analogy with a rubber belt that must be fixed at one end in order to be stretched by strong pulling down, also the surface potential of the photodiode must be pinned in order to create the potential profile enabling a punch-through mode to realize the complete transfer of charge without the image lag.

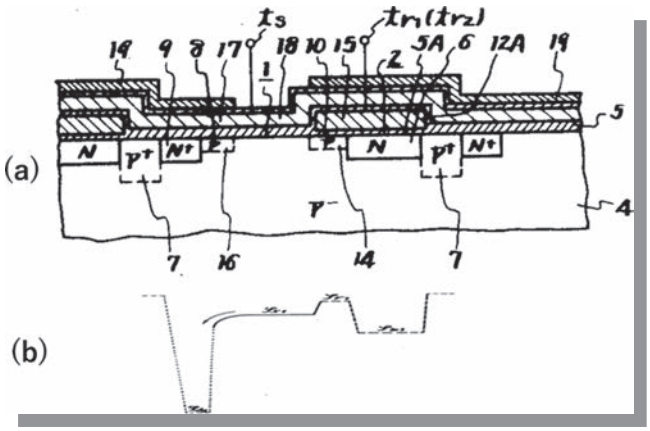

Figure 7. Figures reproduced from Japanese Patent Application JPA1977-126885 [10]: (a) sensor, (b) potential profile for the OFD punch-through action

The world's first Pinned Photodiode with the Global Shutter and the Electronic Shutter functions

The JPA1975-127646 patent application [7] defined the world's first PNPN triple junction type PPD, also equipped with an in-pixel MOS capacitor type buffer memory. This device together with two other ones, also invented by Sony [8, 9], enabled realization of the global shutter clocking scheme needed for modern CMOS image sensors. The electronic shutter clocking scheme was invented in 1977 by Sony and used in the MOS/CCD dynamic photo capacitor [10] (Fig. 7a) with the in-pixel lateral anti-blooming overflow-drain (OFD). The potential profile at the OFD punch-through action with the complete photo signal-charge transfer-and-draining action into the in-pixel lateral OFD is presented in Fig. 7b. Both pictures are reproductions of drawings in [10]. This punch-through action-mode clocking-scheme can also be applied in the PNPN-triple-junction pinned photodiode. Such a punch-through action corresponds to a triple-junction photo-thyristor switching-on action as originally invented in 1975 [7] (see Fig. 2a).

The two mentioned above types of global shutter clocking schemes in CMOS image sensors are illustrated in Fig. 8a, 8b. Fig. 8a shows the normal global shutter mode, where the light integration time is the same as the unit scanning period (1/60 sec) of the television scanning system, which

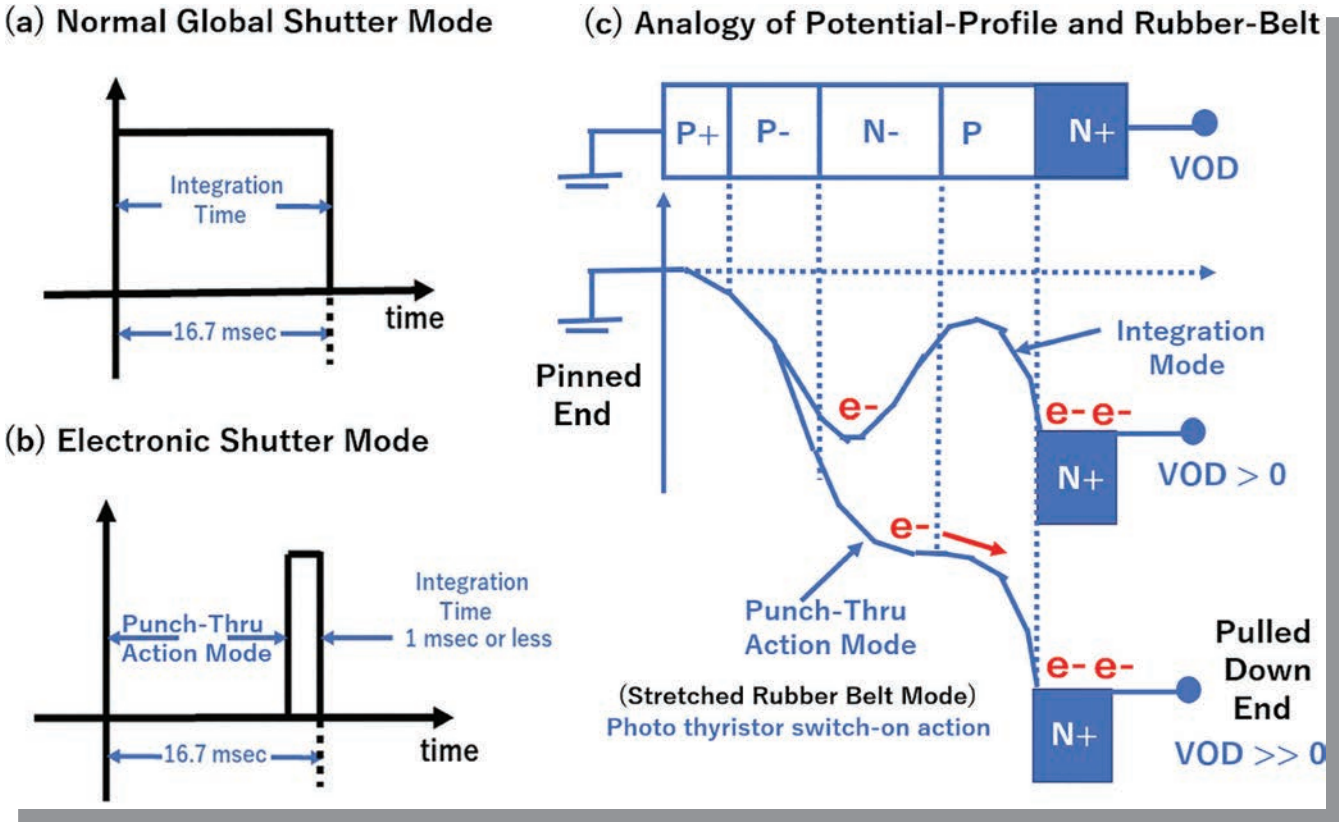

Figure 8. (a), (b) Global shutter clocking schemes for CMOS image sensors: normal global shutter mode, electronic shutter mode; (c) the electrical potential profile of the P+PN-PN+ triple junction type PPD in the photo thyristor switch-on mode and in the integration mode

is too long to obtain a clear still picture of a fast-moving action-object. Fig. 8b shows a special case of the global shutter with a shorter exposure time, namely the electronic shutter which is controlled by adjusting the clocking pulse width of the in-pixel clocked overflow drain (OFD). Invention of the electronic shutter revolutionized the completely mechanical parts-free solid-state image sensor world [10].

In 1987, Kikuyo Ishikawa and her team at Sony used the electronic shutter clocking scheme and applied successfully for the first time in the world in a complete and finalized form for production of the P+PN-PN+ triple junction type PPD [19, 20] with the anti-blooming vertical-overflow-drain (VOD). Fig. 8c illustrates in a simplistic way a principle of operation of such a device in the integration mode and in the punch-through mode. In both modes the potential is pinned at the P+ area and the analogy to the rubber belt stretching model is visible.

The world's first Interline Transfer-type CCD Image Sensor

When the first interline transfer (ILT)-type CCD image sensor was proposed, the widely used floating surface N+P single junction type photodiode suffered from the serious image lag problem. Philips 1975 patent application on the buried photodiode [6] and Sony 1975 patent applications on the pinned photodiode [7-9] both were originally intended to apply for the ILT type CCD image sensors. Teranishi at NEC also filed in 1980 a patent [15] on the buried photodiode structure, very similar to the one proposed in 1975 by Philips, and reported at IEDM 1984 [17]. These photodiodes also apply in modern CMOS image sensors. However, it has to be mentioned that in the scope of the patent [15] the floating surface with surface electric field exists in the device. Consequently, both the surface and the buried charge storage region become floating. Due to this, the buried photodiode defined in the patent [15] may have a serious image lag. Therefore it cannot be deemed a PPD.

Sony developed in 1980 and reported in [14] the ILT-type CCD image sensor, using a thin polysilicon (SIPOS) gate type MOS photo-capacitive type sensor structure with the in-pixel lateral OFD for the anti-blooming and electronic shutter function capabilities. The photo sensor structure was of a MOS/CCD photo capacitor-type which had the complete charge transfer capability and the no image lag feature as shown in Fig. 7 reproduced from Japanese Patent Application JPA1977-126885 [10].

At IEDM 1982, Teranishi's team presented a NEC-developed ILT-type CCD image sensor, using the PNP double junction type Buried Photodiode [17]. The details of the image lag data were reported. Neither LOCOS nor STI were used in the manufacturing process. The schematic view of the device is shown in Fig. 5c.

KODAK developed and reported at IEDM 1984 the ILT-type CCD image sensor using the PNP double junction type pinned photodiode [18]. KODAK emphasized there the importance of the pinned surface in order to achieve the complete charge transfer capability and the no image lag feature. The LOCOS step was used in manufacturing of the device that is shown in Fig. 5d.

Sony reported in a Japanese domestic journal [19] and also at SPIE 1989 conference [20] the ILT-type CCD image sensor, using the PPD of the PNPN triple junction-type with the anti-blooming and the electronic shutter function capabilities. Also in this work, it was emphasized that the pinned surface is a prerequisite for the complete charge transfer capability, the no image lag feature and also the high frequency electric shutter function, in order to achieve the completely mechanical-part-free solid-state image sensors.

The lost invention of the Pinned Photodiode

The Pinned Photodiode technology greatly contributed to design, development, and improving the performance of back-illuminated CMOS image sensors. Sony applied for three basic patents JPA 1975-127646 [6], JPA 1975-127647 [7] and JPA 1975-134985 [8] on pinned photodiodes in the Japanese Patent Office. However, Sony did not apply to any US Patent Office and other overseas patent offices. The invention was completely forgotten by the rest of the world until June 26, 2020 when Sony finally disclosed officially the 1975 patent applications and quoted the Sony efforts in 1978 of developing the first PNP junction type PPD [33]. Subsequently, Semiconductor-History Museum of Japan also published a supporting article [34].

Pinned Photodiode adopted for Back-Illuminated CMOS Image Sensors

The Pinned Photodiode is a technology that contributes to improving the performance of back-illuminated CMOS image sensors, and the history of inventions and product development is as below.

After the invention of the back-illuminated N+NP+N double junction-type PPDs, the N+NP+NP triple junction-type PPDs, and the PNP double junction-type PPDs, Sony succeeded in making for the first time in the world a principle-prototype of a frame transfer (FT) CCD image sensor that adopted the PNP junction-type PPD technology, having the P+ channel stop region formed by ion implantation near the light receiving section. The related technical paper was presented at the academic conference SSDM 1978 [13]. This achievement was commercialized soon. In 1980, Sony succeeded in making a camera integrated VTR which incorporated the new one-chip FT CCD image sensor. This development was announced during the press conferences held on the same day in Tokyo and New York by the President of Sony, Kazuo Iwama and the Chairperson of Sony, Akio Morita respectively. This announcement surprised the world.

In 1987, Sony succeeded in developing an 8 mm video camcorder that adopted, for the first time in the world, the ILT CCD image sensor with VOD function, which incorporated PPDs with the P+ channel stop region formed by ion implantation near the light receiving section. This camcorder became the pioneer of the video camera market [23-32]. The PPD technology that has been nurtured through such a long history is still used in back-illuminated CMOS image sensors [33-34].

Sony's announcement on the invention of Hole Accumulation Diode (HAD)

In 1987, Sony developed a 2/3-inch, 380,000-pixel CCD image sensor using a Hole Accumulation Diode (HAD) [19-20]. It was a new type of the PPD. Its construction enabled efficient reduction of the dark current noise. This image sensor was next installed in the 8mm VTR integrated video camera "CCD-V90". In the 1990s, the era of passport size video cameras demanded compact CCD image sensors with large numbers of pixels (1/2 inch or smaller with 400,000 pixels or more). As a result, Pinned Photodiodes came to be widely used by manufacturers of the CCD/CMOS image sensors [21]. In 1995, Kodak adopted them for their CMOS imagers.

The future application of Pinned Photodiode for High Quantum Efficiency Solar Cells

Japanese Patent Applications (JPA) [7-9] by Sony in 1975 explained in details and defined the first triple junction type Pinned Buried Photodiode with the in-pixel vertical overflow drain (VOD) function with the electronic shutter capability of the electrically-adjustable exposure time control, realizing the completely film-free and mechanical-parts-free all-digital solid-state image sensors. Sony showed in 1975 in the patent applications that the conventional PN junction depletion region is not the only place to have a barrier potential needed for photo electron hole pair separation. A clever doping-engineering of the pinned surface P+P hole accumulation region can also create the surface barrier electric field to enhance drastically the photoelectron and hole pair separations to increase the short-wave blue light sensitivity. This surface P+P doping-engineering with the completely-depleted buried N- region, together with the metallic-trench formation, by eliminating the substrate-resistance of the cause of Joule-heat, may realize a high quantum efficiency (QE) pinned-buried double-junction pinned-photodiode type solar cell. Thus, the double and multi-junction pinned photodiodes with the excellent QE for the short-wave blue-light spectrum widely used

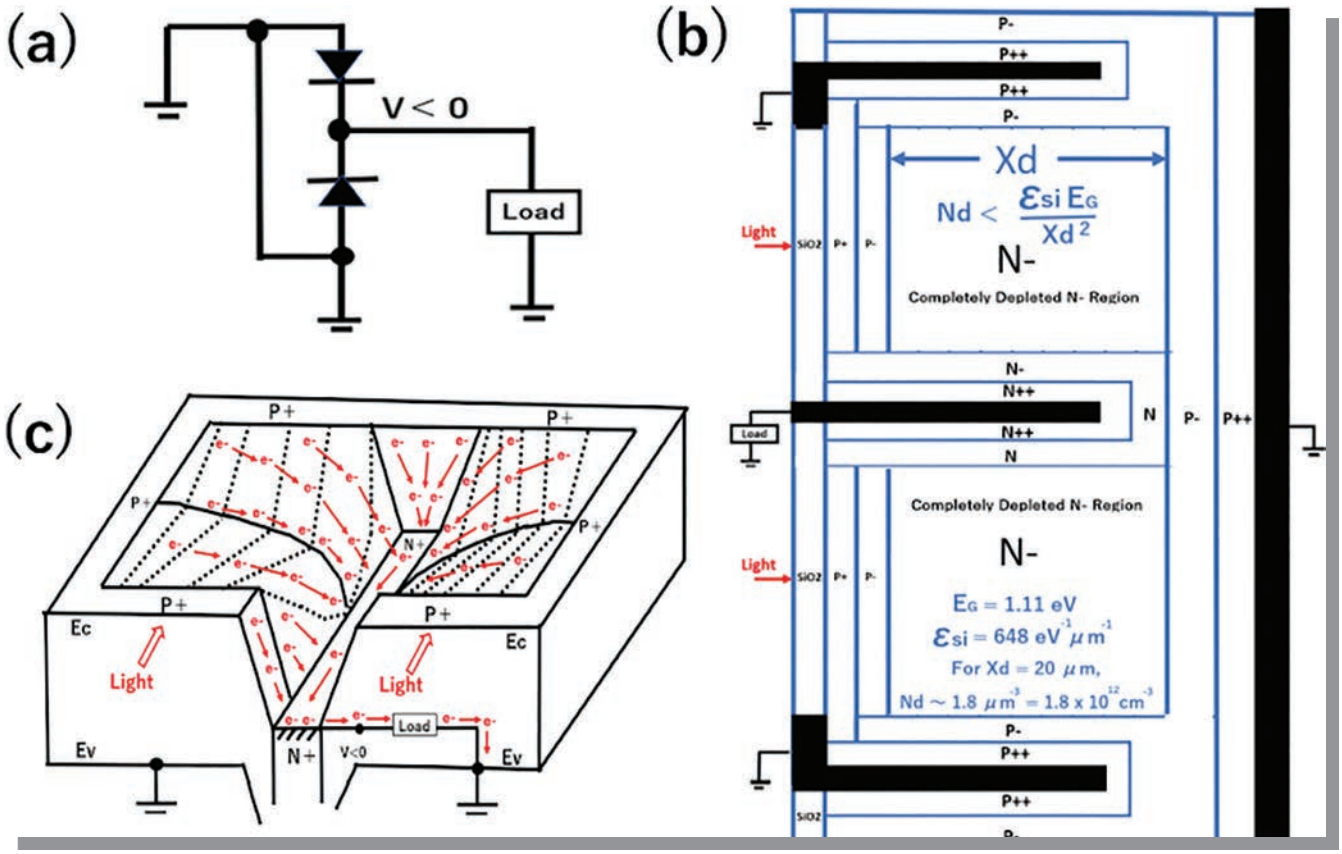

Figure 9. (a) The equivalent circuit of double junction pinned photodiode type solar cell, (b) the cross-sectional view and (c) the two-dimensional potential profile with a completely-depleted buried N- region of strong electric field, guiding photo electrons swiftly into the heavily doped metallic N+ chare collecting region

now in image sensors may have a possible application for future high QE solar cells by using the low-cost high-resistivity silicon crystals.

Image sensors and solar cells both convert the photon energy into the electron energy. Fig. 9 shows a possible future solar cell application of the double junction-type PPD. The lightly doped buried N- region is completely depleted. Thus a strong electric field exists for the photo-electron and hole pair separations. Fig. 10 shows another possible future solar cell application of a multi-junction type pinned buried photodiode with the P+P surface doping variation and the fully depleted multiple buried N and P regions. Fig. 11 explains the advantage of the P+PNPP+ double junction-type solar cell over the conventional N+P single junction-type solar cell. The P+P surface doping profile creates the surface conduction-band bending that enhances photo-electron and hole pair separation at the semiconductor surface resulting in a high quantum efficiency for the short-wave blue light. Contrary to the multi-junction solar cell, the floating-surface N+P single-junction type photodiode has no surface electric field that could support separation of the photo electrons and holes generated in the vicinity of the N+ flat surface, The photogenerated carriers do not move and eventually they recombine with each other, resulting in a poor QE for the short-wave blue-light.

Summary

The article reviews the chronology of development of different types of the pinned photodiodes. Steps towards achieving the excellent short-wave blue-light sensitivity are emphasized. These steps were followed in the past by many successful realizations of the pinned photodiodes and their applications in different image sensors and equipment.

The article is focused on works done by teams from Sony, including double junction-, triple junction-type PPDs, ILT PPDs, HADs, to name a few. Obviously, only a part of the achievements in this area are presented in this paper. The inventions made by teams from the companies like Kodak or Hitachi are reported elsewhere.

The main author's message in this article is that (i) the short-wave blue light sensitivity is the most important

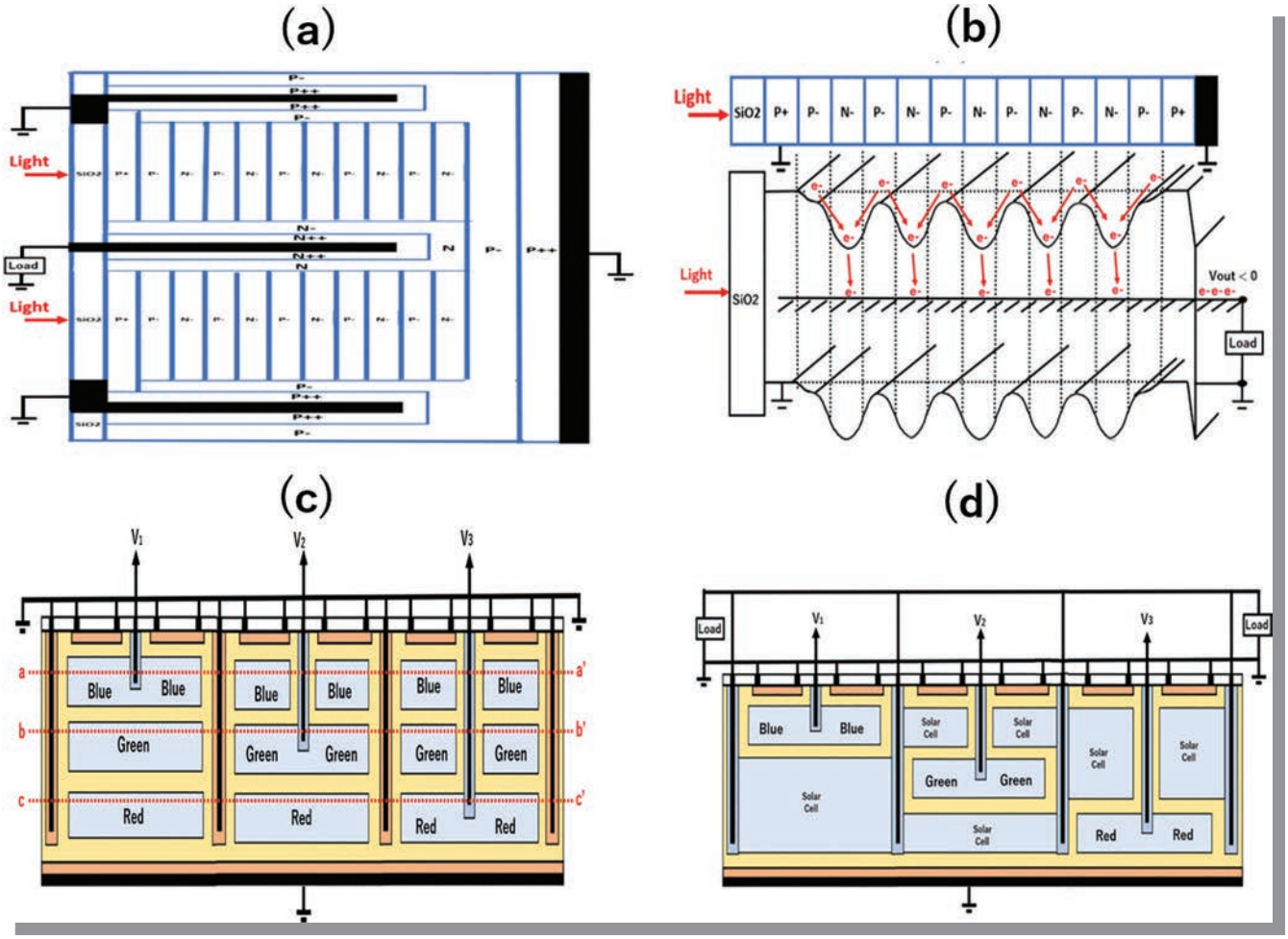

Figure 10. (a) The cross-sectional view and (b) the potential profile of a multi-junction pinned photodiode type solar cell; (c) a color-filter-less color image sensor; (d) a combination of a color-filter-less color image sensor and a solar cell

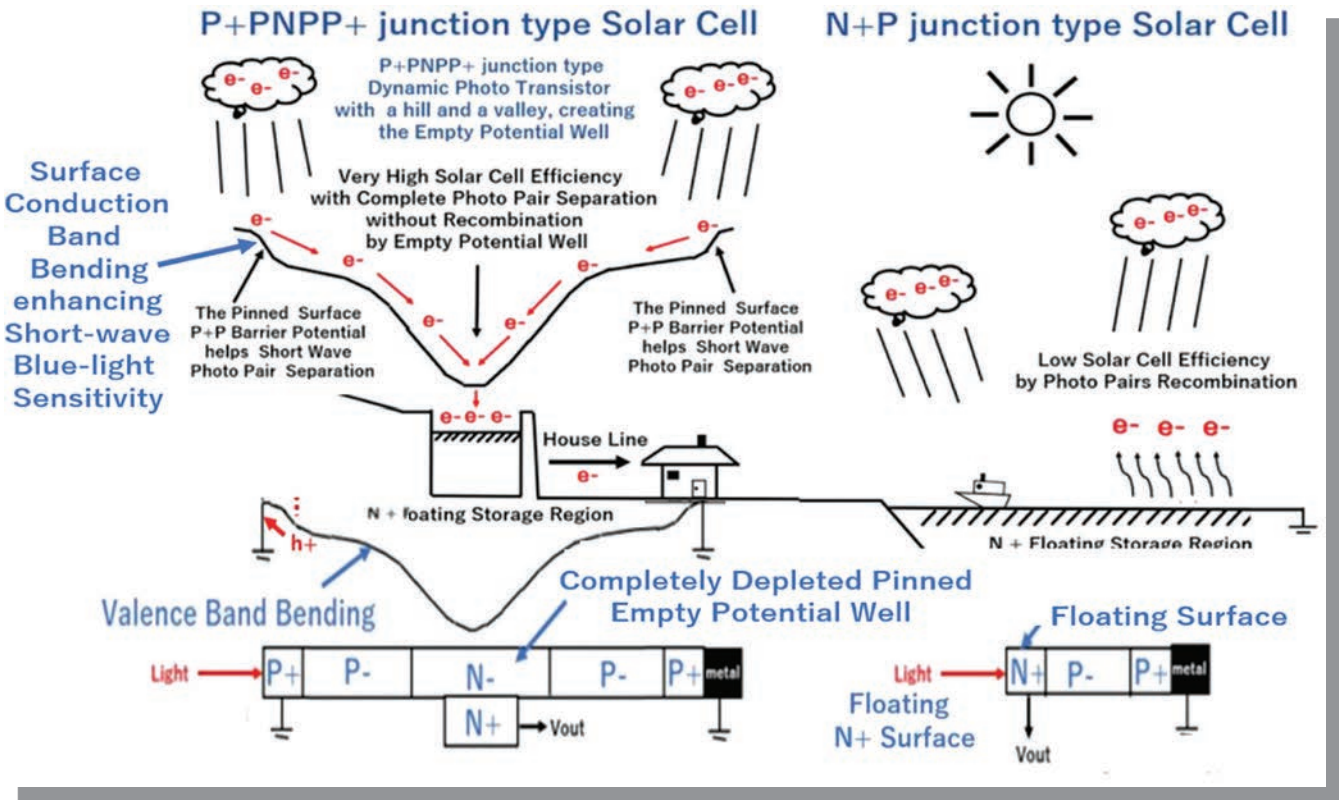

Figure 11. The PNP double-junction PPD with the completely depleted N region and the floating N+ storage region has an excellent quantum efficiency (QE) for the bluelight. The floating-surface N+P single-junction-type photodiode has no surface electric field, where the photogenerated electron and hole pairs do not move and eventually they recombine with each other, resulting in a poor QE for the short-wave blue-light

advantage of the double- and multi-junction pinned buried photodiodes, (ii) the pinned buried photodiodes enabled implementation of the electronic shutter in the image sensors. These are two factors that revolutionized the completely mechanical parts-free solid-state image sensor world.

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Prof. James McCaldin at California Institute of Technology (Caltech) introduced and taught the basic semiconductor device physics at Caltech in 1969 with plenty of side-wall back-ground exciting stories of the Intel self-aligned MOS transistor technology and the newly developed high energy ion implantation technology.

Prof. C. A. Mead and Prof. T. C. McGill at Caltech advised my original 1971 undergraduate work on the Ga2O3-Au Schottky Barrier interface study and characterization, and for guiding my 1974 PhD thesis work on Charge Transfer Analysis of Buried Channel CCD Image sensors.

Sony Image Sensor R/D efforts started in 1969 with the strong initiative of the ex-president of Sony Corporation, Kazuo Iwama, who emphasized the market need of the portable small video camera with no image lag feature for the fast-action and snap-shot pictures. Kazuo Iwama gave Hagiwara a chance to work at Sony in 1975 to build an artificial intelligent image sensor system with the real time robot vision and the powerful digital circuit engines for real time operations.

Under the guidance of Dr. Sei-ichi Watanabe, Sony team of Miyaji, Nakagawara, and other young engineers helped me to develop in 1989 for the first time in the world the 25-nano sec access-time 4 Megabit fast-cache SRAM chip, needed to realize a fast- snapshot full-size image-capturing system for digital solid-state cameras.

SONY bipolar process and device technology gave many hints and guided me to the original 1975 invention and the 1978 successful development for the P+PNP double junction type Pinned Photodiode.

Yoshiyuki Kawana at Sony in 1950s invented the low-collector on-resistance P+P-N+N-P-P+ junction type

bipolar transistor for high frequency operation by thinning the back side of the silicon wafer, a technique now widely used for the modern backside illumination CMOS image sensors to improve sensitivity.

Toshio Kato at Sony in early 1960 invented the silicon surface light etching technique and new SiO2 passivation technique for the P+NP junction type bipolar transistor with the MESA like isolation, which is now known as the shallow trench isolation with the excellent side wall SiO2 to reduce the device leakage current. Both ideas of Yoshiyuki Kawana and Toshio Kato hinted to form in 1975 the concept of the Pinned PNPN triple junction type dynamic photothyristor with the electronic shutter switch-on action.

Sony young-generation engineers, including Hamazaki and Ishikawa chip-design team and Kambe CCD-process team, used in 1987 the triple junction type pinned buried photodiode invented in 1975, which has the built-in VOD structure capable of the electronic shutter and snapshot picture functions, and produced for the first time in the world the all-solid-state snapshot fast-action video cameras, completely free from mechanical parts. The feature of the global shutter function using an in-pixel MOS-capacitor-type global buffer memory became a reality in modern backlit CMOS image sensors by the young generation of Sony engineers after the 45 years since the invention in 1975.

Special thanks go to Prof. Hiroshi Iwai, Dr. Tsugio Makimoto, Ki-ichiro Mukai, Terushi Shimizu, Yasuhiro Ueda, and Dr. Tadakuni Narabu for their encouragement and kind advice. Lastly but not the least, Dr. Sei-ichi Watanabe, Yoshiyuki Kawana and Toshio Kato guided and helped me whenever I was in need. They are all dear friends and mentors in private and public.

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A Review of the 2022 ESSDERC-ESSCIRC Conference: the Annual European Forum on Recent Advances in Solid-State Devices and Circuits

The aim of ESSDERC and ESSCIRC is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. The level of integration for system-on-chip design is rapidly increasing. This is made possible by advances in semiconductor technology. Therefore, more than ever before, a deeper interaction among technologists, device experts, IC designers, and system designers is necessary. While keeping separate Technical Program Committees, ESSDERC and ESSCIRC are governed by a common Steering Committee and share Plenary Keynote Presentations and Joint Sessions bridging both device and circuit communities. ESSDERC and ESSCIRC have evolved over the last years to follow recent fast-growing R&D device, circuit, and system topics. Besides the traditional ESSDERC and ESSCIRC tracks, a number of joint tracks have been introduced, to encourage and facilitate interactions between circuit, system, and device researchers. Along this line, this year for the first time the governance structure of the Technical Program Committees was revised to have a single Technical Program Chair who coordinated the actions of three different Technical Program Co-Chairs, one for the ESSDERC tracks, one for the ESSCIRC tracks, and one for the joint tracks. Attendees registered for either conference had the chance to attend any of the scheduled parallel sessions, regardless to which conference they registered to.

University of Milan-Bicocca was very proud to organize the 52nd European Semiconductor Device Research Conference (ESSDERC) and the 48th European Semiconductor Circuits Conference (ESSCIRC). The event was held in presence, in Milan, Italy, 19–22 September 2022. Notwithstanding the echoes of the global pandemic, which forced the last two editions of the conference to offer virtual attendance, the participation to the event exceeded the expectations, with over 870 registered participants from all over the world (including a significant share from the US and the Far East), i.e., the highest attendance in the last ten years, confirming the event as the flagship European meeting in the field of semiconductor devices and circuits. We would like to thank the organizing team who coordinated the event as well as the administrative team set up around the company Sistema Congressi. The ESSDERC conference was financially sponsored by the IEEE Electron Devices Society and ESSCIRC by the IEEE Solid-State Circuits Society. Many world-class as well as local companies in the field of micro- and nano-electronics present in the northern Italy area co-sponsored the conference:

- *Diamond*: Bosch, Huawei, Infineon, STMicroelectronics
- *Gold*: Sony, Synposys
- *Silver*: ams OSRAM, Analog Devices, INVENTVM, Kioxia, Knowles, Melexis, RedCat Devices, Samsung, SERMA, TDK

- *Bronze*: Cadence, EUROPRACTICE, GlobalFoundries, Innatera, Photeon Technologies, X-FAB

The first day of the conference was devoted to a rich program of workshops and tutorials coordinated by Pietro Siciliano (CNR, IT) and Dirk Droste (Bosch Sensortec, DE), and attended by more than 380 people. Seven full-day and two half-day tutorials were proposed in parallel sessions. The two half-day tutorials focused on *Wide Bandgap Semiconductors for Energy Efficiency and RF communications* and *Gallium Nitride in Power Electronics Converters, Motor drive, DC-DC, and Lidar*. The full-day tutorials covered a broad range of topics of interest for both the device and the circuit communities, including key aspects for the future development of the micro- and nano-electronic industry at the European level: *Wafer-level 3D Stacked Imagers: Technologies and Sensors Architectures, BEOL Compatible Ferroelectric Device Technologies for Neuromorphic Computing, Bosch - ASIC Development for MEMS Sensors - Challenges and Solution Approaches, A Year of Open Source MPWs: Review, Takeaways and Roadmap, Wearable Applications and Artificial Intelligence Based on 2D materials, Computing Architecture for AI, Future of Short Reach Interconnect*. In addition, three half-day dissemination workshops were organized on *Smart Power Technologies and Applications, Embedded Artificial Intelligence (EAI) – Devices, Systems*, and *Industrial Applications, and IPCEI (Important Project of Common European Interest)*.

The conference was then officially opened by the general chair of the conference, Prof. Andrea Baschirotto (University of Milan-Bicocca, IT), who welcomed the attendees and introduced the four Plenary (joint), the three ESSDERC, and the three ESSCIRC Keynote Presentations. After the introduction and conference opening, the joint plenary presentations by David Tonietto (Huawei Technologies, US) and Tim Gutheit (Infineon Technologies, DE) followed. David Tonietto held a talk titled "The Future of Short Reach Interconnect" which gave the attendees a vision on high speed electrical interconnect and new approaches in optical interconnect to improve performance, energy efficiency and density. Tim Gutheit's talk "Semiconductors Take the Driver's Seat - Challenges and Opportunities for the Car of the Future" provided outlooks on advanced semiconductor technologies and concepts which will be instrumental to tackle the challenges related to innovations in modern vehicles, autonomous driving and electrification. Two additional joint plenary presentations took place in the following two days of technical program, one given by Dirk Droste (Bosch Sensortec, DE) titled "Integrated Circuits as Key Enabler for Today's Smart MEMS Sensors" and one by Domenico Arrigo (ST-Microelectronics, IT) titled "The Next "Automation Age": How Semiconductor Technologies Are Changing Industrial Systems and Applications". In addition, three ESSDERC keynote presentations were given by Heike Riel (IBM Research, CH) on "Quantum Computing Technology and Roadmap", by Victor Veliadis (PowerAmerica and North Carolina State University, US) on "SiC Power Device Mass Commercialization", and by Iuliana Radu (TSMC Corporate

Figure 1. A picture from the questions and answers time right after the end of the joint plenary presentation by David Tonietto (Huawei Technologies, US) entitled "The Future of Short Reach Interconnect". The keynote speaker is standing at the podium together with the conference General Chair, Prof. Andrea Baschirotto (University of Milan-Bicocca, IT)

Research, TW) on "The Scaling Potential of Transistors with Low Dimensional Materials". The three ESSCIRC keynote presentations were delivered by Rinaldo Castello (University of Pavia, IT) on "Reminiscing Through 40 Years of CMOS Analog Circuit Design: from Audio to GHz", by Massimo Alioto (National University of Singapore, SG) on "From Less Batteries to Battery-Less: Enabling a Greener World Through Ultra-Wide Power-Performance Adaptation Down to pWs", and by Vida Ilderem (Intel, US) on "Innovations for Intelligent Edge". On top of that, 176 contributed papers with deep insights and high-level technical content were presented during the conference in 44 sessions, and can be found in the proceedings published on IEEEXplore. The 44 sessions were organized in order to keep consistency with the different tracks to which the contributions were submitted. Specifically, there were 7 ESSCIRC tracks focused on different aspects of circuit design (from analog to digital, RF/mmWave, and power), 3 ESSDERC tracks (Advanced Technology, Process and Materials - Analog, Power and RF Devices - Compact Modeling and Process/Device Simulation) as well as 3 Joint tracks that welcomed contributions in which device- and circuit-level aspects merged together in tackling relevant and hot topics (Emerging Computing Devices and Circuits - Memory Devices and Circuits towards non von Neumann - Devices and Circuits for Sensors, Optoelectronics and Display).

In addition to the technical sessions, the conference hosted several noteworthy events. At the end of the tutorials and workshops, the conference hosted a panel discussion on the contributions of the local area (i.e., Lombardy, the region in which Milan is) to the field of microelectronics and the related growth perspectives. The discussion, hosted by Andrea Lacaita (Polytechnic of Milan, IT), started with a welcoming speech by Giovanna Iannantuoni (Rector, University of Milan-Bicocca, IT) and Fabrizio Sala (Lombardy region council member for education, university, research, innovation and simplification, IT) and saw the participation of Francesco Svelto (Rector, University of Pavia, IT), Giuliano Busetto (Digital Industries CEO Siemens S.p.A and Past President of "Federazione ANIE", IT), Renato Lombardi (Huawei Fellow, President of Italy Research Center, IT), Alessandro Matera (CEO of Infineon Technologies Italy, IT), and Giuseppe Notarnicola (President of STMicroelectronics Italy, IT). The event featured fruitful and lively discussions promoted also by the presence, in the audience, of a significant number of young students and of technical staff members from several companies. The following day, a mentoring event took place at lunch organized by the IEEE Young Professionals and Women in Engineering and co-sponsored by the IEEE Electron Devices Society (EDS) and Solid-State Circuits Society (SSCS). The event saw a significant participation from the young PhD students, post-docs, and early stage professionals – especially women – present at the conference who had the chance to connect with SSCS and EDS executives and luminaries in the field while having an informal lunch break. Another notable event was held two days later, i.e., a panel discussion on the EU Chips Act. In this event, high representatives of the EU Commission, industry and academia discussed the expected actions and impact of the Act as a response by the EU Commission and Member States to the current scenario which, due to the recent health and supply crisis, demonstrated the importance of the semiconductor sector for the EU societal needs and industrial base. The discussion, moderated by Joachim Burghartz (Director of the Institute for Microelectronics Stuttgart IMS CHIPS, DE), was participated by Alessandro Aresu (Member of European Semiconductor Expert Group, IT), Sabine Herlitschka (CEO, Infineon Technologies, AT), Carlo Reita (CEA-Leti, Director Strategic Partnerships and Planning, FR), Enrico Sangiorgi (University of Bologna, Italian Research Ministry, Coordinator of the Technical Board for the study regarding Next generation semiconductor technologies, IT - Sinano Institute), and Lucilla Sioli (European Commission, Director for Artificial Intelligence and Digital Industry).

The conference also included an intriguing social program. The welcome reception took place at the iconic "Castello Sforzesco", one of the largest castles in Europe, and included the possibility of a guided visit to Michelangelo's "Pietà Rondanini" and to the "Merlate" (battlements) for all attendees. The Gala Dinner took place at the "Museo Nazionale della Scienza e della Tecnologia Leonardo da Vinci", one of the largest science and technology museums in Europe nestled in the cloisters of a Renaissance monastery. The event offered the possibility of dining with the view of the hull of the "Luna Rossa" racing boat suspended at the ceiling and saw the artistic contribution of singers and musicians from the "La Scala" theater in Milan.

In Summary, ESSDERC-ESSCIRC 2022 was an inspiring event with ample participation and a rich and stimulating program. The ESSDERC-ESSCIRC community is looking forward to another exciting edition in Lisbon, Portugal, 11–14 September 2023.

Prof. Francesco Maria Puglisi
2022 ESSDERC Technical Program Co-Chair
University of Modena and Reggio Emilia
Italy

Prof. Felice Crupi
2022 ESSDERC Publication Chair
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Systems and Architectures (SA)

Kirk Bresniker, Hewlett Packard Labs Chief Architect, HPE Fellow/VP, IRDS SA Co-Chair

Introduction

Prominent both in the name and the organizational structure of the International Roadmap for Devices and Systems is what differentiates the IRDS from prior and peer road mapping efforts: a focus on whole-of-application co-design and systems engineering. It was shaped by drawing from both the International Technology Roadmap for Semiconductors and the IEEE Rebooting Computing communities. The compartmentalized and segmented technology development stacks of the past encouraged individual advancement and achieved very strong economic and social benefits. However as we increasingly hit harder physical limitations of conventional design and methodology, segmentation is a relative luxury that we can no longer afford. The demand for computation at greater scale, novelty and complexity is accelerating as society struggles to tackle the ever more challenging problems of gaining insight in a time that matters and with energy consumption that enables us to sustainably provide the benefits it offers equitably to all. Achieving these goals while facing the headwinds of increasing technical challenges as we transition from the second era of Moore's Law Scaling (Equivalent Scaling) to the third (3D Power Scaling) across memory, computational and communications devices demands a co-design methodology.

As seen in Fig. 1, since the inception of the IRDS Roadmap in 2017 this whole-of-stack co-design methodology has been reflected in the organization of the International Focus Teams (IFTs), and in fact this structure continues to evolve as approaches at each level in the stack diversify. Of particular note are the two IFTs shown at the top of the diagram, Application Benchmarking (AB) and the topic of this article, Systems and Architectures (SA). To the challenge of co-design AB brings the critical understanding of "what do we currently and what will we need in the future to be able to compute?". With AB answering "What?", then SA strives to bring the understanding of "Where?". SA strives to catalog the boundary conditions of size, weight, power, privacy, security, and

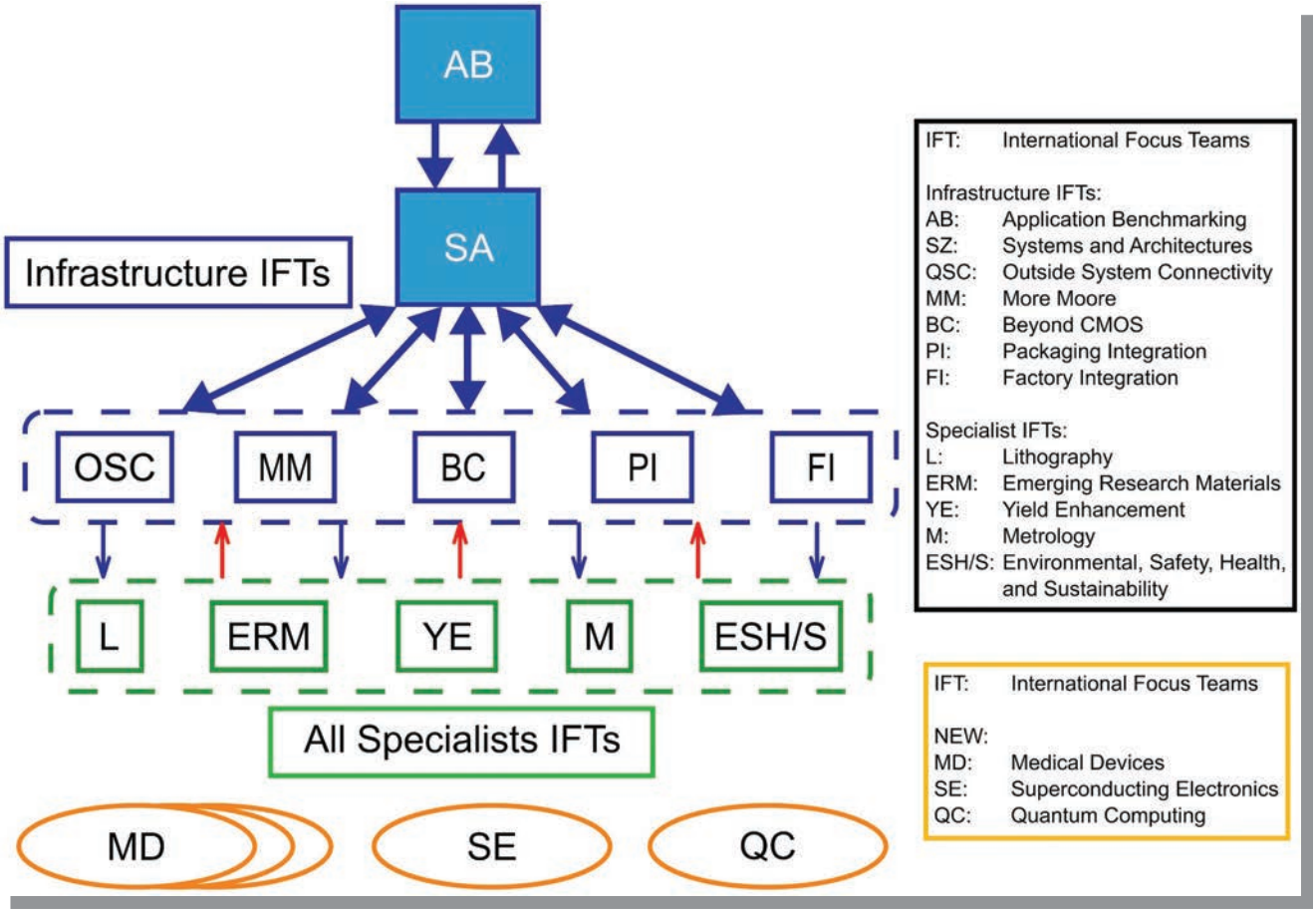


Figure 1. IFT Structure from the 2017 IRDS Executive Summary Chapter

sustainability where computing will need to take place. Complex computing is rapidly moving beyond the relatively benign environment of the data center out to occupy design envelopes from embedded and implanted systems at the edge and up to the facility scale engineered systems of the hyperscale cloud provider and the exascale Supercomputer.

Chapter Methodology Evolution

To facilitate bringing this understanding to the IRDS community, the inaugural SA roadmap chapter adopted a methodology based on a taxonomy of systems to identify both common technical and market drivers that cut across all system categories and those which are unique and create opportunities for co-design and collaboration with other IFTs. While this certainly excludes economically interesting segments, the initial four categories of Internet-of-Things/Edge (IoTe), Cyber-Physical Systems (CPS), Mobile Devices (now expanded to Physical Augmentation Devices) and Cloud Systems were viewed as having both market defining scale as well as technology defining demands that admit the whole-of-stack co-design. This is re-evaluated annually with every roadmap update and in fact during the most recent update the original Mobile Devices category has been expanded to Personal Augmentation devices because the original definition was deemed both too narrow a category within the overall market and because other personal system devices beyond the mobile handset were driving new engineering constraints.

By bringing the analysis of these categories, we would be best informing the other IFTs. Within each category we have tracked market drivers, key technical challenges and opportunities, and, as we are an integral part of the road mapping process, a matrix of key technical figures of merit cross-checked against the deeper and more expansive metrics tracked in the other roadmap chapters. In this way, the SA Chapter has a role as an entry way for systems level engineering communities into the deeper insights available across the IRDS.

A market driver of particular note that has truly become ubiquitous over the lifetime of the SA effort has been the pervasive adoption of AI driven solutions. These solutions are of particular interest to the SA analysis because they add significantly to the constraints which must be simultaneously satisfied across a complex system-of-systems infrastructure. To the existing demands that require a confluence of energy and infrastructure supply chains is added the demands of the data supply chain, data flowing in for the creation and continuous improvement of models, data flowing out in the form of those models, massive data flowing in for immediate edge inference and deep cloud storage and analysis and finally data flowing out in the form of actions as scale. This was first examined in a separate 2018 IRDS White Paper, "Preparing for Data-Driven Systems and Architectures – Edge, Cloud, and Core" and then became the basis for the first comprehensive revision to the chapter in 2019.

As a part of that revision, the SA chapter first incorporated and has continued to refine a cross reference between the four systems categories and the now eleven Size, Weight and Power (SWaP) design centers. This is an expansion of the component level Power and Cooling tracking in the inaugural SA chapter edition and also annotates additional integrated technologies important for a particular design center. This highlights both the constraints which are common across each of the four system categories as well as the increasing diversity of constraints that each category has encompassed as they have all been marshalled for use in data driven AI solutions. It is important to note that while the chapter has always analyzed the component and now the design envelope power considerations, the overall system-of-system energy efficiency gained or lost by specific application of each of the design envelopes for a particular use is beyond the scope of the chapter, but has been a point of broader collaboration, such as the joint work with the IEEE International Network Generations Roadmap (INGR) Energy Efficiency chapter and the US DoE Energy Efficient Computing R&D Roadmap Outline for Automated Vehicles.

Taxonomy of Systems

The four categories of systems tracked in the most recent 2022 roadmap edition are:

1) Internet-of-things edge (IoTe) devices provide sensing/actuation, computation, security, storage, and wireless communication. They are connected to physical systems and operate in wireless networks to gather, analyze, and react to events in the physical world. These are ubiquitous-scale objects that pervade the environment.
2) Cyber-physical systems (CPS) provide real-time control for physical plants. Vehicles and industrial systems are examples of CPS. These can be considered 'human analog'-scale objects that fill niches previously covered by people.
3) Personal Augmentation devices such as smartphones, wearables and AR devices provide communication, interactive computation, storage, and security. For many people, smartphones provide their primary or only computing system. These are typically human-scale objects intended to augment the capabilities of an individual. In prior revisions of this chapter, we tracked this category as Mobile Devices, but this is no longer sufficient to capture the increasing diversity in this category.
4) Cloud systems power data centers to perform transactions, provide multimedia, and analyze data. Cloud systems represent a trend towards a synthesis of design principles and methodologies taken

from traditional enterprise, high performance scientific, and web native compute. Increasingly these systems are utilizing artificial intelligence to continue to improve operational efficiency, becoming CPS in their own right. These are macro-scale, distributed systems.

While the shift from the Mobile Systems to Personal Augmentation systems is the largest change to this taxonomy over the first five years of SA road map tracking, all of the categories have undergone refinement and it is instructive to follow the evolution of each over that time period as individual categories but also as there are increasingly combined. Dynamic topologies consisting of edge-to-cloud, large scale, and intelligent social infrastructure systems with complex interlocked information life cycles are becoming increasingly common. Each category is continuing to demand ever greater capacity in diminishing size, weight and power (SWaP) envelopes,

DESIGN ENVELOPE	SYSTEM CATEGORY				INTEGRATED TECHNOLOGIES
Beacon & Sensor Nodes	IoTe	Personal Augmentation Devices	CPS		Trusted data sources 2.5D/3D integration of sensors, memory, accelerators, computation, and comms Energy Harvesting with inducted power boost modes SRoT/Blockchain trust mechanisms
Access Point					Unified 5G/Wi-Fi access point for IoT sensor network Identity, Activity, Locality triangulation ML/AI augmented operation
Aggregation Point					Robust environmentals Edge local secure hosting of containerized workloads Static composition Smallest IT/OT (Information technology / Operational Technology) Blended Platform
Edge Hardened					Robust environmentals Legacy PXI/AXIe plus next gen modular FF Static composition Robust IT/OT Blended Platform target at several capacity points
Personal Sensor Network					Sensor Fusion Platforms for ADAS, SCM, SNS, etc. Gaming applications with milisecond or microsecond latencies Computation for security satisfying frameworks like GDPR
User Equipment					5G/6G Smartphones Wearables with ultra-low power consumption Graphics/AR/VR devices as human analog-scale objects
Single System Flex					OPC/Rack/Tower systems with next gen modular FF option bays and electrical/optical memory fabric (Gen-Z/CXL) expansion Static fabric configurations between reboots Low cost point-to-point expansion
Enclosure Composable				Cloud Systems	Blade Enclosure augmented with next gen modular FF and memory fabric at the enclosure and rack level Enclosure level switching of fabrics Static/Dynamic fabric configurations
Rack Scale					Dense next gen modular FF enclosures with integrated switching Large Scale memory fabric enclosure as endpoint Dynamic fabric configuration Dematertialized and legacy free Design for Flex Capacity, Co-Lo, aaS Consumption models Containers on memory fabrics
Aisle/Pod Modular					Dense next gen modular FF enclosures with integrated switching ToR switch Dynamic fabric configuration Dematertialized and legacy free Design for Flex Capacity, Co-Lo, aaS Consumption models Petascale HPC and Petascale Enterprise in-memory DB/Analytics
Exascale HPC					DC scale memory-semantic fabric over photonics All liquid/conduction cooling environmentals Aisle/Pod modular for I/O nodes 2.5D/3D integrated CPU/GPU/Memory modules

Figure 2. SWaP Design Centers across infrastructure system categories

giving economic motivation to gaining as much as we can from conventional approaches as well as even greater potential for novel approaches.

System Category – IoTe

This roadmap provides separate analysis of IoT Edge (IoTe) devices and Cyber-Physical systems (CPS). In originally selecting both categories a primary distinction was made as to the real-time nature of CPS systems which often necessitates full data lifecycles from sensing to action below 1 second and often in the millisecond or microsecond regimes. In both power and communications, IoTe devices are more likely to be wirelessly or even intermittently connected to network resources and they can be the most exposed to harsh environmental conditions and physical security challenges. At the same time, the vast amounts of data that they are capable of sensing and the energy, security, privacy and sustainability challenges of speculatively transmitting all that data to the cloud areincreasingly demanding that in-sensor AI inference and even training applications be housed in IoTe endpoints.

IoTe design is driven by the total cost of ownership over the entire lifecycle of the system, from initial deployment through ongoing maintenance (battery replacement for example) and finally through decommissioning and eventual reclamation. In some cases the lifetime operational expense can greatly exceed the capital expense of the system and for both energy and communications, this places a premium on stand-alone capabilities such as energy harvesting and wireless communications with zero-touch provisioning. Hybrid battery plus harvesting (B+H) as well as multimodal harvesting (H1+H2) will both continue to be factored in to support increasingly complex AI operations in IoTe devices. Processing power for IoTe devices exists at the lowest operational tiers, from 10mW down to 1mW active power dissipation. Even at these tiers, ultra-fast power-up/power-down at the end-point level and charge rationing at the function level will continue to play a part in IoTe endpoint design.

The devices themselves are often exposed to the most challenging environmental, security and safety conditions including those far too dangerous or remote for human presence or maintenance. While this has always been a design consideration, what is new for the IoTe end-point and the devices, and firmware that are used to construct it, is that they now may be called upon to be the root of an attestation chain linked to silicon features such as Physically Uncloneable Functions (PUFs), that offers proof in a zero-trust model that neither they nor the data that they provide has been fabricated, adulterated or injected as false signal. They will also need to maintain cryptographic protection of data at rest and in motion further taxing the end point energy budget.

System Category – CPS

Cyber-physical systems are networked control systems. These distributed computing systems perform real-time computations to sense, control, and actuate a physical system. Many cyber-physical systems are safety-critical, and thus the target of adversarial attacks not only against the installed systems and the personnel which use and maintain them, but increasingly sophisticated attacks back through the entire supply chain. They interface to the systems they control via both standard and proprietary interconnects broadly known as operational technology (OT), where ruggedness, extended environmental capabilities, low-cost have historically been paramount over considerations such as security and attestation. As these systems are increasingly connected edge-to-cloud, this will present an increasing attack surface, either for data theft, false signal injection, systems commandeering, or as a back door into the IT domain.

CPS systems vary greatly in scope and scale, from an individual drone or autonomous vehicle to intelligent factory scales systems and thus will utilize the full range of processor power tiers. The cyber-physical system is increasingly being paired with a digital twin, the intersection of simulation/modeling plus massive data analytics and advanced AI/ML. Today this is being done after the creation of the CPS, but in next generation design methodologies of dynamic, AI/ML optimized, CI/CD delivered engineered systems, design and analysis in the digital domain will seamlessly transition to the test and control of the physical system.

System Category – Personal Augmentation

Personal augmentation devices integrate computation, communication, storage, capture and display, and sensing. These systems are highly constrained in both form factor and energy consumption. As a result, their internal architectures tend to be heterogeneous. Cores in modern personal augmentation units include: multi-size multi-core CPUs, GPUs, video encode and decode, speech processing, position and navigation, sensor processing, display processing, computer vision, deep learning, storage, security, and power and thermal management. In the SA methodology, this category evolved from the Mobile Device system category, which while it was always cognizant that the mobile device handset of 2017 might represent the entire IT personal investment and footprint for an individual, was still too narrow to encompass the increasingly diverse applications of personal augmentation endpoints, either in economic value or engineering criteria.

Personal augmentation devices provide multiple use cases: telephony and video telephony; multimedia viewing; photography and videography; email and electronic communication; positioning and mapping, authenticated

financial transactions, health and fitness monitoring, personal safety and environmental warning. Current and upcoming market drivers include: gaming and video applications; productivity applications; social networking; augmented reality and context-aware applications, and mobile commerce. Personal augmentation devices already make use of AI technologies such as personal assistants. Deployment of AI on and through personal augmentation devices will accelerate.

This represents a transformation of the personal augmentation system from consumption endpoint serviced by Content delivery networks (CDNs) pre-positioning relevant content globally to content generation and integration endpoints in mesh topologies much more complex and dynamic than today's CDNs. Future ad hoc mobile mesh communities focused on live events, AR/VR multiparty gaming, or cooperative AR work environments will connect personal device to personal device and link to low-latency, distributed-edge compute infrastructure as well as multi-cloud global infrastructure.

The processors used in personal augmentation systems range from the 100mW to 10W tiers, but have the distinct challenge that they are excluded from thermal management tools such as heat sinks or fans and must also often have the added demand that they be comfortable when worn over extended periods of time. As personal augmentation systems, the charge/discharge cycle is ideally matched to the user's active period or failing that, enabling fast re-charge to minimize productivity disruptions. Here the increased demand runs into the challenges that battery chemistry evolves slowly and that the safety concerns of increasing energy density and capacity may in fact provide a regulatory limit lower than the design capabilities. These drivers have placed personal systems at the forefront of heterogeneous integration at the monolithic System-on-Chip (SoC) and the multi-chip integration level as well as frequently consuming the most advanced process steps available. This heterogeneous trend is now being reflected in the Cloud system category and it will be interesting to see for the innovations tracked in the More Moore (MM) and Beyond CMOS (BC) roadmap chapters which of the extreme environments is the more aggressive adopter of novel computational approaches.

System Category – Cloud

The term cloud refers to the engineering of data center scale computing operations—compute, storage, networking engineered for scale and for continuous resource redeployment and reconfiguration via APIs. Whether they are operated publicly or privately, they offer an on-demand, as-a-service consumption model. While they had their origins in web services; media streaming, shopping and commerce; they are increasingly broadening their applications base to big data for social networking, recommendations, and other purposes; precision medicine; training of AI systems, and high-performance scientific computation for science and industry.

As noted above in the discussion of Personal Augmentation, at the inception of the IRDS Roadmap a key characteristic of Cloud in both web-scale and HPC scientific compute was homogeneity, node after node, aisle after aisle of identical equipment. Starting with the dot com era, this was repurposing of existing COTS data center or even workstation compute, storage and networking technology, but over the ensuing decades these have become precision cloud native systems engineered at the data center scale featuring bespoke processor designs, networking interface and switch ASICs, and workload specific accelerators via FPGAs or ASICs. What began as the utilization of the as-a-service consumption model to foster independence of the user from a particular piece of hardware infrastructure by enticing them with agility and an operational expense model, is now progressing fostering independence from particular architectural approaches. The progression from physical systems to virtual machines, then from VMs to containers, then from containers to "serverless" functions is economically incentive by both providers and consumers, but so is the heterogeneous compute model demonstrated in the More Moore (MM) and Beyond CMOS (BC) roadmap chapters. An active area of research is to resolve these tensions and permit fine-grained as-a-service consumption of accelerated heterogeneous compute.

While the initial SA roadmap chapter tracked a homogeneous CPU dominated architecture that did not recognize GPUs, the 2022 update initiated tracking three categories of cloud native processors:

Latency sensitive processors: these processors are optimized for lowering any aspect of latency, usually prioritizing single thread performance. They have rich out-of-order execution resources with advanced branch prediction and cache prefetching mechanisms, a deeper cache hierarchy with relatively larger last level cache, and large main memory with standard DDR technologies to accommodate a large dataset. Intel Xeon, AMD EPYC, and Amazon Graviton are representative examples of these processors.

Throughput oriented processors: these processors are specially optimized for compute and data movement bandwidth, prioritizing parallel processing efficiency. They emphasize data level, thread level, and core level parallelism of the workload to achieve higher performance. In order to integrate more compute units, out-of-order execution resources and memory hierarchy are simplified. Integrated memory modules with high bandwidth memory (HBM) or GDDR are usually used to increase memory to processor bandwidth. Examples of these processors are GPUs such as NVIDIA A100, A64FX used in Supercomputer Fugaku, and vector processors such as SX-Aurora Tsubasa.

Compute centric processors: these processors are specially designed for achieving very high compute throughput with less emphasis on main memory bandwidth. They usually have a large SRAM on-chip memory assuming the dataset of the current workload fits in the on-chip memory. They can achieve very high compute density utilizing high bandwidth data supply from on-chip SRAM to functional units. Deep learning and inference applications are the main target of this type of processors. Representative examples of these processors include Cerebras WSE CS-2, Tesla D1, Esperanto ET, Graphcore Colossus MK2 GC200 IPU, Groq TSP, SambaNova SN10.

Longer Term Considerations

With each annual update to the roadmap, we strive to identify long term, sustained forces that drive system and system-of-system changes and in our most recent update we examined three societal and application pull forces.

The first is the continuation and in fact acceleration towards the evolution of edge to cloud platforms hosting pervasive data analytics. All of the system categories tracked in the SA chapter are interdependent. Personal augmentation devices, IoT edge devices, and cyber-physical systems all provide data that is analyzed by cloud systems. Many complex systems exhibit characteristics of both IoT and CPS. Certain aspects of data centers and cloud systems—power management and thermal management, for example—make use of cyber-physical and IoT techniques.

Second is the need to focus on ensuring supply chain anti-fragility. Manipulation of the global supply chain has become a valid target for both political and financial gain in the early 21st Century. On top of this, we anticipate increasing volatility as a result of climate change, geo-political unrest and the disruption of the move to AI upon modern society. Success under these conditions requires not just a robust and resilient supply chain position, but one that should be strengthened by volatility rather than merely resistant to it. This is certainly not exclusively a technology challenge, it hinges on policy and public and private investment, it is one where the technology community needs to lead in outreach to educate and partner with leadership teams at the local, national, and global scale and tools like the IRDS can be a critical advantage in that effort.

The final theme is the transition from decision support systems to decision-making systems. Decision support systems have evolved from the systems of record which engendered the relational data base systems to support transactional business records, systems whose power and scale demand was linearly proportional to population. Later these were layered with systems of engagement which brought in mobile and cloud native hyperscale engineering, and while power and scale demand was now proportional to the Cartesian product of relationship graphs, the human-centric design models which support human decisions also perpetuates human limitations. With the rise of decision making systems, where pervasive AI replaces humans in decision processes, where every byte everywhere is admitted to analysis to gain real time insight and that insight leads to action at scale, we imagine a hyper-competitive enterprise run with a super-human level of operational excellence and sustainability. Intelligent mobility; a sustainable, zero-emission, fully distributed energy mesh; a 5G/6G communications infrastructure, each are examples of social infrastructure where energy, bandwidth, latency could be transparently optimized for sustainability, equity, and societal benefit. There's a pattern: massive public/private infrastructure investments, occupying space in the real world that reaches to every single one of us, the shift to real-time data driven control, all in highly regulated sectors, which makes trust and transparency just as important as efficiency and opportunity.

Open Invitation

The Systems and Architecture chapter of the International Roadmap works to bridge the deep understanding of the Applications Benchmarking of what we need to compute with the continuous advancement of the Infrastructure and Specialist IFTs by cataloging the demands and constraints of IotE, CPS, Personal Augmentation and Cloud systems categories and every design envelope from a Bluetooth low energy beacon to an Exascale supercomputer. As the chapter title implies, this is a Systems Engineering pursuit and as such it benefits greatly when we apply the specific boundary conditions of privacy, security, sustainability of particular challenges rather than work speculatively. So if you are a systems engineer with insights or contribute, or if you are looking to understand the connections and implications device technology and the deep insights available across every IRDS chapter as view through a systems engineering lens, then we'd invite you to join the IRDS SA discussions directly or to propose a cross-community collaboration.

Report by the organizing committee: Arokia Nathan, Ling Li, Yong Lian, Samar Saha, Xiaojun Guo, Andrew Flewitt, Woo Soo Kim, Kai Wang, Gangqiang Yang, Susthitha Menon, Mengwei Si, Camilo Velez Cuervo, and Jun Yu

The IEEE Electron Devices Society successfully hosted the 2022 IEEE International Flexible Electronics Technology Conference (IFETC) in the wonderful city of Qingdao, China, 21–24 August 2022. This premier conference, fully financially sponsored by IEEE Electron Devices Society, was dedicated to flexible electronics technologies for sensors, displays, and in general large area flexible electronics systems. It was run in hybrid mode to attract virtual global participation due to COVID restrictions. IFETC 2022 was 4th in the series with previous conferences in Ottawa (2018), Vancouver (2019), Shanghai (2020 but canceled due to COVID), and Columbus Ohio (2021 Hybrid).

IFETC offered a rich three-day hybrid program of oral and poster presentations organized into several parallel sessions comprising: • 7 plenaries given by prominent multi-disciplinary experts (5 industry, 2 academia) • 14 regular sessions on materials processing and device integration; sensors, actuators, and bioelectronics; energy harvesting and storage; circuits and systems integration; displays; and emerging applications • 4 focus sessions covering topics in brain-computer interfaces; wearable electronics, electronic skin for smart robotics, flexible neuromorphic devices and systems • 4 industry focus sessions in heterogeneous and hybrid integration; device-circuit interaction and compensation; from lab to fab; flexible electronics; and scalable manufacturing • 58 poster presentations • 6 pre-conference tutorials on 3D printing, sensors, flexible displays, and wearable systems. In addition, the conference hosted special sessions for EDS Young Professionals and Women in EDS (WiEDS) Networking.

Appreciation and Award Certificates were given to Women in

IFETC 2022 WiEDS Appreciation Certificates

P Susthitha Menon, Chair, IEEE Women in Electron Devices Society

Dr Siyi Hu, Miss Chenxuan Hu, Miss Xiaohua Bai

IFETC 2022 Young Professionals Appreciation Certificates

Chair, Professor Chen Jiang, Tsinghua University, China

Active-Matrix Digital Microfluidics Chip for Efficient Droplets Manipulation	Patterning ITO using a Laser Cut Kapton® Tape Mask for Flexible PVDF Applications	Low-Voltage High-Performance Intrinsically Stretchable Optoelectronic Transistors	Strategy toward High-Mobility Oxide Semiconductor Thin-Film Transistors by Atomic Layer Deposition	A Flexible Tactile Sensor Interfaced with a TFT Analog Front-End for Material Texture Recognition
Dongping Wang, Qi Huang, Longqian Xu, Siyi Hu, Hanbin Ma, Suzhou Institute of Biomedical Engineering and Technology, CAS, China	Kyle M Schvaneveldt, Annie Laughlin, Elias Guanuna, Keaton Shurilla, Luke Johnson, Jessica Staker, Quinn Hunsaker, Daniel Smalley, Brigham Young University, USA	Kai Liu, Yunlong Guo, Yunqi Liu, Institute of Chemistry, CAS, China	Mengwei Si, Shanghai Jiao Tong University, China	Jianle Lin, Huimin Li, Anqi Li, Bowei Jiang, Xinghui Liu, Kai Wang, Sun Yat-Sen University, China

IFETC 2022 Best Paper Awards

Low power organic phototransistor for image enhancement under weak illumination	Ionic defect analysis in flexible hybrid perovskite memristor using deep level transient spectroscopy	Flexible, planar, and stable electrolyte-gated carbon nanotube field-effect transistor-based sensor for ammonium detection in sweat
Peijin Huang, Xiaokuan Yin, and Xiaojun Guo	Himangshu Jyoti Gogoi, Abdul Andrabi, Raja Muddam and Arun Mallajosyula	Mattia Petrelli, Bajramshahe Shkodra, Martina Aurora Costa Angeli, Alessandra Scarton, Silvia Pogliaghi, Roberto Biasi, Paolo Lugli, Luisa Petti
School of Electronic Information and Electrical Engineering, Shanghai Jiao Tong University, Shanghai, China	Dept. of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati, Assam,` India	Faculty of Science and Technology, Free University of Bozen-Bolzano, 39100, Bozen, Italy Microgate Srl, Bolzano, Italy 3Department of Neuroscience, University of Verona, Italy

Electron Devices, Young Professionals, and Best Papers in the conference.

With respect to the Conference Proceedings and Special Issue, the two-page abstracts submitted to the 2022 IFETC Conference will be hosted in IEEE Xplore. Extended version of the abstract will be invited for submission of a full-scale journal paper to IEEE's new journal on Flexible Electronics, *J-FLEX*. Submissions subject to IEEE's standard review process.

Overall IFETC 2022 was very well attended with participants from multiple time zones with a total of 177 papers from 12 countries summarized below. IEEE is very proud of the success of IFETC 2022, despite being hybrid. Also showing are photos of selected highlights of the conference.

Participation Metrics

Plenary Talks	7
Tutorial Talks	6
Technical Sessions	21
Invited& Contributed Talks	106
Posters	60

China	118
USA	14
UK	10
India	7
Germany	7
Canada	7
Italy	4
South Korea	3
Malaysia	2
Singapore	2
Spain	1
Japan	1
France	1
Egypt	1
Finland	1
Total	**177**

General Chair, Arokia Nathan and Technical Program Chair, Xiaojun Guo giving their opening remarks

Kai Wang and Arokia Nathan chairing the pre-conference tutorials

Conference exhibit area for industrial sponsors and posters

The organizing committee is highly appreciative of the major support of the • local team in Qingdao and support teams from CAS and ACXEL at Suzhou and Foshan, respectively • sponsors and local municipal Govt of Qingdao • Shandong University and School of Information Sciences. Very importantly, we thank the speakers and participants for making IFETC 2022 such a great success! We thank the financial sponsors for their generous support (list of sponsors shown below) and we look forward to seeing you, whether in real or virtual form, in San Jose, 14–15 August 2023.

Upcoming Technical Meetings

IRPS 2023 News and Updates

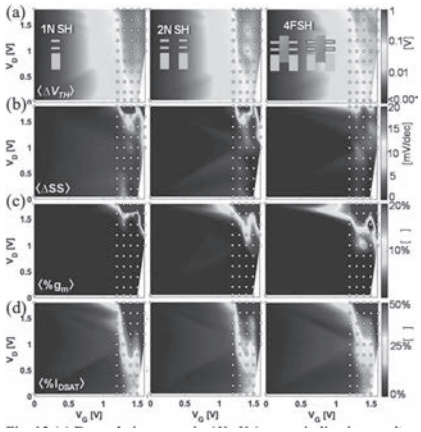
The IRPS 2022 Best Paper Awards have been announced. Congratulations to all award winners! The winning papers will be presented during IRPS 2023 which was advertised in the Newsletter issue October 2022.

Best Paper

Evaluating Forksheet FET reliability concerns by experimental comparison with co-integrated Nanosheets

E. Bury, A. Chasin, B. Kaczer, M. Vandemaele, S. Tyaginov, J. Franco, R. Ritzenthaler, H. Mertens, P. Weckx, N. Horiguchi, D. Linten

Imec, Leuven, Belgium and A.F. Ioffe Physical-Technical Institute, Russian Academy of Sciences, Saint-Petersburg, Russia

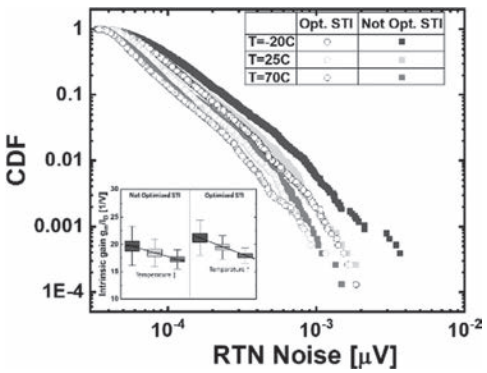


Best Posters

Impact of Electrical Defects located at Transistor Periphery on Analog and RTN Device Performance

L. Pirro, P. Liebscher, C. Brantz, M. Kessler, H. Herzog, O. Zimmerhackl, R. Jain, E. Ebrand, K. Gebauer, M. Otto, A. Zaka, J. Hoentschel

Global Foundries Fab 1 LLC & Co.KG, Dresden, Saxony, Germany

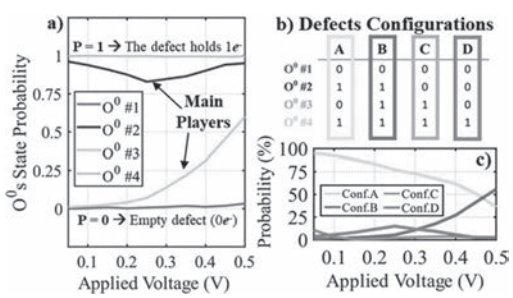


Best Student Paper & People's Choice

The Relevance of Trapped Charge for Leakage and Random Telegraph Noise Phenomena

S. Vecchi, P. Pavan, F. M. Puglisi

Dipartimento di Ingegneria "Enzo Ferrari", Università degli Studi di Modena e Reggio Emilia, Modena (MO), Italy



Board of Governors Meeting—December 2022

MK Radhakrishnan
IEEE EDS Secretary

EDS Board of Governors meeting in December 2022 was organized at Hilton San Francisco Union Square Hotel on December 4, 2022. EDS President, Ravi Todi welcomed the attendees for this year-end face to face meeting after a long break due to pandemic. Ravi presented the major highlights including the overall summary of the activities in 2022 and the successful culmination of the year with the technical activities. All the motions were presented and the voting will take place via email after the meeting.

Bin Zhao, President-Elect presented the ExCom meetings summary. The term limit changes to elected members and appointees to EDS management team and Technical and Standing Committees were presented. The term limits for BoG members and Vice Presidents to remain as two terms in a lifetime and others may be varied. This is in view of having more active volunteers from both YP, and an experienced team in the EDS management.

EDS Treasurer, Roger Booth presented the financial status reporting a very healthy finance in 2022. The expense reduction in the previous year due to pandemic helped to attain this state whereas the revenue from conferences have also reduced, but not at the same level. 50% of the operating margin can be utilized for new initiatives. The budget for 2023 has been presented with an expectation of a healthy operating margin.

EDS Secretary, MK Radhakrishnan presented the Secretary's report and Newsletter report. Minutes of the mid-year BoG meeting were submitted for approval. Newsletter charter needs an update to include the procedure for EiC appointment which was presented. Also, the new Charter for EDS Communication Committee needs approval and the motion was presented.

Kazunari Izhimaru, VP of Meetings informed that some of the conferences were in person mode this year whereas others were in hybrid format. Among the EDS financially sponsored conferences, IEDM is now held as a full event with a good participation. A motion to approve the technically co-sponsored conferences for next year was made

Navakanta Bhat, VP of Education informed the successful organization of webinars every two weeks in the whole year. The podcasts featuring interviews with illustrious members of our community have been very successful attracting many. Summer schools organized at different Regions, especially Region 9 and 10 have benefited a large number of students. Under the upskilling courses for industry, two courses have been approved for 2022. EDS Education Achievement Certificate program is now getting ready to benefit members who attend various educational programs.

Arokia Nathan, VP Publications & Products informed that all EDS journals (TED, EDL and JEDS) have an overall improvement in the Impact Factor. The acceptance rate for all three journals remains more or less the same as in the previous year. The new EDS Magazine has been approved by IEEE publications and the first issue is slated to be published by July 2023. Two motions, one for the approval of financial co-sponsorship of JxCDC and other to approve changes in the Publications Charter have been submitted.

Murty Polavarapu, VP Regions and Chapters, reported that EDS Chapters, especially student chapters, are growing in Regions 9 and 10. Most of the Chapters have organized meetings in 2022 and are being reported through L31. Regional Chapters meetings are being organized and the latest one in Kolkata for EDS South Asia Chapters was very successful. The DL programs are getting more in person style, whereas virtual DLs are also continuing. As part of EDS celebrations of 75 Years of Transistor, various Chapters are organizing special events.

Membership development report from VP for Membership was presented by Ravi Todi. Currently EDS has more than 10,000 members worldwide with growth mostly in Regions 10 and 9. Undergraduate student member strength is mostly concentrated in Region10, whereas the graduate student memberships are mostly from Regions 1-6, Region 8 and 10.

John Dallessase, VP for Technical Committees reported that there are 15 TCs with about 170 TC members and one more TC on Quantum Technologies is being initiated. Most of the Committees are healthy. TC members provide healthy support for Webinars and special issues. A nomination pattern is planned for enhancing the TC members/Chair recruitment.

Doug Verret, VP Strategic Directions, presented the EDS strategy outline to oversee future directions. Strategic goals identified during the workshop and the KPIs were discussed. A marketing campaign to communicate EDS strategy in plan during 2023 is planned.

YP Committee Chair, Mario Aleman, presented a Young Professionals committee report. A number of activities

were reported. EDS visibility in Social Media platforms is very good, especially on LinkedIn.

The Women in Electron Devices (WiEDS) report was presented by its Chair Susthitha Menon through video. A number of activities were reported for this new Committee. Also, EDS 75th year of Transistor celebrations committee activities were presented by Manoj Saxena through a video report.

Ravi Todi, EDS President, reporting to the EDS Board of Governors

Giovanni Ghione, Editor-in-Chief of TED presented the status of the journal, showing progress in paper submission and acceptance. Jesus del Alamo, Editor-in-Chief of EDL presented EDL status which shows the Impact factor of EDL has been much improved. JEDS Editor-in-Chief report was presented by the VP of publications.

Barbara de Salvo, 2022 IEDM General Chair presented the latest status of the IEDM 2022. The Tutorials and Short courses had good participation. The conference registration is peaking up and is almost the same as the pre-pandemic period.

Fernando Guarin presented the names of newly elected Fellows from EDS. The success rate is comparable to that of previous years. Cary Yang gave a summary of EDS Nominations and Elections. Cor Clayes presented the Humanitarian activities report. EDS office and Staff report was presented by Patrick McCarren.

Ravi Todi thanked all attendees of the meeting for their participation and support throughout the year, as well as EDS Staff for their dedicated effort to make the Society one of the vibrant IEEE Societies. The meeting was adjourned at 5.00 pm.

MK Radhakrishnan
IEEE EDS Secretary

The Future to Which we Aspire

Doug Verret
EDS Vice President of Strategic Directions

Mission

To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition while enhancing public visibility in the field of Electron Devices.

Vision

Promoting excellence in the field of electron devices for the benefit of humanity.

Imagine that you are a time traveler and that you have visited the earth in 2032. What did you see? I am pretty sure that you saw a voracious demand for technology, a huge matrix of people connected to their favorite devices, to other people and to all the things in their environment near and far. You also very likely observed a stupendous and ever-increasing demand for energy and for cyber security. My crystal ball for predicting exactly which technologies will dominate is not any better than anyone else's, but what I can say with some confidence is that what you saw in your magical carpet ride was transistors, capacitors and resistors at the foundations of all of it. That is because electron devices comprise a foundational technology and will remain so for the foreseeable future.

As enduring as electron device technology will be, there is no guarantee that the Electron Devices Society will endure. That will depend upon how well we serve our members, the electron devices community and mankind.

This question was on the minds of a group of EDS thought leaders this summer as they convened in a workshop format to contemplate the future of the Society. Where are we now? Where are we going? How will we get there? They took the transtemporal journey to 2032 and looked at the Society. What did they see? They saw *a welcoming, inclusive, diverse, and vibrant society with healthy and eager participation and engagement across geographic, cultural, and technical areas by students, academicians, and industry professionals for robust mutual benefit. Members and leadership saw themselves*

reflected in the organization and its activities equally. And they saw diverse perspectives amplified.

This was a vision of what the delegates saw and agreed that it is the dynamic to which we aspire. They noted in that vision that it is the community aspect that draws members together and attracts new members because it is modern, engaging and exciting. At the same time, it offers members the technical content that is up to date and available through multiple channels and on demand. It is everything members need to succeed at their fingertips and whenever they want it.

The vision that the delegates saw was translated into a narrative which they want to share with Society members in anticipation of an on-going dialog to promote the idea that the odyssey to this vision is never complete but continually changing and adapting as technology evolves and needs change. This is how the delegates documented the vision narrative.

They saw…

EDS committing to and investing in the next generation, providing training, seeking and incorporating their perspectives and priorities, and serving as a conduit for professional development, future leadership, and enhancing all career stages.

Local EDS communities providing indispensable professional advancement opportunities, disseminating leading-edge technical knowledge, and promoting networking channels with meaningful and enjoyable engagement activities that attract new and ongoing members alike.

EDS leadership, committees, and local communities in reciprocal dialog and working collaboratively on member wants, needs, programs, and creative ideas for implementation.

EDS sponsoring rapid technical information exchange, leading conferences, and field focused publications with the best bibliometrics and fastest turn time and top conferences providing rich opportunities for networking, education and learning, and generating high-quality archived conference content.

Led by its education and technical committees, EDS is the first to provide global content on leading-edge technologies in the field of electron devices which is available anywhere and at any time in multiple formats and languages.

EDS amplifying its impact and reach by partnering with IEEE Societies and Councils, NGOs, and industry partners to generate and disseminate technical content beyond what it can do on its own.

Electron Device practitioners enabling technologies to serve and benefit humanity.

EDS is in an ever evolving and thriving state, nimbly and rapidly adapting and innovating through societal and professional changes and shaping the future workforce.

EDS stimulating and organizing local groups to leverage the Society's global technical knowledge to enact and energize positive and sustainable change in underserved communities.

EDS is a sought-after societal partner in IEEE for executing high-quality and sustainable humanitarian projects and leveraging the expertise of IEEE-wide experts to train project teams to see the greatest impact and inclusion in these efforts.

What is the Strategy?

EDS can do anything, but we cannot do everything. Which specific strategies should we pursue that will enable achievement of our vision? The workshop delegates determined that the Strategic Goals already in place were the right ones and elected not to change them.

1) Be the first place that students and technical professionals working in the field of electron devices go to for the information and services that are indispensable for their success.
2) Equitably foster diverse and inclusive communities of practice to facilitate information exchange, collaboration and professional development for greater technological innovation and excellence to benefit all humanity.
3) Establish a process and allocate sufficient resources to support innovative projects that apply electron devices and technology for humanity to address one or more of the United Nations sustainable development goals.
4) Develop synergistic relationships outside EDS to accelerate technological progress in multi-disciplinary areas.

Core Values

The delegates realized that our vision and mission are not complete and cannot be achieved unless the culture of the Society enables and supports our quest. Hence the delegates adopted, in accordance with IEEE Code of Conduct, a set of core values defined by the Executive Committee. Core values are intended to articulate the deeply ingrained principles that guide all the Society's actions. They can never be compromised. They describe how the members behave in pursuit of the Society's goals. It is what members and non-members expect to encounter when they interact with the people in the Society.

We are…

- *trustworthy* ⇛ we are transparent and honest; we keep our word
- *respectful* ⇛ we are civil, courteous and polite in our actions and our discourse
- *inclusive* ⇛ we seek full engagement from all members; we exclude no one; there are no ranks

- *ethical* ⇛ we do nothing to harm individuals or the environment; we follow the law
- *open* ⇛ we listen to new ideas; we are aware of and adapt to change

How will we Get There?

Of concern to the delegates was the question of how we will know if we are making progress toward our vision. A static strategic plan is really a dead plan. To measure progress the delegates developed six Key Performance Indicators (KPIs), each in support of one or more strategic goals. These are intended to be reviewed semi-annually by the Forum and adjusted as necessary once their efficacies have been assessed. All KPIs are required to be measurable, have a complete date and have an owner. To achieve the targets each owner will develop one or more initiatives in support of his/her KPI. The recommended KPIs from the Workshop require approval from the Forum. [As of this writing the Forum had not met.]

Recommended KPIs

2024

- EDS will increase women in membership and leadership across all roles in the society to match their percentage in IEEE. This will be a living goal, with a target of 1% per annum set over the next two years.
- Initate an EDS+X workshop series that targets a topical area defined by an organizing committee which brings in a non-EDS society to focus on an emerging or important multi-disciplinary area and target industrial participation in EDS conferences by at least XX%.
- Each fully financially sponsored publication will have a) achieved or maintained "Q1" status (scimago) and b) increase the number of downloads of all our journals by 5% per year.

2025

- EDS will average at least one new joint project or collaboration between an EDS standing committee and entities outside of EDS per year. Prior to 2025, an external activity coordinating committee will be formed that both recommends and evaluates proposals from the standing committees on outside projects.
- EDS events (website, webinars, DLs, MQs, Summer school, special networking activities at conferences, career mentoring) are prominent in connecting people to industry/academia internships and job openings worldwide, with a cumulative number of more than XX participants in events.

The Workshop on the future of the Society

2027

- EDS will facilitate the creation of a platform that enables educational efforts such as certificate programs that might be offered in conjunction with partners from University or Industry. At least one educational program will be launched using this platform by 2027.

Responsibilities of the Members

The strategic plan is meant to be dynamic and living. The vision and targets are fixed but the paths are many and varied. It is not something done to you, the members or *for* you. It is something we want to do *with* you. For this to become a reality continuous dialog up and down is vitally important. That is your first responsibility….to communicate your feedback, your wants, your needs and your ideas.

For the plan to be nurtured and to grow, the milieu and our culture must be enabling. Thus, your second responsibility is to live the core values. That is what will lead to full engagement and make the plan come to life.

Feedback is Essential!

Enter your comments at: https://ieee-collabratec.ieee.org/app/workspaces/8209/Electron-Devices-Society-Strategic-Plan/activities

You can create an account on Collabratec with or without IEEE membership at no cost to you.

Doug Verret
EDS VP of Strategic Directions

Message from EDS Newsletter Editor-in-Chief

Daniel Tomaszewski
EDS Newsletter
Editor-in-Chief

Dear Readers, Members of the IEEE Electron Devices Society,

Welcome to the IEEE EDS Newsletter issue January 2023. Let me briefly introduce to you only a part of the rich content.

We are very sorry to share with you obituaries of two outstanding researchers and engineers who passed away recently: Hermann Gummel and Nick Holonyak. They were great successors of pioneers of semiconductor electronics. Their ideas and achievements were extremely important for further development of microelectronics and optoelectronics.

The future of the Electron Devices Society is a subject of the article by Doug Verret, EDS VP of Strategic Directions who shares with us a vision of the Society and a short- and long-term strategy to realize this vision that was elaborated during the Strategic Planning Workshop in June 2022. It is an important document. Please, read it, discuss and give your feedback. The Society News section also brings to you a summary of the EDS BoG meeting that was held in the frame of IEDM 2022.

I believe that creating the new EDS-sponsored IEEE Electron Devices Magazine will help realize the strategy described by Doug Verret. On the inside back cover, Joachim Burghartz, the Founding Editor-in-Chief of ED-M, announces and briefly presents the Magazine. We wish the ED-M Editorial Team great success in their mission.

The Section devoted to the 75th Anniversary of Transistor brings very interesting reflections of outstanding experts in the field of micro- and nanoelectronics: Yuan Taur and Sandip Tiwari. That is not all. One more article related to the Anniversary is presented in Regional News. It describes the celebration of the 75th Anniversary of Transistors at ISBAT University, Kampala, Uganda. Continuing a thread of Africa, let me draw the readers' attention to the beautiful article reporting the humanitarian EDS project carried out in Kenya. In my opinion, the main message of both articles is that education is an extremely important, if not the most important task to realize not only in Third World countries, but everywhere. It's a great challenge for different communities worldwide, including the Electron Devices Society, to offer their expertise for such an important goal.

In the Technical Briefs section, please find highlights of IEDM 2022, ESSDERC/ESSCIRC (ESSXXRC) 2022, and IFETC 2022. More ESSXXRC- and IFETC-related events are reported in the YP and WiEDS sections. The next item of the Technical Briefs section, is the article about works of Systems and Architectures International Focus Team, one of IRDS sections. Please, find also a very interesting article on the history of silicon Image sensors. Its author, Yoshiaki Hagiwara was one of the leading researchers and inventors in this field. I would like to draw your attention to a very interesting article in the WiEDS section written by Dr. Hisayo Momose, IEEE Fellow and showing her inspiring professional career.

You have certainly noticed that this Newsletter issue has a new two-column layout. The EDS Board of Governors approved our suggestion to change the layout to have more flexibility and space efficiency in the Newsletter design. Such a format becomes consistent with other IEEE journals.

Dear Readers, if you have any suggestions, comments regarding the Newsletter contents, the new layout, please do not hesitate to contact us. We will be very glad to receive your feedback. Interesting views will be presented with the consent of the authors, along with our replies in the Letters to Editors section. Finally I would like to wish you a prosperous and healthy New Year 2023.

Sincerely,
Daniel Tomaszewski

In Memory of Hermann K. Gummel

The semiconductor industry lost a giant when Hermann Gummel passed away on September 5, 2022 at the age of 99 years. Anyone who has been involved with bipolar junction transistors in the last fifty years will recognize his name immediately from the Gummel-Poon model, Gummel's method, and the Gummel number. But Hermann also made tremendous contributions in the field of Electronic Design Automation (EDA), where he developed original "fast SPICE" circuit simulation techniques as well as numerous EDA tools and methods, The sheer volume of pioneering contributions by Hermann is matched only by the quality of his work.

Dr. Hermann K. Gummel (1923–2022)

Hermann was born on July 6, 1923 in Hannover, Germany to Hans and Charlotte Gummel, the middle brother of an older sister, Bärbel, and younger brother, Achi. Hermann grew up in very turbulent times in Nazi Germany and, after graduating from high school, was enlisted as a radio operator for the German army in World War II. He was wounded by shrapnel and taken prisoner during the Normandy Landing (D Day). Hermann was sent to a hospital in Scotland where the compassionate care of the doctors and staff managed to save his leg from amputation. Hermann was forever grateful for this, but he suffered pain in his leg for the rest of his life.

After the war, Hermann enrolled at Phillips University in Marburg, Germany as a wounded veteran, where he fell in love with and later married Erika Reich. They were married for 64 years before Erika's passing in 2016. Hermann received his Diplom degree in physics from Philipps University in 1952. He then was awarded a Fullbright scholarship to Syracuse University and received his MS (1952) and PhD (1957) degrees in theoretical semiconductor physics. While he was a graduate student, Hermann and Erika were blessed with two daughters, Monica and Margaret.

After graduate school, Hermann joined Bell Laboratories in Murray Hill, NJ. He worked at Bell Labs for thirty years until his "retirement" in 1986, after which he worked as a "consultant" for another ten years. In his forty year career, Hermann made an astonishing number of contributions to the integrated circuit (IC) industry which is ubiquitous in our lives. When Hermann first started at Bell Labs, he began working to understand the physics of bipolar junction transistors (BJTs), which at the time were the workhorse of the semiconductor industry. Hermann realized that the device equations that govern the detailed behavior of BJTs were far too complicated to solve by hand unless gross simplifications were made, so he turned to computer methods. This led Hermann to develop Gummel's method to solve numerically the BJT device equations. Using his programs and techniques, Hermann performed an extensive study of the physics of BJTs. This, in turn, led him to develop the Integral Charge-control Model (ICM), which is the most elegant solution to the BJT device equations ever derived. Hermann and colleague H. C. (Sam) Poon then developed the Gummel–Poon model which made possible accurate simulation of circuits containing BJTs and which was added to the SPICE program at UC Berkeley fifty years ago. Anyone who has worked with bipolar junction transistors in the last fifty years also is familiar with the Gummel plot, used to characterize bipolar transistors, and the Gummel number, which is a fundamental parameter of a bipolar junction transistor.

For most engineers, Hermann's work with bipolar junction transistors would be sufficient for a distinguished career with the accolades that accompany such accomplishments. But Hermann was just getting started! At this point, Hermann was a second-level manager responsible for a department of 30 engineers, but he still made time for engineering breakthroughs. In 1976, Hermann conceived the idea of a timing simulator that would run much faster and accommodate much larger circuits, compared to SPICE, albeit at a sacrifice in the accuracy of the results. This led to the prototype program MOTIS (MOS Timing Simulator) which was the beginning of "fast SPICE" timing simulators—more accurate than logic simulators and much faster than circuit simulators. To quote A. Richard Newton, Dean of the UC Berkeley College of Engineering, "While I think Hermann would agree with me that none of the specific mathematical techniques used in MOTIS was new in and of itself, it was the combination of techniques, data structures, and code that produced a simulation system that had a very broad impact. Once the work was published, it was implemented and extended in virtually every major semiconductor house and at many universities throughout the world."

Hermann was a true visionary and had a clear understanding that the size and complexity of integrated circuits was increasing much faster than a human's ability to cope. Computer-aided design tools were now a necessary part of the IC design process, and Hermann was at the forefront

of EDA tool development. He developed tools for schematic capture (SCHEMA), graphical layout editing (GRED), and parasitic capacitance extraction (HCAP), to name just a few, while managing a department that had now grown to over 100 engineers at two Bell Labs locations.

After Hermann's "retirement" in 1986, he turned his attention to the problems of modeling the MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor), which had been the workhorse of the semiconductor industry for a decade. In 1990, Hermann published a set of numerical tests for MOSFET models to ascertain if the model produced physically reasonable results. Most first-generation and second-generation models did not, which resulted in incorrect results and convergence problems in the simulation of MOSFET circuits. Again, the "Gummel Rules" were an absolutely brilliant contribution to the field of MOSFET modeling.

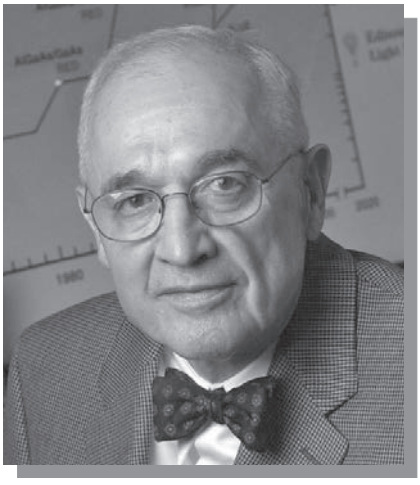
In 1983, Gummel received the David Sarnoff Award "for contributions and leadership in device analysis and development of computer-aided design tools for semiconductor devices and circuits." In 1985, Gummel was elected to the United States National Academy of Engineering for "contributions and leadership in the analysis and computer-aided design of semiconductor devices and circuits." In 1994, he was the first recipient of the Phil Kaufman Award.

Hermann is without a doubt the most brilliant person I have ever known. He also is the hardest working person I have ever known. He was at Bell Labs every day of the week and stayed so late that he knew the cleaning crew by their first names. Some of his colleagues wondered if Hermann ever slept. As a manager, Hermann was honest, fair, and very demanding. But Hermann also was quiet, shy, and totally unassuming and unpretentious. I often wondered to myself how somebody so brilliant and so successful could be so humble. We will miss Hermann, but his achievements are woven into the fabric of our EDA tools and we will never forget Hermann.

Laurence W. Nagel
Omega Enterprises Consulting

Obituary for Nick Holonyak, Jr.

Nick Holonyak, Jr, known as "the Father of the visible Light Emitting Diode (LED) and visible Diode Laser" for his ground-breaking work on the first visible (red) direct bandgap GaAsP alloy semiconductor laser passed away in Urbana, IL on September 18, 2022 at the age of 93.



Prof. Nick Holonyak, Jr. (1928–2022)

Professor Holonyak was born on November 3, 1928 in the southern Illinois coal-mining town of Ziegler, IL. He earned his BS (1950), MS (1951), and PhD (1954) degrees in Electrical Engineering from the University of Illinois. He worked on germanium semiconductor research as the first PhD student of Professor John Bardeen, the two-time Nobel Laureate in Physics for the "Transistor" and the "BCS Theory of Superconductivity." After graduation, Holonyak worked at Bell Laboratories in Murray Hill, NJ, under Dr. John Moll and co-developed the first three-terminal p-n-p-n transistor switch commonly called the semiconductor-controlled rectifier (SCR). SCRs are widely used in applications ranging from wall dimmers and power drills to switching and power inversion in high voltage transmission lines for the power electronics industry.

After military service with the Army Signal Corps in Japan, Holonyak joined the General Electric Company. He developed the first visible "red" light-emitting diodes (LEDs) of GaAs1-xPx alloy semiconductors and identified the "direct-indirect" transition in these alloy compositions with defined energy bandgaps. In 1962, he demonstrated the first visible laser diode, emitting in the red spectral region at ~710 nm at 77K. Derived from this laser diode by the high photon extraction and internal ***e-h*** recombination radiation efficiency (quantum efficiency), he proved LED was an "ultimate lamp" and predicted in 1963 that LEDs would be used in TV and computer displays, car lamps and solid-state lighting. Thus, he is recognized as "the Father of LED".

In 1963, Holonyak was invited by Bardeen to join the faculty at University of Illinois at Urbana-Champaign. He was appointed a full Professor in Electrical Engineering and Physics. In 1977, he demonstrated the first quantum-well (QW) laser diodes by LPE, composed of multiple thin layers ~50nm thick of $In_{1-x}Ga_xP_{1-z}As_z$ quantum wells at UIUC. Subsequently in 1978, Holonyak (with R. D. Dupuis)

developed QW Lasers grown by MOCVD technology. Today, virtually all semiconductor LEDs and laser diodes incorporate Holonyak's QWs and use MOCVD for mass production of devices used in displays, solid-state lighting, and optical communications.

From 1980 to 1990, Holonyak investigated various post-growth processes, including impurity-induced layer disordering and (with J. Dallesasse) the controlled oxidation of Al-bearing III-V semiconductors to form stable "native oxide" insulating regions selectively inside a device structure. Today these innovative processes are used for the commercial laser diodes including oxide-defined apertures for vertical-cavity surface-emitting lasers (Oxide VCSELs) which have seen pervasive use as energy-efficient sources for high-speed optical data communications in data centers and enterprise networks, 3D sensing in smart phones (including imaging and facial recognition), autonomous vehicles and cryogenic computing.

In 2003, Holonyak (with M. Feng) realized that the direct-bandgap bipolar transistor base ***e-h*** recombination photon energy could be a new optical signal output. With quantum wells embedded in the base of a heterojunction bipolar transistor (HBT), they demonstrated the first laser operation in a forward-active transistor, called the "transistor laser" in 2004. Combining electrical and photonic functionality, the transistor-laser is an ideal component for electronic-photonics ICs that could open a new frontier in inter- and intra-chip optical data links and all-optical logic processors to alleviate the latency and overhead associated with massive data movement in today's network fabrics.

In his 50-year career at UIUC, Holonyak published over 600 refereed technical articles and directed 60 PhD students, many of whom have made important contributions of their own to wide-ranging fields. Holonyak's many awards and honors include the Queen Elizabeth Prize, the Draper Prize, the Global Energy Prize, the Japan Prize, the National Medal of Science, the National Medal of Technology, and the IEEE Medal of Honor. He is survived by his wife Katherine (Kay) Holonyak. Today, the world is brighter with energy-efficient LED solid-state lighting and communicates via high-speed laser-based data communication because of Holonyak's innovative contributions. He is an international treasure and his contributions have touched us all.

Professors Milton Feng
and John Dallesasse
University of Illinois at
Urbana-Champaign

Professor Santosh Kurinec – the Recipient of 2022 Region 1 William Terry Distinguished Service Award

Professor Santosh Kurinec

It's a great pleasure to inform you that Dr. Santosh Kurinec, IEEE Fellow, received 2022 IEEE Region 1 William Terry Distinguished Service Award for IEEE service, and outstanding research and teaching semiconductor technology and promoting semiconductor workforce generation. This award is intended to recognize those whose personal efforts have provided leadership, creativity, guidance, hard work and inspiration in a wide range of IEEE activities over a significant and sustained period of time.

Dr. Santosh Kurinec is the Professor of Electrical & Microelectronic Engineering at Rochester Institute of Technology (RIT). She served as the Department Head of Microelectronic Engineering from 2001–2009 after which she took an academic year sabbatical at IBM T.J. Watson Research Center, Yorktown Heights, NY as a visiting scholar. Dr. Kurinec is a Fellow of IEEE, Member, NY State Academy of Sciences, and the IEEE Electron Devices Society Distinguished Lecturer. She received the 2012 IEEE Technical Field Award for Outstanding Undergraduate Teaching. She was inducted in the Women in Technology Hall of Fame in 2018.

We hope that Dr. Santosh Kurinec will share with the EDS Newsletter readers more details of her outstanding professional career and comments and impressions which may be inspiring for EDS members.

Dr. Santosh, our congratulations and best wishes for a successful education, research and service in IEEE.

Daniel Tomaszewski,
EDS Newsletter EiC

Announcement of the 2022 EDS PhD Student Fellowship Winners

The Electron Devices Society PhD Student Fellowship Program was designed to promote, recognize, and support PhD level study and research within the Electron Devices Society's field of interest.

EDS proudly announces three EDS PhD Student Fellowship winners for 2022: **Asir Intisar Khan** – Stanford University, United States; **Nilesh Pandey**, Indian Institute of Technology Kanpur, India; **Shaochuan Chen**, RWTH Aachen University, Germany. Brief biographies of the recipients appear below. Detailed articles about each PhD Student Fellowship winner and their work will appear in forthcoming issues of the EDS Newsletter.

Asir Intisar Khan

Asir Intisar Khan is a Ph.D. candidate in the Electrical Engineering department at Stanford University, supervised by Professor Eric Pop. He received his Master of Science (M.S.) in Electrical Engineering from the same department at Stanford. Prior to joining Stanford in 2018, he received another M.S. (2018) and a Bachelor of Science (2016) in Electrical and Electronic Engineering from Bangladesh University of Engineering and Technology. His research efforts and vision encompass exploring novel materials and their functionalities to enable energy-efficient memory, computing devices and interconnects for 3D heterogeneous integration. His research work has enabled the lowest-to-date switching current density in phase-change memory technology and has been featured in Forbes Magazine and IEEE Spectrum. He also received the best student paper award for technology in 2022 IEEE Symposium on VLSI Technology and Circuits. He has held Research Intern positions at TSMC and IBM TJ Watson Research Center. Asir is a recipient of the Stanford Graduate Fellowship, Stanford Electrical Engineering Departmental Fellowship, and the 2022 IEEE EDS PhD Student Fellowship.

Nilesh Pandey

Nilesh Pandey's Ph.D. Nilesh Pandey completed his undergraduate from the National Institute of Technology, Kurukshetra (INDIA), in Electronics and Communication Engineering (2017). During his undergraduate studies, he developed a keen interest in semiconductor device modelling. Nilesh started to work in the semiconductor device modelling area in 2015. He published his first paper in IEEE T-ED during his undergraduate study. That paper formulated a new fundamental approach to solving the 2-D Poisson's equation using Green's function approach leading to more than ten publications in prestigious journals such as IEEE T-ED and IEEE EDL.

Shaochuan Chen

Shaochuan Chen (graduate student member of IEEE and IEEE EDS) received his bachelor's degree in Engineering at North China Electric Power University (NCEPU) in 2016. He is currently pursuing doctoral degree in Electrical Engineering and Information Technology with Electronic Materials Research Laboratory (EMRL) at RWTH Aachen University, Germany. His doctoral study is supervised by Prof. Dr. Rainer Waser and Dr. Ilia Valov (Forschungszentrum Jülich). His research aims at developing emerging non-volatile memories, including valence change memories (VCM) and electrochemical metallization memories (ECM) for data storage and neuromorphic computing applications. His work include the micro and nanoscale fabrication of two terminal memory devices, oxide semiconductors preparation by physical and chemical vapor deposition, and electrical characterization of memristive switching behavior. His recent research is focusing on the understanding of nanoscale charge (electron and ion) transport at electrode-solid electrolyte interface, formation of electron conducting channels in the oxide semiconductors, and materials and devices design for achieving high-performance memristive and neuromorphic functionalities. He is also involved in the supervision of master students to complete their master projects at RWTH Aachen University. The student projects include investigating active electrode impurity impact on the electrode ionization, cation migration and switching dynamic in tantalum oxide based electrochemical metallization memories, and studying metallic doping influence on the electrical properties and reliability of tantalum oxide and hafnium dioxide valence change memories. He has published 15 technical papers, including journal papers in Advanced Materials, Nature Electronics, Advanced Functional Materials, and Chemistry of Materials. Some of the work were selected as journal covers. During his graduate study, he obtained the international mobility fellowship from Soochow University to join the Electrical and Computer Engineering Department of University of California Santa Barbara, where he worked on the development of memristive devices based on two dimensional layered materials for artificial neural network applications.

Subramanian Iyer
EDS Student Fellowship Committee Chair
University of California, Los Angeles
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Announcement of the 2022 EDS Masters Student Fellowship Winner

The Electron Devices Society Masters Student Fellowship Program was designed to promote, recognize, and support Masters level study and research within the Electron Devices Society's field of interest.

EDS proudly announces the winner of the 2022 EDS Masters Student Fellowship.

Kamal Rudra Chatterjee

Kamal Rudra Chatterjee Kamal Rudra is a second-year graduate student at the University of Michigan, Ann Arbor pursuing his master's in Electrical and Computer Engineering with a specialization in Solid State and Nanotechnology. He is a recipient of SPIE Laser Technology, Engineering and Applications Scholarship 2022 and J.A. Woollam Company Scholarship 2022 by SVC Foundation. More recently, he was awarded the J.N. Tata Endowment Gift Scholarship for academic excellence by the Tata Education and Development Trust. He is currently working on multiple challenging research themes at the University of Michigan; namely on fabrication photonic devices as well as characterization of solid-composite electronic materials.

Rudra wishes to contribute and be a catalyst in the growth of semiconductor and photonics industry.

Subramanian Iyer
EDS Student Fellowship Committee Chair
University of California, Los Angeles
s.s.iyer@ucla.edu

Announcement of the 2022 EDS Undergraduate Student Fellowship Winners

The Electron Devices Society Undergraduate Student Fellowship Program was designed to promote, recognize, and support undergraduate level study and hands-on experience within the Electron Devices Society's field of interest.

EDS proudly announces the winner of the 2022 EDS Undergraduate Student Fellowship.

Alexander Yovanovich

Alexander Yovanovich is a fifth-year Microelectronics student at the Rochester Institute of Technology. He is currently working within Dr. Stefan Preble's photonics research group on two primary projects, one for photonics education, and another for implementing lithium niobate modulators using silicon nitride waveguides. His interest in the field of photonics started almost by accident, picking up an introductory class after the start of last semester while making some last-minute schedule corrections. As the course progressed, he became more interested in the field as it combined many of the aspects that interest him within the field of microelectronics, including materials science, computing/data processing, and device design. This interest led to a summer research assistantship within the RIT Integrated Photonics group which in turn drove his current end-of-degree capstone projects. As a student, he has always been interested in the fields of engineering and physics, completing an independent study of processor design in high school and exploring various projects involving physics and/or electrical engineering in his spare time. This interest in understanding what makes things work has been the driving factor in his educational goals to date, with his initial interest in the field of microelectronics originating from the aforementioned independent study and the realization of how immensely complex the devices that drive the modern digital world must be. Through his study of how to manufacture such devices as part of his degree, he has furthered an understanding of physics, materials science, chemistry, statistics, and many more (often unexpected) fields. With this knowledge, he hopes to continually learn more and attempt to understand the extremely broad and interdisciplinary nature of device design. In addition to his undergraduate studies, Alexander also is a member of Air Force Reserve Officer Training Detachment 538 at RIT and is due to commission into the United States Space Force as an electrical engineer upon graduation. From his time in the ROTC program, he has come to appreciate the complexities of various non-technical leadership and management skills. He hopes to put these skills to work in combination with his technical background to bridge the knowledge gap present within many engineering projects and more effectively drive the field of microelectronic devices forward. In the final year of his degree, he anticipates learning much more while implementing the skills and knowledge gained over the course of his undergraduate study through the execution of his two capstone technical projects.

Durga Misra
EDS Undergraduate Student
Fellowship Committee Chair
New Jersey Institute of Technology

Call for Nominations

PhD and Masters Student Fellowships and Undergraduate Student Scholarships

The IEEE Electron Devices Society invites nominations for our society sponsored Student Fellowships and Scholarships. These annual awards are given to promote, recognize, and support graduate, masters, and undergraduate level study and research within the scope of Electron Device technologies.

EDS Masters Student Fellowship
Prize: US $2,000 and award plaque
Submission Deadline: 15 May 2023

EDS PhD Student Fellowship
Prize: US $5,000 and travel funds
to IEDM for award presentation
Submission Deadline: 15 May 2023

EDS Undergraduate Student Scholarship
Prize: US $1,000 and award plaque
Submission Deadline: 15 May 2023

Please help to promote these funding opportunities to students in your personal and professional network!

My Journey as a Researcher in the Semiconductor Field

Hisayo S. Momose (IEEE Fellow)

I was engaged in research and development in the semiconductor field for more than 30 years. I am delighted by the opportunity to reflect on my life as a researcher. When I was a child, I liked reading, and I read many books from diverse areas, including fairy tales, history, adventure, and science fiction. In addition, I read stories about great people in a biographical book series for children. I especially liked female protagonists such as Murasaki Shikibu, Marie Curie, and Helen Keller. Murasaki Shikibu was a female Japanese author who, in the early 11th century, wrote what is considered to be one of the world's first novels. These female protagonists' charming personalities and sincerity toward their work left a strong impression on me.

I chose science as my major after thinking about my future career in high school and university, because I wanted to scientifically investigate various materials and living creatures that exist in the natural world. Although there were few women among the faculties of science and engineering at universities, I did not hesitate to make that choice. In retrospect, I may have somehow been influenced by my two older brothers, who both have a PhD degree in science and were already pursuing their careers as researchers. In my mid-twenties, I joined Toshiba Corporation. The company, as a general electronics manufacturer, had many technical areas for research and development; this aspect appealed to me. In addition, several female seniors from the same university where I studied were already working there as researchers, and their advice was extremely helpful when I was thinking about my future line of work.

My life as a researcher in the company started with the development of memory devices. This became an interesting and challenging job for me. It was the generation when the 1 Mbit DRAM was still under development. I felt that we were at the forefront of research in this field. It was a few years before my country passed the Equal Employment Opportunity Act. Female researchers were restricted in some aspects of labor management, such as the total number of hours worked per year. Despite being in that era, I was fortunate to be given the same opportunities as other male researchers in many aspects of my work, such as choosing research themes and planning experiments. I am grateful to my laboratory heads, bosses, and colleagues for their consideration and encouragement. There was also an in-house network of approximately 30 female researchers at that time, including a few with careers spanning over 20 years. I was fortunate to have exchanged information with them on various other issues in addition to work.

However, when I returned to work after about a year of childcare leave in my mid-thirties, I felt restless with my colleagues' activities. This was because in only one year, the main research subjects of my group had already shifted a few generations from the 0.25 μm generation

Members of the Center for Semiconductor Research & Development in Toshiba Corporation under cherry blossoms in full bloom in 2006. Dr. Momose is on the far right side of the front row

technologies to 0.1 μm generation technologies. Nevertheless, taking on challenges with a fresh mind seemed to have a positive effect; consequently, I was able to obtain interesting research results. The research I conducted at that time enabled me to become an IEEE Fellow later.

My research theme at that time was the development of high-performance and highly reliable MOS transistors of the 0.1 μm generation. For approximately three years, I had repeated trial and error approaches to fabricate high-quality stacked thin-film insulators for the 0.25 μm generation containing thin nitride and oxide films. The knowledge I had gained at that time effectively contributed to my new research. After my return from childcare leave, I found for the first time that ultra-thin gate oxide transistors with small gate lengths operate normally and exhibit significantly higher DC performance even in the direct-tunneling regime. That was the highest value at that time. I can still vividly remember that my boss and colleagues were surprised at the high drive current when I first showed them the experimental results at our group meeting.

After some additional evaluations and discussions, at the 1994 IEDM, I presented my paper, which was press-released before the meeting as one of the remarkable technical highlights of the meeting. The work demonstrated for the first time that transconductance of over 1.0 S/mm is possible in Si devices, as long as a very-high-capacitance gate insulator is used. It was also confirmed that the MOSFETs have the suppression of the short-channel effects for Vth rolling because of the improved gate bias controllability of the channel potential through the thinner gate insulator. Subsequently, the prediction of gate insulator thinning in the International Technology Roadmap for Semiconductors (ITRS) was aggressively changed from the 1994 edition to the 1997 edition. When I visited the Semiconductor Industry Association (SIA), I was honored to hear that they had considered my research results when writing the roadmap. In addition, as a corporate researcher, I was pleased that this work was included in the periodic brochure for the shareholders of my company as a promising study.

Thereafter, I became increasingly curious about the various properties and concerns regarding the MOSFETs with thin gate insulator. Over several years, I thoroughly investigated the transistors, including their AC and RF characteristics, uniformity, reliability, noise, and channel orientation dependence. It was exciting for me to choose a theme that I was interested in as well as plan, perform, and discuss the experiments. In these studies, I presented nearly ten papers accepted by the IEDM and VLSI Symp as the first author. I was pleased to learn that these were timely studies that matched the interests of the audience at the time. These studies provided me with many opportunities to conduct seminars and lectures for young engineers in this field and students. In my mid-forties, I became the first female IEEE Fellow in Japan; hence, I also had several opportunities to share my experience at the domestic WIE meeting.

At Toshiba, we had many talented researchers and engineers involved in design, process, evaluation technology, materials, and so on. They were sufficiently kind to lend special equipment for sample preparation and to perform TEM evaluations. The opportunity for discussions with them while conducting cutting-edge research and development was extremely significant and beneficial. I believe that this was the key to improving the quality of my research and I was fortunate to have been in this environment.

Since then, the subjects of my research gradually changed and expanded along with the changes in the times and society, such as toward analog devices, thin-film transistors, and imaging devices. I also had the opportunity to conduct joint research with external research institutes, according to need. After moving to a university in my mid-fifties, in addition to pursuing my own study, I had more opportunities to support the research activities of young professors and researchers. When I was developing novel materials such as organic photoconductive films, I recalled discussing the experimental results and future applications with professors and students who specialize in organic films. Such discussions with various experts outside my field always made me feel refreshed.

The experience I gained through activities in the EDS Society was beneficial for expanding my interests and identifying new research subjects. Fortunately, I had many opportunities to discuss research trends with EDS members and received advice on my research from them. In addition, I served as one of the editors in the field of MOS devices in *IEEE Transactions on Electron Devices* for 10 years and handled more than 400 manuscripts in the area. This was a worthwhile experience for me.

In my long research journey, I enjoyed thinking deeply and planning studies to solve difficult problems. The results obtained, whether expected or not, also provided me with many opportunities to consider and ponder the root causes. This process was always thoroughly enjoyable. I hope that young people will be able to enjoy their research life by focusing on what they are interested in, and to make giant strides in good research environments.

Semiconductor products in today's IT society require an extremely large variety of technologies, and their development has involved the wisdom and efforts of numerous people in the past as well as the present. Although my research itself might only be a negligible part of that endeavor, I am honored that I was able to contribute even a little to the overall development. I express my gratitude to everyone who worked with me for more than 30 years at Toshiba Corporation and Yokohama National University for their encouragement, support, and discussions.

Dr. Momose *has more than 30 years of experience in research and development at Toshiba Corporation, Japan*

(1984-2015) and Yokohama National University, Japan (2015-2017). She was a guest professor at National Yang Ming Chiao Tung University, Taiwan (2017–2021). She was engaged in the research and development of Si transistors ranging from 1.2 μm to sub-50 nm, static RAMs, CMOS/BiCMOS logic LSIs, RF/MS analog CMOS, thin-film transistors, oxide semiconductors, imaging devices, and photoconductive devices. She has authored or co-authored nearly 200 papers published in technical journals and the proceedings of international/domestic conferences.

In recognition of her contributions, she was awarded an IEEE Fellow (2005), and a Fellow of the Japan Society of Applied Physics (2009). She has also received several awards and honors, including the Commendation for Science and Technology from the Minister of Education, Culture, Sports, Science and Technology, Japan (2009). She served as a member of the technical program committee at more than ten academic symposia in the field, including IRPS (1992-1994) and IEDM (1997-1998 (CMOS and Reliability), 2013-2014 (Display and Sensors)). In addition, she served on several EDS executive committees, including EDS fellows committee (2007-2014). She served as an editor on the IEEE Transactions on Electronic Devices (2005-2014), and then as EDS Vice President of Publications and Products (2016-2018).

The 4th IEEE Women in EDS (WiEDS) Session at IFETC 2022

By Chenxuan Hu, Arokia Nathan, Xiaojun Guo, Jun Yu, P Susthitha Menon

On the 21 August 2022, the second day of the 4th IEEE International Flexible Electronics Technology Conference (IFETC) 2022, Miss Qianqian Huang and Miss Chenxuan Hu of the Women in Electron Devices Society (WiEDS) moderated a hybrid lunch networking session for the conference attendees. The session with the topic "Career Growth via IEEE EDS," was attended by a physical audience of 20 people at the Haiqing Hotel in Qingdao, China and virtually too. Prof. Merlyne de Souza (Sheffield University), IEEE EDS Vice President of Memberships, gave a virtual welcoming speech, followed by Assoc. Prof. P Susthitha Menon (National University of Malaysia - UKM), chair of WiEDS, who shared her journey with IEEE and EDS. Prof. Qianqian Huang from Peking University, who is an IEEE EDS Early Career Award Winner, shared her life experience from an undergraduate student to an assistant professor working with IEEE EDS, and how it helped place her career in very good footing. Prof. Arokia Nathan (General Chair of IFETC2022 and VP Pubs, EDS),

Prof. Qianqian Huang from Peking University, IEEE EDS Early Career Award Winner, shared her career progression

Attendees of the 4th IEEE IFETC 2022 Women in EDS (WiEDS) session

Prof. Jun Chen from Sun Yat-sen University as well as Prof. Hanbin Ma from Chinese Academy of Sciences shared their experience with the students from Shanghai Jiaotong University, Central South University, Jinlin University. This event was supported by the IEEE-IFETC Organizational and Steering Committee and WiEDS.

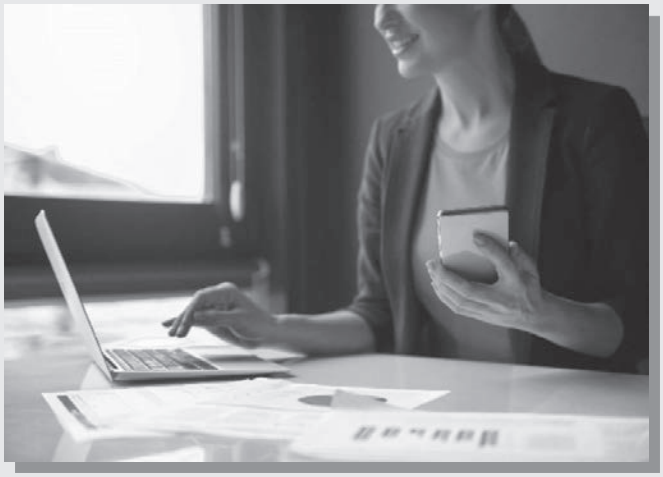
Women in Engineering Careers—The Time of Your Life!

Panel Session and Networking at IEDM 2022

We had a great Women in EDS Panel discussion on 5 December in San Francisco. Thanks to our distinguished EDS members who shared their life journeys and advice to participants. IEDM attendees also had the opportunity to connect with our members at the EDS exhibit or online. The ladies generously shared their contact information to increase outreach to those who were not able to attend the early morning panel session.

EDS is so fortunate to have role models like Jeewika Ranaweera, Pei-Wen Li, Francesca Iacopi, and Mukta Ghate Farooq who volunteer their time to encourage and inspire others.

Pei-Wen, Jeewika and Mukta



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https://www.ieee.org/membership/benefits/index.html

EDS Young Professionals

The 4th IEEE IFETC 2022 Young Professional (YP) Session

By Chen Jiang, Chenxuan Hu, Arokia Nathan, Xiaojun Guo, Jun Yu, P Susthitha Menon

On the 23 August 2022, the third day of the 4th IEEE International Flexible Electronics Technology Conference (IFETC) 2022, Dr Chen Jiang, a previous recipient of the IEEE EDS PhD Student Fellowship, moderated a networking session for young professional attendees, with oral presentations from five outstanding speakers delivering their early-career research outcome. The session was attended by an audience of 25 people physically at the Haiqing Hotel in Qingdao, China and virtually. During the session, Chen Jiang briefly introduced the aim of IEEE and EDS in supporting young professionals and the purpose of the Young Professionals Session launched in IFETC 2022. The five presentations were from Dongping Wang from Chinese Academy of Sciences, Kyle Schvaneveldt from Bringham Young University, Kai Liu from Chinese Academy of Sciences, Mengwei Si from Shanghai Jiao Tong University, and Jianle Lin from Sun Yat-Sen University. All presenters received acknowledgement certificates from IFETC 2022 General Chair, Prof. Arokia Nathan. This event was well-received by conference participants.

Dr Chen Jiang's introduction of the 4th IEEE IFETC 2022 Young Professionals (YP) session

Joint Society Young Professionals and Women in Engineering Mentoring Event at ESSDERC/ESSCIRC 2022

By Luisa Petti and Susanna Reggiani

On 20 September 2022, the second day of the annual European forum on recent advances in Solid-State Devices and Circuits (ESSDERC/ESSCIRC 2022), a mentoring event took place during the lunch break. It was organized jointly by IEEE Young Professionals and IEEE Women in Engineering and co-sponsored by IEEE Electron Devices Society (EDS) and IEEE Solid-State Circuits Society (SSCS). Abira Altvater and Danielle Marinese (SSCS), the organizers of an analogous event in the previous years, welcomed Luisa Petti (WiEDS) and Susanna Reggiani (EDS) proposing the new format. Eighteen mentors answered the call and almost all of them were present at the event. After brief introductions of both Societies, Abira moderated a very nice ice-breaking activity, asking the mentors to introduce themselves with 3 words and following 3 sentences. Next, a hybrid networking session nicely followed for the conference attendees and mentors present in the room. The event saw a significant participation of the young PhD students, Post-docs, and early stage professionals – especially women – present at the conference who had the chance to connect with SSCS and EDS society members while having an informal lunch break. More than 40 attendees enjoyed the fruitful mentoring session!

Mentoring event: sharing 3 words and 3 sentences with the attendees

IEEE EDS HUMANITARIAN GRANT REPORT FOR THE OFF-GRID SOLAR SCHOOL AND SMARTBOX PROJECT IN THE MAASAI TRIBAL VILLAGE OF EMPASH, KENYA OCTOBER 2022

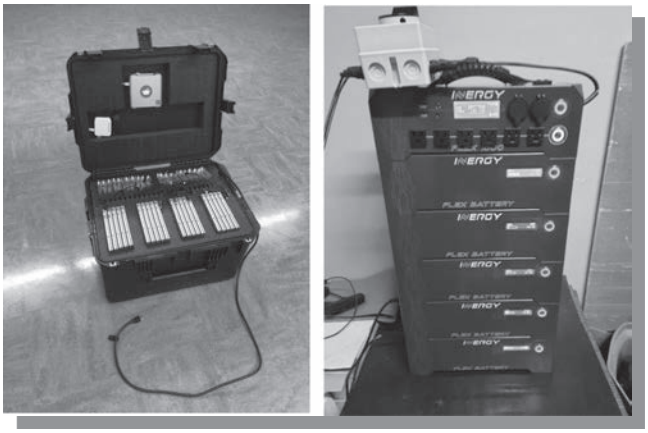
BY STEPHEN PARKE

Education is a most formidable tool in transforming our world. Education brings fulfillment, reduces poverty, increases chances for a healthy life, empowers women, and promotes peace. But, more than 72 million children around the world remain unschooled. The Sub-Saharan region of Africa, particularly the disenfranchised Maasai children of Kenya and Tanzania, are severely affected due to lack of access to water, electric power, teachers, curricula, computers, and internet.

Wilson Kamau, PhD Materials Engineering, founder of non-profit toEnable.org, grew up in Mukurwe, a village outside of Thika Town in Central Kenya. It has 500 people, 2000 cows, and 6000 goats. Wilson was fortunate to receive outside help to complete primary school and then high school, where he caught the vision to become a chemist. He found generous support to attend Africa Nazarene University in Nairobi and then Northwest Nazarene University in Boise, ID, graduating with a Chemistry degree. He went on to graduate school at University of Nevada, Reno and persevered to receive a PhD in Materials Engineering. He now works for a major US engineering company! With his wife Rebecca, he has founded the non-profit toEnable.org to bring basic human needs (clean water, food, power, etc) and primary and high school education to the village of Empash. In 2019, Dr. Kamau reached out to his alma mater, NNU, to request the help of interdisciplinary design teams of senior engineering students to design a modular, classroom building that could be assembled in a simple manner in remote sites, like the village of Empash, off-road and off-grid. This classroom is replicable, using locally available materials and talent.

The school building with solar panels in the village of Empash

Two consecutive years of "Firm Foundation" student teams designed the modular classroom for 40 primary school students and delivered their PE-reviewed building plans to the local Empash construction team. This involved developing new lightweight masonry wall panels made of "Aircrete." (although traditional stone was ultimately used) ToEnable funded the construction, and the first two adjacent modular classrooms were completed July-October 2022. Dr. Kamau also requested NNU's



SmartBox and Solar Power system installed in the village of Empash

Kenya Energy "Kenergy" student team to design a 10kWh per day off-grid solar power system for this new school. It is capable of charging 20 cell phones, 20 laptops, LED lights, a small medicine fridge, and a novel off-grid, off-internet classroom learning system known as SmartBox. Our team worked with Idaho-based, off-grid solar company Inergy to design a safe, robust, simple to maintain system for the Empash School. This university-industry collaboration placed state-of-the-art solar equipment in one of the neediest and most practical locations on earth in a very short time.

Without any internet connection to the Cloud, the terabytes-sized SSD RACHEL server inside the SmartBox delivers a vast collection of curated content for K-12 education, distributed through the classrooms and village wirelessly with a WiFi router to 20 chromebooks (two students on each) and other laptop or cellphone users in the community. The 20 chromebooks, server, router, and teaching data projector are recharged nightly (in 4 hours) from the solar power system, then run on battery power the entire school day. SmartBox has extensive interactive educational resources including Wikipedia, Khan Academy, African Storybook Project, 1000's of reading books, e-textbooks, History of Women Leaders in Africa, languages, videos, animations, art & music, and two audio headsets per laptop, for quiet team learning in the classroom. Lack of qualified teachers is a serious problem in remote areas, but students can learn on SmartBox, even in the absence of enough qualified teachers. It is also a powerful learning resource for the teachers themselves. The SmartBox and its tech equipment are all housed in a strong, wheeled Pelican Case that is securely locked nightly inside a steel security cage alongside the Solar Battery Stack.

Children with chromebooks in the classroom

NNU Engineering traveled a few years ago to a rural off-grid school in Liberia to install a SmartBox, along with SmartBox creator Gary Friesen, from Innovative Education Inc. (IEI). In three years of use in that setting, SmartBox helped that school to rise to the top in Liberia on the West African Examination Council (WAEC) high school graduation exam. In 2014, the school only had a 23% grad rate. In 2017, they jumped to a 88% grad rate! The Empash Primary School in Maasailand is the first school in Kenya to receive SmartBox. Hands-on training was held for the Empash teachers both before and during our weeklong install visit to Empash in mid-October 2022. Some of the teachers trained had never used a computer/laptop in their life! Now they are proficient enough to teach their primary school children how to use them.

Dr. Stephen Parke, NNU Engineering Professor and IEEE EDS Humanitarian Council member led a team of 12 NNU students to Africa Nazarene University near Nairobi, Kenya from August-December 2022 to study alongside their fellow Kenyan students. 16-23 October, Dr. Parke and this NNU student team along with Dr. Kamau and his ToEnable team, traveled six hours by 4WD to transport, install, and train teachers on this new Solar Power and SmartBox system in the newly completed Empash School.

NNU Engineering student volunteer training Empash teachers on SmartBox chromebook system

Volunteers from NNU, Boise

At the end of this week, the entire village and school children came out to celebrate the opening of this new, modern primary school. There were speeches, dances, singing, food, and much thanksgiving in prayer for this huge change wrought in this small village. There are now 66 students enrolled in this new school, with 100 more on a waiting list. There is no doubt that this school will produce many more Dr. Wilson's and Dr. Rebecca's in the future. Thanks to IEEE EDS Humanitarian Council for their generous $16,000 grant to help begin the transformation of these students' lives for this village of Empash and surrounding ones.

STEM4FUN community program: Promote STEM interest among 1500 students

By Ahmad Sabirin Zoolfakar, Norhayati Soin, P. Susthitha Menon, Rozina Abdul Rani, Maizatul Zolkapli and Azrif Manut

A total of 1500 primary and secondary school students in Selangor, Negeri Sembilan and the Federal Territory of Kuala Lumpur are targeted to be involved in the STEM4FUN community program organized by the College of Engineering Studies of Universiti Teknologi MARA (UiTM) in collaboration with The Institute of Electrical and Electronics Engineers (IEEE) Electron Devices Society (EDS) Malaysia. The program was funded by the 2022 EDS Humanitarian Project Grant.

Students from Selangor, Wilayah Persekutuan Kuala Lumpur and Negeri Sembilan had a great time in STEM4FUN activities

The STEM4FUN community programme is a knowledge transfer program that uses demonstrations of electronic blocks (Snap Circuits), drones, augmented virtual reality, and robots to provide exposure and foster interest in subjects based on science, technology, engineering, and mathematics (STEM). This exposure is intended to encourage students to pursue STEM majors in higher education and then in their careers.

The STEM4FUN programme includes exposure to cutting-edge technology such as green technology, the use of gadgets or technological devices to strengthen students' understanding of STEM subjects, and it is also a new learning experience about STEM, particularly in the field of electron devices. STEM4FUN is also implemented in collaboration with other IHLs, such as Universiti Malaya and Universiti Kebangsaan Malaysia, and industry to form a Quadraple Helix between university entities, industry, government agencies, the Ministry of Education Malaysia, and the community, which is schools. Strategic partners supporting this programme include The Institute of Electrical and Electronics Engineers (IEEE) Electron Devices Society (EDS) Malaysia, the National STEM Centre, AR Distributor as well as Selangor, Negeri Sembilan and the Federal Territory of Kuala Lumpur Education Department.

According to the Project Leader, Associate Professor Ir. Dr. Ahmad Sabirin Zoolfakar, and five members, Prof. Ir. Dr. Norhayati Soin, Associate Prof. Dr. P. Susthitha Menon, Ir. Ts. Dr. Rozina Abdul Rani, Ir. Dr. Maizatul Zolkapli, and Ir. Dr. Azrif Manut, this activity exposes 1500 students and 300 schoolteachers to STEM knowledge in producing skilled human capital. Students must be nurtured and homed in their use of technology through creativity, while also developing critical thinking skills. The excellence of STEM students at the tertiary level can encourage research, the development of new inventions, and innovation.

This project has the full support of the National STEM Centre, the Malaysia Ministry of Education, and the State Education Departments of Selangor, Negeri Sembilan, and the Federal Territory of Kuala Lumpur. The STEM4FUN program has been implemented in schools across Selangor, Negeri Sembilan, and the Federal Territory of Kuala Lumpur beginning in July 2022.

North America (Regions 1, 2 & 3)

IEEE EDS One Day Tutorial on Neuromorphic Computing & AI

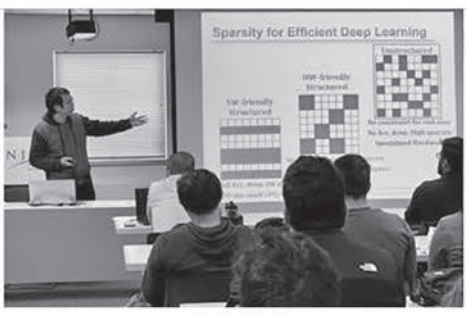
— by Durga Misra

An IEEE EDS Educational event, a tutorial, was conducted by the ED/CAS joint Chapter of North Jersey Section on 16 November 2022, on Neuromorphic Computing and artificial intelligence (AI) at New Jersey Institute of Technology (NJIT). The event was publicized on the NJIT website and the participant registration was also done through the website. Thirty-eight undergraduate and graduate students were registered for the event. The program started with breakfast and coffee followed by a poster session where the poster presenters described their posters for five minutes. The posters were ReD-LUT: Reconfigurable In-DRAM LUTs Enabling Massive Parallel Computation" and "Power Reduction and Conductance Quantization by Process Optimization in HfO_2-Based RRAM Devices for In-Memory Computing."

Following the poster presentation, the tutorial session started. An introduction of IEEE Electron Device Society's activities and the membership benefits was provided by Prof. Durga Misra, Chapter Chair of ED/CAS Chapter and Department Chair of Electrical and Computer Engineering Department of NJIT. The first tutorial was given by Prof. Jack (Qingxue) Zhang of Purdue University on "Brain-Inspired AI on the Edge for Precision Medicine" where he discussed how uniquely combining AI theories, neuromorphic learning algorithms, efficient computing, and wearable/IoT monitoring, can target smart health. He also highlighted the efforts on both efficient learning and neuromorphic learning for wearable big data applications. The second tutorial was given by Prof. Bo Yuan of Rutgers University on "Algorithm and Hardware Co-Design for Efficient Deep Learning: Sparse and Low-rank Perspective" where he introduced the algorithm/hardware co-design works for energy-efficient deep neural networks (DNN) from both the sparse and low-rank perspectives. He also demonstrated the benefit of using structured and unstructured sparsity of DNN for designing low-latency and low-power DNN hardware accelerators. The third tutorial was given by Prof. Shaahin Angizi of New Jersey Institute of Technology on "Toward Opportunistic and Fast Integrated Sensing and Computing for Edge Imaging Systems," where he described the cross-layer (device/circuit/

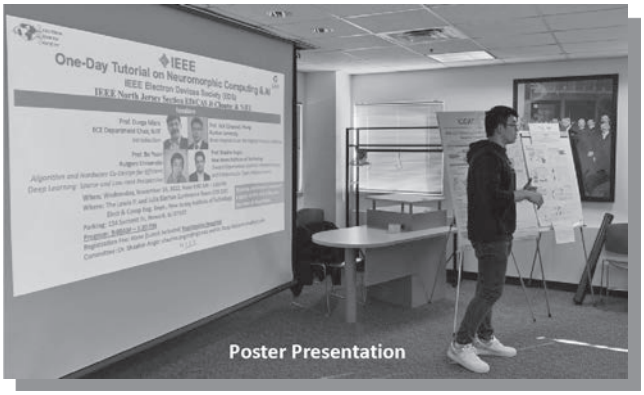
Participants

Prof. Jack



Prof. Bo Yuan

Prof. Shaahin



architecture/application) co-design of energy-efficient and high-performance processing-in-sensor and processing-in-memory platforms. This enables a smooth transition from the current cloud-centric IoT approach to a data-centric approach, whereby the mobile edge devices can opportunistically perform computation close to the sensor by repurposing the sensor/cache to a data-parallel processing unit remarkably reducing the power consumption and latency of data transmission to a back-end processor. At the end of the tutorials an additional question and answer session was conducted for general discussion. The program ended with lunch for all the participants.

Sister Society provides keen insight into Silicon Valley origins for Ohio's Intel plans

—by Paul R. Berger

The Columbus EDS/PHO chapter invited Mr. Paul Wesling, a Distinguished Lecturer for IEEE Electronics Packaging Society (EPS) to speak on "**Characteristics of Successful Tech Hubs and Start-ups: Lessons from the Origin and Growth of Silicon Valley**" on 14 September 2022. Prof. Paul Berger first introduced Ohio State's

Paul R. Berger opens the event

Ohio State's President Kristina Johnson welcomes Mr. Paul Wesling

President Kristina Johnson, who gave a short talk on the two new Intel fabs being built near Columbus and the opportunities (and responsibilities) the university has; she then introduced Mr. Wesling.

The event was hybrid, with guests from California, New York, Texas, Washington, Michigan, Indonesia, Bhutan, and now posted on IEEE.tv:https://ieeetv.ieee.org/video/characteristics-of-successful-tech-hubs-columbus

The talk itself was very animated and engaging, with a number of good illustrations of the lessons that Wesling gives for other up-and-coming tech hubs to consider adopting. The slides were quite helpful in explaining how the Santa Clara Valley became the leading tech hotbed in the early part of the 20th century, and the legal, IP, and corporate environment conditions that helped it to succeed. The Q&A session raised a number of good questions and observations.

~Rinus Lee, Editor

Europe, Middle East & Africa (Region 8)

MTT/ED/AP/EP/SSC West Ukraine Chapter

—by Mariya Antyufeyeva

The recent Chapter activity was focused on the organization of the 2022 IEEE 18th International Conference on Perspective Technologies and Methods in MEMS Design (MEMSTECH), which was held on 7–11 September 2022. The Conference was co-sponsored by the IEEE Ukraine Section and MTT/ED/AP/EP/SSC West Ukraine Chapter and was held in the online format. The other sponsors were Lviv Polytechnic National University (Ukraine), Wroclaw University of Science and Technology, and AGH-University of Science and Technology (both from Poland). The aim of the Conference was to exchange experience between the scientists from

Dr. Mykhaylo Melnyk, Chapter Chairman, serving the MEMSTECH-2022 online sessions

Ukraine and abroad in the field of design, manufacturing, research and use of microelectromechanical systems (MEMS), and to establish cooperation between scientists and educational institutions to prepare and implement the international projects and grants. The most perspective topics of the Conference were related to miniaturization of the electron devices, in particular devices ranging in size from microns to millimetres, micro-actuators, micro-robots, micro-batteries, and measurement of micro-phenomena. Such topics allowed collecting the reports representing the latest achievements in the miniaturization of the electronic devices. The most interesting and advanced presentations were "Finite Element Analysis of Magnetic Shielding for a Miniaturized MEMS Displacement Sensor" (Poland/Turkey), "Theoretical Investigation of the Magnetostriction Process in a Newly Developed Microstructure Thermal Formation Device" (Lithuania), and "Numerical Simulation and Analysis of the Acoustic Standing Wave Field Stability in Acoustofluidic Microchannel" (Ukraine). Despite the online format proposed by the Organizing Committee of the Conference because of war in Ukraine, the active discussions on the reported presentations continued after the scheduled time. The decision to organize the MEMSTECH-2023 in-person, proposed by the Conference organizers, was strongly supported by the Conference participants at the Closing ceremony.

~Mykhaylo Andriychuk, Editor

Learning From the Brain to Save Energy

An interview with Prof. Max C. Lemme and Prof. Rainer Waser made by Tobias Schlößer

Scientists at Forschungszentrum Jülich and RWTH Aachen University want to create a leading international location for neuromorphic AI hardware together with companies from the region.

Establishing a technological basis for neuro-inspired AI hardware from Europe-that is the goal of the NeuroSys future cluster and the NEUROTEC project, where Forschungszentrum Jülich and RWTH Aachen University are cooperating with each other. To this end, an internationally leading location for neuromorphic hardware-computer chips inspired by the human brain-is to be created in the Jülich-Aachen region in collaboration with local high-tech companies. Following a meeting at the Jülich-Aachen Neuromorphic Computing Day, which took place at Forschungszentrum Jülich on 24 May 2022, the researchers are now providing an insight into the interim status of the projects.

NEUROTEC entered its second phase at the end of 2021 and will receive total funding of around 36 million euros over five years from the German Federal Ministry of Education and Research (BMBF). The future cluster "NeuroSys-Neuromorphic Hardware for Autonomous Artificial Intelligence Systems," prevailed in last year's Clusters4Future ideas competition and will receive up to 45 million euros in funding from the BMBF.

In this interview, Prof. Rainer Waser of Forschungszentrum Jülich and RWTH Aachen University, coordinator of NEUROTEC (Neuro-inspired Technology of Artificial Intelligence for Future Electronics) together with Prof. Max Christian Lemme of RWTH Aachen University and AMO GmbH, coordinator of the future cluster NeuroSys (Neuromorphic Hardware for Autonomous Systems of Artificial Intelligence) explain the current status of developments.

Prof. Rainer Waser, what exactly do we need such neuromorphic computer chips modeled on the human brain for?

Prof. Rainer Waser: In NEUROTEC, we are focusing on a promising area of the future, namely hardware for artificial intelligence applications. With our approach, we are addressing a very fundamental problem, the energy problem: Because the use of AI is currently still very energy-intensive. The training of models is usually done on supercomputers and requires more and more computing time. Every 3 to 4 months the computational effort doubles, at least this is the trend of the last few years.

Neuromorphic systems with artificial synapses promise to solve these tasks much more efficiently-by several orders of magnitude-than is possible with conventional digital computers. In the long term, a wide range of applications is conceivable: from the smallest nanosensors, the "smart dust", to intelligent implants with energy-autonomous AI control, pattern recognition chips in mobile devices, online-trainable controllers in Industry 4.0, vehicle-based AI electronics for autonomous driving, to mainframe computers that in turn emulate the brain or centrally solve complex AI tasks for the surrounding economy.

The NEUROTEC project is funded by the "Sofortprogramm für den Strukturwandel." It is intended to help create new jobs in the Rhenish mining region even before the end of coal mining. What exactly do you have in mind?

Prof. Rainer Waser: We plan to support local industry, particularly in the area of basic technologies. The professional sectors that we are addressing extend far beyond actual chip production. This also includes, for example, plant engineering, measurement technology and electronics development. The NEUROTEC II project phase has got off to a very good start since November 2021 and almost all work packages are on schedule. Some work packages are even slightly ahead of their time.

The technology is currently still in the research and development phase. Nevertheless, there are already some initial concrete successes to report. Naturally, these are initially primarily jobs for specialized staff, before the technology matures and the focus shifts to industrial production, when the technology becomes widely used. A current example: Prof. Heuken from AIXTRON SE highlighted at the Jülich-Aachen Neuromorphic Computing Day the prospects that will open up in the next few years in terms of new jobs at AIXTRON in connection with the new 2D materials. These materials are being investigated in the NEUROTEC project for their suitability for neuromorphic computing.

What are the advantages of this neuromorphic hardware you are developing?

Prof. Rainer Waser: Conventional computer chips are based on transistors. We would like to supplement these transistors with a novel memristive component. Such a "resistor with memory" resembles the synapses in natural nerve cells and is therefore particularly suitable for artificial neural networks, such as those used for artificial intelligence applications.

An important feature of neuromorphic chips is that computing processes and memory are no longer physically separated. The data transfer between processor and memory that takes place continuously on conventional computers with so-called Von Neumann computer architecture is extremely energy-intensive and slows down computations. In contrast, we envision neuromorphic chips with artificial synapses that can do both: Store information and process it at the same time. Computing is then performed directly in-non-volatile-memory; this is also known as computing-in-memory. And it makes it possible to process information in a highly parallel manner. The model here is actually the human brain, which requires an average of just 20 Watt. That is several orders of magnitude less than the energy requirements of a supercomputer that performs similar functions using AI.

Prof. Max Christian Lemme, in the NeuroSys future cluster, you are driving forward complementary developments in the field of neuromorphic hardware. The topic is also being intensively pursued globally. Where does the region stand in terms of global competition?

Prof. Max Christian Lemme: The BMBF's Future Cluster Initiative has the explicit goal of quickly translating excellent cutting-edge research into applications, and doing so in regional alliances. To achieve this, we have brought together researchers along the entire value chain in the NeuroSys future cluster who have worldwide visibility in their respective disciplines. In addition, there are regional companies and start-ups from the high-tech sector. We now cover the entire field from new materials to image and speech processing and medical technology, and expand the concept with socio-economic issues-i.e. research on the ethics of AI, on consequences for the job market and on viable business models for "AI Hardware Made in Europe".

An advisory board of scientists and international companies completes the cluster. So, I dare to say that we are on par with the global competition. What is missing in the region is a modern semiconductor factory for AI chips, the location of which we have formulated in our vision. With the excellently trained engineers and scientists in the region, including Belgium, the Netherlands and the Ruhr area, the proximity to the research institute IMEC in Belgium and the leading manufacturer of lithography equipment ASML in the Netherlands, we have an excellent argument.

How far has the technology come?

Prof. Max Christian Lemme: As is often the case, there is no simple answer. It is already possible to produce special neuromorphic chips using conventional technology. However, these are still far from the energy efficiency of the brain. Here, the new technologies from resistive switching oxides, phase change materials or even 2D materials can take us much further. However, their use is always a question of industrial manufacturability. This varies from material to material, and it currently looks as if each generation of new materials will also bring a boost in efficiency. It is therefore very important to already be working closely on the two projects with manufacturers of material deposition systems such as Aixtron from Herzogenrath or deep tech start-ups such as Black Semiconductor or Aixscale Photonics.

In parallel, however, the Future Cluster is also working with industry at the higher levels of the value chain. Here, there are several start-ups in the region such as Clinomic Medical, Gremse-IT or a company co-founded by my RWTH Aachen colleague Prof. Rainer Leupers shortly after the NeuroSys launch. So, we are already working on all technology levels to realize the goals and are still in the acceleration phase after an excellent flying start!

More information:
www.neurotec.org
https://www.neurosys.info
Peter Grünberg Institut, Elektronische Materialien (PGI-7)
Forschungsschwerpunkt Neuromorphes Computing
https://www.eld.rwth-aachen.de/go/id/psfz/
Video: https://www.youtube.com/watch?v=tJghcXPby48

Contact person:

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Mini-Colloquium on Memristive Devices

—by Mike Schwarz

The ED Germany Chapter organized a hybrid Mini-Colloquium entitled "Memristive Devices" on 7 September 2022. It was held in the timeframe of the 6th Schottky Barrier Symposium on MOS Devices at the Competence Center for Nanotechnology and Photonics (NanoP) of THM-University of Applied Sciences. It was organized by the EDS Germany Chapter and co-sponsored by THM. The MQ was attended by 19 IEEE participants, as well as other non IEEE members.

The Organizing Committee (Prof. Kloes from THM, Prof. Calvet from CNRS, and Prof. Schwarz from THM) made a successful MQ possible and happen by inviting top level experts on various domains of memristive devices. Topics regarding technology towards simulation and modeling were targeted.

After a short welcome by Prof. Schwarz and Prof. Kloes with instructions, the session began with the lecture "Characterization of materials and devices at the nano/atomic-scale" by Prof. Mario Lanza from KAUST (SA). Prof. Lanza offered detailed insights on AFM methods and their challenges to be considered during the characterization of

Prof. Benjamin Iniguez introducing TMD memristors. The inset is showing Prof. Lanza during his AFM presentation

memristive materials. After the lecture a long discussion took place on various questions from the participants.

The feedback of both lecturers and participants was very positive to the organizers who planned for longer time slots to enable detailed discussion.

After a coffee break, the MQ was continued by Prof. Enrique Miranda from Universitat Autònoma de Barcelona (ES) with a talk entitled "Compact modeling of memristive devices for neuromorphic computing". First, Prof. Miranda introduced the newbies/rookies into the topic of memristive devices and went through different aspects of the compact modeling of the memristive devices. He showed details in static and dynamic modeling and their impact on the model IV characteristics in DC and time domains. Finally, he offered a SPICE compact model which allows for multiple crossbar array circuit simulation. Afterwards, discussion on the aspects, limitations and advantages took place.

The last point of the MQ was a talk by Prof. Benjamin Iniguez from Universitat Rovira i Virgili (ES) on "Challenges and solutions in compact modeling of TMD memristors". He started his lecture with an introduction and physical mechanisms in TMD memristors. Afterwards, Prof. Iniguez showed and reviewed modeling solutions and their results. Finally, he gave a conclusion and outlook of the status quo and where further solutions are required.

Finally, Prof. Schwarz closed the MQ and thanked all the speakers and participants for being part of this MQ and their contributions. Present attendees met afterwards for dinner in an old castle nearby the university.

6th Symposium on Schottky Barrier MOS (SB-MOS) devices

—by Mike Schwarz

The 6th Symposium on Schottky Barrier MOS (SB-MOS) devices was held on 8 September 2022 at the Competence Center for Nanotechnology and Photonics

at THM-University of Applied Sciences. It was organized by the EDS Germany Chapter and co-sponsored by THM. It was attended in hybrid form by approx. 50 participants. The Symposium was preceded by the MQ on "Memristive Devices" (see a more detailed article in this issue).

After a short welcome by Prof. Alexander Kloes with a detailed schedule, the presentations started with Prof. Richard Forbes from University of Surrey (UK). Prof. Forbes reported on "Apparent conceptual oversight in the statistical mechanics of the reverse-biased Schottky junction, and equivalent devices" with fundamental physics on Schottky junctions. He reported on what appears to be a fundamental oversight in the basic statistical mechanics of counting transfers of electrons across a boundary between different media. As physicist he encouraged scientists to be precise in their articles in wording on field emission, thermionic emission or more precisely thermal emission, etc. This message was acknowledged by the participants.

The next talk was given by Prof. Radu Sporea from University of Surrey on the topic "Contact-controlled TFT design addressing barrier-induced limitations". He offered that contact-controlled thin-film transistors are able to achieve superior gain, low-voltage saturation and uniform performance at the expense of switching speed and current density. Prof. Sporea showed that conventional TFT-oriented optimization strategies require adaptation when the contact properties dominate. He covered them systematically in this talk, alongside new insights into strategies for reducing temperature dependence. After the presentation a lot of discussions took place which allowed for a short coffee break. The discussions continued during the break.

Afterwards, in the talk "Prospects of SBMOS for cryogenic applications," Prof. Laurie Calvet from CNRS (FR) gave very interesting insights about experimental devices based on superconducting Schottky barriers also well known as Josephson junctions. She explained the history, challenges and improvements of those junctions targeting quantum computing applications. The participants were very interested in the topic and a lot of discussion took place after the presentation.

The Symposium continued with "SPICE compact modeling of amorphous oxide semiconductor memristive devices for memristive neural network," by Guilherme Carvalho, the PhD candidate from Universidade do Porto (P). He presented different experimental Mo/a-IGZO/Ti/Mo memristors and their capability by the device electrical characteristics, where he deposited the IGZO film by RF-magnetron co-sputtering from three binary ceramic targets. He matched the Dynamic Memdiode Model (DMM) from Prof. Enrique Miranda's group, which is well suited for SPICE simulation of hybrid CMOS-memristor circuits. Those results were benchmarked by simulating a single layer perceptron (SLP) circuit while classifying the handwritten images of the MNIST dataset, reaching an accuracy of ~90%.

Prof. Radu Sporea during the discussion on his presentation

The session was continued by the work of the PhD candidate Yiyi Yan from Université catholique de Louvain (BE) on the topic of "Hexagonal Boron Nitride Memristor Based on a NanogapSelf-Formed." Ms. Yan offered detailed process comics of the different steps she applied to manufacture her devices. Those were supported by optical images (TEM, SEM) of important steps, e.g. Pt silicidation or the wet transfer of CVD-grown-BN sheets. Impressive was the uniformity of the PtSi process as well as the impact of the various steps and changes onto the memristor device performance, which finally led to significant improvements.

After the lunch, PhD candidate Christian Römer from THM—University of Applied Sciences (DE) gave some new insight in "Compact Modeling of Injection Current and Channel-Resistance Effects in Reconfigurable Field-Effect Transistors". Christian showed the problem of describing the current-voltage characteristics of long channel Schottky barrier field-effect transistors. Namely, the resistance of the channel must be considered in the characteristics. He showed a closed-form and physics-based compact model that combines a Schottky-barrier injection with the current limiting effect of a channel resistance. The model demonstrated an excellent agreement with experimental data from NamLab.

Afterwards, Prof. Aníbal Pacheco-Sánchez from Universitat Autònoma de Barcelona (ES) continued on the topic of "Schottky barrier characterization of one-dimensional field-effect transistors." He introduced into the topic and offered a new approach for 1D devices by the Landauer-Büttiker approach, which led him to a 1D LBM (Landauer-Büttiker Model). Prof. Pacheco-Sánchez compared the model with the 3D AEM and offered a lot of results for the extracted Schottky barrier heights. During the discussion afterwards, the experts agreed that this model is helpful by extracting the Schottky barrier height of 1D devices.

The last presentation of the Symposium was given by Prof. Walter Weber from TU Vienna (AT) and entitled "Exploring the novel Al–Si_xGe_{1-x} Schottky FET system for the realization of functionality enhanced transistors, optoelectronics

and cryo-electronics." He referred to activities of the last decades on Silicon-Germanium and Aluminum material systems in microelectronics. Prof. Weber explained that by combining these materials in the form of geometrically confined nanowires and nanosheets, new types of junction formation processes have been recently discovered. It has been found that pure Al-Si nanometer-scale systems form atomically sharp Schottky, void-free and single crystal heterojunctions through a thermally driven material solid-state exchange reaction. The reliable Al-Si and Al–Si_xGe_{1-x} nano-junctions have been found to be promising for the realization of runtime reconfigurable transistors (RFETs) featuring electrically programmable n- and p-type polarity control due to their near midgap Fermi level pinning behavior. Pure Ge and Ge rich Si_xGe_{1-x} channels functionality can be further increased to feature tunable negative differential resistance (NDR) that can be exploited for oscillators and enhanced photodetectors. In addition, the high purity of the single-crystal Al formed by exchanging the Ge and Si_xGe_{1-x} layers allows superconductivity below the critical temperature of 1.46 K and the observation of supercurrents in Ge providing a promising device platform for cryogenic electronics. As before, also here a lot of discussion took place.

Prof. Laurie Calvet closed the Symposium with some final remarks that Schottky barrier junctions offer a wide spectrum of applications.

~Mike Schwarz, Editor

A Report on Student Activity to Celebrate 75th Anniversary of Transistors at ISBAT University, Kampala, Uganda, East Africa

—by Mayur Kumar Chhipa

On 12 October 2022 from 2:00pm to 3:00pm (GMT+3), a Student Activity was organized by Students from Department of Electronics and Communication Engineering, Computer Science Engineering, Faculty of ICT, ISBAT University, Kampala, Uganda during Orientation for Fresher's (Fall-2022) Semester.

It was the first such student activity, to encourage and motivate young students towards Electronics Engineering and STEM to their newly enrolled fresher's. An activity, where semester 3, 5 and 7 of Electronics and Communication Engineering and Computer Science Engineering students came together to prepare Poster Presentation about different types of Transistors and their History (Since 1947 to 2022).

Around 30 students were involved in Poster Presentation, 150 fresher students and 4 faculty members along with Dr. Pradeep Kumar, Director Academic Affairs, ISBAT University.

Please find below Student Guidelines for Poster Preparation, shared with them in advance to prepare the posters accordingly:

Transistor topics that were discussed:

1) BJT NPN
2) BJT PNP
3) FET and its types
4) N-channel JFET
5) P-channel JFET
6) N-channel MOSFET
7) P-channel MOSFET
8) FinFET
9) MESFET
10) UJT
11) Power MOSFET

Note:

1) Each topic was proposed to have 3 students discussing the following
   i) The history of the transistor, i.e. name of the inventor, place, and year of the invention,
   ii) Circuit diagram of each transistor,
   iii) Characteristics of each transistor (input and output of each characteristics),
   iv) Application of each transistor.
2) All participating groups were provided with all the necessities to be used in their presentation, such as sketch pens and poster paper, etc.

Please find below the Program Schedule of the Orientation Program for Freshers:

ISBAT UNIVERSITY
A CHARTERED UNIVERSITY

Orientation Program for Freshers

Wednesday, 12 October 2022 between 9:30am–4:30pm
Venue: 7th Floor, Auditorium

9:00–10:05	Registration
10:00–10:05	National Anthem (East Africa and Uganda)
10:05–10:10	Prayer
10:10–10:20	Welcome Speech by Prof. K. M. Mathew – Vice Chancellor
10:20–10:30	Address by Special Guest Mr. Luis Lechiguero – Program Manager, Delegation of European Union to Uganda
10:30–11:00	Blended Learning A Talk by Dr. Pradeep Kumar - DAA
11:00–11:30	Address by Chief Guest – Dr. Isabel Sarabia Andugar, Vice Dean, UCAM, Spain
11:35–11:40	National Anthem (Uganda and East Africa)
11:45–12:20	Academic calendar and activities by Dr. Giju Paul – Academic Registrar
12:20–12:55	Briefing on ERP/LMS by Mr. Manjesh Thomas – Head QA
12:55–1:00	Briefing by Guild

1:00–1:30	Health break
1:30–2:00	Briefing by Librarian
2:00–3:00	Student activity to celebrate 75th Anniversary of Transistor
3:00–4:00	Institute by Heartfulness Institute Uganda
4:00–4:30	Departmental Briefing by the respective Deans
4:30	Disperse

Please find below some glimpse of the Celebration:

Transistors 75th Anniversary: Posters Preparation by Students

Transistors 75th Anniversary: Celebration attended by newly joined Fresher's (Fall-2022)

Mayur Kumar Chhipa
Convener, Transistor 75th Anniversary Celebration
ISBAT University, Kampala, Uganda

Asia & Pacific (Region 10)

ED/SSC Hong Kong Chapter

—by Yansong Yang

On 8 July 2022, the IEEE Hong Kong Joint Chapter of Electron Devices and Solid-State Circuits (ED/SSC) hosted a distinguished seminar given by Prof. Shimeng Yu, an associate professor of electrical and computer engineering at Georgia Institute of Technology. The title of his lecture was "Recent Progresses on Ferroelectric Devices and Applications to Compute-in-Memory." Prof. Yu presented the recent progresses on doped HfO_2-based ferroelectric devices, including the fundamental device physics, machine learning-assisted predictive modeling framework, computer-in-memory for deep neural network acceleration, and 3D NAND architecture based on FeFET for ultra-large-scale machine learning.

Shimeng Yu, Anirban Bandyopadhyay, and Xueyue Zhang

On 29 July 2022, the Chapter hosted a distinguished seminar given by Dr. Anirban Bandyopadhyay (IEEE Fellow), the senior director and head of Strategic Applications within the Mobility & Wireless Infrastructure Business Unit of GlobalFoundries, USA. The title of his lecture was "Differentiated Silicon Technologies to enable next-generation 5G and 6G radio". The emergence of enhanced mobile broadband (eMBB) connectivity based on mmWave 5G generated huge interest in the entire telecommunication ecosystem. Dr. Bandyopadhyay introduced the challenges in the emergence of mmWave 5G mobile broadband connectivity, including the coverage, transmitted power efficiency, system cost, and scaling and long-term reliability of the hardware system. Dr. Bandyopadhyay mentioned that the carrier frequencies will go even higher than 100 GHz, particularly for D-band (120-160GHz) applications in both communication and sensing. As the representative of GlobalFoundries, Dr. Bandyopadhyay also introduced the recent research directions in GaN-based power devices, which our chapter members are interested in.

In addition to the distinguished seminar given by senior EDS members, the HK EDS chapter also invited junior researchers to give talks. On 2 September 2022, Ms. Xueyue Zhang, a PhD candidate in Applied Physics at Caltech, gave a talk on "A Scalable Superconducting Quantum Architecture with Long-range Connectivity". Ms. Xueyue Zhang discussed utilizing photon-mediated interaction to address the limitations in quantum computations. Several state-of-the-art works from her group were introduced.

The IEEE Hong Kong Joint Chapter of Electron Devices and Solid-State Circuits (ED/SSC) plans to participate in HKUST Industry Engagement Day, which is a flagship event in Hong Kong and is expected to attract over 400 senior or middle management-level audiences from the industry and government. This is an excellent occasion to promote the achievements of our EDS chapter members in public.

The IEEE ED/SSC Hong Kong Chapter is also working on organizing the 2023 IEEE Student Symposium on Electron Devices and Solid-State Circuits. This symposium encourages undergraduate and postgraduate students who are working on, or have an interest in the field of electron devices to present their results and exchange ideas with peers and senior researchers in the community.

EDS Kansai Chapter

—by Yuichi Ando

VLSI Symposium Report Meeting

VLSI Symposium Report Meeting was held on 20 July 2022. The meeting was a joint event with SSCS Japan Chapter, SSCS Kansai Chapter, and EDS Japan Chapter. A total of 16 papers covering a wide range of topics such as electronic devices and circuits in the VLSI Symposium were presented. The 172 attendees, including 132 IEEE members enjoyed the insightful sharing.

Kansai Colloquium Electron Devices Workshop

The Colloquium of EDS Kansai Chapter was held on-line on 7 October 2022. EDSK Technical Committee members carefully reviewed papers published in the past year at various prestigious conferences and in technical journals, such as IEDM, SSDM, and IEEE Transactions, and nine papers from authors in the Kansai area invited to this workshop. The award committee selected one paper for the Best Paper Award and one paper for the Student Best Paper Award. Thirty attendees, including fifteen EDS members, enjoyed the interesting talks.

2022 International Meeting for Future of Electron Devices (IMFEDK):

IMFEDK 2022 will be held on 28-30 November 2022 in Kyoto. IMFEDK was established by IEEE EDS Kansai Chapter in 2000, with over 20 years of history. In this period, many latest topics in a wide range of fields related to electronic devices (Silicon, Compound, Emerging devices, circuits, Industrial, MEMS, sensors, etc.) were presented. IMFEDK has been giving scientists chances to disseminate their research results and young engineers & university students the opportunity to grow on their own. Several prominent speakers will present 2 keynote speeches, 13 Invited talks, and 3 special session speeches in IMFEDK2022. Also, 15 oral and 21 poster presentations will be shown. Please refer to the following website for more details: https://www.ieee-jp.org/section/kansai/chapter/eds/imfedk/

~Tuo-Hung (Alex) Hou, Editor

ED Delhi Section Chapter

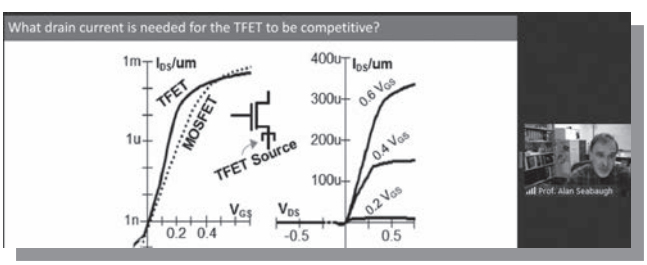
—by Harsupreet Kaur and Manoj Saxena

The ED Delhi Chapter, DBT Star College Status Program, Deen Dayal Upadhyaya College, University of Delhi and The National Academy of Sciences India – Delhi Chapter jointly organized a Virtual Mini-Colloquia (MQ) on "Emerging Device Architectures for Tunnel FET" as part of the commemoration of "75th Anniversary of Transistor Invention" during 26 September 2022 to 5 October 2022.

- 26 September 2022—Professor Alan Seabaugh, Department of Electrical Engineering, Notre Dame Nanoscience and Technology on the topic "Steep transistors for low voltage computing."
- 27 September 2022—a talk on "Highly repeatable room temperature negative differential resistance in AlN/GaN resonant tunneling diodes with Unipolar Light Emission" was delivered by Prof. Paul R. Berger, Ohio State University.
- 29 September 2022—Prof. Elena Gnani, University of Bologna, Bologna, Italy gave a DL talk on "Tunnel FETs: Device Physics and Realizations."
- 30 September 2022—A Distinguished Lecture (DL) "Trends and Challenges in Micro- and Nanoelectronics for the Next Decade," was delivered by Professor Cor Claeys, Fellow IEEE, Past President IEEE EDS (2008-2009), Fellow ECS, Leuven, Belgium.
- 4 October 2022, a DL talk entitled "Energy efficient 2D Tunnel FET and FET switches for co-integration of Von-Neumann and neuromorphic integrated circuits and applications" was delivered by Professor Adrian M. Ionescu, Nanolab, Ecole Polytechnique Fédérale de lausanne (EPFL), Switzerland
- The concluding DL talk of the MQ was held 5 October 2022 on the topic "Device Engineering for Nano electronics and Nanosystems in the Energy and Variability Efficient (E.V.E.) Era, which was delivered by S. Deleonibus, Fellow IEEE, Emeritus Fellow Electrochemical Society, CEA Research Director Secretary IEEE Electron Devices Society (2016-2017).

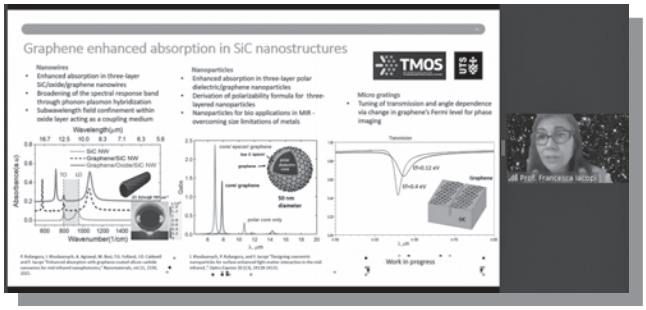
There were 183 participants (IEEE: 43 and Non-IEEE: 140) at the MQ traveling from Bangladesh, Brazil, China, Croatia, Finland, Germany, Hong Kong SAR, India, Italy, Japan, Kazakhstan, Korea, Republic of Mexico, Nepal, Netherlands, Serbia, Spain, Taiwan and the United States.

To commemorate the Centenary Celebration of Delhi University and 75th Anniversary of the Transistor Invention, the Department of Electronic Science, University of Delhi South Campus in collaboration with Training and



Professor Seabaugh delivering his distinguished lecture

Organizing committee and participants



Professor Francesca Iacopi delivery her Distinguished Lecture online

Placement Cell, Maharaja Agrasen College, University of Delhi and supported by IEEE Electron Devices Society Delhi Chapter organized One Week Hands-on Faculty Development Program (Online-Self Paced) on "Python Programming for Electronics." The resource person for this program was Ms. Arzoo Sabharwal (Data Scientist, IBM) and the workshop was designed according to National Educational Policy (NEP-2020) to provide exposure to Python Programming. The workshop was attended by over 45 participants including 10 IEEE members.

The ED Delhi Chapter, Department of Electronic Science (University of Delhi, India), DBT Star College Status Program of Deen Dayal Upadhyaya College (University of Delhi, India) and the National Academy of Sciences India—Delhi Chapter jointly organized a hybrid Mini-Colloquia (MQ) on "History, Prospect and Future of Graphene based Devices and Systems," as part of the commemoration of 75th Anniversary of Transistor Invention.

1) The first talk was delivered 11 October 2022 by Professor Cary Y. Yang, Formerly President of IEEE EDS & Director, TENT Laboratory, Santa Clara University, on the topic "3D Nanocarbon Interconnects."
2) 14 October 2022—"Compact modeling of 2D semiconductor Field Effect Transistors" was given by Professor Benjamin Iniguez, University Rovira i Virgili.
3) 15 October 2022, an in-person DL on "In-Memory Computing Circuits Using Multi Level Spin Memories" was delivered by Professor Brajesh Kumar Kaushik, Department of ECE, IIT-Roorkee, Roorkee, India
4) 18 October 2022, the fourth DL on "Graphene for Transistors, Optical Neuromorphic and Neurorobotics" was given by Prof. Chao-Sung Lai, Senior Member, IEEE, Department of Electronic Engineering, Chang Gung University, Taiwan.
5) 19 October 2022, the DL on "Complementing silicon technologies with graphene for More-than-Moore applications" was presented by Prof. Francesca Iacopi, Professor of Nanoelectronics and Nanophotonics, School of Electrical and Data Engineering, Faculty of Engineering & IT, University of Technology Sydney, Australia
6) A DL on "Fundamentals and recent advances in electronic and plasmonic terahertz devices utilizing graphene-based 2D materials" by Taiichi Otsuji, Dr. Eng., Professor, Research Institute of Electrical Communication, Tohoku University, Sendai, Japan
7) The concluding DL on "Unconventional Applications of Graphene in Electronic Tattoos and Biosensor Technologies" by Professor Deji Akinwande, The University of Texas was held on 10 October 2022.

The Hybrid MQ was attended by 189 delegates from Bangladesh, China, France, Hong Kong SAR, India, Italy, Saudi Arabia, Serbia, Taiwan and the United States.

On 15 October 2022, an in-person research conclave for research scholars of the Department of Electronic Science, University of Delhi was organized. The conclave aimed to bring together Ph.D. students working in areas of "Electronics Devices & IOT" and "Material Science and Technology." Over 30 oral presentations were judged by external experts from IIT, Delhi Technological University, National Physical Laboratory (NPL, New Delhi, India) and the first and the second prizes were given in each of the four parallel sessions. Over 50 delegates attended the Research Conclave. The presentations were focused on small-signal equivalent circuit modeling for large gate

Participants and judges during one of the sessions of the research conclave

Organizing committee and participants of in-person Training Program on New Measurement Technologies & Simulation Techniques in Electronics

IEEE EDS Summer School: Samadrita Das (Chair, from left), Dr. M. Kavicharan, Prof. S. K. Tripathy, Prof. Brinda Bhowmick, Prof. T. R. Lenka, Chapter Advisor, Prof. Koushik Guha, Secretary, NTC (right), and Student Members of PhD, PG and UG

periphery GaN HEMT; Designing and modeling of biosensor and hydrogen gas sensor using Junctionless FinFET; Ga_2O_3 MOSFETs for high power applications; Synthesis of 2D materials, etc.

During 17–18 October 2022, an in-person Training Program on New Measurement Technologies & Simulation Techniques in Electronics was organized. The program covered the ADS-Keysight training program along with RF & Microwave Fundamentals; Parametric analyser (DC IV, PULSE IV, Transient and CV Measurement) and Vector network analyser. The Program was attended by 54 PG students, Research Scholars and Faculty members from 16 different Institutions of Delhi/NCR.

ED National Institute of Technology—Silchar Student Branch Chapter

—by T.R.Lenka

The Chapter in association with IEEE Nanotechnology Council Chapter, and the Department of Electronics and Communication Engineering, National Institute of Technology Silchar organized the IEEE EDS Summer School on "Recent Trends in Micro/Nanoelectronics Devices" from 20–24 August 2022 in hybrid mode. The Distinguished Lecturers, namely, Dr. Wladek Grabinski (MOS-AK, EU), Dr. Roberto S. Murphy Arteaga (INAOE, Mexico), Prof. Adelmo Ortiz-Conde (USB, Venezuela), Prof. G. N. Dash (Sambalpur University, India), Prof. Ajit Panda (ECOE, Bhubaneswar, India), Prof. Gilson I. Wirth (UFRGS - Universidade Federal do Rio Grande do Sul, Brazil), Prof. Jacobus W. Swart (State University of Campinas, Brazil), Prof. Joao Antonio Martino (University of Sao Paulo, Brazil), Prof. Vikram L. Dalal (Iowa State University, USA), Prof. Marcelo Antonio Pavanello (Centro Universitario FEI, Sao Bernardo do Campo - Brazil) delivered the distinguished lectures on state-of-the art emerging research on Micro/Nanoelectronics Devices and their applications.

In addition, the following invited speakers delivered technical talks at the summer school: Prof. Hieu Pham Trung Nguyen (NJIT, USA), Prof. Koushik Guha (NIT Silchar), Prof. Brinda Bhowmick (NIT Silchar), Prof. Kumar Prasannajit Pradhan (IIITDM, Chennai).

Prof. T. R. Lenka (NIT Silchar) delivered a talk on "*75th Anniversary of Transistor*" at the summer school. Around 60 participants consisting of faculty, students (EDS member and non-member) from all areas of India attended and successfully completed the EDS Summer School.

Panimalar Institute of Technology—Chennai, ED Student Branch Chapter

—by Preethi Gandhi G S

The Chapter organized many activities for the benefits of the students of the institution. The activities were primarily organized by the ED Student Branch Chapter in association with other IEEE chapters and technical associations. The Chapter organized a "Webinar on Global Networking with IEEE Collabratec" on 25 September 2022. The session was carried out by Mr. Pavan Gowda.R, Customer Experience Engineer at Dell Technologies. The speaker discussed the usage of IEEE Col-

"Getting Started with AI/ML as a Beginner," by Mr. Neavil Porus

Robotics Workshop at the Heritage Institute of Technology, Kolkata

A Technical Talk at the Heritage Institute of Technology, Kolkata

labratec, advantages of using it, handling of accounts in IEEE Collabratec.

The Chapter organized a webinar on the topic "Joy of Volunteering with IEEE." The session was held on 10 October 2022. The speaker, Mr. Mallellu Sai Prashanth, IEEE Education Society Representative to IEEE Young Professionals Committee. The speaker shared the benefits of IEEE membership. Nearly 40 participants from various educational institutions attended the session.

The Chapter organized a technical talk on the topic Getting Started with AI/ML as a Beginner. The speaker was Mr. Neavil Porus, Machine Learning Alumnus-Batch 2020, Cognizance, IIT Roorkee. The fundamental algorithms of machine learning were explained. Nearly 40 participants from various Educational Institutions attended the session.

ED Heritage Institute of Technology Student Branch Chapter and IEEE EDS Center of Excellence

—by Atanu Kundu

The Robotics Club of Heritage Institute of Technology, Kolkata (HITK), in collaboration with the IEEE EDS Center of Excellence and IEEE EDS Student Branch Chapter, HITK organized 'MAZERUNNER' a Robotics competition on 23 September 2022, at the HITK campus. The event hosted 47 teams consisting of 133 participants from various departments of the Institute. The students prepared their robots with great enthusiasm and tested their technical zeal while racing down the challenging maze. The team 'Omega' emerged as the winner followed by the team 'Three-bit' and the team 'Phoenix' as first runner-up and second runner-up respectively.

The Chapter also organized a very similar kind of workshop, entitled "BUILD-A-BOT 101"on 1 June 2022.

A technical talk on the topic, 'Quantum wire metal-oxide-semiconductor (QW-MOS) structures for developing the Voltage Tunable Quantum Dots (VTQDs)' was held on 28 September 2022 at the IEEE EDS Center of Excellence, Heritage Institute of Technology. The lecture was delivered by Prof. Sanatan Chattopadhyay, Department of Electronic Science, University of Calcutta. The lecture discussed the basics of quantum dots and how voltage tunability is interesting and useful.

ED Nepal Chapter—Uttar Pradesh Section Chapter

—by Rajendra Parajuli

The Chapter organized a technical talk "Effect of B, N & C sites vacancy defects in (G/h-BN) HS of 2D materials" on 26 August 2022, at the Central Department of Physics, Tribhuvan University, Kirtipur, Kathmandu, Nepal. Professor Hari Krishna Neupane, Asst Prof. Amrit Campus, Tribhuvan University was the speaker.

The Chapter in association with the Department of Physics, Amrit Campus, Tribhuvan University, Kathmandu, Nepal, organized a two-day National Conference on

Technical talk on "Effect of B, N & C sites vacancy defects in (G/h-BN) HS of 2D materials" on 26 August 2022

National Conference on Advances in Atmospheric and Material Science

Advances in Atmospheric and Material Science. The conference was held 6–7 November 2022. It was supported by the International Science Program, Uppsala University, Sweden, the Nepal Physical Society (NPS) and the Nepalese Society for Women in Physics. The conference was attended by about 68 participants from different parts of Nepal. Among them, there were 10 IEEE members.

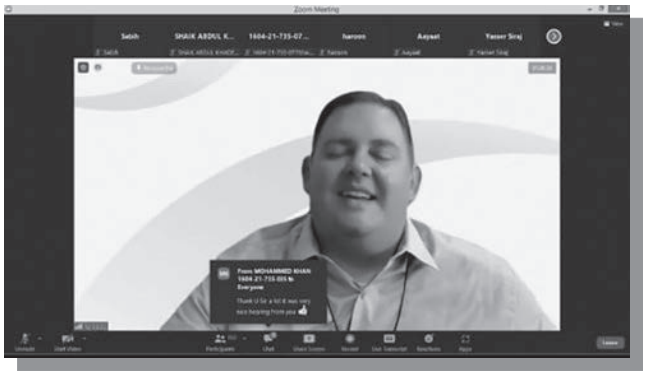
There were two keynote lectures given by Prof. Dr. Bhadra Pokhrel, past president of IEEE/ED Nepal Chapter, and Prof. Dr. Ram Prasad Regmi, faculty at Tribhuvan University. There were also two invited talks by Dr. Sanju Shrestha, Treasurer of IEEE/EDS Nepal Chapter, and Dr. Hom Bahadur Baniya, faculty at Tribhuvan University. Apart from these, there were 21 contributory oral presentations and 13 posters.

ED Muffakhamjah College of Engineering & Technology Student Branch Chapter

—by Maliha Naaz

The Chapter organized on 25 July 2022 a webinar on 'Wireless Power Transmission' by Ky Sealy, WiTricity Engineering Fellow. The speaker shared his knowledge on the various wireless power transmission technologies.

The Chapter also organized an induction program on 5 November 2022 for the fresh students, motivating them to become IEEE members.



Webinar on Wireless Power Transmission by Ky Sealy

ED Calcutta University of Technology Student Branch Chapter

—by Koyel Mukherjee, Apabrita Sengupta and Soumya Pandit

The Chapter was revived with active participation by the newly constituted executive committee members. The Chapter took active part in organizing STEX'22 on 27 September 2022 at the Institute of Radio Physics and Electronics, University of Calcutta. The program was organized jointly with the IEEE Photonics Society Student Branch Chapter. It was an exhibition cum competition of Models on Science and Technology. The students of different colleges and universities were invited and they participated to exhibit their sophisticated models in this event. There were thirteen models presented by students (not more than five students per model) of Institutions like Institute of Engineering and Management, Heritage Institute of Technology, Supreme Institute of Management and Technology and University of Calcutta. The models were open for exhibition and were evaluated by two judges. The best three models were awarded with trophies and certificates.

The winning team exhibited a model on "INJECTABLE STIMULI RESPONSIVE RAFT POLYMERIZED SMART HYDROGEL FOR PHOTODYNAMIC THERAPY OF CANCER." The team was a group of 4 students from the Department of Polymer Science and Technology, University of Calcutta. The second prize was awarded to a group from Institute of Radio Physics and Electronics, University of Calcutta and the third prize was also awarded to another group from Institute of Radio Physics and Electronics, University of Calcutta. Certificates were distributed to all the

Few moments of STEX 2022

registered participants who exhibited their models as well as to the volunteers who were involved in this program. The full enthusiasm of the hosting and participating students throughout the day reflected the grand success of the event.

ED Malaysia Kuala Lumpur Chapter Electronics in Coding & Robotics STEM Program

—by Hasnizah Idris, P Susthitha Menon, Ahmad Sabirin Zoolfakar

A Train the Trainer Session for the Electronics in Coding and Robotics STEM programme was held on the 5 September at the Institute of Microengineering and Nanoelectronics (IMEN), Universiti Kebangsaan Malaysia (UKM) by STEM Champion 2022; Assoc Prof Dr. P Susthitha Menon. The session was attended by 6 lecturers from the Faculty of Electronic Engineering & Technology, Universiti Malaysia Perlis (UniMAP). The lecturers were trained to use the Electronic Blocks with Coding, Tobbie II robot and SolarBot kits.

Eventually, a Train the Student STEM session was held at Sekolah Tengku Budriah (STB), Arau Perlis on 1 October 2022. This event was conducted in collaboration between FEET UNIMAP, IEEE EDS Malaysia, IEEE Sensors & Nanotechnology Council Malaysia Joint Chapter (SNCMJC) and STEM Club, Sekolah Tengku Budriah (STB). This half-day program was attended by a total of 32 students from Sekolah Kebangsaan Tengku Budriah, Arau. Thirteen (13) academic staff from the Faculty of Electronic Engineering & Technology, Universiti Malaysia Perlis (UniMAP) and two (2) teachers from the school's STEM Club have conducted the program. All educational kits were provided by IEEE EDS Malaysia and they're including 1) Tobbie II Robot which uses micro:bit programmable board and Microsoft MakeCoder Editor or Phyton Editor for coding and 2) Snap Circuits with coding (using Bluetooth-powered SC controller and enabled via app-driven BOTcode and Blockly codes).

Report on the 15th IEEE-International Conference on Semiconductor Electronics (ICSE 2022)

—by Nurul Ezaila Alias, P Susthitha Menon, Ahmad Sabirin Zoolfakar

The 2022 IEEE International Conference on Semiconductor Electronics (ICSE2022) was successfully held online from 15-17 August 2022 via Webex. The conference was organized by IEEE Electron Devices Malaysia Chapter and IEEE Malaysia Section. ICSE2022 was chaired by IEEE EDS Chair, Assoc. Prof. Ir Ts Dr. Ahmad Sabirin Zoolfakar from UiTM Shah Alam and Technical Chair was Ts Dr. Nurul Ezaila Alias from UTM Johor. There were 42 papers presented at the conference with more than 50 participants attending from around the world.

ICSE2022 was proud to feature Prof. Koichi Sasaki from Hokkaido University, Japan, Prof. Lung-Chien Chen from National Taipei University of Technology, Taiwan and Assoc. Prof. Dr. P. Susthitha Menon from Universiti Kebangsaan Malaysia, Malaysia as the keynote speaker.

Train the Trainer Session at IMEN UKM and Train the Student STEM Session at STB Arau Perlis

Results of the Best paper/best presenter awards are as follows:

Best paper Cluster 1: MEMS & Nanoelectronics	"*Electrochemistry of Green Ag Nanoparticles Modified Electrode Surface*" by Yasmin Abdul Wahab et al, Universiti Malaya
Best paper Cluster 2: Nanophotonics	"*Analysis and Design of an Efficient and Wideband Common Collector Class B Amplifier for Auxiliary Envelope Tracking Supply Modulator*" by Zubaida Yusoff et al., Malaysia Multimedia University
Best paper Cluster 3: IC Design And Manufacturing	"*Enhancement of Film Uniformity by Controlling Solution Viscosity on Fabrication of Silsesquioxane Thin Films*" by Mat Tarmizi et al, SIRIM Berhad, Malaysia
Best paper Cluster 4: Material, Process & Product	"*Investigation of Hybrid Graphene-hBN and Graphene-GO as a Direct Contact Heat Spreader*" by Nur Julia Nazim Bulya Nazim et al., Universiti Teknologi Malaysia & MIMOS Semiconductor Sdn Bhd, Malaysia
Best paper Special Cluster	"*Die-Level Defects Classification using Region-based Convolutional Neural Network*" by Usman Ullah Sheikh et al., Universiti Teknologi Malaysia
Best Paper Award EDS	"*Investigation of Hybrid Graphene-hBN and Graphene-GO as a Direct Contact Heat Spreader*" by Nur Julia Nazim Bulya Nazim et al., Universiti Teknologi Malaysia & MIMOS Semiconductor Sdn Bhd, Malaysia
Best Paper Award IET Malaysia	"*Enhancement of Film Uniformity by Controlling Solution Viscosity on Fabrication of Silsesquioxane Thin Films*" by Mat Tarmizi et al, SIRIM Berhad, Malaysia
Best Presenter Award	"*Performance Analysis of Junctionless Multi Bridge Channel FET with Strained SiGe Application*", Syafizah Afidah Affandi, Universiti Teknologi Malaysia

Prof. Koichi Sasaki from Hokkaido University (Keynote title: Contribution of excited states of molecular nitrogen to surface reactions in nitrogen plasmas), Prof. Lung-Chien Chen from National Taipei University of Technology (Keynote title: Properties and sensing applications of $MA_3Sb_2Br_9$ bulk crystals and $(PEA)_2(MA)_3Sb_2Br_9$ thin films) and Assoc. Prof. Dr. P. Susthitha Menon from Universiti Kebangsaan Malaysia (Keynote title: Plasmonics in Biosensors and Electronic Devices. This is the 15th conference in the ICSE series since 1992 which aims at bringing together researchers from industry and academia to gather and explore various issues and trends in the field of semiconductor electronics.

Else than that, for the first time, the conference featured a pre-recorded Women in Electron Devices (WiEDS) and Young Professionals (YP) session which was aired during the lunch break of the conference. The session was moderated by WiEDS Chair, Assoc Prof. Dr. P Susthitha Menon from UKM and welcoming remarks were given by EDS Malaysia Chapter Chair, Assoc. Prof. Ir Ts Dr. Ahmad Sabirin Zoolfakar from UiTM Shah Alam. The session, which featured 3 prominent speakers; Ir Bernard Lim from EDS Penang Joint Chapter, Ir Ts Dr. Nurul Ezaila Alias from UTM Johor and Assoc. Prof. Dr. Rosminazuin Ab Bakar from IIUM, was entitled Career Growth via Professional Networking. The speakers shared their experiences on how their involvement in professional organizations such as IEEE EDS sparked their personal and career growth in an exponential way. The recording of the event can be viewed on YouTube: https://youtu.be/2ke2rShXO4o

ICSE2022 offered Invited Papers to academicians and researchers from the industry for every track session, Best Paper Award for each cluster, and the Best Presenter Award to student presenters. ICSE2022 is also pleased to offer 2 special awards which are the Best Paper Award EDS and Best Paper Award IET Malaysia. This time around, we are honored to receive a sponsor from the IET, Malaysia. Altogether ICSE2022 had 6 track sessions, therefore, 6 invited papers were offered to the academicians and researchers from the industry to present their work as invited speakers for the respective track session. The Best Paper Awards were accorded based on 4 main clusters and 1 special cluster and all the papers were evaluated by the Technical Program Committee. The Best Presenter Award to the student was evaluated by the session chairs. Overall, the conference achieved its main objective of bringing together researchers from industry and academia to gather and explore various issues and trends in the field of semiconductor electronics.

~Sharma Rao Balakrishnan, Editor

—Report by the organizing committee: by Arokia Nathan, Xiaojun Guo, Hanbin Ma, Kai Wang, Di Geng, Sanjiv Sambandan, Chen Jiang, Slobodan Mijalkovic, Radu Sporea, Jun Yu, Samar Saha, Benjamin Iniguez, Yvan Bonnassieux, Yukun Huang, and Wei Tang

The General and Technical Program Chairs are pleased to report a successful 2022 IEEE International Conference on Computer-Aided Design for Thin Film Transistor Technologies (CAD-TFT). This EDS technically sponsored conference was dedicated to computer-aided-design (CAD) of thin-film transistor (TFT) technologies for displays, sensors, and in general large area or flexible electronics systems. Computer-aided-design techniques at all levels have become increasingly important for the TFT community to connect device technologies with manufacturing, for circuits & systems. This CAD-TFT annual conference provided the needed forum for engineers and scientists to get together and promote research on CAD techniques at all levels for TFT technologies and new applications, train students, young researchers and engineers, and very importantly, build international, academic-industry, and cross-level collaborations.

CAD-TFT was a rich two-day hybrid program of oral presentations given by prominent multi-disciplinary experts in areas related to: device physics of TFTs and operating principles; compact TFT device models for circuit simulation; model implementation and circuit analysis techniques; model parameter extraction techniques; TFT design for displays and emerging applications, including flexible electronics; and TCAD including materials and processing.

CAD-TFT 2022 was 14th in the series with previous workshops/conferences and their evolution as follows:

2006—Started in Cambridge, UK as Workshop on Compact TFT Modeling for Circuit Simulation
2008—Continued in Cambridge, UK
2009 in London, UK
2010 in Tarragona
2012 in Cambridge
2013 in Grenoble
2014 in Nanjing re-branded as Int Conf on CAD for TFT Technologies
2016 in Beijing continuing as CAD-TFT Conf
2017 in Cambridge, UK
2018 in Shenzhen, China
2019 in Tarragona, Spain
2020 in Tianjin, China
2021 in Cambridge, UK
2022 in Shandong, China

CAD-TFT offered a rich two-day hybrid program of 21 talks covering various aspects of TFTs together with an embedded Mini-Colloquium to commemorate the 75th Anniversary of the Invention of the Transistor, "Can sub-6nm node meet 6G?"

There will be a Special Issue comprising full-scale journal papers of oral presentations made at the conference that will be published in IEEE's J-EDS. Submissions subject to IEEE's standard review process.

The organizing committee is highly appreciative of the major support of the local team in Qingdao and support teams from CAS and ACXEL at Suzhou and

Professor Jamal Deen, McMaster University, Canada, delivering one of the opening talks

On-site participants of the IEEE EDS 2022 CAD-TFT Conference

Foshan, respectively, sponsors and local municipal Govt of Qingdao, Shandong University and School of Information Sciences. Very importantly, we thank the speakers and participants for making CAD-TFT a success! We thank the financial sponsors for their generous support (list of sponsors shown below) and we look forward to seeing you, whether in real or virtual form, in San Jose, where CAD-TFT will be co-located with IFETC 2023, 14–16 August.

Hosted by the IEEE EDS Beijing Section Chapter at Shandong University, Qingdao, China, 20 August 2022

Arokia Nathan, Darwin College, Cambridge University, UK

In commemoration of the 75th Anniversary of the Invention of the Transistor, the IEEE Electron Devices Beijing Chapter held a mini colloquium (MQ) entitled, "Can the sub-6nm node meet 6G?" The MQ was a half-day hybrid event co-located between the CAD-TFT 2022 (http://cad-tft.org) and IFETC 2022 (https://attend.ieee.org/ifetc-2022/) conferences. The MQ hosted a broad range of topics representing the multi-disciplinary nature of the emerging GHz devices and circuits and millimeter-wave (mmWave) applications.

The silicon integrated circuit (IC) continues to have an unprecedented impact on every aspect of modern society, ranging from communications and security to healthcare and industrial automation. Over the last five decades, the relentless pursuit of IC device miniaturization for manufacturing high-performance and high-density very large scale integrated (VLSI) circuits and systems has led to the creation of a digital society. Operating speeds continue to be pushed to increasingly higher and higher frequencies enabling baseband operation in mobile devices in the 30 GHz vicinity, which is expected to provide more bandwidth and lower latency. Millimeter-wave communications will soon become part of the 5G/6G standards, alongside developments to push communications to the THz bands. The availability of bandwidth at these frequencies will offer a multitude of opportunities to increase throughput of a new generation of wireless networks. Although this area of research is relatively new, we witness a tremendous growth in the literature related to the electromagnetic properties of mmWave communications, and in particular, free space propagation loss and its susceptibility to hindrances.

The MQ presented a forum for engineers and scientists to discuss these issues and hear recent developments from experts in areas ranging from transistors and integrated circuits to antennas & propagation and communication networks, along with challenges faced in design of 6G transceiver systems and networks.

The MQ extended over multiple time zones with speakers spanning San Jose, California, USA to Shanghai, China. The opening speaker was Patrick Fay, IEEE Fellow, from University of Notre Dame, USA, whose presentation, High Performance III-N Devices for 6G and Beyond, highlighted the significant advancements needed in device technologies to meet the promise of 6G and beyond. He underscored the unique properties of the III-N material system which enable new approaches for designing mmWave transistors for power amplifiers, low-noise amplifiers, and signal switching and routing. This was followed by a highly informative lecture, Differentiated Silicon Technologies to Enable 6G Radio, by Anirban Bandyopadhyay, FIEEE from Global Foundries Inc, CA, USA. His talk focused on the hardware challenges for mmwave and subTHz radio, and the performance limits of semiconductor technologies particularly CMOS over process nodes. He drew special attention on how silicon technologies based on differentiated partially and fully depleted SOI (PDSOI & FDSOI) and SiGe technologies can address the hardware challenges of integrated radio for mmWave performance and reliability. Samar Saha, FIEEE, from Prospicient Devices, CA, USA, followed with a detailed historical account, The Invention that Changed the World: Evolution of Transistors Enabling Digital Ecosystem, drawing attention to how progress in modern society has evolved from the point contact transistor to the relentless pursuit of transistor device technologies at the 6-nanometer nodes and beyond. His talk overviewed the continuous evolution of the IC device structure and manufacturing technology that will enable 6G wireless communications networks. The next speaker was Albert Wang, FIEEE, University of California at Riverside, replacing Yogesh who had a last-minute scheduling conflict. Albert's address was on electrostatic discharge (ESD); the all-important hazard to ICs. His lecture, ESD-RFIC Co-Design: From RF to mm-Wave, reviewed various practical ESD protection design techniques focusing on high-frequency ICs for wireless systems. He highlighted key design considerations in RF ESD protection and the impact of ESD on RFIC co-design.

The MQ slightly switched gears with the next three lectures on communications and related circuits.

In-person attendees of the hybrid MQ, Can the sub-6nm node meet 6G, in commemoration of the 75th Anniversary of the Invention of the Transistor

Xuyang Lu from the Shanghai Jiao Tong University, China gave a presentation, Integrated Phased Array sub-THz Transceivers for 6G Communication, emphasizing how advances in nanofabrication have enabled more effective tools for communication in the mmWave and THz frequency regimes. He shared some novel architectures of integrated beamforming methods to improve the efficiency of THz phased array communication. This was followed by Chong Han, Shanghai Jiao Tong University, China, whose lecture, Terahertz Communications for 6G and Beyond: Challenges, Advances and Future Directions, gave a comprehensive overview of cutting-edge THz communications strategies for 6G wireless networks and beyond. He identified and discussed the outstanding barriers that future wireless system designers must tackle to reap the full benefits of THz communications in the 6G and beyond era. Diving deeper into telecommunication circuits was Jagadheswaran Rajendran of the University Science Malaysia, Penang. His lecture, CMOS Power Amplifiers and VCO Design Perspectives for 6G Wireless Communication, introduced case studies of various design techniques for power amplifiers and voltage-controlled oscillators, linearizers, matching networks, varactor tuning with enhanced negative resistance and inductive tuning and indirect varactor tuning, concluding with emerging materials for THz amplifiers into the next decade.

The final two talks covered heterogeneous ICs and reconfigurable intelligent surfaces for 6G. Zhou Xing, FIEEE at Nanyang Technological University, Singapore, gave an interesting lecture, Monolithic Co-integration of III-V Materials into Foundry Si-CMOS in a Single Chip for Novel Integrated Circuits, that described a vertical innovative platform realised through inserting III-V layers into a conventional Si-CMOS foundry process. He presented a unified compact model for generic GaN/InGaAs-based HEMTs in the context of the hybrid III-V + CMOS technology developed for future heterogeneous integrated circuits. This was followed by the final lecture, Distributed large MIMO and reconfigurable intelligent surfaces for 6G, by Tommy Svensson, Chalmers University of Technology, Sweden. Here, he introduced the ongoing research towards 6G with a special focus on distributed large MIMO (D-MIMO) and reconfigurable intelligent surfaces (RIS), both of which are promising techniques to meet the envisioned capabilities required in 6G communications, localization and sensing for more efficient, reliable, high capacity and low latency communications.

Overall, the MQ was well attended with participants from multiple time zones, and the feedback from both the speakers and the audience was very encouraging, which primarily was because of its cross-disciplinary character! Indeed, there were numerous suggestions to expand the MQ to a full day workshop next year.

EDS MEETINGS CALENDAR

THE COMPLETE EDS CALENDAR CAN BE FOUND AT OUR WEB SITE: HTTP://EDS.IEEE.ORG. PLEASE VISIT.

2023 7th IEEE Electron Devices Technology & Manufacturing Conference (EDTM)	07 Mar – 10 Mar 2023	Seoul, Korea (South)
2023 IEEE International Reliability Physics Symposium (IRPS)	26 Mar – 30 Mar 2023	Monterey, CA
2023 35th International Conference on Microelectronic Test Structure (ICMTS)	27 Mar – 30 Mar 2023	Tokyo, Japan
2023 24th International Symposium on Quality Electronic Design (ISQED)	05 Apr – 07 Apr 2023	San Francisco, CA
2023 International VLSI Symposium on Technology, Systems and Applications (VLSI-TSA/VLSI-DAT)	17 Apr – 20 Apr 2023	Hsinchu, Taiwan
2023 24th International Vacuum Electronics Conference (IVEC)	25 Apr – 28 Apr 2023	Chengdu, China
2023 34th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)	01 May – 04 May 2023	Saratoga Springs, NY
2023 IEEE International Memory Workshop (IMW)	21 May – 24 May 2023	Monterey, CA
2023 IEEE International Interconnect Technology Conference (IITC) and IEEE Materials for Advanced Metallization Conference (MAM)(IITC/MAM)	22 May – 25 May 2023	Dresden, Germany
2023 35th International Symposium on Power Semiconductor Devices and ICs (ISPSD)	28 May – 01 Jun 2023	Hong Kong

2023 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)	11 Jun – 13 Jun 2023	San Diego, CA
2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)	11 Jun – 16 Jun 2023	Kyoto, Japan
2023 IEEE International Flexible Electronics Technology Conference (IFETC)	13 Aug – 16 Aug 2023	San Jose, CA
2023 IEEE International Conference on Quantum Computing and Engineering (QCE)	17 Sept – 22 Sept 2023	Bellevue, WA
2023 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)	26 Sept – 29 Sept 2023	Kobe, Japan
2023 45th Annual EOS/ESD Symposium (EOS/ESD)	01 Oct - -6 Oct 2023	Riverside, CA
2023 Middle East and North Africa Solar Conference (MENA-SC)	02 Oct – 05 Oct 2023	Dubai, United Arab Emirates
2023 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)	14 Oct – 18 Oct 2023	Monterey, CA
2023 IEEE 33rd International Conference on Microelectronics (MIEL)	16 Oct – 18 Oct 2023	Nis, Serbia
2023 IEEE/ACM International Conference on Computer Aided Design (ICCAD)	28 Oct – 02 Nov 2023	San Francisco, CA

IEEE Electron Devices Magazine will be launched Soon!

I am happy to inform you that the first issue of the **IEEE Electron Devices Magazine (ED-M)** will be published in June 2023. ED-M is the new initiative of the IEEE Electron Devices Society. It will be issued by IEEE with the full financial support of our Society.

Joachim N. Burghartz
Founding Editor-in-Chief

The Magazine focuses on the publication of peer-reviewed tutorial and survey papers related to the wider field of electron devices and their applications. It may also include articles dealing with environmental, societal, and humanitarian issues. Besides, columns by renowned experts will be included, dealing with educational, research, industrial and open topics and sharing personal opinions in a compact format. Also, news related to the Electron Devices Society will be displayed in the Magazine, including the President's Column and conference reports.

The IEEE Electron Devices Magazine will be published quarterly, with issues appearing in March, June, September and December. Most issues of the Magazine will include a "focus section," that will feature topical articles invited by guest editors. Each issue will be displayed in light of the given focus topic. The nearest ones' leading themes will be:

- June 2023: 75th Anniversary of the Transistor
- September 2023: Neuromorphic Computing
- December 2023: Semiconductor Manufacturing
- March 2024: Quantum Computing (tentatively)

In addition to the invited topical articles, contributed technical articles on all topics related to the field of electron devices will be presented. Their Authors are advised to try to match their submissions to the Editorial Calendar, though this is not a strict requirement.

I do hope that you, the readers of the Magazine, will find its contents interesting and may vividly react to them in the letters to the Editor (ED-M-editor@ieee.org). I also strongly encourage you to contribute to the Magazine with your articles and personal opinions.

More information about ED-M, including information about paper submission, indexing, subscription, access, can be found at: https://eds.ieee.org/publications/ieee-electron-devices-magazine

Prof. Dr. Joachim N. Burghartz
Founding Editor-in-Chief
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EDS Vision, Mission and Field of Interest Statements

Vision Statement
Promoting excellence in the field of electron devices for the benefit of humanity.

Mission Statement
To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.

EDS Field of Interest
The EDS field-of-interest includes all electron and ion based devices, in their classical or quantum states, using environments and materials in their lowest to highest conducting phase, in simple or engineered assembly, interacting with and delivering photo-electronic, electro-magnetic, electromechanical, electro-thermal, and bio-electronic signals. The Society sponsors and reports on education, research, development and manufacturing aspects and is involved in science, theory, engineering, experimentation, simulation, modeling, design, fabrication, interconnection, reliability of such devices and their applications.