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RAMAC® 305

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RAMAC® 305

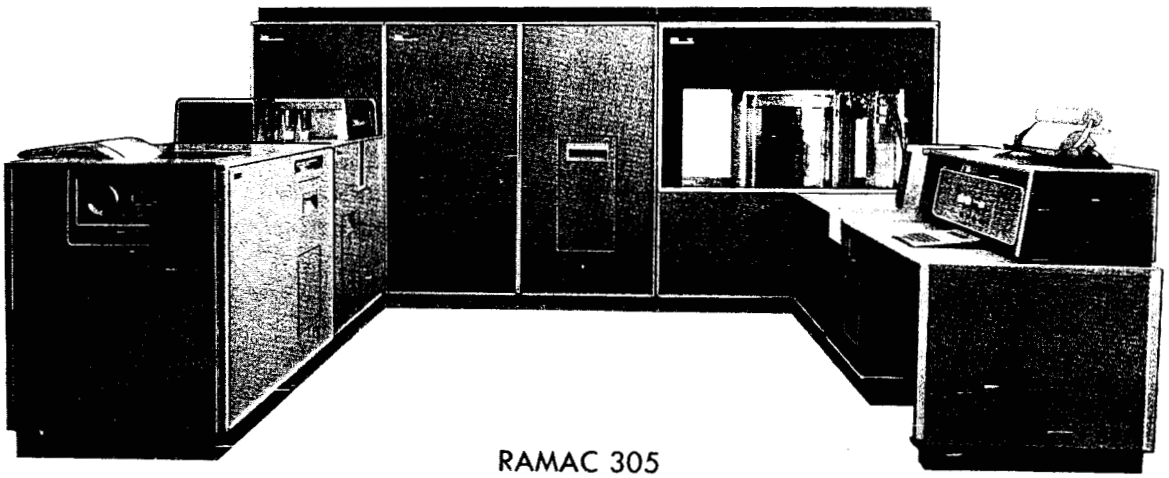
MAJOR REVISION

This CE Manual of Instruction, Form 227-3534-0, replaces but does not obsolete the previous RAMAC CE Manual, Form 227-7610-0. The circuit descriptions in this manual are written to "E" level System Diagrams.

The new and optional features listed below are included in this manual, replacing the RAMAC New Features Manual, Form R27-3506-2.

Reset Multiply	Remote Air Compressor
Blank Transmission Test	Input Rearrangement
Record Advance Overflow	381 Remote Printing Station
Program Exit Splits	407 Printer
Dual File	382 Paper Tape Reader
Dual Access	Compander
Dual Process	Increased Processing Speed

Contents



RAMAC 305

IBM RAMAC 305

The RAMAC 305 is a complete accounting system, capable of performing most of the accounting operations required by the various transactions in modern business. These business transactions are processed individually as they occur, so that each accounting record in the file represents its actual, up to the minute, status at all times. Accounting records, which are stored in the RAMAC file, are automatically adjusted and updated following each transaction. This technique of accounting is called *in-line processing*.

In-line processing is not, in itself, a new concept of accounting. It was the prevalent system in the days prior to the development of mechanized accounting, when the number of transactions to be handled and the number of accounts to be maintained were few. With the growth of business activity and the development of accounting machines, other techniques were adopted. Batch processing, as performed by IBM punched card accounting machines, became the most efficient system for handling business requirements.

Development of a machine to perform accounting functions by in-line processing has long been desired. However, the most fundamental requirement of such a machine is its ability to read, alter, and replace any of the file records in any random sequence. Such a machine was not practical until the development by IBM of the 350 Random Access File. This file is an integral part of the RAMAC.

Five million characters of business facts are stored in the file so that they can be referred to, adjusted, updated, entered or extracted the moment a business transaction is made. This processing technique is made possible by the ability of the random access file to store the information contained in 62,500 80-column standard IBM cards within the machine. This information is contained in 50,000 100-character records in the file. Any one of these records may be reached in a maximum access time of 800 milliseconds (.8 second). The effective access time is usually much less, and may be reduced to zero in some programs. This ability to obtain any record in the file without appreciable loss of time makes possible the posting of transactions as they occur. This immediate processing leads to the availability of more timely information, and consequently to closer control over business transactions.

For example, in the area of inventory control and invoicing, for a single customer order the machine may:

1. Determine availability
2. Check customer credit
3. Price each item
4. Adjust stock balances
5. Invoice the customer
6. Prepare the accounts receivable record
7. Accumulate usage data for sales analysis
8. Credit the salesman's commission account
9. Perform various other related operations

Each operation is performed in sequence for each order. Periodically, under card control, sales analysis and other reports may be obtained, based on the accumulated usage data.

The procedures made possible by the ability to store five million characters and to obtain them from memory without appreciable loss of time, eliminates the need for sorting, collating, and successive runs.

Current processing of minute-by-minute data means dynamic accounting instead of a history for management to review.

Closer control over inventory, results in reduced inventory charges as well as increased service to customers by reducing back orders.

Continuous processing eliminates the need for accumulating customers' orders before making a run. This makes possible a continuous flow of orders through the office and warehouse, resulting in a much smoother operation and better service to customers.

Character Coding

In the card, each character is stored in a particular column in the form of punched holes. The vertical position of each punch determines the character. In RAMAC, each character is stored in a particular character position of a process drum track or file record; it is stored in the form of magnetized spots rather than punched holes. Just as the location of a punched hole within a card column determines its Hollerith code identity, the location of a magnetized spot within a

character position determines its binary code identity. Each magnetized spot is called a "bit," and there is an exclusive arrangement or combination of bits for each character.

Within RAMAC, all data is read, transferred, and written serially by word, character, and bit. There are eight bit positions within each character position. They are identified as bits S, X, 0, 1, 2, 4, 8, and R. Bit S merely provides a space between the recording bit positions of each character, and is not used in the bit coding. Bit R has no numeric or alphabetic value, but is added to certain characters so that every character will have an odd number of bits. This convention makes possible a technique whereby RAMAC may perform a validity check on each character transferred.

Translation from Hollerith code into binary code involves the substitution of a particular bit or combination of bits for each Hollerith punch. The table below gives the binary equivalent of each Hollerith punch.

Major Units and Functions

The major units of RAMAC include the 305 Processing Unit, the 350 File, the 323 Punch, the 370 Printer, the 340 Power Supply, the 380 Supervisory Station, and the card reader, which technically is a part of the 380.

Processing operations, including all data transfers, arithmetic, logical decisions, plus the mechanical operations of reading cards, changing file address, punching, and printing, are normally under complete control of the stored program, supplemented by control panel wiring. The operator, however, may select the program, start, stop, or alter processing operations from the supervisory station. In addition, the operator may obtain any record from the file without halting automatic processing.

With the addition of optional features or the rearrangement of the basic units, the customer may change the capacity of the machine. Several files may serve a single process unit for a dual file system. One file can be used by two process units for dual processing. With the use of two access arms on a single file the access time may be greatly decreased. Input and output may be changed by the addition of a 382 Paper Tape Reader or a 407 Printer. For output at remote locations the customer may use 381 Remote Printing Stations with remote inquiry.

Process Drum

All transfers of data in the RAMAC begin or end at the process drum in the 305 (Figure 2). The drum is a cylinder, coated with magnetic recording material and revolving at 6000 RPM. It is divided into circular tracks

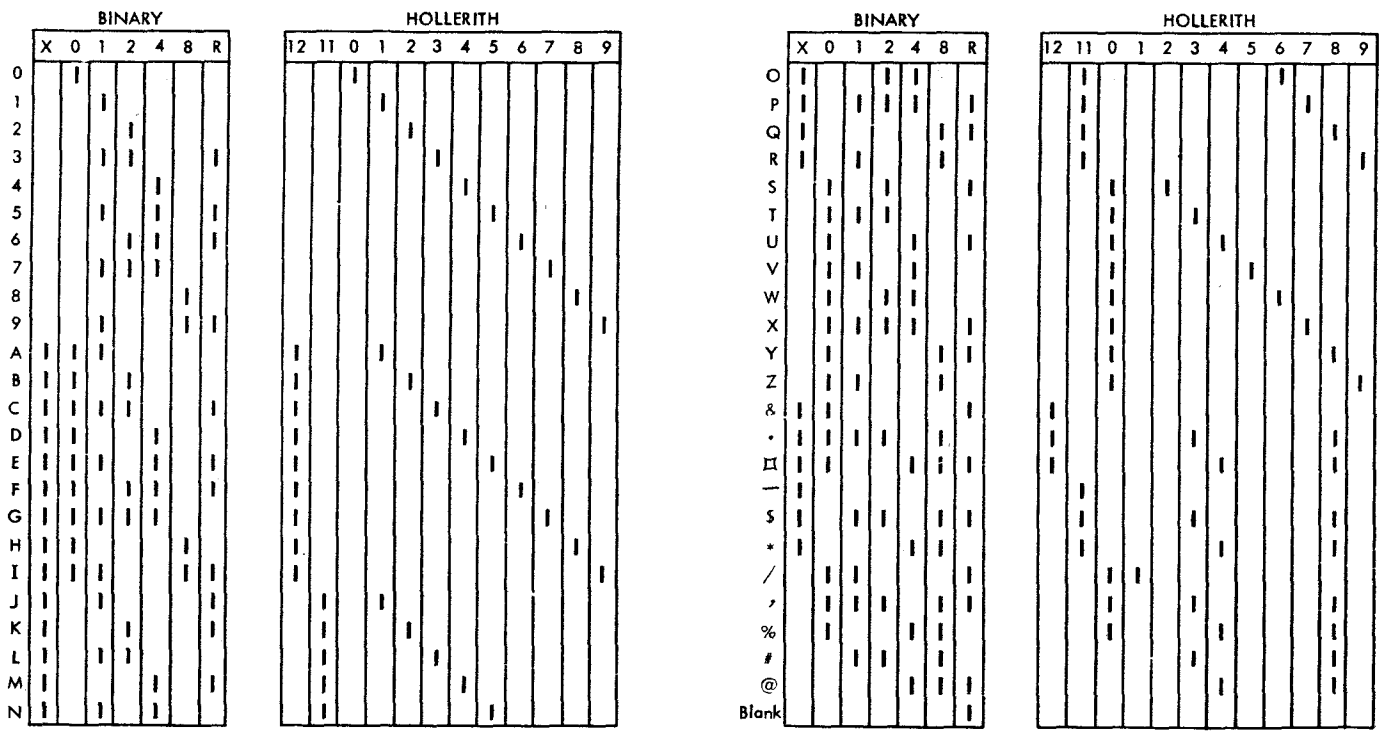


Figure 1. Hollerith Character Coding and RAMAC Binary Character Coding

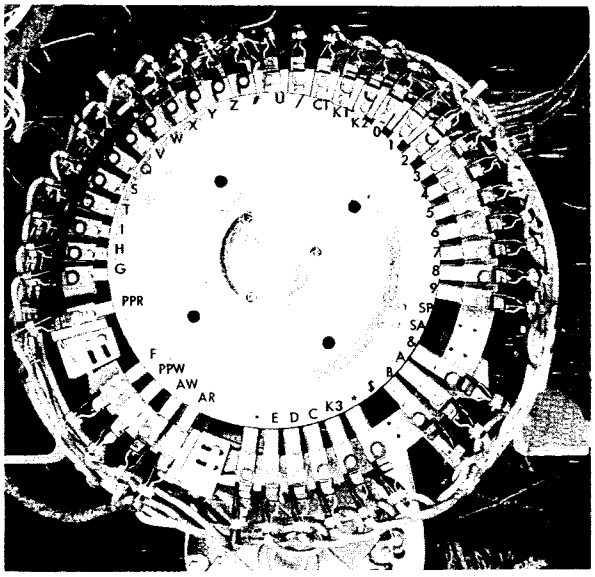


Figure 2. Process Drum Head Layout

(Figure 3), most of which have a read-write coil so positioned that data may be recorded within the tracks in the form of magnetized spots. The standard machine has 32 addressable tracks; four for general storage, twenty for instructions or storage, three for arithmetic operations, three for input from the reader, one for the typewriter, and one for output to the 370 Printer or 323 Punch. Additional tracks for output or general storage are available as optional features.

On each track 100 characters are written serially (sequentially). The 100 character track is divided in fields of 10 characters each (Figure 4). Because of the direction of the revolution of the drum the first character written or read is character 99, often referred to as character 9 field 9 (F9C9), while the last is character 00 (F0C0). Each character position is further broken down into the 7 bit system of coding with an S (space) bit separating each character position.

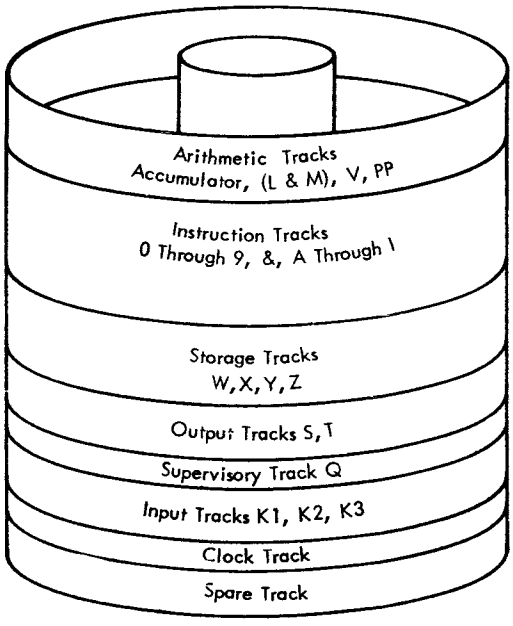


Figure 3. 305 Process Drum

Basic machine timing during a transfer to or from the drum is directly related to the angular position of the drum. An additional permanent track on the drum, known as the clock track, generates the basic timing pulses (Figure 4). This track is broken down into character pulses, then into bit pulses. Regardless of the physical location of the drum heads, all character 99's are read or written at the same time as established by the clock track.

Because the drum is revolving at 6000 RPM, one revolution takes 10,000 μs. Between character 00 and character 99 there is a 400 μs gap leaving 9,600 μs per 100 characters or 96 μs per character. This is the rate at which characters are read from or written on the drum.

Core Buffer

When transferring data from one track on the drum to another track it is necessary to have an intermediate storage area, capable of storing 100 characters. Without this additional storage area all transfers would have to be from a particular character position of one track to the same character position on the new track.

The storage unit used is a 100 character magnetic core buffer. In any transfer of data the flow is from one track to cores, and then from cores to another track. Normally the cores are not addressed. The cores are assigned character positions from 00 to 99 and read-in or read-out starts at character 00. Note that this timing is the reverse of the drum where we always read or write character 99 first. Figure 5 illustrates the transfer of data from K track to W track through the core buffer. The cores are being read into at a rate established by the drum clock track, i.e., 96 μs per character.

Random Access File

The third and largest storage area in the system is the file. This device consists of 50 metal disks, coated on both sides with a ferrous oxide recording material. These disks, slightly separated from one another, are mounted on a vertical shaft which revolves at 1200 RPM. Information is stored in the form of magnetized spots in tracks around the top or bottom side of the disks. At the side of the stack of disks there is an access arm that moves under electronic control to any desired track on any disk. Two magnetic read/write heads

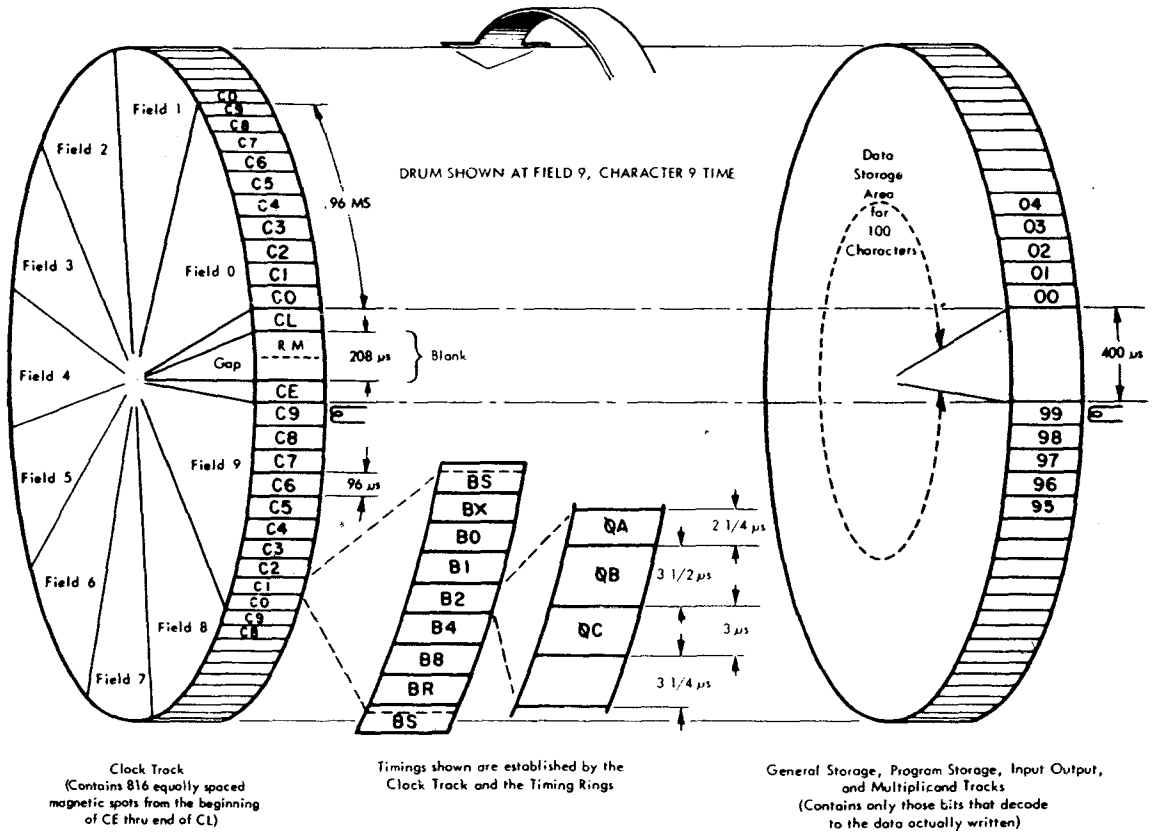


Figure 4. Drum Timing and Data Assignment

(top and bottom) mounted on the access are used to read or write information.

The file is available with a capacity of 5,000,000 characters or 10,000,000 characters. On the 5,000,000 character file there are ten 100-character records stored on each track (five on each side of the disk), and there are 100 tracks on each disk. The tracks are divided into 5 equal segments or records of 100 characters each. These segments are numbered sequentially, 0 to 4 on top and 5 to 9 on the bottom (Figure 6). The tracks are numbered from 00 to 99 moving from the outside to the center.

We now have a method of addressing any record on the file. A 5-digit number is used, the first two digits being the disk number, the third and fourth, the track number, and the last the record number. Disk address 35439 will position the head at track 43, record 9 (bottom of disk), disk 35.

On the 10 million character file, the track density has been doubled, i.e., there are 200 tracks per disk. The tracks are still numbered from 00 to 99, but they repeat 00 to 99 again on the same side. The second or inside 100 tracks on the top disk, become disk address 01. The inside of the bottom disk becomes disk address 99. In the above example disk address 35 would now refer to the 18th disk from the top, the inside one hundred tracks.

The disks are revolving at 1,200 RPM, about one-fifth the speed of the drum. There are five times as many characters passing the head in one disk revolution. The result is practically the same character rate as on the drum, or 100 μs per character. However, there is no way to synchronize the drum with the file. When reading from the file to the drum we must use our core buffer again. Transferring from or to the file, the entire record must be transferred starting with character 99.

Input and Output

The card reader, a part of the 380 Console Unit, is used to enter data into the system. This data is in Hollerith form, read digit by digit, and must be translated to binary form and written on the drum serially. The input data is automatically written on K track. The console can be used to manually read in data to a

specified drum track or file record. Q track is the input and output track for the typewriter. The 382 Paper Tape Reader may also be used for input.

Standard output devices are the 370 Printer, 323 High Speed Punch. These two devices use only S track or S and T track. As an optional feature the 407 may be used as output. An additional device for output is the inquiry feature of the 380 or 381 Remote Station.

Stored Programming

Rather than use a control panel for all control of operation, the RAMAC refers to its own storage units for its next instruction, previously stored as a 10-digit coded instruction. Twenty drum tracks are used to store instructions (tracks 0-9, &, A-1). Each field within the track may contain a 10-digit instruction. Thus we have a possible 200 program steps which the RAMAC will automatically refer to in sequence, starting with program step 000 (F0 track 0) and repeating after program step 199 (F9 track I). Any instruction location not used for an instruction may be used for general storage.

By using its stored program, the RAMAC can transfer data and compute. To punch, print out, feed a new card, compare results and make logical decisions, or change the program sequence, control of the machine is turned over to the 305 control panel by special coded characters in the 10-digit instruction. For reference purposes only, the character positions of an instruction are coded as follows:

$T_1\ A_1\ B_1\ T_2\ A_2\ B_2\ M\ N\ P\ Q$

In data transfer, which is the basic operation, the characters in the different character positions of the instruction have the following significance:

T_1—Track of origin. Read from this track.

A_1B_1—Character position on above track where reading should begin.

T_2—Track of destination. Write the characters transferred on this track.

A_2B_2—Character position where writing should begin.

MN—Total number of characters to be transferred.

P—Program exit code. Any character in this position causes an impulse to be emitted from a corresponding hub on the control panel. This impulse occurs after the instruction has been completed, and may be used to test decision elements and to cause the program counter to be skipped to some new level. Such an impulse may also be used to initiate mechanical functions, such as printing, or feeding a new card. A character in this section is often called a "P flag."

Q—Control code. Certain characters in this position modify the instruction, for example: "1" changes an instruction from a transfer of data to a comparison of the data in the from and to locations. "5" causes an accumulator reset prior to an add or subtract operation. A character in this section is often called a "Q flag."

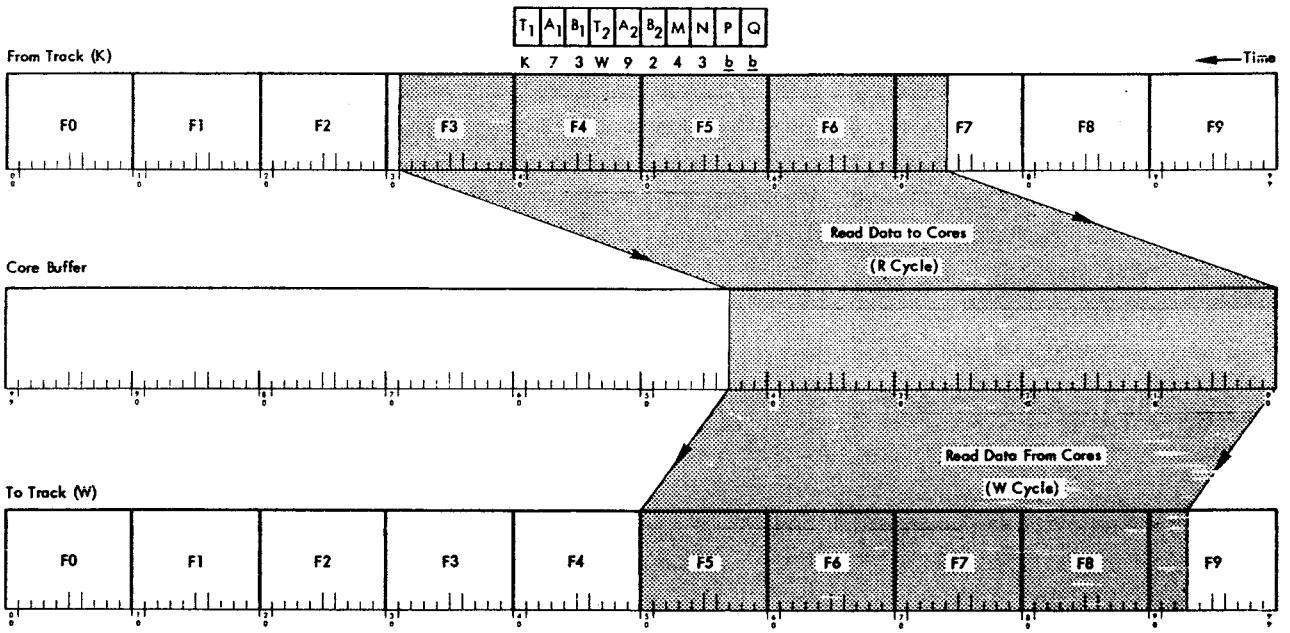


Figure 5. Track to Track Transfer

The P and Q sections of the instruction are often blank. In program planning, a blank instruction is indicated by the symbol b.

Instruction Example

If it is desired to transfer thirteen characters from position 21-33 of track X to positions 65-77 of track Y, the instruction is:

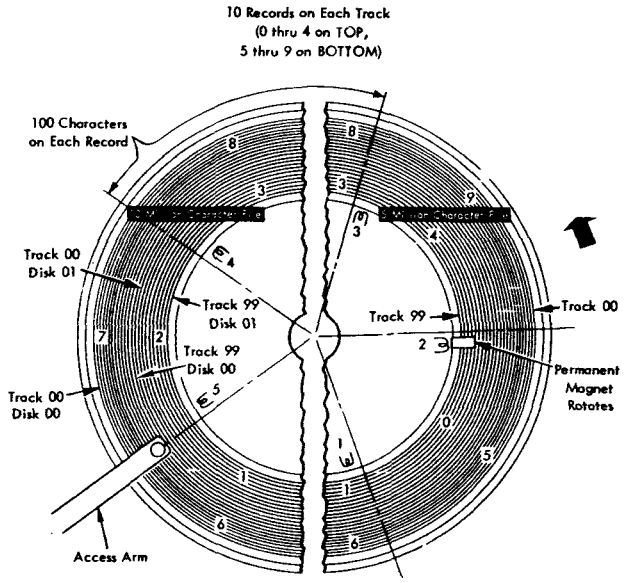
T_1	A_1B_1	T_2	A_2B_2	MN	P	Q
X	33	Y	77	13	b	b

If it is desired that this instruction be a comparison of data rather than a transfer, the instruction becomes:

T_1	A_1B_1	T_2	A_2B_2	MN	P	Q
X	33	Y	77	13	b	1

If it is desired to test the result of the comparison in order to select a new step of the program counter, a P flag must be included. This character may be any of the alphabetic or numeric characters or one of several special characters, each of which has a corresponding program exit hub on the control panel; for example:

T_1	A_1B_1	T_2	A_2B_2	MN	P	Q
X	33	Y	77	13	$	1



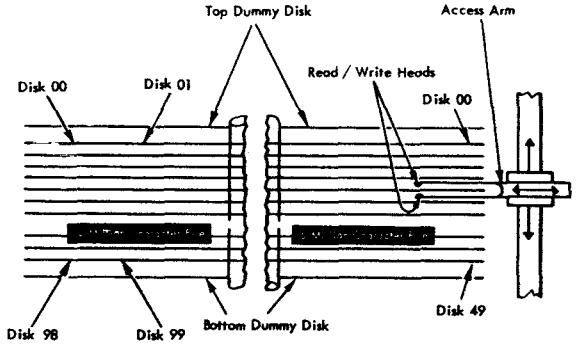


Figure 6. Random Access File—Disk, Track, and Record Selection

Address Identification

A discussion of programming requires an identification of the various tracks or addresses within RAMAC which may serve as the origin or destination address in data transfers or other operations.

	From	To	
	W	W	
General Storage	X	X	
tracks	Y	Y	
	Z	Z	
			Program Step Nos.
	0	0	000-009
Instruction tracks	1	1	010-019
(may also be used	2	2	020-029
for general storage)	3	3	030-039
	4	4	040-049
	5	5	050-059
	6	6	060-069
	7	7	070-079
	8	8	080-089
	9	9	090-099
	&	&	100-109
	A	A	110-119
	B	B	120-129
	C	C	130-139
	D	D	140-149
	E	E	150-159
	F	F	160-169
	G	G	170-179
	H	H	180-189
	I	I	190-199
Add		L	
Subtract		M	
Read out	L		
Read out and reset	M		
Multiplicand	V	V	
Multiply		N	
Divide (optional)		P	
Input track	K	K	
Output track	S	S	
Optional output track			
(printer)	T	T	
File record	R	R	

File address register (also initiates a servo to the new file address)		J
Inquiry track	Q	Q
Character selector (causes the character to be analyzed into Hollerith Code Components)		– (hyphen)
Core Buffer		– (hyphen)

Data Flow and Logical Organization

The general data flow of the RAMAC 305 is shown in Figure 7. Notice this diagram does not include the controlling units and circuits. The need for these units will not be apparent until data flow is understood.

Data, either instructions or factors, is entered from the reader to K track. Following any read operation the information must be transferred from K to some other storage location, then another read operation may take place (Figure 5). The flow is from K track into the core buffer and then out to the drum. When all the information has been loaded, processing may begin. The operator resets the machine and then pushes program start, which will cause the RAMAC to move sequentially through the program steps beginning with step 000.

Each transfer instruction will require at least three drum revolutions, each of which is considered a machine cycle. To differentiate one cycle from the other, we shall call them instruction cycle, read cycle, and write cycle, or I, R, and W. During the I cycle the instruction will be read from the drum directly to the instruction register for analysis. The storage location referred to will be determined by the program counter which advances from 000 to 199 and then resets.

During the R cycle the T_1 character in the instruction register is analyzed and a drum head is selected for reading. The A_1B_1 characters tell the machine where on the selected track to begin reading while the MN determines the stopping point. This information flows to the core buffer. If $T_1 = R$ the file is selected and the data moves from the file to the cores.

During W cycle the T_2 character is analyzed, a drum head is selected for writing and data is read out of the cores to the drum. If $T_2 = R$, the flow is to the file.

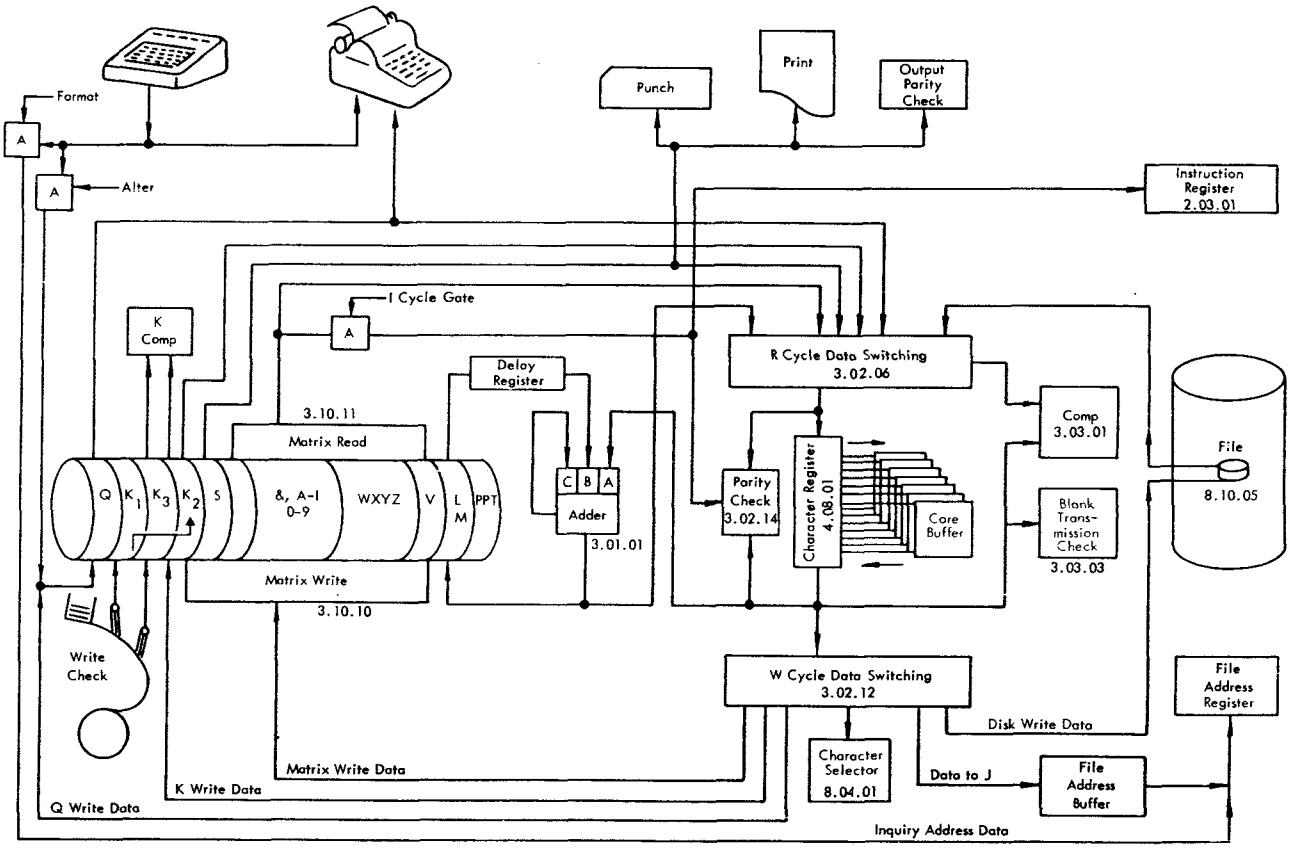


Figure 7. RAMAC Data Flow

A_2B_2 and MN determine the exact location within the track for the data. This represents the most common machine instruction and data flow.

When reading or writing on the file the 5-digit address must be placed in the control circuits prior to the T_1 or T_2 of R instruction. This is done with a special command of $T_2 = J$, often referred to as a servo command. The disk address itself is the first five characters read from the selected track as established by T_1. During W cycle this address moves from cores to the file address register. This register is a relay storage device. Due to the relative slowness of relays, more than 30 milliseconds is needed to complete the operation. Following W cycle the machine goes through two additional cycles, D and P, before advancing to the next instruction.

When processing is complete and the result is to be punched or printed, it is first necessary to transfer the data to one of the output tracks, S or T. This same instruction should provide an impulse to the control panel which can be wired to print or punch. This is done by placing some character in the P position of the instruction. Once again relays must be picked, resulting in extra cycles following W cycle. The sequence is IRWDP with the specific program exit hub emitting during P cycle.

Each of these machines cycles, I, R, W, D, and P are basically 10 millisecond cycles of the process drum; however, it is sometimes necessary to extend an R or W cycle to some multiple of the process drum cycles.

On the data flow diagram notice a parity check is made on every transfer, before entering cores and after leaving cores. Parity is checked during print or punch out. The instruction is parity checked during I cycle. Basically this means the bits within each character are checked for an odd count. There is also a check for the accuracy of the input data. The reader has two sets of brushes and within the process unit a comparison will be made to be sure the same information is read at each set of brushes.

The arithmetic unit consists of the adder, the delay register, and 10 accumulators. Each of the 10 accumulators occupies 1 field on the L (or M) track. The partial product track is a non-addressable track used only to develop the product or quotient, while the V track is used for storing the multiplicand. Addition, subtraction, and multiplication are standard machine functions while division is optional.

The console is represented by the keyboard and typewriter. With the format key the operator may manually enter an address into the file address register and cause the file to servo. When the access arm has located the correct record, the data will move from file to cores, from cores to Q track, and from Q track to the typewriter. The only path to or from the typewriter to the process unit is via Q track. Data may be placed on Q track from some other storage location, then printed on the typewriter. At the typewriter it may be partially or completely altered and then replaced in the original location.

The electronic circuits used in the RAMAC 305 are built around pluggable units. A pluggable unit will generally include one or two electronic tubes and the associated circuitry. The components of a standard circuit are mounted on a frame provided with a standard 10 pin electronic tube base (Figure 8). To bring the unit into use, it is plugged into its corresponding socket on one of the electronic gates; hence, the designation "pluggable unit."

The object of the "Electronics" section of this manual is to give a functional understanding of the operation of the circuits used in RAMAC. Although there are approximately 70 different pluggable units in use, there are a comparatively small number of basic circuits from which these units have been derived. These basic circuits will be our main concern in this section.

Quite often a functional circuit is composed of several pluggable units. For instance, the drum matrix read amplifier ("System Diagram 3.10.11") consists of two units, AM314 and AM315. The Overbeck ring (1.01.05) is another example of a functional circuit made up of several units. This should be kept in mind when applying the principles of operation of a basic circuit to the actual pluggable units.

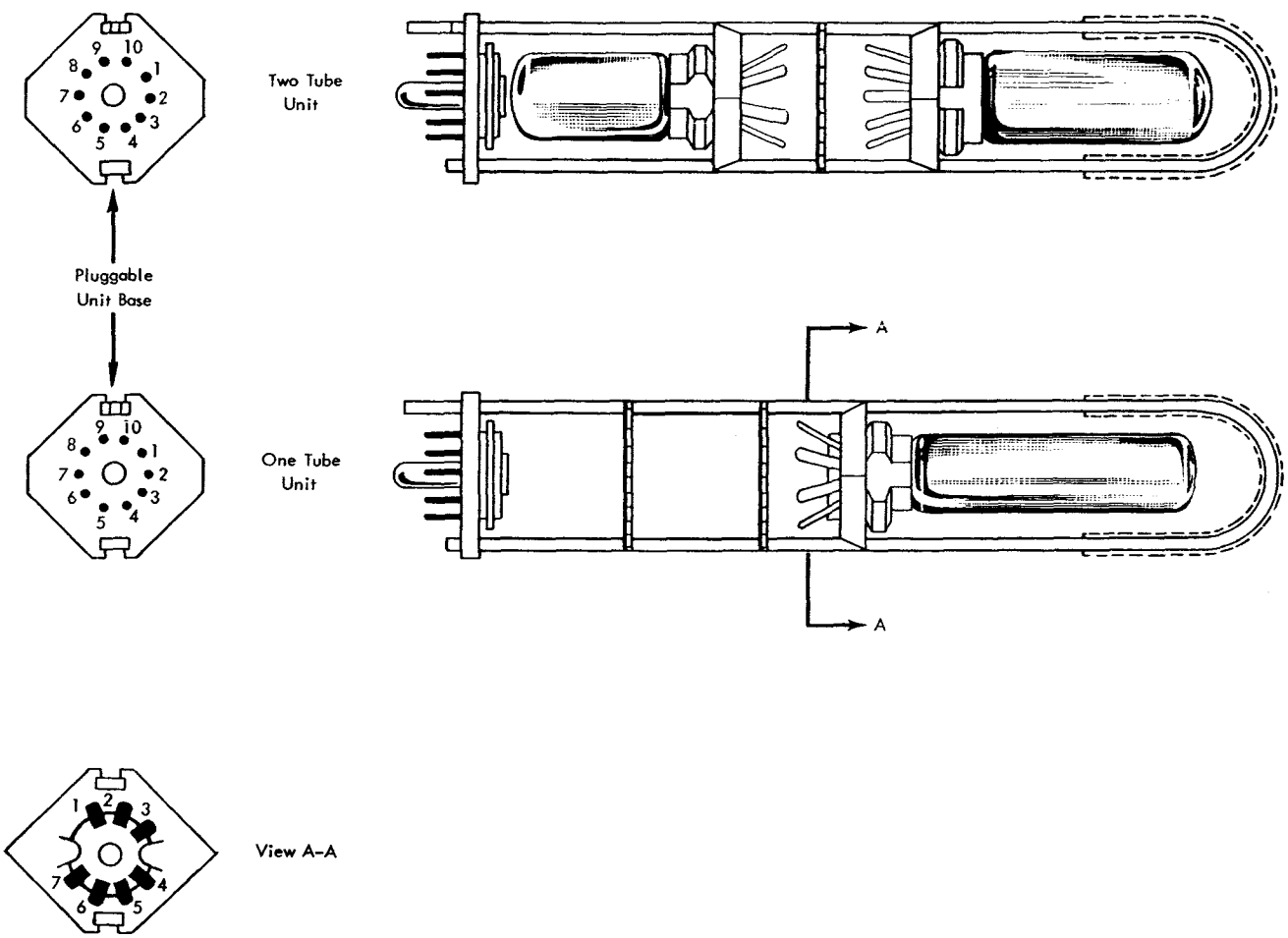


Figure 8. Electronic Pluggable Unit Assembly

Basic circuits plus the conventions relating to pluggable units and "System Diagrams" are described in this section. Pluggable unit components are described separately in "Component Circuits."

Conventions

The following conventions are used in this section, the "System Diagrams," and the "Component Circuit" diagrams.

Standard Levels

Standard levels are used in the circuits in which the signal is either absent or present. The nature of many circuits, however, necessitates their having non-standard outputs. Such circuits are the file servo circuits, and the signals read from the process drum, core buffer, and file. Non-standard levels are frequently converted to standard levels by means of the scheme illustrated in Figure 9.

The nominal standard levels are as follows:

Nominal plate level:	Up 140v;	Down +50v
Nominal cathode level:	Up 12v;	Down −38v

In practice, these levels will vary slightly throughout RAMAC. However, nominal values are used throughout this section of the manual.

Physical Location of Pluggable Units

The pluggable units used in the 305 Process Unit are mounted on three electronic gates, as shown in Figure 10. Each gate is subdivided into three panels. For identification purposes, the panels are numbered consecutively from 1 to 9 (a 10th panel, mounted differently, supports the mercury relays). Each panel is provided with 264 sockets arranged in 24 columns (A to Z with I and O omitted) and 11 rows (1 to 11). The location of a pluggable unit, plugged into one of these sockets, can be given in terms of three symbols: e.g., 3F2 specifies the location of the socket on panel 3, column F, row 2. Panel wiring is brought out to edge connectors.

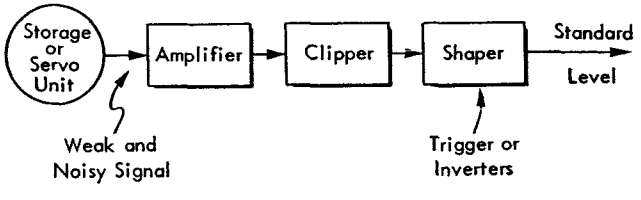


Figure 9. Conversion of Weak Signals to Standard Level

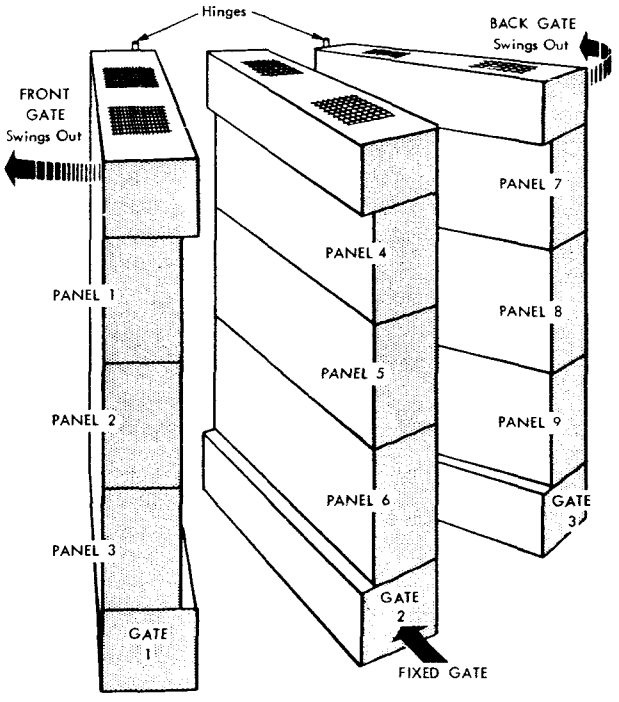


Figure 10. Electronic Gates and Panels

The pluggable units are used in the 350 File before System 305-10220 are arranged in 2 rows (numbered 1 and 2) of 20 columns (A to V with I and O omitted). The location of a pluggable unit on the file is given in terms of two symbols: e.g., K2 specifies the location of the socket in column K, row 2.

Beginning with 305-10220, the file pluggable units are mounted on an electronic gate. These pluggable units are numbered from 1 through 16 for horizontal rows and lettered A through D for vertical columns.

Symbols for Pluggable Units

A pluggable unit is represented on the "System Diagram" by a rectangle subdivided into four sections.

The bottom section contains a code, such as AM301, which refers to a definite type of standard circuit.

The next to bottom section contains the code indicating the physical location of that unit, in some cases one pluggable unit includes 2 identical circuits, each using one section of a dual tube. The left hand section is designated by the letter *a*, the right hand section by *b*. The letter *a* or *b* is added to the location code of the unit so that the code 6B11a indicates section *a* of the tube circuit in the pluggable unit located on panel 6, column B row 11.

The next to top section contains the symbol for the logical function performed by the unit in the particular circuit where it is used. The same electronic circuit may be used to perform different logical functions.

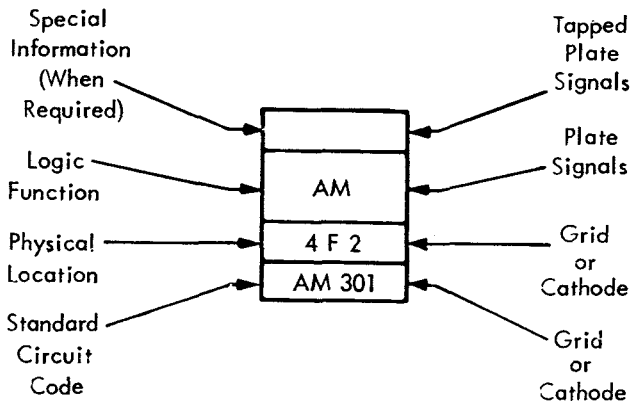


Figure 11. Pluggable Unit Logic Block Diagram

For instance, the pluggable unit coded DD301 may be used as an AND circuit (logical symbol A), or as an OR circuit (logic symbol O), or as an isolator (ISOL).

The top section may be used when additional information is required. Thus, in the case of a single-shot circuit, the unit coded CU302 contains the components which determine the duration of the single shot pulse. The length of the pulse is recorded in the top section. In the case of circuits which represent diodes, the orientation of the diode is often shown in the top section.

Note that in the case of trigger circuits, section 2 of the block diagram also contains information relating to the manual reset of the trigger. This will be explained later.

Input and Output Signals

These signals are indicated by arrows on the input and output lines on the "System Diagrams." As a general rule, certain types of signals are associated with a definite section of the pluggable unit block diagram.

Top Section:	Tapped Plate Signals
Center Top Section:	Plate Signals
Center Bottom Section:	Grid or Cathode Signals
Bottom Section:	Grid or Cathode Signals

This general rule does not apply to some of the units, such as diodes. The function of the unit will usually make it clear whether this rule is applicable or not. In doubtful cases, reference should be made to the circuit diagram for the unit.

Test points are indicated by the pin number on the pluggable unit where the signal is available.

Trigger Conventions

A trigger is ON when its left side is conducting. Its right plate is then high. A trigger is OFF when its right side is conducting. Its right plate is then low.

Resistor and Capacitor Conventions

The following values apply to resistors unless otherwise stated in the diagram:

1. Wattage: 0.5 is understood.
2. Tolerance: 5% is understood.
3. Resistance value: K is understood (e.g., 10,000 ohms is written as 10).

The following values apply to capacitors unless otherwise stated in the diagram:

1. Voltage: 600v is understood.
2. Tolerance: 20% is understood.
3. Capacitance value; μfd is understood.

Abbreviations

The following abbreviations are used throughout "System Diagrams, Component Circuits," and this manual:

A_1	tens position of FROM instruction
A_2	ten position of TO instruction
ACC	access
ACCR	accumulator
ACLR	alternating current line regulator
ACLR—MB	alternating current line regulator meter back
ACLR—MF	alternating current line regulator meter front
ALBAR	alarm bar
AMPL DRUM CLOCK	amplified drum clock
AR	accumulator track read
ASM	assembly
AW	accumulator track write
B_1	units position of FROM instruction
B_2	units position of TO instruction
Bs	bit space
B0	bit 0
Bx	bit x
B1	bit 1
B2	bit 2
B4	bit 4
B8	bit 8
BR	redundancy bit
C0—C9	characters 0-9
CB	circuit breaker
CE	character early
CE	customer engineer
CHAR	character
CHAR & FLD RING GATE	character and field ring gate
CHAR RING DRIVE	character ring drive
CHB	check brushes
CHK	check
CL	card lever, or character late
CLM	clamp
CLP	clip, or clipper
COMP	component
CONN	connector
CPC	control cable parallel connector
CPL	control panel
CT	clock track
CTR	counter
D	diode
DB	distribution board
D CYCLE	delay cycle
DF	dummy fuse
DHP	drum head plug
DSE	digit selector emitter

E	emitter (cam-370)
ECN	end connector
F0–F9	field 0–field 9
FB	fuse box, or file binder post
FBS	card feed barrier strip
FCB	card feed circuit breaker
FCP	fuse control panel
FD	feed
FIL	filament
FLD RING DRIVE	field ring drive
FNA	slow blow signal type fuse
FNJ	slow blow signal type fuse
FNM	slow blow non-indicating fuse
FRN	slow blow non-indicating fuse
GCP	punch control panel
GEN	generator
GERM	germanium diode
GND	ground
H	hold coil–relays
HD 0/3	head 0 or head 3
HD 2/5	head 2 or head 5
HD	heavy duty relay
I	incandescent light
Ix, I0, I1, I2, I4, I8	program bits x, 0, 1, 2, 4, 8
I CYCLE	instruction cycle
IMMED	immediate
INLK or INTL	interlock
INLK SW	interlock switch
INSN	instruction
I/O	input or output
ISOL	isolation
JP	Jones plug
L	lower
L1	line terminal #1
LC0–LC9	line character 0-9–cores
LF0–LF9	line field 0-9–cores
12LPB	latch pick relay #12 on B side
LR RESET	latch relay reset
LT	latch trip, or light
MAN	manual
MIC	immediate blow signal type fuse
MIJ	immediate blow signal type fuse
MLPR	multiplier
MN	number of character to be transferred
MR	mercury wetted relay
MT	motor terminal
NE	neon
P	pick coil–relay, or punch–323
P3C	power parallel 3 connectors
P5C	power parallel 5 connectors
PBS	punch barrier strip
PCB	punch circuit breaker, or power circuit breaker
PCL	punch card lever
PCP	process unit control panel
PEM	punch emitter
PNL	panel
P on L	power on light
POT	potentiometer
PP	partial product
PPR	partial product read
PPW	partial product write
PRBS	printer barrier strip
PRG	program
PROC	process
PS	program shaft–370
PT	point
PWR	power
Q	special instruction
RA	read amplifier
RBS	resistor barrier strip
R CYCLE	read cycle
RCM	read clutch magnet
RD	read
RDR	reader
RE	read emitter
REG	register
RES	reset, or resistor
REWR	rewrite
RF3	radio frequency choke coil #3
RG12	germanium rectifier #12
RLY	relay
RM	reference mark
RUB	rubber
R/W	read or write
SBS	supervisory station bar strips
SC	shoe connector
SCB	supervisory circuit breaker–380
SCP	supervisory station control panel
SOL	solenoid
SPEC	special
STAT 1	status 1
STAT 2	status 2
STP	stop
STR	start
STRD	standard
SW	switch
T_1	FROM track address
T_2	TO track address
TB	terminal block
TD	time delay
TFMR	transformer
THPLAS	thermo plastic
TRF	transfer
TRK	track
TS	terminal strip
U	upper
W CYCLE	write cycle
WP	Winchester plug
WR	write
WRB	write brushes

Indexing of System Diagrams

The five digit number at the upper right hand corner of each system diagram is an indexing of that diagram according to the following table.

DIAGRAM NUMBER	CATEGORY	MACHINE INVOLVED
0.XX.XX	Reference	305
1.XX.XX	Processing information	305
2.XX.XX	Processing information	305
3.XX.XX	Processing in formation	305
3.10.XX	Drum	305
4.XX.XX	Cores	305
5.XX.XX	Arithmetic	305
6.XX.XX	Supervisory station	380
7.2X.XX	Card Reader	380
7.4X.XX	Punch	323
7.7X.XX	Printer	370
8.XX.XX	File	350
9.XX.XX	Power Supply	340
10.XX.XX	Paper Tape	382

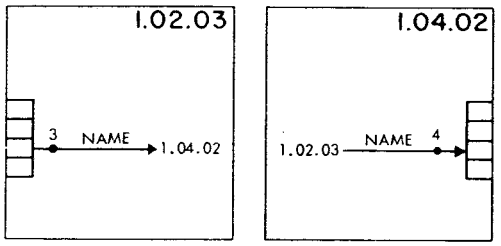
Point to Point Wiring Representation — System Diagrams Relay Circuits

The relay circuits in the "System Diagrams" are drawn point to point, i.e., the wires in the machine go from one relay point or coil to another exactly as drawn.

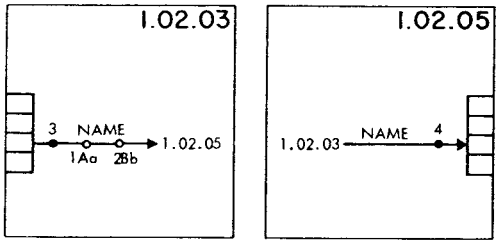
Modified Point to Point Wiring Representation — System Diagrams Electronic Circuits

The electronic circuits in the "System Diagrams" employ modified point to point representation as follows:

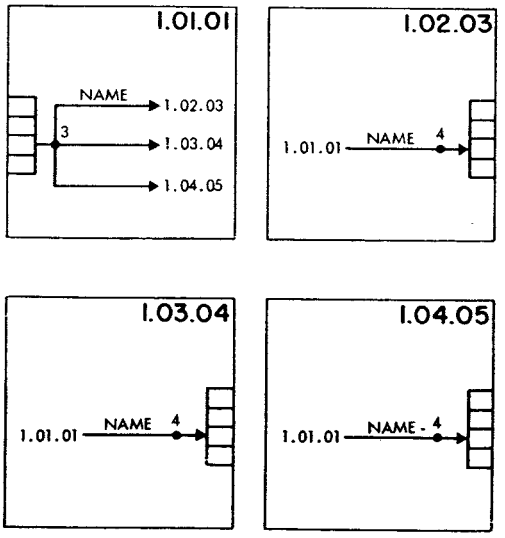
The line originates at pin 3 of the unit on 1.02.03 and goes directly to pin 4 of the unit on 1.04.02.



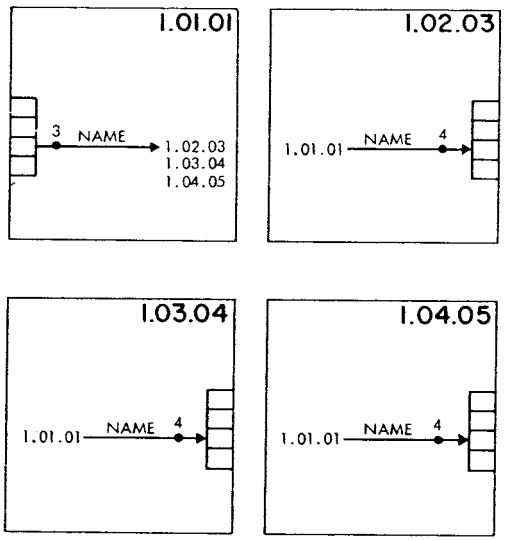
The line originates at pin 3 of the unit on 1.02.03 and goes to panel 1 edge connector 1Aa. It then goes to panel 2 edge connector 2Bb, and then to pin 4 of the unit on 1.02.05.



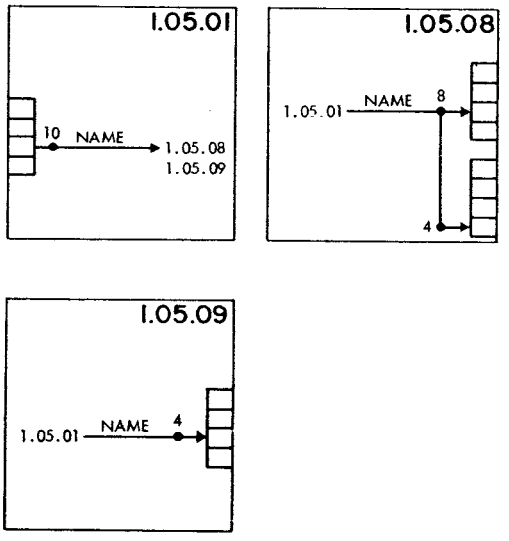
Three lines are output in parallel from pin 3 of the unit on 1.01.01. One line goes to pin 4 of the unit on 1.02.03, another to pin 4 of the unit on 1.03.04, and another to pin 4 of the unit on 1.04.05.



One line is output from pin 3 of the unit on 1.01.01. Three pages are listed on the output line. This shows that the line goes first to pin 4 of the unit on 1.02.03, from there to pin 4 of the unit on 1.03.04, and from there to pin 4 of the unit on 1.04.05.



If a line goes to more than one point on a given page, the last point on that page connects the first point on the next page of the serial connection list. The output from pin 10 of the unit on 1.05.01 goes first to pin 8 on 1.05.08, then to pin 4 on 1.05.08, then to pin 4 on 1.05.09.



Combinations of the above 5 basic representations are used in the system diagrams.

Circuit and Component Descriptions

The basic circuits used in the pluggable units fall into the following categories:

1. Logic circuits: a) AND circuits; b) OR circuits; c) Inverters; d) Triggers.
2. Driving and level setting circuits: a) Cathode followers; b) Inverters; c) Amplefiers.

AND Circuits ("System Diagram" Symbol: A)

An AND circuit may have two or more inputs. When all inputs are high, a high output will result. Physically, the AND circuit consists of two or more diodes suitably interconected. Diodes have a small resistance to electron flow from the cathode to the plate (forward), but a large resistance to flow from the plate to the cathode (back). Diodes may be either crystal or vacuum tube type. In RAMAC the crystal type is not used in AND or OR circuits, but is used in a few circuits to control the direction of current flow. With crystal diodes the forward resistance is usually negligible, but the back resistance cannot be assumed to be infinite. With vacuum diodes, the forward resistance must be reckoned with, but the back resistance can be assumed to be infinite.

All vacuum diode AND circuits operate at cathode levels. A typical example of the operation of an AND circuit is shown in Figure 12.

The input signals come from a low impedance cathode follower driving circuit. The output goes to a high impedance load. The plates of the diodes are connected together and returned to +140v through resistor "R." As long as the two inputs remain low (−38v) current flows through both diodes and the output is low (−38v neglecting diode forward resistance). If input 2 is raised to +12v but input 1 remains at −38v, diode 1 will continue to conduct while diode 2 is cut off, and the output will remain low.

In a multiple input AND switch, if any input remains low, then the diode with the low input will conduct,

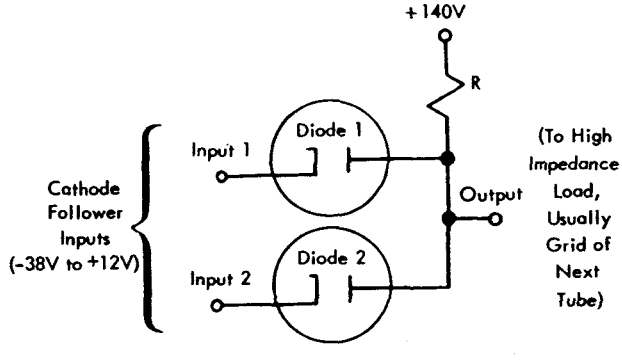


Figure 12. AND Circuit

while the high input diodes are cut off, causing the output to be low. If all inputs are raised to +12v, current will flow through all diodes and the output voltage will be the same as the input voltage (neglecting forward diode resistance). Thus, the output voltage always follows the lowest input voltage regardless of the number of inputs.

Positive OR Circuit ("System Diagram" Symbol: O)

Like the AND circuit, the positive OR circuit may have two or more inputs. Unlike the AND circuit, when any one positive OR input is high, the output is high. The basic diode interconnection for a positive OR circuit is shown in Figure 13.

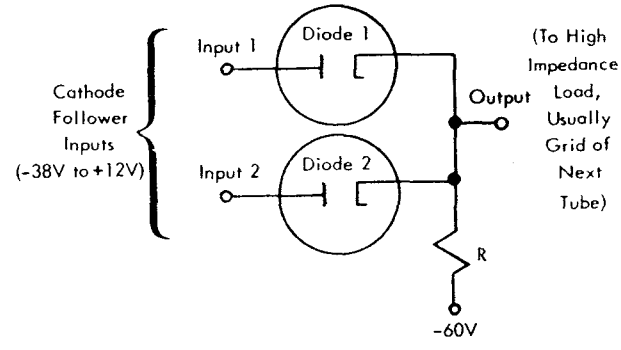


Figure 13. OR Circuit

The input signals come from a low impedance cathode follower driving circuit. The output goes to a high impedance load. The cathodes are connected together and returned to −60v through resistor "R." As long as both inputs are low (−38v) both diodes conduct equally and the output remains low (−38v neglecting forward diode resistance). If input 1 is raised to +12v, diode 1 conducts while diode 2 is cut off, and the output becomes +12v (neglecting forward diode resistance). As soon as input 1 is again dropped to −38v, both diodes again conduct equally and the output becomes low. Thus, the output voltage always follows the highest input voltage.

Negative OR Circuit ("System Diagram" Symbol: NO)

The negative OR circuit performs the same function with negative pulses that the positive OR circuit performs with positive pulses. The diode interconnection for the negative OR circuit is identical with that of the positive AND circuit (Figure 12). The inputs are normally +12v. Whenever one input decreases to −38v, the output follows it in accordance with the principle established for AND circuits: the output always follows the lowest input voltage.

Types of AND and OR Circuits

The AND and OR Circuits used in RAMAC are not limited to simple diode circuits. A basic AND circuit may include an inverter ("System Diagram" symbol AI) or a cathode follower ("System Diagram" symbol AK) depending on the type of output desired. Another type AND circuit uses thyratrons. ("System Diagram" symbol ATH). Some OR circuits are made up of neon diodes which use plate level inputs. For more details about AND or OR circuits, see "Component Circuits."

Inverter ("System Diagram" Symbol: I)

The inverter circuit produces a negative shift at its plate when a positive shift is applied to the grid, or a positive shift at its plate when a negative shift is applied to the grid. This property is used to invert logical conditions.

The inverter also amplifies and shapes signals. Therefore, it is also used as level setter and pulse shaper. Different circuits are used, depending on which of these properties is to be emphasized.

The basic circuit is shown in Figure 14. When a positive pulse is applied to the grid, the grid rises above cutoff, the tube conducts, and the plate voltage drops. At the end of the pulse, the grid voltage drops below cutoff, the tube becomes non-conducting, and the plate voltage rises to +140v.

Figure 14a illustrates the level-setting characteristic of the inverter. The tube is biased so that the grid voltage swing from cutoff to full conduction is a small portion of the input pulse swing. And, since the circuit also gives amplification, the output level can be set to any desired value. Thus, a badly shaped, nonstandard level input pulse is restored to an almost "square" output pulse at the right level.

Figure 14b: An input voltage divider has been added in order to accept high input level pulses. The tube then operates under the same conditions as in Figure 14a. Since the grid resistance is now higher, the added resistor, in series with the grid, is bypassed by a capacitor to speed up the response.

Figure 14c: Response to positive shifts only is required. A capacitor is added in series with the input signal to differentiate the shifts occurring at the plate of the trigger preceding the inverter. A negative shift merely cuts off the tube farther and produces no change in the inverter output.

Figure 14d: The input pulse is obtained through relay contact points. To reduce the "noise" due to contact-chatter, an integrating circuit is used in the input circuit.

Figure 14e: For additional shaping of the inverted pulse, a compensating capacitor "C_c" is added in the output circuit. The stray capacitance is represented by "C_s." The output wave shape when "C_s" is charged by R_1 is shown in Figure 14e (i). When "C_c" is added, the RC time constant of the charge path is reduced. The resulting wave shape is shown in Figure 14e (iii).

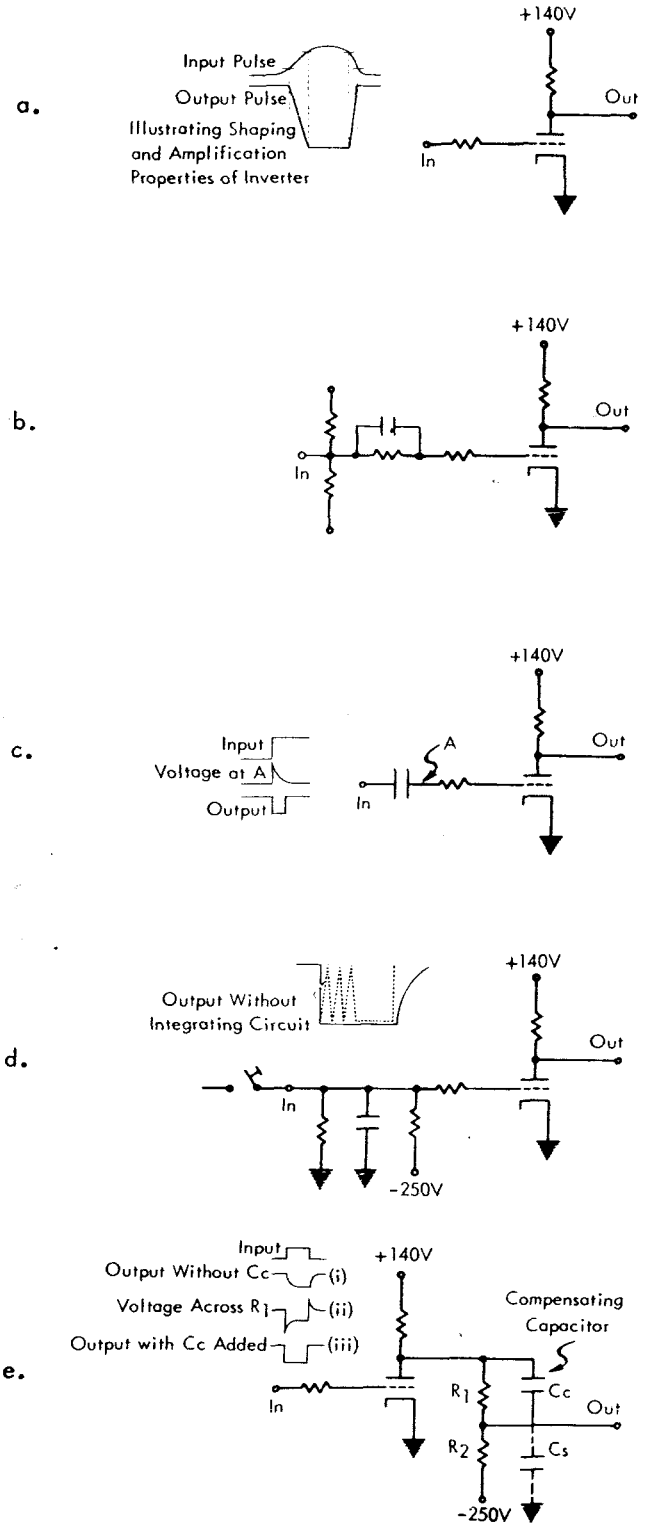


Figure 14. Basic Inverter Circuit and Variations

The Schmitt Trigger (component type TR311) is an application of the use of inverters as described by Figures 14d and 14e. This application allows ragged, noisy input pulses to result in squared-up output pulses. Two inverters are used in series in the TR311 so that a positive output can be obtained from a positive input. (See "Component Circuits.")

Triggers ("System Diagrams" Symbol: T)

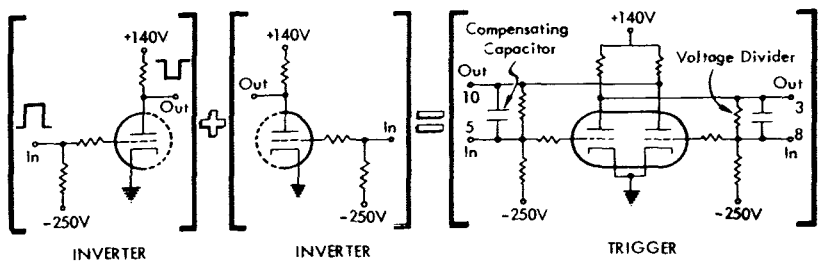
A trigger is a bi-stable multivibrator. This means that it remains in either of two stable states until it is forced by an external signal to assume the other state. The forcing action is called triggering or flipping. The bi-stable property of a trigger makes it useful as a storage device. It is used in registers, counters, and gate-forming circuits.

General Trigger Circuit Operation

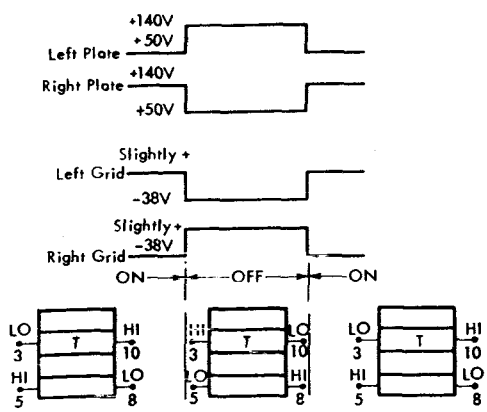
A trigger circuit resembles two inverter circuits with the plate output of each inverter coupled to the grid of the other inverter (Figure 15). In one stable state, the left tube is in full conduction while the right tube is cut off. In the other state, the right tube conducts while the left tube is cut off. To flip the trigger from one state to the other, an external signal must be applied to a sensitive point in the trigger circuit. This point may be a grid or a plate of the trigger. Since the gain of a conducting tube is greater than the gain of the non-conducting tube, it requires less energy to flip the trigger by applying a negative voltage to the conducting grid than by applying a positive voltage to the other grid. The trigger may also be flipped by applying a negative voltage to the high plate of the trigger. In any case, the input signal must initiate a regenerative action to cut off the conducting tube and bring the other tube into full conduction. A small grid current is allowed to insure that the plate is at its lowest voltage level, and that small grid voltage fluctuations cannot initiate this regenerative action. A neon lamp is sometimes connected between plate and ground to give visual indication of the state of the trigger.

Grid Flip — Direct Input (TR306)

The most common way to flip a trigger is to apply a positive or negative pulse to a grid. Assume that the trigger is OFF (the right plate is low), and it is to be flipped ON by applying a negative pulse to the right grid (Figure 15). The negative shift to this grid cuts off the right tube, thereby raising the right plate voltage. This rising voltage is applied to the left grid through its voltage divider, As a result, conduction starts in the left tube, and the left plate voltage decreases. Since the negative input signal is also applied



(a) Basic Trigger Circuit



(b) On-Off Convention

Figure 15. Basic Trigger Circuit and Trigger ON-OFF Convention

to the left plate through the voltage divider, a regenerative action is initiated. The voltages are stabilized when the left grid reaches ground potential. The voltage dividers keep the grid level sufficiently low to prevent the positive going trailing edge of the pulse from flipping the trigger back again.

As long as the external negative signal is maintained to the right grid, the trigger is "clamped," and cannot be flipped by a signal to any other input.

A somewhat greater positive signal applied to the left grid of a trigger that is OFF will cause the trigger to flip. This signal causes the left tube to conduct and initiates a regenerative action similar to that outlined above.

Grid Flip — Capacitor Input (TR 307 and TR 308)

The inserting of a capacitor in series with each grid makes the trigger sensitive to only negative grid inputs. Triggers TR307 and TR308 are such triggers. Assume that we have a capacitor input trigger that is ON. (See Figure 16.)

With the trigger ON, the left grid is close to cut off and the right grid is below cut off. A negative pulse of about −3v to the left grid is enough to start regenerative action to cut off the left tube. The attenuation caused by the small input capacitor will keep normal input signals within this range. A +3v input to point *A* at the right grid would not affect the trigger since this grid is about −30v below cut off. However, should a sufficiently large positive signal be applied to the right grid, the trigger would flip, but such a signal would indicate machine trouble.

Binary Input

If a series of negative pulses is applied to the high grid of a capacitor input trigger the first pulse flips the trigger, and the following pulses have no effect. The action is the same as that described in the previous paragraph. To flip the trigger in the other direction, a pulse must be applied to the other grid, which is now high. If the grids are tied together and a series of negative pulses applied to the grids, the trigger will then be successively turned ON and OFF as each pulse is received. A trigger operating under these conditions is loosely called a "binary trigger." These triggers are used extensively in counter and ring circuits.

Plate Pullover

A trigger may also be flipped by applying a negative voltage to the high plate of the non-conducting tube of the trigger. The voltage of that plate is thus "pulled down," hence the name "plate pullover." If only a positive signal is available, it is of wrong polarity to flip the trigger by the plate pullover method. An inverter is therefore used to provide the correct polarity and level.

If an inverter is used to plate pullover a trigger that is OFF (Figure 17), a positive signal pulse applied to the grid of the inverter will cause the plate voltage to drop from 140v to 50v. The left plate of the trigger, which is connected to the plate of the inverter, will also drop from 140v to 50v. The left trigger plate, connected to the right trigger grid through a voltage divider, will drive the right trigger grid down below cut off. As a result, the right trigger plate rises, pulling the left trigger grid up through its voltage divider. As the left trigger grid approaches ground potential, the left trigger tube begins to conduct, pulling the left trigger plate voltage down, which is the same direction as the initial shift applied by the inverter. This regenerative action continues until the left trigger grid reaches ground potential, where voltages are stabilized with the left trigger tube fully conducting and the right trigger tube cut off. The trigger is now ON. The input pulse could now be removed without reflipping the trigger, because the conduction of the left trigger tube holds the left plate voltage down. The plate level of the inverter follows that of the left plate of the trigger.

If the inverter continues to conduct holding the left trigger plate down, the trigger is "clamped." No other input to the trigger can cause it to flip, because the regenerative action cannot be initiated as long as the left tube is held in full conduction.

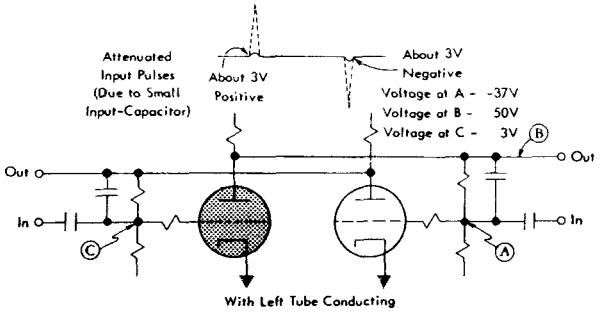


Figure 16. Capacitor Input Trigger

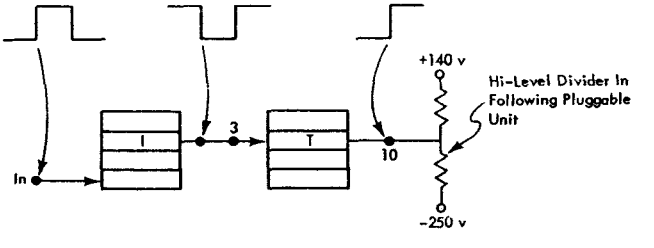


Figure 17. Trigger Plate Pullover

Trigger Reset

(See "Component Circuits" for diagrams of units.)

When power is first turned on, either side of a trigger may start conducting. It is therefore essential that, before any operation is attempted, the triggers be reset to their correct status.

Triggers always reset by raising one grid voltage above cut off. Each grid resistor is connected through a voltage divider to −250v. There is one exception: the right voltage divider of TR308 is connected to −182v. (The reason for this will be made clear later.) The left voltage divider is always connected to pin 4, the right divider to pin 6. To reset a trigger OFF, the reset voltage is removed from pin 6. The right grid voltage rises above cut-off and the regenerative process is initiated. The right tube conducts, the left tube is cut off, and the trigger is OFF.

Some triggers must be reset while the machine is cycling; in other words, they must be reset automatically and at "electronic speeds." For instance, a trigger may be reset at a given time during a machine cycle, ready to be set at some later time during the same cycle. In this case, an "electronic reset" unit IF301, is used. (See "Component Circuits".) The output of the electronic reset unit (pin 3, normally at −182v) is applied to pin 6 (the right grid voltage divider) of trigger TR308. When a reset pulse is applied to the IF301 unit, the level at pin 3 is raised to 0v. The voltage at pin 6 of the trigger rises above cut-off to force that side of the trigger into conduction.

Other triggers are reset at a time when the machine is not cycling. The reset in this case is initiated as a result of a manual operation at the console. The different ways in which this manual reset can be accomplished are shown in Figure 18. In each case, the reset pin of the trigger is returned to −250v. When the key is depressed, the reset line is open (through relay points) and the voltage at the reset pin rises to ground potential. A capacitor between the reset key and ground serves to protect the −250v supply from transients resulting from contact bounce at the relay points.

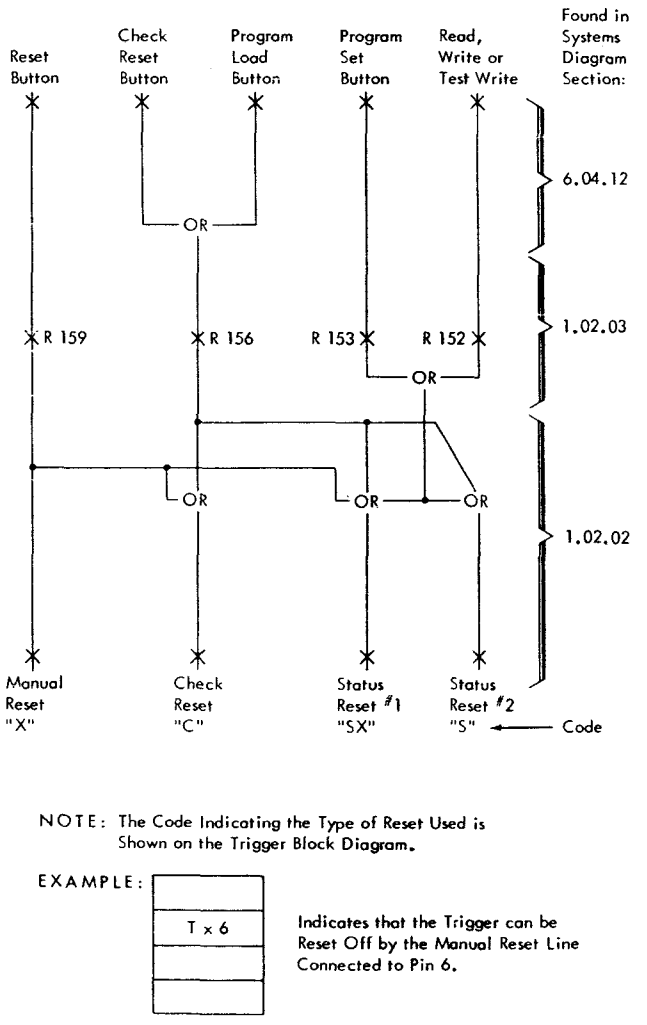


Figure 18. Trigger Manual Reset

Single Shot Multivibrator

A "single shot" circuit, as used in RAMAC, is a monostable multivibrator which, when impulsed by a positive shift, produces an output pulse of a predetermined length. A single shot circuit is used whenever a pulse of a given length is required. The start of the pulse is determined by the time at which the single shot is triggered by the positive shift, and the end of the pulse is determined by the delay introduced by reactive components within the single shot.

We may recognize two differences in single shot pulse requirements:

a. Relatively short, accurately timed pulses, such as used for timing purposes.
b. Longer pulses not so accurately timed, used to provide a "minimum delay." The requirement is that, provided a given minimum delay is obtained between start and end of pulse, the length of the pulse is not critical.

These two requirements lead to the use of two types of single shot circuits. For pulses where the timing is critical, a multivibrator with an LC tank circuit is used. The inductance of the coil in the tank circuit is adjustable, so that the length of the output pulse is adjustable. For the pulses where timing is not so critical, a multivibrator with capacitor coupling between left grid and right plate is used. The value of the capacitor is chosen to give the desired pulse length and is mounted externally.

Adjustable Single Shot: SS302

The SS302 unit is used to produce accurately timed pulses. The basic circuit is shown in Figure 19. The tank circuit is mounted on a separate pluggable unit, CU302, and the diode is part of a third pluggable unit, DD301.

The left grid is biased more negatively than the right grid so that the stable state of the multivibrator is with the right tube conducting. In this state the right plate voltage is low and the output is down. A positive pulse applied to the input is differentiated by the input "C."

The resulting positive peak raises the left grid voltage above cut off, so that the left tube starts to conduct. As the left tube conducts, its plate voltage drops. This drop is applied to the right grid through coupling capacitor "C_c"; the right grid voltage is lowered and conduction through this tube decreases. The result of the shifts at the two grids is to turn the left tube on and to cut off the right tube. (The action is similar to the flipping of a trigger described earlier.) The right plate is now high.

The current which starts to flow through the left tube also flows through the LC circuit. Damped oscillations are set up, and the current through the left plate oscillates. During the first half cycle of oscillation, the plate voltage decreases from +140v to a minimum value, then increases back to +140v. (See Figure 19.) During the second half cycle, the voltage would increase beyond +140v, but the diode across the LC circuit becomes conducting and effectively shorts out the tank circuit. The result is that only one negative voltage pulse has been produced at the left plate. The frequency, or length, of that pulse is determined by the tank circuit time constants.

At the end of the "half cycle of oscillation," the left plate is again at +140v. The rising left plate voltage and rising right-grid voltage (through "C_c") cuts off the left tube and turns on the right tube; the output, after being high for a period of time equal to half an oscillation of the tank circuit, is now down again.

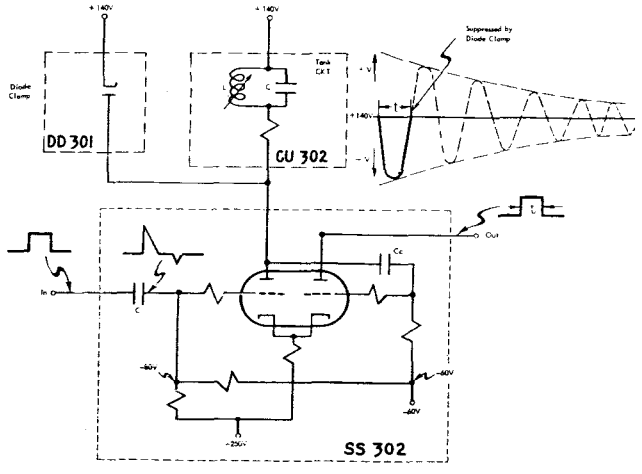


Figure 19. Basic Circuit of Single Shot SS302

The output pulse length can be adjusted by changing the time constant of the LC circuit. For this purpose, the inductance of the coil has been made adjustable, giving a range of output pulse lengths from 2 to 5 micro seconds. The position of the core within the coil can be varied by screwing the core in or out as required. If a little more than 5 microseconds delay is required, the time constant may be further increased by adding an external fixed capacitor across the capacitor in the tank.

Non-Adjustable Single Shot: IN307

An IN307 unit may be used when long output pulses are required and the desired tolerance on the pulse length is not closer than about 15%.

The unit contains two inverters. By cross connecting the grid of one inverter to the plate of the other, a multivibrator circuit is formed. The basic circuit is shown in Figure 20. Observe that the circuit is completed by the external addition of a lead and certain components, in particular capacitor "C_c" which determines the length of the output pulse. The voltage values indicated on the diagram are approximate, and will be used as a help in explaining the circuit operation. In the stable state, the left tube is conducting, and point "A," Figure 20, is at +2v. Point "B," on the other side of the coupling capacitor "C_c," is at +140v, the right plate potential.

The trailing edge of a positive plate level pulse is differentiated at capacitor "C_1," giving a negative spike at point "A." This voltage drop cuts off the left tube causing its plate to rise. The rise of the left plate voltage through the voltage divider causes the right grid to rise. The rising of the right grid causes this tube to conduct. With full conduction, the voltage at point "B" drops from +140v to about +30v. This drop of 110v is impressed across capacitor "C_c" to cause point "A" to drop 110 volts below its original +2v or to −108v. Point "A" now begins to rise toward +140v as capacitor "C_c" discharges through resistor "R." The values of resistor "R" and capacitor "C_c" in this RC network determine the discharge rate of "C_c." To make time *t* in Figure 20 equal to 180 microseconds, "C_c" = 330 $\mu\mu f$ since "R" always = 1 MEG. When point "A" reaches about −8v, the left tube will again conduct, causing its plate voltage to go down, cutting off the right tube and making its plate rise. The capacitor "C_c" now charges up causing point "A" to return to +2v. This charging continues until the original static state is reached with 138v across capacitor "C_c."

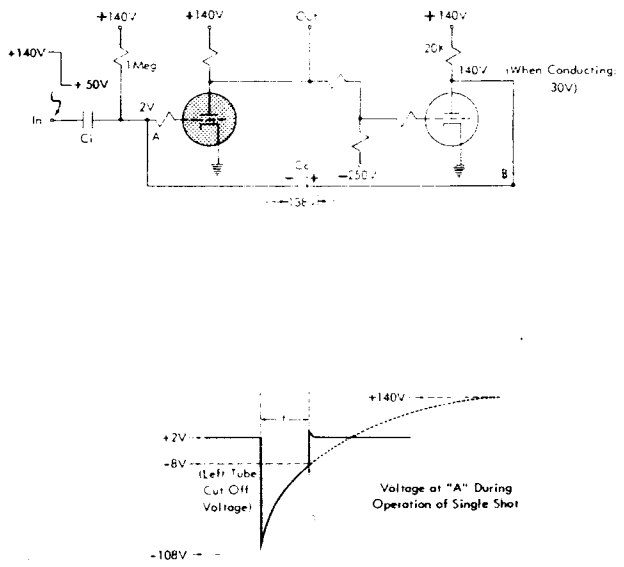


Figure 20. Basic Circuit of Single Shot IN307 (Left Tube Conducting)

The output pulse is usually obtained from the left plate, giving a positive pulse, but it may be obtained from the right plate to give a negative pulse.

Voltage Amplifiers (AM, AMI)

Amplifiers, as such, perform no logic function. They are used mainly to amplify weak signals from certain circuits. These signals are usually at non-standard levels, but after amplification will generally be shaped and "level set" to a standard level. It is to be expected that amplifier circuits will vary appreciably from one pluggable unit to the other. The common feature of all voltage amplifiers, with few exceptions, is that a weak signal applied to the grid will appear as an amplified signal at the plate. A notable exception is the AM316 unit, which is not an amplifier at all, but chiefly a gating or switching unit. The special features of each AM type circuit are reviewed in "Component Circuits," under the respective circuit code numbers.

Current Amplifiers (CD, RD)

These units are used where current rather than voltage is to be amplified. The load is in series with the plate, so that a small voltage change at the grid produces a large current change through the load. Each CD or RD unit uses a type 6350 tube.

Current amplifiers are used chiefly in the matrix and core buffer circuits and to drive mercury relays. The output signals are thus non-standard, and vary with each application. The main features of each pluggable unit are reviewed in the "Component Circuits" under the respective circuit code numbers.

Cathode Followers (K)

Cathode followers are widely used throughout RAMAC circuits as power amplifiers. The chief advantages of a cathode follower circuit are high input impedance and low output impedance.

The plate of the cathode follower is connected directly to +140v and the output is connected directly to the cathode, which has a load resistor between it and −60v. A voltage divider network at the input insures that the grid voltage will be between +12v and −38v. This choice of grid voltages allows the tube to conduct all the time, and merely varies the amount of conduction. Greater conduction, caused by a rise in grid voltage, will be reflected by a rise at the output. Thus the cathode voltage follows the grid voltage.

In actual practice, the cathode voltage will be slightly higher than the grid voltage, and since the voltage amplification factor of a cathode follower is less than 1, the amount of difference will vary with the voltage at the output. Since the difference between grid and cathode voltages is about 1 volt, it is usually ignored.

The low impedance (stable voltage level) output is of great importance in the use of cathode followers as power amplifiers. This stable output voltage level is obtained regardless of voltage changes in the output load by the following actions within the cathode follower:

1. Suppose that the output load voltage decreases by an increase in load. This decrease in voltage will cause the cathode to become more negative (farther from grid potential), which will increase tube conduction, causing the cathode voltage to tend to rise. These opposing actions balance and the cathode output voltage remains the same as before.

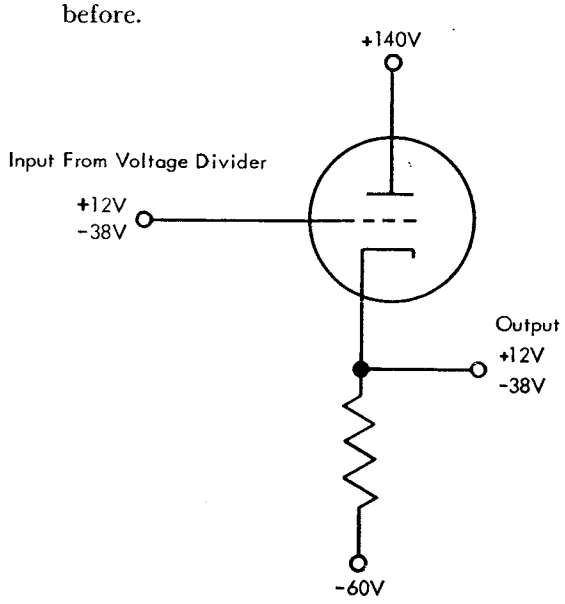


Figure 21. Basic Cathode Follower Circuit

2. Suppose that the output load voltage increases by a decrease in load. This increase in voltage will cause the cathode to become more positive (nearer grid potential). With the cathode more positive, the tube will conduct less, causing the cathode voltage to tend to drop. These opposing actions balance and the cathode output voltage remains the same as before.

An increase or decrease in current through the output load will tend to change the voltage at the cathode, but the voltage here is self regulated as outlined above.

The actual cathode follower pluggable units may perform a logical function in addition to providing driving power. Examples include the AK, IK, and OK units which perform the logical AND, Inverter and OR function, respectively.

Thyratrons (TH)

The thyratrons used in RAMAC are 2D21, heated cathode, xenon filled, tetrode gas tubes. The thyratron has several characteristics which distinguish it from a vacuum tube.

When the thyratron grid is brought up to a critical voltage, the tube fires (conduction starts). Once conduction starts, electron flow through the gas causes ionization, which prevents the grid from exerting further control over conduction. To stop conduction, either the plate circuit must be opened or the plate voltage lowered to a value at which ionization cannot be sustained. Both methods are used in RAMAC thyratron circuits.

There is a delay in the starting and stopping of thyratron conduction due to ionization and de-ionization times. Ionization time for the 2D21 as used in RAMAC circuits is 1 to 2 microseconds. This delay can be decreased by pre-ionization, which is accomplished by allowing a small electron current to flow before the firing pulse is applied to the grid. Pre-ionization is accomplished by raising the screen grid to a sufficiently high potential, as in thyratron units TH303 and TH304. De-ionization time is the time it takes for the grid to regain control after the plate voltage has been removed. Since this time can be several hundred microseconds, it limits the frequency of operation of a thyratron.

THYRATRONS IN RAMAC CIRCUITS

("System Diagrams" Symbol: ATH)

All thyratron circuits used in RAMAC perform a logic AND function; they require two input signals to be made to conduct. The basic thyratron circuit is shown in Figure 22. The coil of the relay controlled by the thyratron is in series with the plate circuit. The grids are maintained at a voltage sufficient to insure pre-ionization.

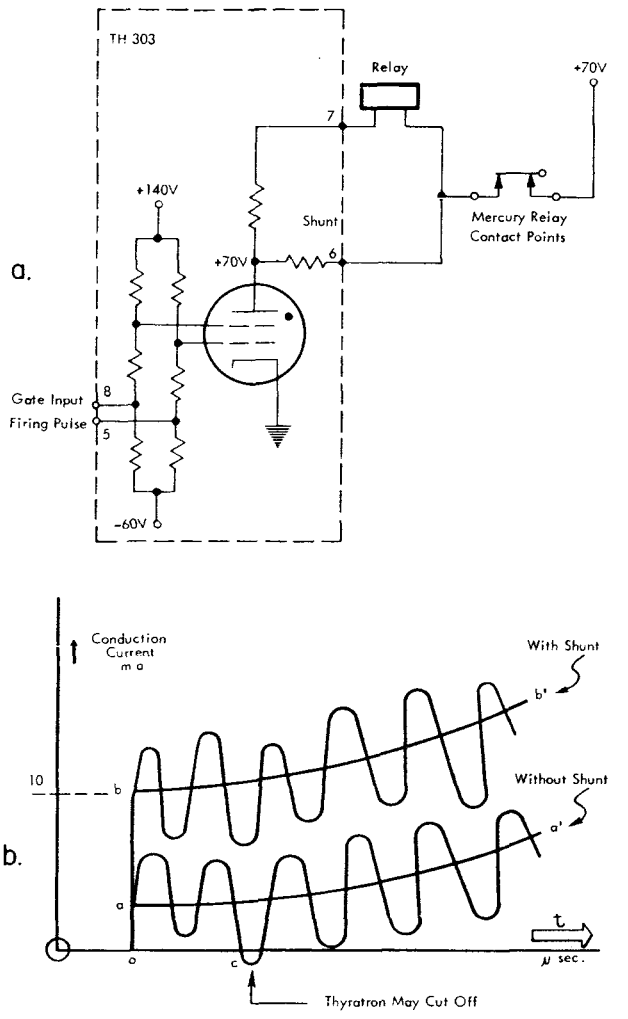


Figure 22. Basic Thyratron Circuit

To fire the thyratron, two input signals are required. Usually a short firing signal is applied to the control grid. The signal is obtained from a thyratron driver unit, IF302, which has a cathode follower output suitable for driving several thyratrons in parallel. This cathode follower output pulse is non-standard, from −40v to +28v. The gating pulse has standard levels +12v to −38v which is applied to the screen grid. When both grid inputs are high, the thyratron fires and current flows through the plate circuit, energizing the relay in the plate circuit.

RESET BY OPENING THE PLATE CIRCUIT

To extinguish the thyratron, the relay points must be opened. When the plate voltage is removed, the thyratron is cut off and the relay drops.

When this type of reset is used, a shunt resistor (part of the thyratron pluggable unit) is connected across the relay coil to the +70v supply, through the points of a mercury wetted relay. The reason for the use of

the shunt is illustrated in Figure 22b. At the instant that conduction begins, a small conduction current, represented by the ordinate "o-a," is established. The current then increases exponentially, due to the inductive reactance of the relay coil, until full conduction is attained. However, within a very short time after firing, the conditions within the gaseous area where ionization is taking place are far from steady. As a result, the current does not increase smoothly along curve "a-a'," but osciliates erratically, somewhat in the manner shown by the wavy line between "a" and "a'." It is possible for the current to decrease momentarily to zero, thus cutting off the thyratron. To avoid the possibility of the tube cutting itself off before it has had a chance to conduct fully, a shunt resistor is added to increase the initial current to about 10 ma (ordinate *o-b* in Figure 22b). The conduction current then oscillates about curve "b-b'" without danger of crossing the zero current axis.

Reset of a Thyratron by Another Thyratron

To accomplish the resetting of one thyratron by another thyratron, the two plates are coupled together through capacitor "C" as shown in Figure 23. The relay coil is connected in series with the plate resistor of the TH303 unit and the +70v line. Since the TH303 unit is used only as a reset unit, it contains the coupling capacitor but no shunt resistor, and its plate resistor has a different value because there is no relay in its plate circuit.

One of the two thyratrons will continue to conduct until the other is fired. Following is a description of this resetting action.

Assume that TH303 is conducting, energizing the relay. The voltage at point "A" will be about +12v. Since TH304 is cut off, the voltage at "B" is +70v, giving a drop across "C" of 58 volts. When TH304 is fired, the voltage at point "B" drops to +12v, forcing the voltage at point "A" to drop instantaneously to −46v. An instantaneous −46v at the plate of TH303 cuts it off. The voltage at point "A" then rises exponentially to +70v as the capacitor "C" charges.

When TH303 is now fired, the process is repeated in the other direction cutting off TH304.

The transient change in plate voltages is shown in Figure 23a. TH303 is initially conducting. When TH304 is fired, the capictor potential drops about 58v, then charges up and peaks a little above +70v due to the inductance of the relay coil. When TH303 is fired, its plate drops about 58v. The capacitor again

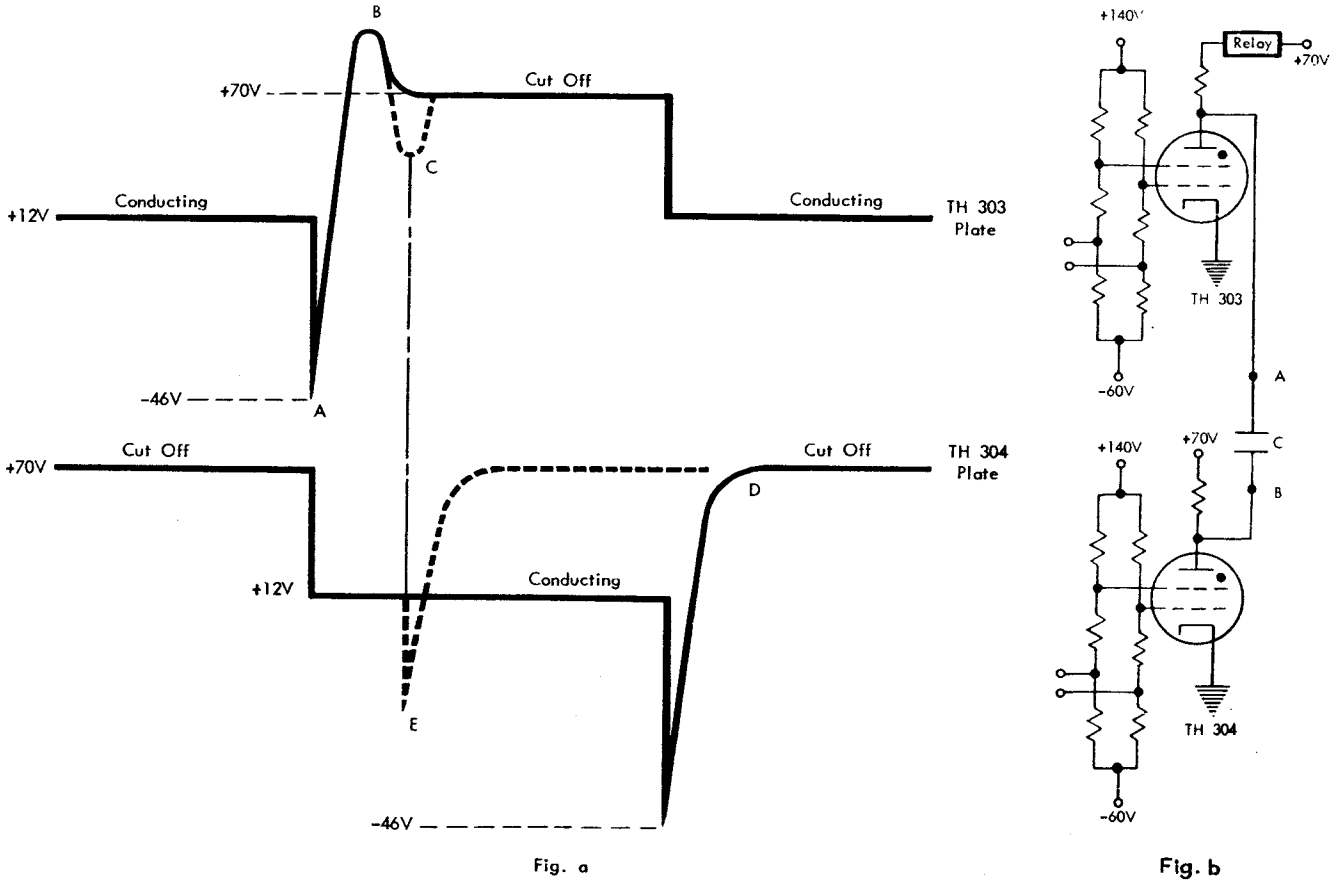


Figure 23. Reset of a Thyratron by Another Thyratron

charges, and since TH303 has no inductive load, its plate voltage rises without overshoot, as shown at "D."

The shunt resistor (across the relay coil) is not required in this type of reset. The effect of a shunt is illustrated by the overshoot shown in dotted lines at "C." This overshoot might be large enough to drop the plate voltage of TH304 to cut off, as shown at "E." The large current peaks obtained from the capacitor on switching insure a satisfactory operation of the thyratrons without the shunt resistor.

Mercury Wetted Contact Relays (MR)

Mercury relays are used in RAMAC as circuit breakers. The relays consists of a pair of N/O and N/C contacts. an armature, and a small pool of mercury sealed within a glass capsule in an atmosphere of hydrogen at a pressure of 225 PSI (Figure 24). Capillary action of the mercury causes it to constantly bathe the operating contact element. The capsule is located in the center of the relay coil. The operating contact element is held against the N/C points under the spring tension of the reed. Since the armature is off center within the capsule, energizing the coil will cause the armature to seek the center, causing the operating element to transfer to the N/O points.

For further description of construction and operating characteristics, see "Component Circuits."

Modified Binary Counters

Four capacitor input triggers and an inverter may be connected as shown in Figure 25 to form a circuit that will count to nine and then return to zero. Assume that all triggers are OFF and we have zero stored in the counter.

The *first* negative input pulse to trigger 1 turns this trigger ON. One is now stored in the counter.

The *second* negative input pulse turns trigger 1 OFF, causing the right plate voltage to drop. This negative

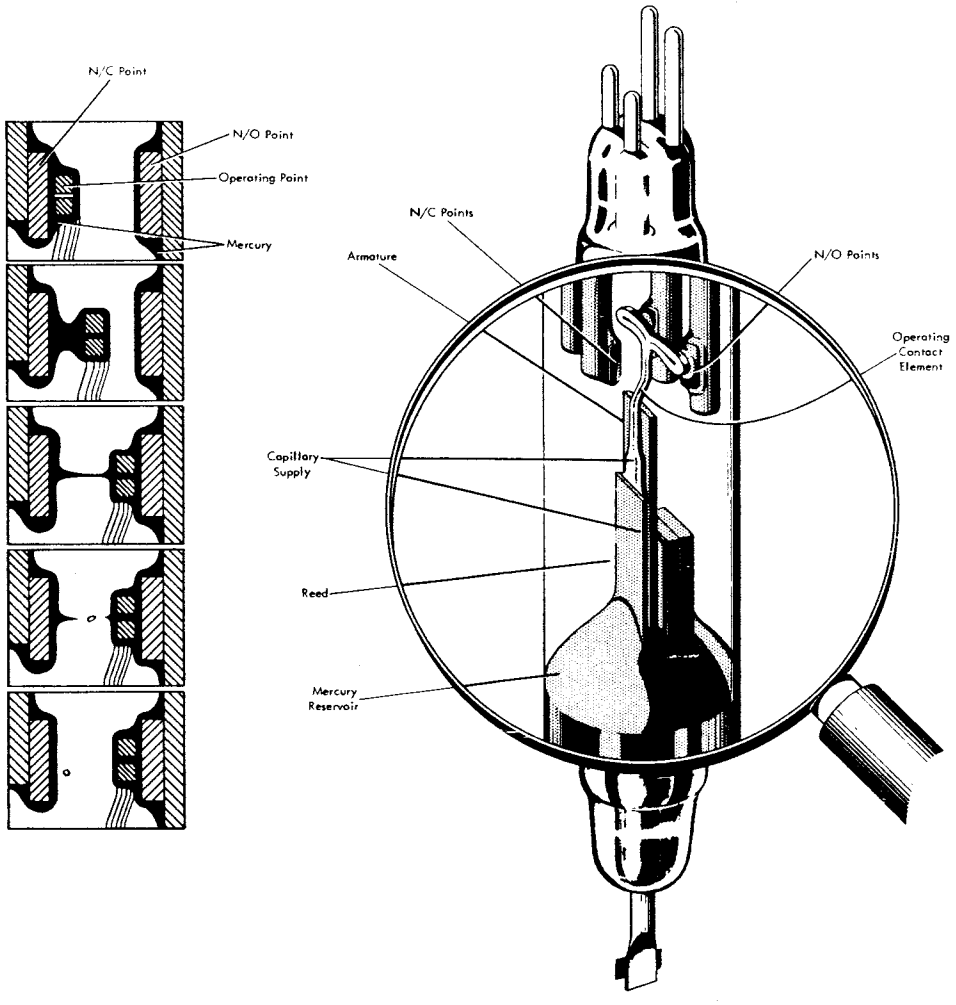


Figure 24. Mercury Wetted Contact Relay (Energized)

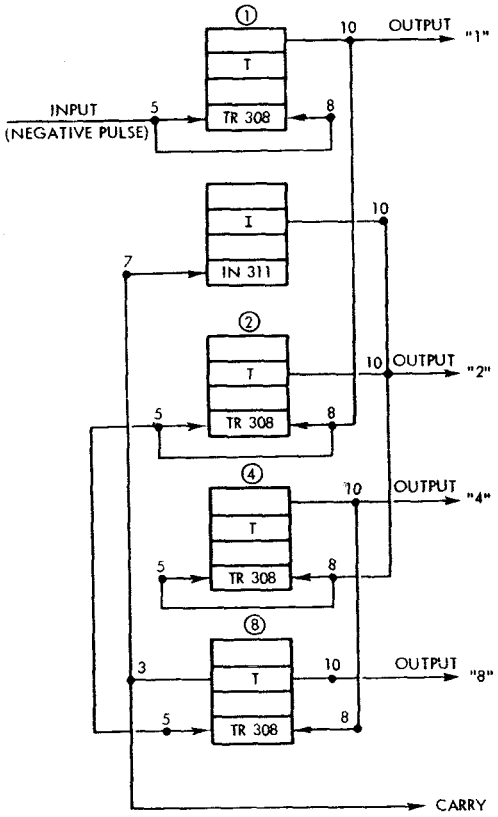


Figure 25. Modified Binary Counter

shift from pin 10 turns trigger 2 ON, but does not affect trigger 8 since it is already OFF.

The *third* negative input pulse turns trigger 1 ON. The positive shift from pin 10 of trigger 1 does not affect trigger 2. Triggers 1 and 2 are now ON.

The *fourth* negative input pulse turns trigger 1 OFF. The negative shift from pin 10 of trigger 1 turns trigger 2 OFF. The negative shift from pin 10 of trigger 2 turns trigger 4 ON.

The *fifth* pulse turns trigger 1 ON. Trigger 4 is still ON.

The *sixth* pulse turns trigger 1 OFF and trigger 2 ON. Trigger 4 is still ON.

The *seventh* pulse turns trigger 1 ON. Triggers 2 and 4 are still ON.

The *eighth* pulse turns trigger 1 OFF, which turns trigger 2 OFF, which turns trigger 4 OFF, which turns trigger 8 ON.

The *ninth* pulse turns trigger 1 ON. Trigger 8 is still ON.

The *tenth* pulse must turn all the triggers OFF. This is accomplished as follows: The input pulse turns trigger 1 OFF. The negative shift from pin 10 turns trigger 8 OFF and attempts to turn trigger 2 ON. However, the voltage rise at pin 3 (left plate) of trigger 8 is inverted and applied to pin 10 (right plate) of trigger 2. This clamps **trigger 2 so** that it cannot turn ON. Thus all **triggers are OFF.**

Trigger 8 provides a **positive output** shift from the left plate on the *tenth* **pulse only. This** carry pulse may be inverted and used as **the input to** another modified binary counter, forming **a 2 position** counter that will count to 99.

Any counter trigger **may have an** amount set in it by plate pullover before **the negative input** pulses start. The input pulses will **then cause the** counter to advance from the number **initially set in it.** This principle is used in several counters **in RAMAC.**

Resetting these counters **is accomplished** by electronic reset of each trigger **before new** amounts are stored. (See "Trigger Reset.")

Overbeck Ring (Figure 26)

The Overbeck ring is used to supply timed pulses within computer circuits much as cam operated circuit breakers supply timed pulses on mechanical machines. It consists of a set of triggers with a common input from the *ring drive line* which carries pulses supplied by the process drum.

Figure 26 shows an 8 position Overbeck ring with positions 4-7 left out for clarity. Initially the triggers are reset OFF with the exception of the *home* trigger, which is ON. Each negative input pulse will turn OFF the trigger that is ON. The fall of the voltage at pin 10 of the trigger being turned OFF will grid flip the next trigger ON. This continues through a closed ring, since pin 10 of trigger 8 is connected back to pin 8 of trigger 1. Note that the output is taken from pin 10 of each trigger.

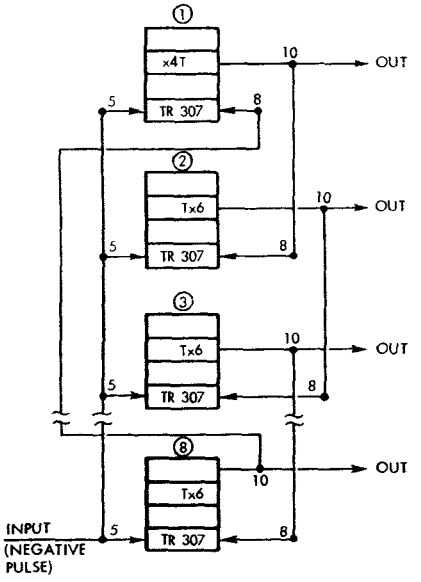


Figure 26. Overbeck Ring

Basic Machine Timings

All operations performed by RAMAC are based on the transfer of data. This transfer of data falls into 6 categories, each of which will be treated in separate sections of this manual, in the following order:

1. The transfer of data from track to track on the process drum.
2. The transfer of data to and from the file.
3. The transfer of data from punched cards.
4. The transfer of data to punched cards.
5. The transfer of data to a printed report.
6. The special transfer of data that performs arithmetic.

In order to control the data as it is written or read from the drum or file, it will be necessary to have basic timing pulses available. These pulses which are recorded on the drum clock track, will tell the machine the exact position of the drum at any instant (Fig. 4).

The process drum clock track also has a gap which defines the beginning of a drum cycle. Because we have a number of different types of cycles, it is further necessary to define these cycles and place them in some logical sequence. In this manner the RAMAC can keep track of all data as it is transferred.

Drum Gates and Pulses

Clock Pulses (Figure 28)

816 recorded spots on the clock track are used to develop the other machine pulses and gates. The 208 μs gap signals the end or the beginning of a drum cycle. The 100 character positions with 8 bits result in 800 pulses of 12 μs duration and an additional two characters, character early and character late, result in 816 pulses. The clock amplifier (3.10.30) takes the small sinusoidal voltages, shapes and amplifies them to standard level pulses.

Reference Mark (Figure 27)

The reference mark signals the start of a drum revolution. It is generated on 1.01.00 by Schmitt trigger 1H2. The lack of amplified drum clock pulses during the gap allows the 470 $\mu\mu f$ capacitor to discharge. When 1H2-7 reaches −6v, 1H2 flips, causing 1H2-10 to drop. The resulting negative spike from the 130 $\mu\mu f$ capacitor is shaped by 1G3a. The positive spike caused by the reflipping of 1H2 as clock pulses start again has no effect in 1G3a.

Phase Pulses (Figure 28)

The three phase pulses drive the timing rings and help control data flow. ∅A advances the timing rings; ∅B is a delay to allow timing triggers to settle down; and ∅C controls the transporting of data. These phase pulses are generated as follows:

∅A is generated on 1.01.01 by single shot 1Y1, which is triggered by the rise of each clock pulse. 1Y2 is adjusted for a 2¼ microsecond pulse output from 1Y1.

∅B, 3½ microseconds long, is generated by 1V1, which is triggered by the inversion of the fall of ∅A.

∅C, 3 microseconds long, is generated at 1T1 by the inversion of the fall of ∅B.

Bit Pulses (Figures 29, 31)

Bit pulses are used to select data bits from a drum track. Each is available on 1.01.05 from pin 10 of its own trigger. The 8 bit triggers form an Overbeck ring.

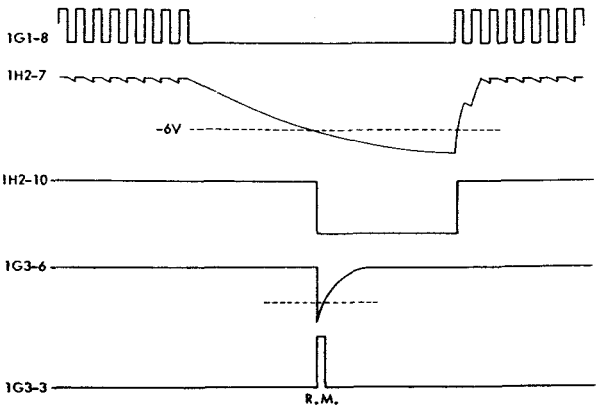


Figure 27. Development of the Reference Mark Pulse

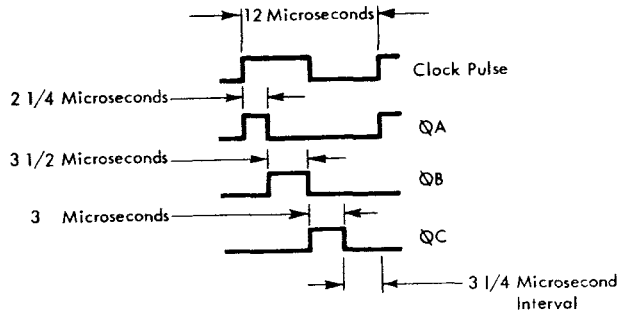


Figure 28. Expanded View of One Clock Pulse

(See Section 2 for Overbeck ring operation.) 1R4, the Bs trigger, is the only one that is manually reset ON, and is the home position. The bit ring is driven through 1Z2a by the inversion of ØA, which comes from 1Z3 when not clock error and not manual reset are present. Not manual reset is developed on 1.01.02 at 1H3 by plate pullover by the first RM after a manual X reset. Not clock error will be developed later.

Character and Field Ring Gate (Figures 30, 31)

The character and field ring gate signals the presence of the data containing area of a track beneath its read-write head, and is high from the beginning of C99 through C00. It is developed on 1.01.06 from 1M5-3. A manual reset before processing starts causes 1M5-3 and 1L5-10 to be low. The first RM flips 1L5 ON, but the positive pulse from 1L5-10 does not affect 1M5. The first BsØB after RM flips 1L5 OFF. The fall of 1L5-10 flips 1M5, bringing up the character and field ring gate. Note on Figure 31 that the first BsØB after RM is BsØB of C99. There is no BsØB during CE.

The character and field ring gate is dropped by the inversion of F0 carry to 1M5-8. F0 carry results from turning off the F0 trigger at the end of C00 time (1.01.09).

Character Gates (Figures 29, 30)

The character gates are used to select a specific character or group of characters from the drum track. Each

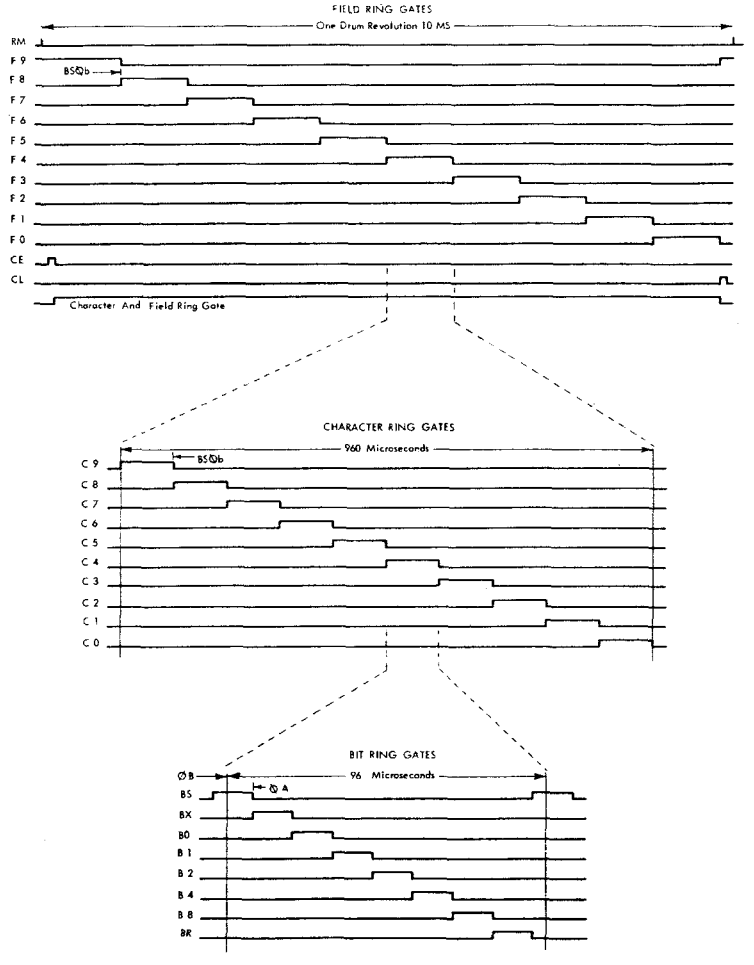


Figure 29. Timing Pulses and Gates

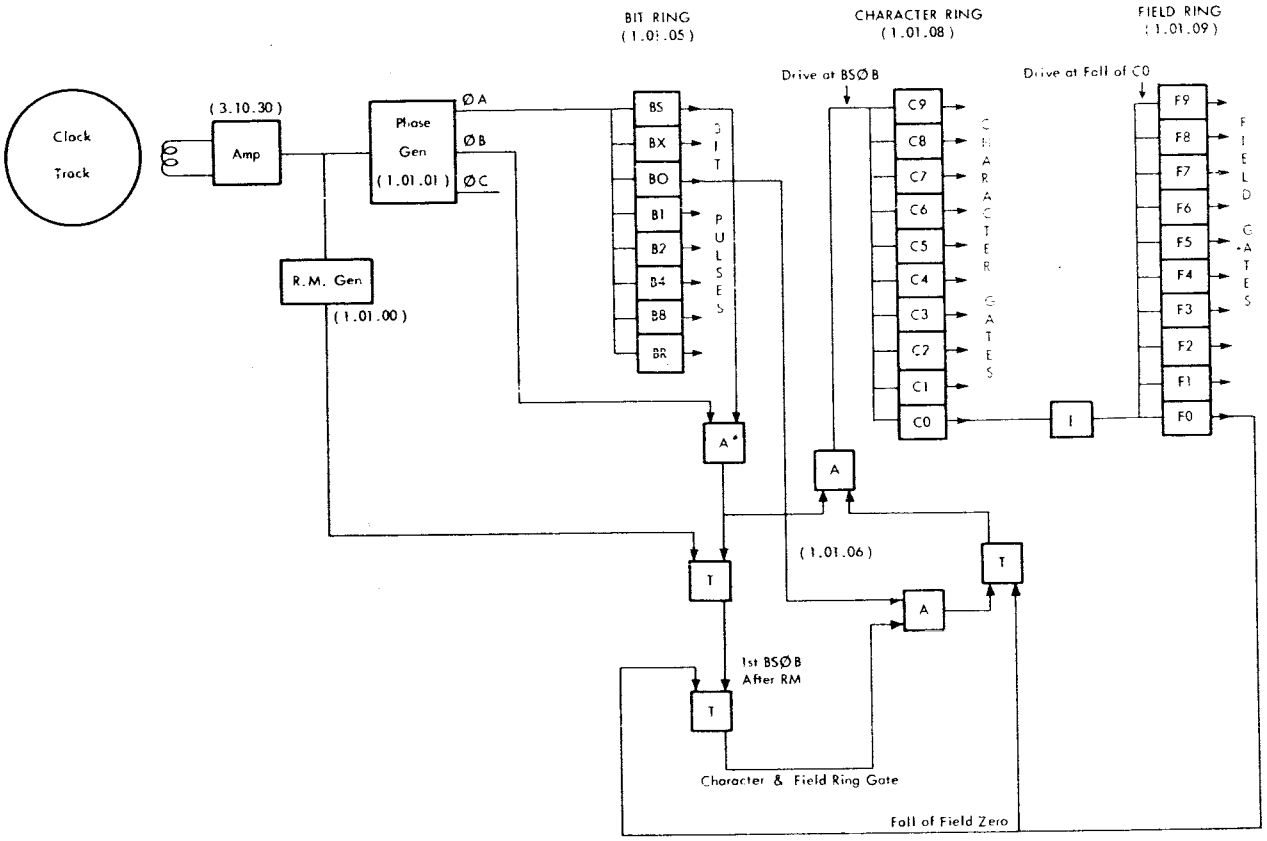


Figure 30. Timing Ring Drives

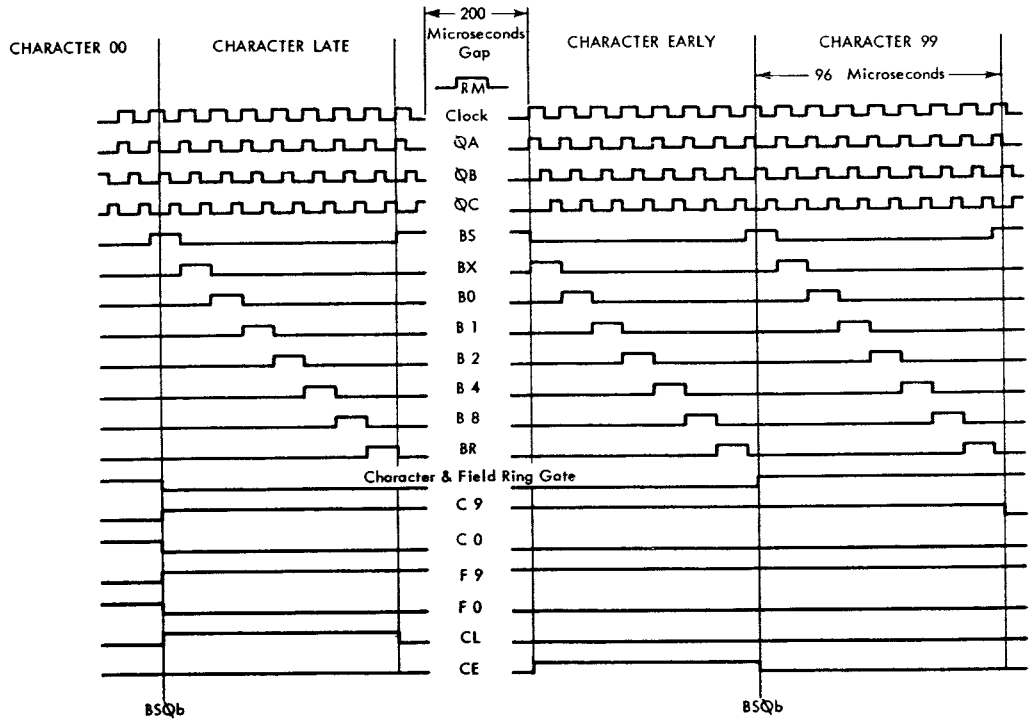


Figure 31. Gates in the Vicinity of the Gap

is developed by its own trigger in a 10 trigger Overbeck ring (1.01.08). The C9 trigger, 1Q5, is the home position. The ring is driven by Bs∅B from 1.01.06, where it is gated by the output of 1M4-10. 1M4 is flipped ON from 1P5a at B0 of C99, which is the first B0 during the character and field ring gate. The gating of the character ring drive is necessary since there are 102 Bs∅B pulses during a drum cycle, but only 100 of these may be allowed to drive the character ring in order to keep it in time with the drum.

The output of the C9 trigger is gated by character and field ring gate at 1Q6a on 1.01.08, since the C9 trigger is ON from the end of C00 through C99.

Field Gates (Figures 29, 30)

The field gates are used with the character gates to select a group of characters from a drum track. Each is developed by its own trigger in a 10 trigger Overbeck ring. The F9 trigger, 1Q7, is the home position. The output of 1Q7 is gated by the character and field ring gate, since it is ON from the end of F0 through F9. The ring is driven from 1.01.06 by the inversion of C0. C0 provides a positive shift when the C0 trigger is flipped OFF (1.01.08).

Character Early (Figure 31)

Character early is a gate one character in length coming just before C99, and signalling the start of the data containing area of a drum track. It is developed on 1.01.07 from 1M6-10. 1M6 is flipped ON when 1N6 is flipped OFF by the fall of Bs which is the rise of the first ∅A after RM. Note that 1N6 was flipped ON by RM.

Character early gate falls when 1M6 is flipped OFF by the fall of not character and field ring gate, which comes from 1M5-10 on 1.01.06 at the leading edge of C99.

Character Late (Figure 31)

Character late is a gate one character in length that comes just after C00, signalling the end of the data containing area of a drum track. It is developed on 1.01.07 from 1L7-10. 1L7 is flipped ON by the fall of not F0 carry, which is at the fall of C00. Character late gate falls when 1L7 is flipped OFF by the fall of 1K7-10, 1K7 is flipped OFF by the next Bs after it was flipped ON by BxCL from 1P5b. Since BxCE also occurs during the not character and field ring gate, it will also flip 1K7 ON, but 1L7 will not be affected, since it is already OFF.

Not Clock Error

Not clock error allows the bit ring to advance (1.01.05). The absence of the not clock error gate indicates that the timing rings are out of sequence, and a clock error exists. Not clock error is developed on 1.01.02 at 1H4-3. 1H4 is manually reset pin 3 high, and will remain thus unless a clock error occurs.

Clock error is indicated by flipping 1H4 ON through plate pullover. If Bs or C9 or F9 triggers are not ON, or the character and field ring gate trigger is ON (either Bs, not gated C9, not gated F9, or not character and field ring gate is low) at RM, the low output of 1H6 will be inverted and anded with RM at 1N4b to plate pullover 1H4.

Machine Cycles

The five basic types of machine cycles,I, R, W, D, and P were explained briefly in the first section. These machine cycles nearly always correspond to a 10 millisecond drum cycle defined as one reference mark to the next. The exception occurs when the process unit is interlocked in a particular cycle awaiting completion of some mechanical action, i.e., servo, reading a card, etc. At this time a machine cycle may be equivalent to several drum cycles.

The sequence of these cycles is illustrated in block form in Figure 32. For a normal track to track transfer three cycles, IRW in that order, are sufficient. The progression here is automatic. As shown in the diagram on some operations a different sequence must be followed. After any W cycle the RAMAC must analyze the instruction or operation further. If it is a file write operation (T_2=R) an IRWRW sequence is necessary so that the information written on the first W cycle may be read back and compared for accuracy.

In the event of a servo (T_2=J), a copy operation (card reader), a P flag, a test read/write or inquiry (console operation), additional time is necessary to energize and test relays, so an IRWDP sequence is taken. In certain special cases even this is insufficient time so the sequence may become IRWDPDDP as shown by the dotted line.

In all 5 types of cycles there are two key triggers for each, the cycle ready trigger and the cycle trigger. The cycle ready trigger comes up before the end of the previous cycle, as soon as the machine has decided what the next cycle will be. The next RM brings on the cycle trigger for that cycle ready trigger, and this trigger will be on until CLBR. One cycle ready trigger coming ON turns OFF the previous one. This sequence is illustrated in Figure 33 and 34.

IRW

The following three 10 millisecond cycles are necessary for a 30 millisecond track to track transfer: I (instruc-

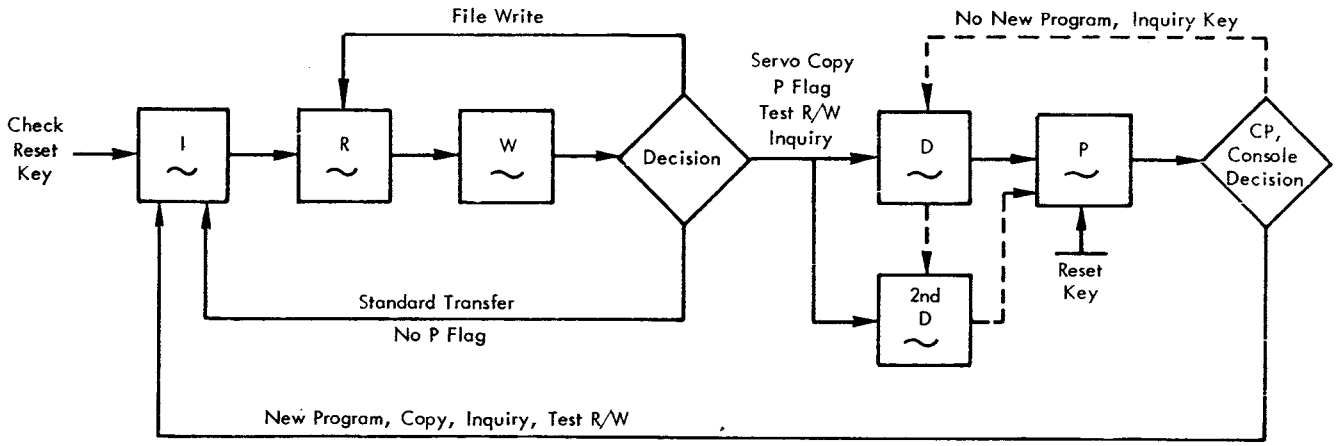


Figure 32. Cycle Sequence Flow Chart

tion) cycle, R (read or from) cycle, W (write or to) cycle.

OBJECTIVES

1. I cycle ready at start of processing.
2. I cycle at first RM.
3. I cycle down at CLB1.
4. R cycle ready and then R cycle (RM to CLB1).
5. W cycle ready and then W cycle (RM to CLB1).
6. Return to I cycle.

I Cycle Ready. To start processing, I cycle ready trigger (1C2-1.03.04) is turned ON by S reset. Depressing the program set key (6.04.12) will develop an S reset as well as establishing the desired program level.

I Cycle. I cycle trigger (1E2-1.03.04) will come ON with I cycle ready ON and the next cycle start pulse,

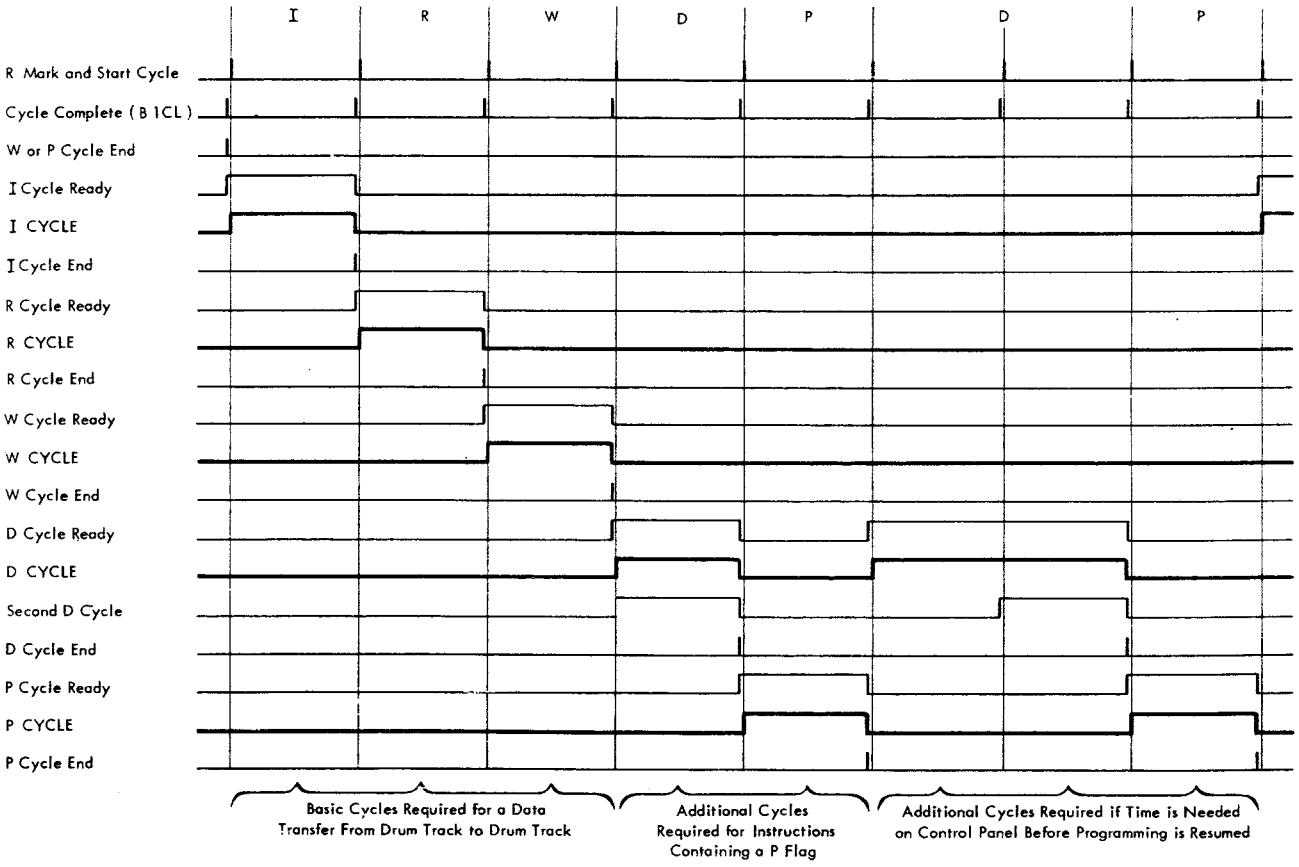


Figure 33. Machine Cycle

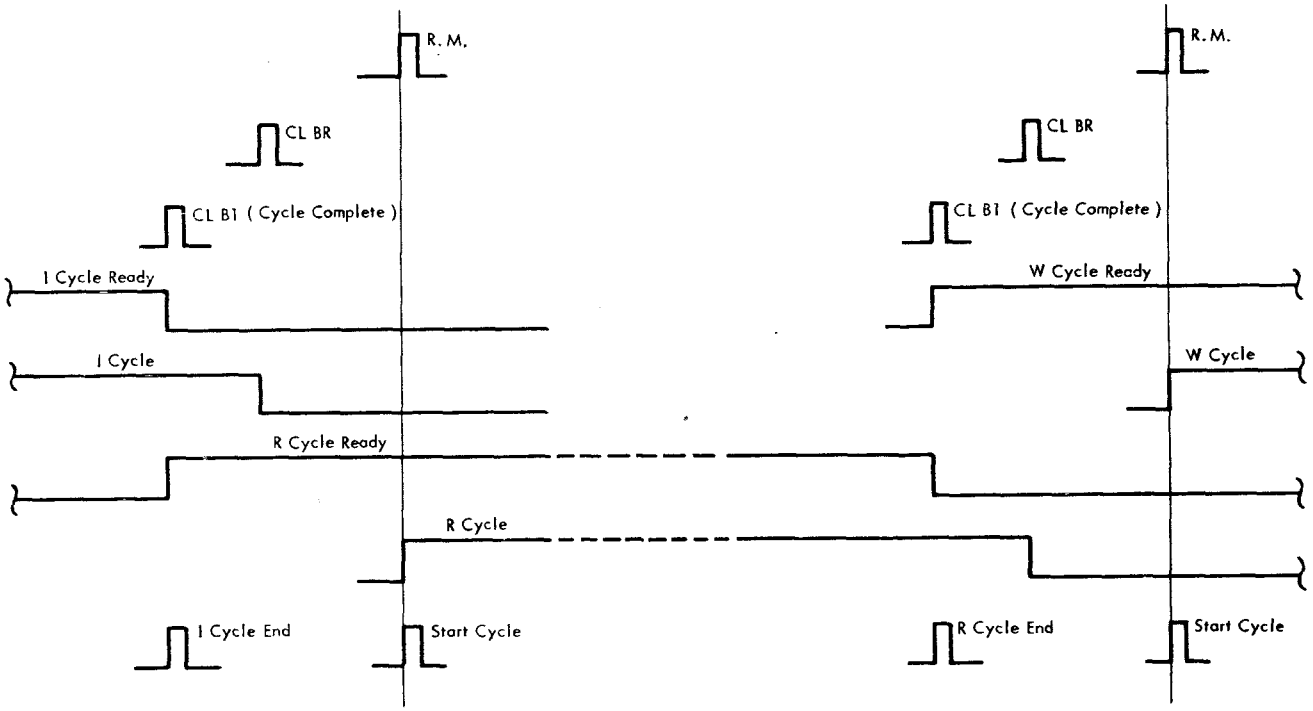


Figure 34. Execution Pulses for Cycle Sequencing

developed on 1.02.09 from a sequence reference mark.

Notice that the development of cycle start is dependent on a number of conditions such as no error indications and no calls for a machine stop. The master stop trigger may be turned 3 pin high by a start developed on 1.02.01. This Schmitt trigger (1U9-1.02.01) is turned 10 pin high through the R161 points. R161 is picked on 1.02.03 by depressing the program start key (6.04.12). It may also be picked by the reader start and program load switches, which will be covered later.

Cycle Complete. I cycle will be complete after one drum revolution. The cycle complete pulse at 1G2 (1.03.04) develops I cycle end pulse which turns off I cycle ready trigger at BrCl, while I cycle remains on. The cycle complete pulse is developed on 1.02.08. The trigger at 1G8 (1.02.08) is turned 10 pin high every B0Cl and 10 pin low every B2 during normal operation. At B1Cl the cycle complete pulse is developed at 1D10a if the previous operation has been completed. The cycle complete gate trigger at 1H9 is turned 10 pin high when none of the six inverters are conducting, i.e., all operations are complete.

I cycle trigger (1.03.04) will be turned off at ClBr if R cycle ready has already been turned on.

R Cycle Ready and R Cycle. The R cycle ready trigger (1C4-1.03.05) will come on when the I cycle ready trigger is turned off (ClB1). This in turn conditions the R cycle trigger, allowing it to be turned on with the next start R cycle. This is actually a cycle start (RM), conditioned on 1.02.10. As the machine advances from one cycle to the next it will always proceed as far as possible without interfering with a previous operation which may still be in process. When one servo-operation (T_2=J) follows another and the first servo is not complete (track not located) the second servo will be suspended in R cycle ready until the AI (1R10b-1.02.10) is cut off. This will be covered more thoroughly in the file section.

R cycle ready can be brought up in one other manner, following a W cycle, at 1B3a (1.03.05). This occurs on a file write operation (T_2=R) and results in IRWRW sequencing.

The conclusion of R cycle is the same as I cycle. R cycle ready off at ClB1 and R cycle off at ClBr.

W Cycle. W cycle sequence (1.03.06) will be the same at I and R cycle, starting with R cycle end. The completion of W cycle, however, can be accomplished in a number of ways. Notice in the cycle flow chart (Figure 32) there are three possible paths after W cycle: R, I, or D cycle. The or switch 1B5 (1.03.06) handles all these possibilities to end W cycle. The conditions anded at 1B4b are used only by the CE for single cycle multiply.

Return to I Cycle. At this point a decision must be made to determine the type of cycle to follow W cycle. The more common is a return to I cycle. The conditions allowing this return are found at 1A2 and 1A3 on 1.03.04. Following I cycle ready the sequence repeats itself.

IRWDP

As can be seen in Figure 32 any operation requiring the energization of relays sets up a DP sequence following W cycle. Also an instruction with a P flag turns control of the program sequence over to the control panel and requires a P cycle to provide a control panel impulse. Let's assume an instruction with a P flag. The IRW sequence is the same as above.

OBJECTIVES:

1. Block I cycle ready following W cycle.
2. D cycle followed by P cycle.
3. Return to I cycle.

Block I Cycle. Following W cycle, I cycle is blocked at 1A2 (1.03.04) since P is not blank.

D Cycle Followed by P Cycle. D cycle ready will be turned on at W cycle end (CLBR) at 1A7 (1.03.07). Not store check will be high except during the first W cycle of an IRWRW sequence (servo). D cycle then proceeds as the previous cycles. One variation is the line labeled second D cycle developed at 1F10b (1.03.07). As indicated in the flow chart (Figure 32), this line will be high along with D cycle in the present sequence. It will be up as long as the D cycle delay trigger (1B8) is 3 pin high. This was accomplished on any previous D cycle at 1B9a (1.03.07). P cycle (1.03.08) begins with the end of D cycle and lasts until the following BRCL.

Return to I Cycle. The conditions permitting a return to I cycle following a P cycle are shown at 1A1 (1.03.04). Following a P flag the new program line should be high since the control panel wiring decided which of the 200 program steps to return to. Copy (card reader) would have been high after impulsing the copy-in hub on the control panel.

Additional Sequences

PDDPIRW. When making an inquiry, the reset key places the machine in P cycle ready with an X reset. When the inquiry key is hit, a double delay cycle will be taken (Figure 32) before going to P and IRW. Also, if the program entry hubs or the program advance hubs do not receive an impulse during P cycle to raise the new program line, the RAMAC will return to D cycle. This will be a DD cycle (2 drum revolutions), followed by a P cycle. This will continue until new program is raised.

During this double delay the second D cycle line will be up only for the second D cycle. The D cycle delay trigger (1B8-1.03.07) is turned 3 pin low (also the D cycle ready trigger) at 1A9a at P cycle end. The next cycle complete pulse, instead of developing D cycle end, turns the D cycle delay trigger three pin high for a second D cycle.

IRWRW sequence occurs on a file write operation ($T_2 = R$) and is developed at 1B3a on 1.03.05.

Program Exit Overlap (Optional)

To speed up process time the W and P cycles can be made to occur simultaneously, eliminating the D cycle. Normal IRWDP is a 50 millisecond operation with the D and P cycle used to energize relays. Occasionally a P flag may not require the picking of relays. In this case the delay may be eliminated, resulting in a 30 millisecond operation.

OBJECTIVES:

1. P cycle during W cycle.
2. Block D cycle.

P Cycle During W Cycle. If the not P cycle line is down the P cycle trigger will be turned ON (1.03.08-optional). This line will be down if 1J7 (1.03.11-optional) conducts during a W cycle at CE. Any operation in which the D cycle is necessary will have the program exit overlap feature blocked at this unit.

This is done by turning the trigger at 1F7 10 pin high or cutting off the OR switch at 1E7a. The use of the MR-7 line to gate the CE pulse at 1C9a (1.03.11) is a pretest of control panel wiring to be sure the P flag is not calling for an operation requiring a D cycle; for example COPY IN. Normally, with MR-7 open this line is at 0 volts through a 1.5K resistor (2.09.11). If the program exit called for is wired to COPY IN, this line will be at −30 volts during W cycle through the following circuit: from −60 volts at DB257-9 (1.03.11-optional), through a 1.5 K resistor to copy in hub on 2.07.01, by control panel wire to the program exit hub selected (2.05.03), to MR-7, through a second 1.5K resistor to 0 volts (2.09.11).

Block D Cycle. (1.03.07-optional) D cycle ready can be turned ON when the W cycle end and not W-P cycle is high. This is raised at 1K8b (1.03.11-optional) only if not P cycle is high. Not P cycle will be low during a W-P cycle overlap.

Track To Track Transfer

All data coming to or from the drum must go to the core buffer with one exception (Figure 7). This occurs during I cycle when the instruction is transferred directly from the drum to the instruction register for analysis. During R cycle, data is read from an addressable drum location into the core buffer. On W cycle it is written from the core buffer into some new drum location. In this section we will discuss first the principles of reading and writing on the process drum, and then reading and writing in cores. Then we can examine in detail each type of transfer.

Read and Write Principles

Drum Magnetic Storage

Figure 35 illustrates the form in which bits and characters exist on a process drum track. Assume that the whole track is magnetized in one direction forming a closed magnetic loop, as shown in Figure 35a. Since no lines of force are intersected as the drum revolves, no voltage will be induced in the read coil. Now an area of the track one bit in length is magnetized at the bit 0 position (Figure 35b). The change in magnetic flux lines at the beginning and end of bit 0 will induce a voltage at the read head as the drum revolves. If two adjacent bit positions are magnetized, the flux pattern will be like that shown in Figure 35c for bit 2 and bit 4 of the character "W". The read signal for a "W" is also shown.

No portion of the 100 recording character positions of the drum track is magnetically neutral. If a bit or series of adjacent bits is written, current is drawn continuously through the center tapped write head coil in the *write 1* direction. The absence of bits causes current to be drawn in the opposite or *write 0* direction.

The brass shim between the ferrite pole pieces forces the magnetic flux down into the drum surface to complete its magnetic circuit. This action causes the drum surface to become magnetized. Current flowing through the coil in one direction will cause magnetization in one direction, while a reversal of current will cause magnetization in the opposite direction. Specific exceptions regarding the manner of recording data will be noted for certain special purpose tracks, such as K1 and K3.

Write Logic

The data coming from cores to the read/write head current drivers during W cycle will be 12 μs pulses ($\varnothing$A to $\varnothing$A) for each bit of information. These pulses will cause the write one side of the head current drive unit to conduct, resulting in 65 *ma* of current through the head coil (Figure 36). This same data line is inverted and placed on the write 0 grid of the current driver, causing it to conduct with 65 *ma* of current when no bits of information are coming from cores. Each of the drum heads is addressable by placing some character in the T_2 portion of the instruction. When writing, the T_2 character should allow only one of the drum heads to draw 65 *ma*. To accomplish this the drum head circuitry is arranged in a matrix (Figure 37). The zone portion of the T_2 register conditions the cathodes of the current drivers in the same zone group for conduction. The numeric portion of the T_2 instruction, gates the write data from cores to the grids of three current drivers of the same numeric group. The result will be only one current driver and head in conduction.

Read Logic

During R cycle and I cycle the information written on the drum will be read. All drum heads will be cutting lines of flux as the drum is revolving; therefore, all head coils will have a 1 volt peak to peak signal across them (139.5v to 140.5v). All heads in the matrix, except S and T, feed a common read data line.

During R cycle all but the selected head output must be blocked. The T_1 character will select one of the 27 current drivers in the matrix for conduction in a similar manner as was done during W cycle. Since there is no write gate however, the T_Z line will allow only 5 *ma* of current to flow in the cathode circuit (Figure 37). This 5 *ma* current through the write 0

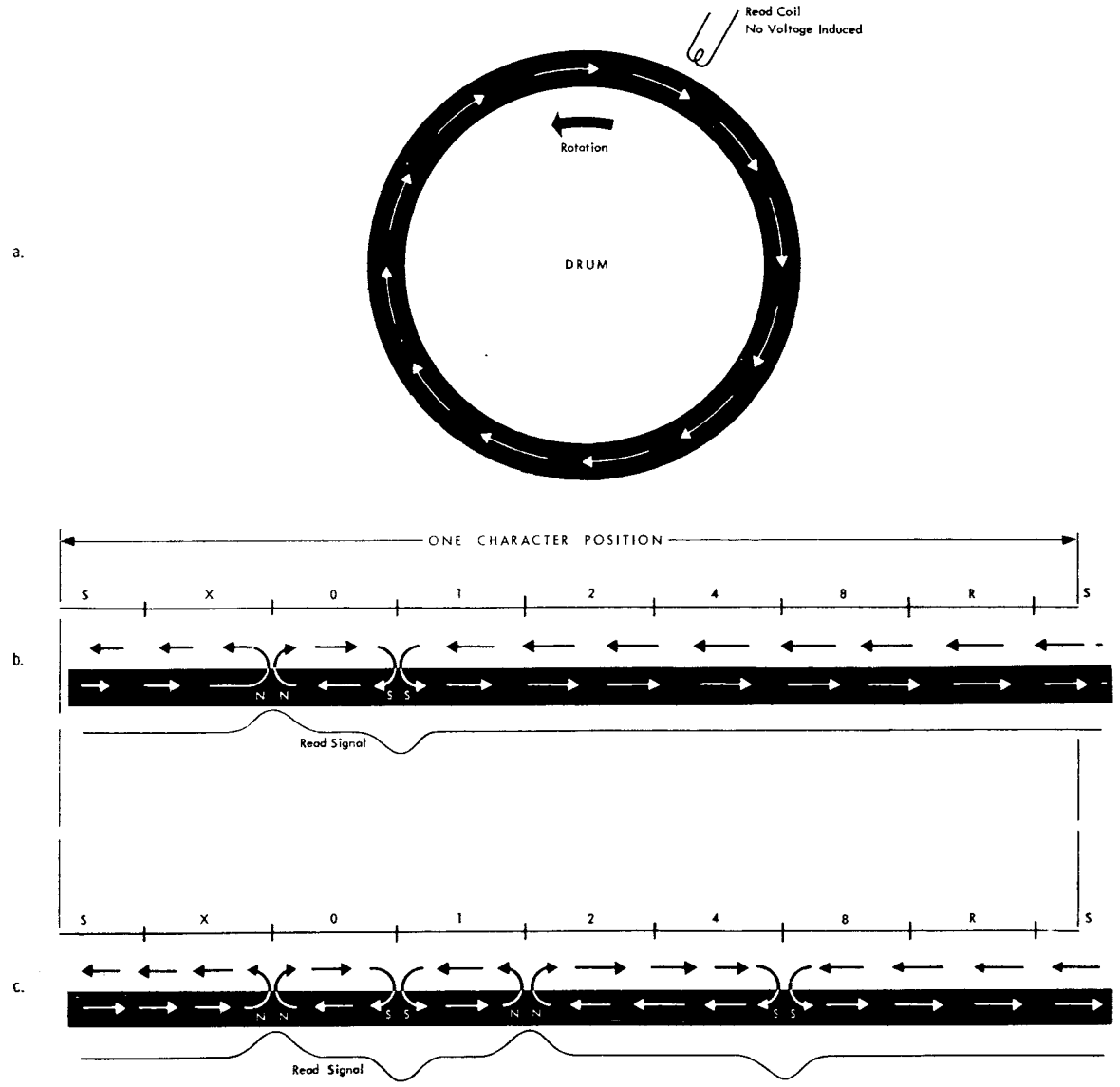


Figure 35. Process Drum Track Flux Patterns

side of the selected head (Figure 36) will drop the plate potential to 138 volts. The common read data line will also be lowered to 138v and the only diode able to transfer the 1v head signal will be that at the selected head. Notice that the three "and" circuits at the bottom of Figure 37 are not true "and" circuits. When both inputs (the TZ line and the write gate) are up, 65 *ma* flows. When only TZ is up, 5 *ma* flows: When TZ is down, no current will flow. Since there is no matrix write data, the three current drivers selected by the TN line will have +10v on their write 0 side. This can be seen in Figure 38.

There are times when we do not want the common read data to reach the read amplifier. When writing or when no head is selected for reading, undesired signals will appear on the common read data line. To control this flow of data we shall develop a matrix read gate and also use a special switching arrangement shown in simplified form in the upper right hand corner of Figure 37. The read data can reach the amplifier input only if the matrix read gate is high and the write gate low.

Three areas of Figure 37, outlined in dotted lines, are drawn and described in detail below.

Selection Circuits

Figure 38 illustrates the circuit action necessary to write a "9" on track C and then to read it. To write, assume the instruction XXXC5301XX which will write the "9" in position 53 of track C. An analysis of T_2 will result in a TN=3, which places the data from cores on the grids of the CD's for position C, T and 3. The

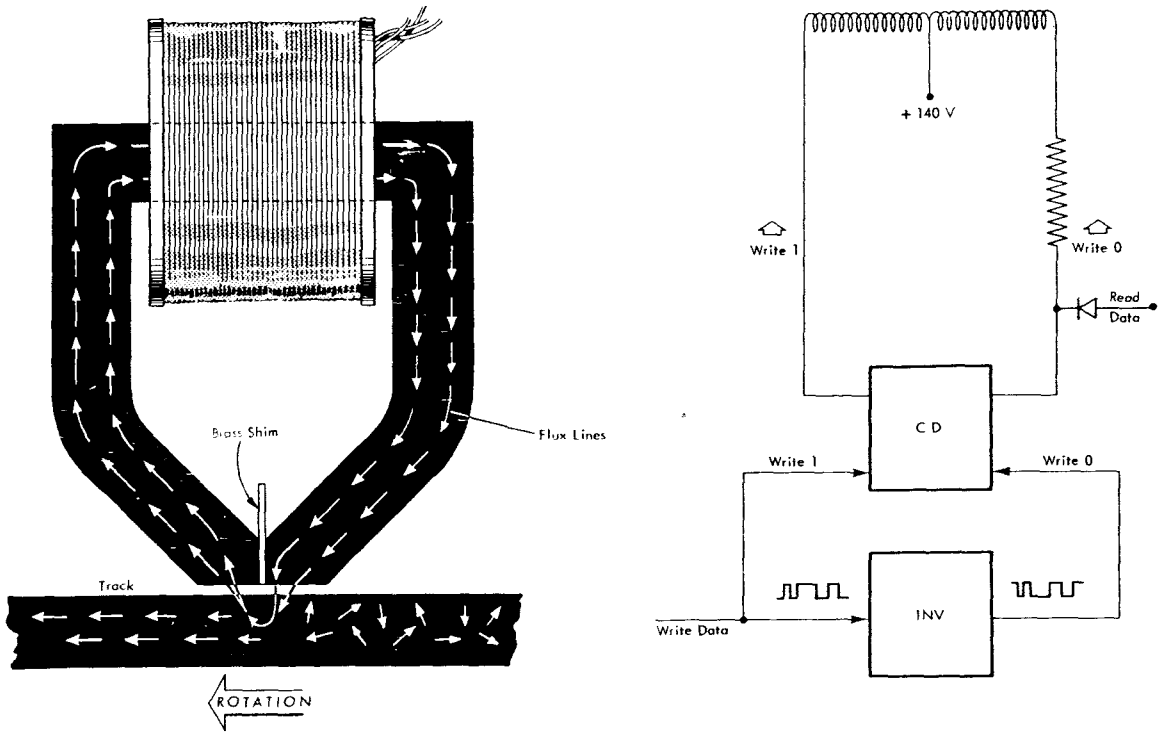


Figure 36. Process Drum Head

grid voltage will vary from −30v to +6v. The voltage placed on the cathode by the zone matrix selection circuits will determine which of the three current drivers conducts and whether it draws 65 *ma* of current for writing or 5 *ma* for reading.

With 0v on the cathode the grid bias is high (+6v) resulting in 65 *ma* of current through the left or right half. With +10v on the cathode the tube barely conducts (−4v bias) with 5 *ma* of current, while +26v on the cathode cuts the tube off. To write, the TZ=12 line is inverted, placing −40v on the plate of 5V7, cutting it off. The write gate is inverted placing − 40v on the grid of 5V1 cutting it off. This means both resistor legs can conduct with electrons flowing from the −60v and the −250v supplies through the current drivers. The result is 0v on the cathodes of all current drivers in the TZ=12 matrix.

To read the "9" on track C an instruction of C53XXX01XX is placed in the instruction register. The analysis of T_1 results in a TN=3. Since matrix write data will be low during R cycle, the inverted matrix write data, on the write 0 grids will be high. The matrix write gate (now low) when inverted, places +28v on the grid of 5V1. The +28v appearing on the cathode of 5V1 will prevent any electrons from flowing up the −60v leg of the resistor network and through diode "d" to the cathodes. The cathodes of the current drivers are placed at +10v by conduction through the −250v leg only and 5 *ma* of current flows. This current through the write 0 side of the C current driver lowers the plate voltage to 138v. The selected read signal, varying from 137.5v to 138.5v appears on the common read data line.

When TZ=12 is low, inverting it places +28v on 5V7, clamping the cathodes to approximately +26v, regardless of the condition of the write gate. This holds all the current drivers in the 12 zone section cut off.

Matrix Read Gate

The input of the common read data line to the read amplifier must be controlled, since there are times when unwanted data appears on this line (Figure 39).

1. During writing, the data being written will appear on the common read line.

2. If no track within the matrix is selected, the data from all tracks will appear on the line, with the line following the most negative signals. The selection of no track within the drum matrix is limited to the following:

   a. No T_1 address. This selects the zone N matrix, but no track within the matrix.

   b. The selection of an 11 zone track, all of which are outside the matrix. However, during a multiply (T_2=N)or divide (T_2=P)operation, reading must take place from the drum matrix during W cycle to develop the answer.

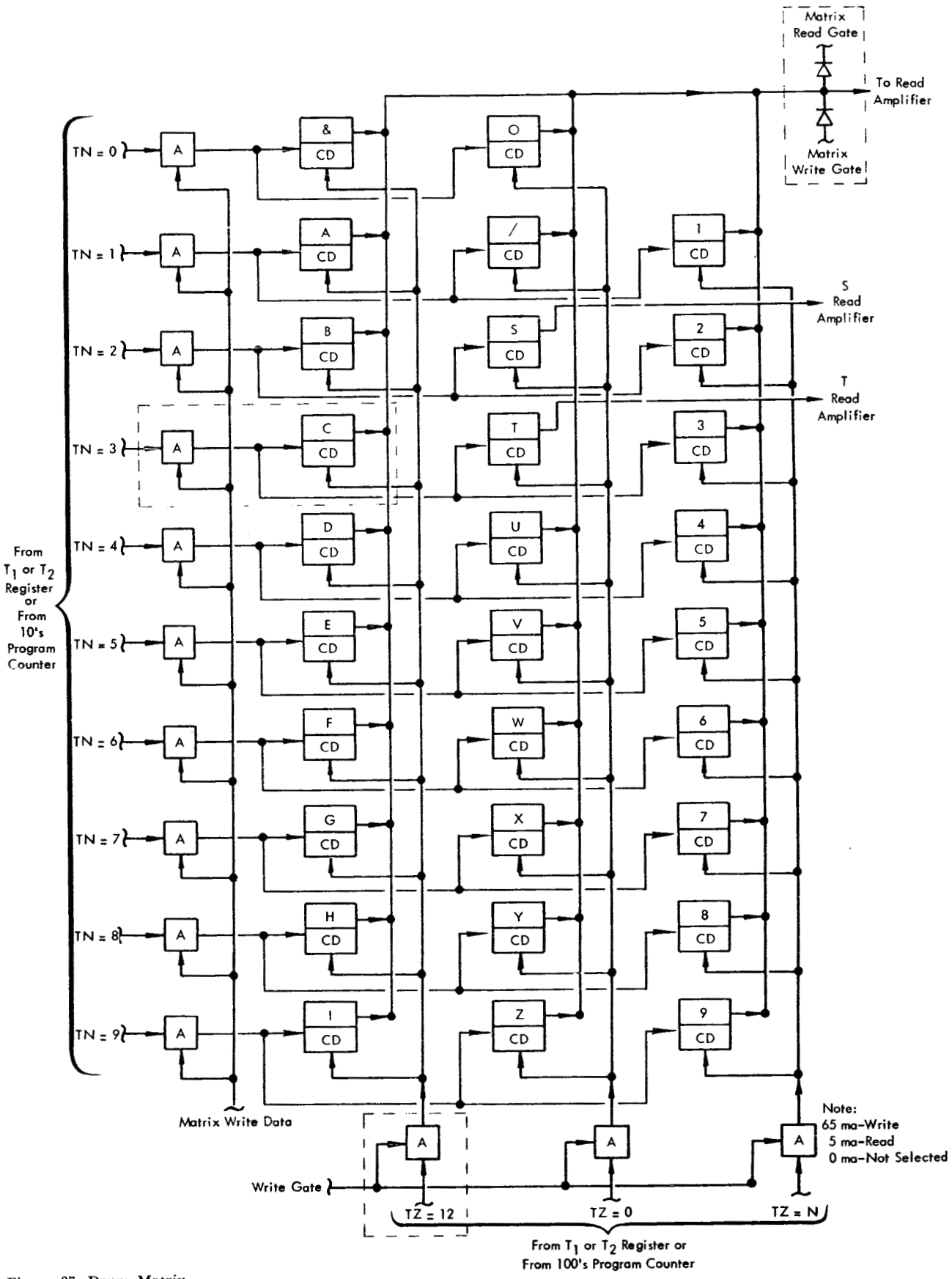


Figure 37. Drum Matrix

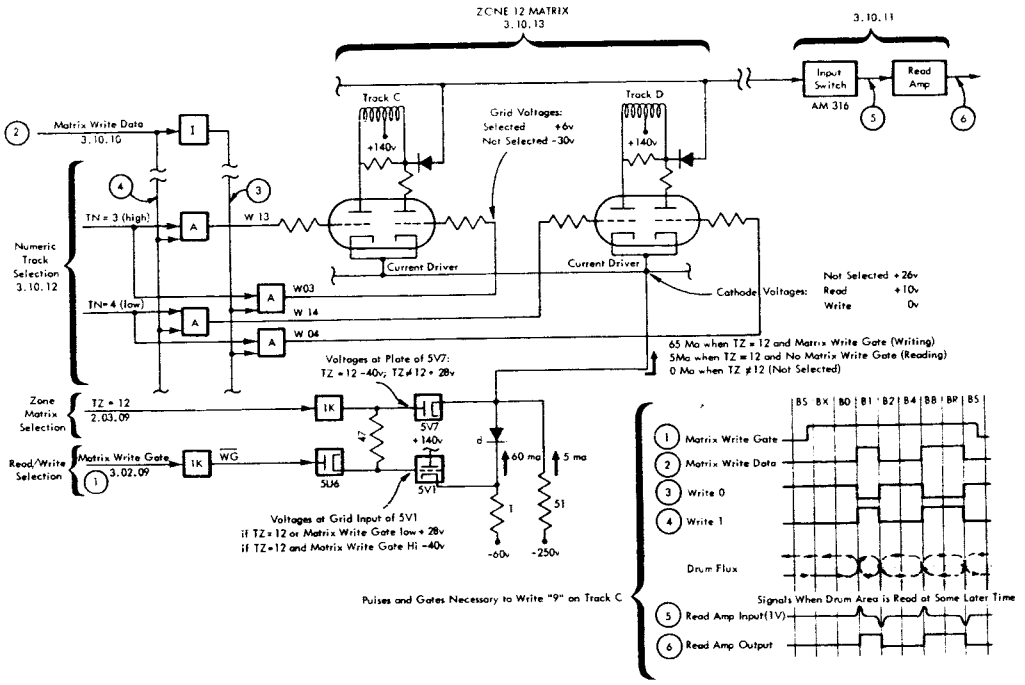


Figure 38. Drum Matrix, Track, and Read or Write Selection for Track C

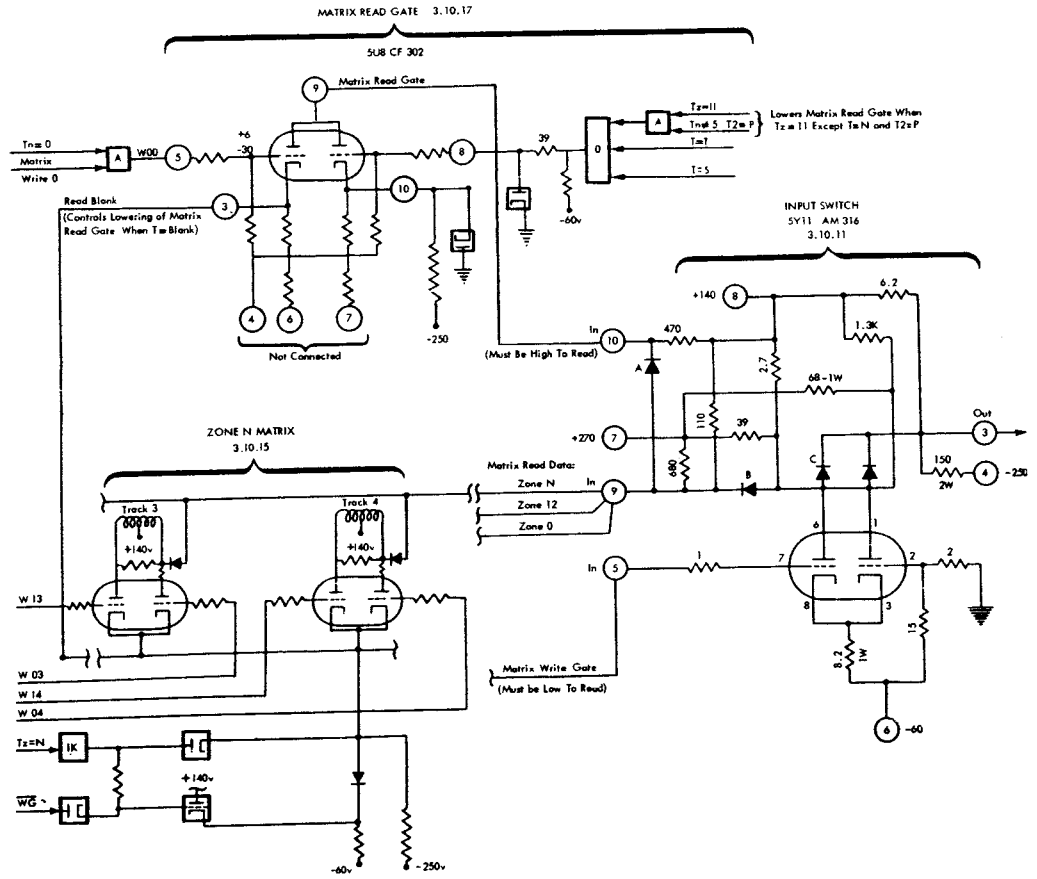


Figure 39. Development of Matrix Read Gate

c. The selection of T and S tracks, which are not within the 0 zone matrix for reading purposes.

The read signal enters the switch at 5Y11 on pin 9, a 1 volt peak to peak signal varying about 138v. During a read cycle the left hand section of the triode will not be conducting and its plate will be above pin 9 and pin 3. The signal will pass through diodes B and C, appearing at pin 3. During W cycle the left hand section of the triode conducts pulling its plate below pin 9, blocking the signal at diode B. This takes care of condition 1 above.

During an R cycle the signal passes through the switch unless the voltage at pin 10 (normally 140v) is lowered, clamping pin 9 below the read signal level at the current driver plates. This occurs if either half of the duo-triode at 5U8 conducts. The right hand side will conduct for conditions 2b and c above. The left hand section conducts when T_1=blank (this raises the TZ=N and TN=0 lines). The grid is brought to +6v by TN = 0 while the cathode is common with the current driver cathodes of the N zone section of the matrix. TZ=N pulls the cathode down from +26v to +10v and the tube conducts, lowering the matrix read gate.

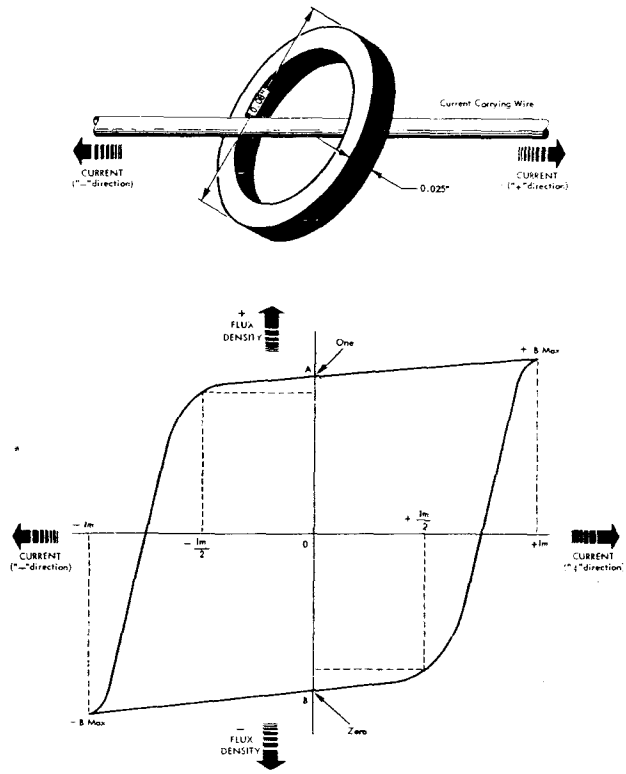


Figure 40. Core Magnetics

Core Buffer

The intermediate storage unit, through which all data being transferred must pass, is the 100 character core buffer. Figure 6 shows its location in the RAMAC system of data flow.

Magnetics of the Core

The basic component of the core buffer is the ferrite core (Figure 40). It is made of a bi-stable alloy capable of maintaining one of two magnetic states indefinitely. This characteristic makes possible the storage of binary information in a core.

The magnetic properties of the ferrite core are illustrated by the hysteresis curve in Figure 40. This curve shows the relationship between the flux density and the magnetizing force as the current is varied between +Im and − Im. Im is the amount of current along a wire threaded through a core necessary to change that core's magnetic state. +Im is the amount of current flowing in one direction, and −Im is the same amount of current flowing in the opposite direction.

In Figure 40, if the core is at the magnetic state labeled B (or zero), and a current of +Im is applied, the core's magnetic flux density will follow the sharply rising curve to +B Max. With the removal of the current, the core's flux density will follow the flat curve to A (or one). The core is said to have flipped.

If the core is already at magnetic state A (one) and a current of +Im is applied, the flux density will follow the flat curve to +B max, and with the removal of the current will return to A (one). The core has not changed magnetic state.

If the core is at magnetic state A (one) and a current of −Im is applied, the flux density will follow the sharply falling curve to −B max. With the removal of the current, the flux density will go to state B (zero). Thus, the core is flipped from one to zero.

If the core is at state B and a current of −Im is applied and removed, the flux density will go to −B max and back to B; the core does not flip.

If a current of ½Im is applied in either the + or − direction, the core will not flip.

If two wires pass through the core, each carrying a current of ½Im the result of the two will be Im. If one of these wires carries a current of Im in one direction, and the other carries ½Im in the opposite direction, the result is the same as the first wire carrying a current of ½Im.

Core Control Logic

Because a single core is a binary storage unit, seven cores are necessary for each character with the RAMAC

seven bit system. For 100 characters 700 cores are necessary. These are arranged in a matrix with 7 planes of 100 cores each (Figure 41). Each plane is 10 cores wide by 10 cores long, the vertical rows reserved for each character within a field while the horizontal rows represent the fields (0 to 9). Each plane represents one of the seven bits, therefore one character will have a single core in each plane.

Because data is transmitted serially by character, we must be able to select one of the 100 character positions to pass + or − Im through at any particular instant. All character 0 cores (70) will have a common drive line passing through them. This holds true for character 1, 2, etc. In addition, all cores of field 0 have a common wire through them. Each of the other fields has a common drive wire, also. By directing $+\frac{1}{2}$Im through character (units) drive line 4 and $+\frac{1}{2}$Im through field (tens) drive line 7 all seven cores in character 74 will have +Im. In a similar manner we can send −Im through any character position simply by reversing the direction of current through the drive lines.

The units and tens lines are controlled by two 10 position Overbeck rings, called the core units ring and the core tens ring, which advance sequentially from character 00 to 99. When transferring to or from the drum the two rings will be advanced with Bs or Br clock pulses respectively. When data is flowing to or from the file, the rings will be synchronized with a disk clock, which will be covered later. The rings will always be reset to 00 before a transfer operation, and begin advancing when the transfer begins. We now have a method of addressing the seven cores of any character position in the core array, by passing $\frac{1}{2}$Im through one units drive line and $\frac{1}{2}$Im through one tens drive line. For ease of explanation we say current in a plus direction will write a one in the addressed cores and current in a minus direction will reset to zero, or read-out of the addressed cores.

During R cycle the data from the drum is written in cores. This requires resetting the addressed cores to zero with a "core read pulse" and then writing "ones" in the same cores with a "core write pulse." This will be done at the end of each character time, i.e., BrØC. Notice on Figure 41, during R cycle, a BrØC pulse first develops a 3 μs "core read pulse" at a single shot to feed the addressed core drive lines. This results in −Im through the addressed cores. The fall of the core read pulse fires a second single shot to develop a 3 μs "core write pulse." This also feeds the drive line to pass +Im through the seven addressed cores, to write "ones." This same core write pulse advances the core units ring to address a new core position for the next read and core write pulses.

During W cycle the cores are read out and the data will go to the drum. Now it is necessary to read-out (or reset) the addressed cores at the beginning of a character time (BsØC) so the data may be placed on

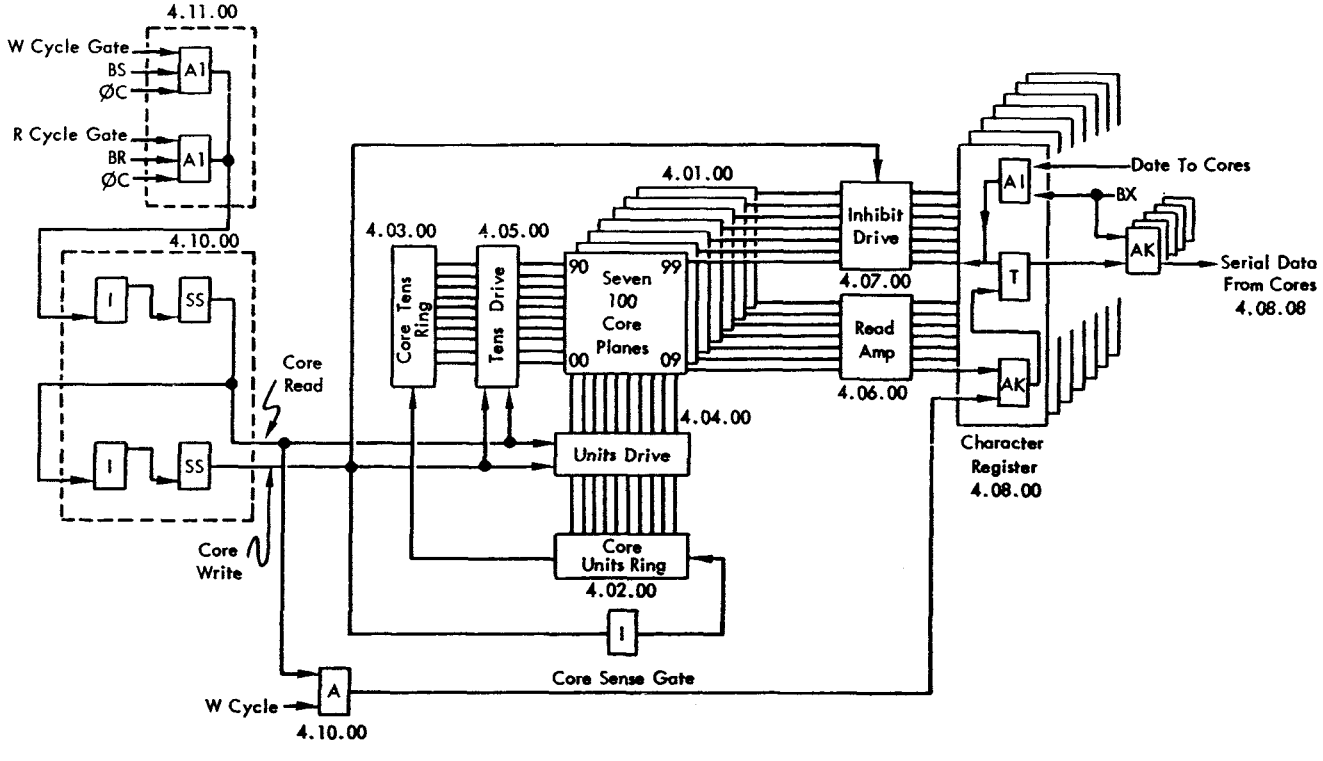


Figure 41. Core Buffer Logic

the data from cores line. Each core read pulse resets the addressed cores to zero as well as reading them out, so it is necessary to write the information back in immediately. This is done by following the core read pulse with a write pulse, just as was done during R cycle. On Figure 41 it is a Bs∅C which develops a 3 μs core read and then write pulse, on W cycle.

To summarize: whether we are transferring data to or from the cores, a read pulse must always be followed by a write pulse.

Core Data Flow

The data flowing to and from the drum is in serial form by bit. The bits are read into or out of cores in parallel. The character register accomplishes this transition. There are seven triggers in the register, one for each bit. To write in cores, ∅C bits coming from the read head (data to cores) are stored in the appropriate triggers for that particular character. At BR time a read pulse resets the cores and a write pulse attempts to store a one in each plane. In order to control which cores in a character position are flipped, an inhibit line is threaded through all the cores in each plane. By passing $-\frac{1}{2}$Im through a particular inhibit line, that core position which has +Im due to a write pulse, will have a resultant current of $+\frac{1}{2}$Im. This is insufficient current to flip the core from the 0 to the 1 state. Because there is an inhibit drive line for each trigger in the character register, we can sample all triggers at core write time and drive those inhibit lines associated with the no-bit triggers. The seven triggers are then reset and the units and tens ring advances for the next character.

To read from cores (W cycle) we must add a fourth line, the sense line. There are seven sense lines; one for each core plane or bit. The read pulse will pass −Im through seven cores. Those cores which are at the 1 state will be flipped, inducing a signal on the appropriate sense line. Any core at 0 will remain unchanged, therefore, no flux change and no induced voltage results in those sense lines. These sense pulses, coming in parallel for any character at Bs time, will turn ON the triggers in the character register. This occurs at the beginning of the character, so the triggers may be strobed to put serial bits on the "data from cores" line. The read pulse destroyed the information in the single character position, so it is necessary to write immediately back into those cores, using the condition of the seven character register triggers to control the inhibit lines.

Core Circuits

The discussion of circuit operation necessary to store data in cores during R cycle and read that data from cores during W cycle follows. Reference is made to Figures 42, 43 and 44. Figures 45 and 46 are sequence charts illustrating core operation during a specific instruction.

OBJECTIVES:

1. Reset the core units and tens rings to 00.
2. Reset and enter the character register from the drum.
3. R cycle core starts to:
   a. Reset the addressed cores with a core read pulse.
   b. Write into cores from character register with a core write pulse.
   c. Advance units and tens ring.
4. W core starts to:
   a. Read into character register from addressed cores with a core read pulse.
   b. Rewrite into cores with a core write pulse.
   c. Advance the units and tens ring.

Core Units and Tens Rings. The ten triggers in each ring (4.02.00, 4.03.00) are reset 10 pin low by the buffer counter reset line from 3.02.10, a CL pulse every cycle unless T=R or N. The core units 0 line and the core tens 0 line will be high, addressing core position 00. The units ring will advance with every pulse on the write gate line (this is the 3 μs core write pulse) and a carry will advance the core tens ring.

A special reset inverter is needed in each ring to prevent the ring from rolling while the reset gate is applied to the right hand grids. When a trigger is cut off a negative shift on pin ten will appear as a negative spike on the right hand grid of the next trigger in the ring. This causes a positive spike on pin 10, the fall of which puts another negative spike on the next grid. Since all pin 10's are connected to the following trigger's grid, the ring would roll, leaving one trigger ON when the reset gate was removed. To block this spike the reset gate is inverted at 4S4a (4.02.00) and 4S4b (4.03.00) and the 10 pin plates on a trigger in each ring are clamped at the low level.

Character Register. Because the data from the drum is in serial form, it is necessary when entering cores to store the bits for each character, X through R, in the character register triggers. Then at the end of each character we can read the data into all seven cores for that character with a write pulse. The seven character registers triggers (4.08.01 to 4.08.07) are reset 10 pin low with a plus pulse on the character register reset line from 4.11.00. During R cycle the R cycle gate ands with ∅C at 4G8a which in turn is gated with bit S at 4G6b to give a Bs∅C reset pulse at the start of each character coming from the drum.

On 4.08.01 (BR character register) the data to cores line has all bits (∅C) from the drum on it. This com-

mon data line is scanned with core bit R's and any drum bit R present flips the trigger 10 pin high. The core bit ring on 4.09.00 is a core clock which will be synchronized with either the drum clock or the disk clock depending on the operation. It is reset to bit S when not operating. When reading into or out of cores it will be advanced by ØA pulses developed on 3.02.02. Notice the ØA, ØB and ØC pulses here are either the Ø pulses from the drum clock or the disk clock.

When a bit is stored in the character register trigger (4.08.01) the bit R write line will be low and the bit R gate will be high. The bit R write line goes to the inhibit drivers on 4.07.00 while the bit R gate goes to the core data out line.

Core Start (R Cycle). On 4.11.00 the core start is a BRØC pulse developed at 4H6 during R cycle gate. On 4.10.00 the start pulse develops a 3 μs core read pulse at single shot 4K5. The fall of this pulse develops the 3 μs core pulse (core write pulse) at single shot 4L6.

Using Figure 42 and diagram 4.04.00 we can see how the core read pulse will reset all cores addressed by the unit and tens rings to "0". In Figure 42 we are working with position 80. The core units 0 line is high conditioning the grid of the CF304 at 4E1. The 3 μs core read pulse (labeled read gate) causes the two CD units, 4Q1 and 4R1 to conduct. Of the ten units switch core transformers in the CF304 units, only the one for position 0 will have current in winding "A" causing it to flip. When it flips $-\frac{1}{2}$Im will be induced in the secondary which is laced through all 70 character 0 cores. In the same manner all 70 cores in field 8 (core tens) receive $-\frac{1}{2}$Im resulting in $-$Im in 7 cores of character 80. This flips all these cores to the "0" state.

The core write pulse (labeled write gate) follows immediately and causes current to flow in all b windings of the 10 unit drive transformers and the 10 tens drive transformers. This current is in the opposite direction of that through winding "a". Since the units 0 and tens 8 transformer cores were the only ones flipped during the core read pulse, only these two transformer cores can change their flux direction during the core write pulse. Since transformer action is caused by changing flux lines only these two secondaries will have $+\frac{1}{2}$Im induced in them, resulting in +Im in the 7 character 80 cores.

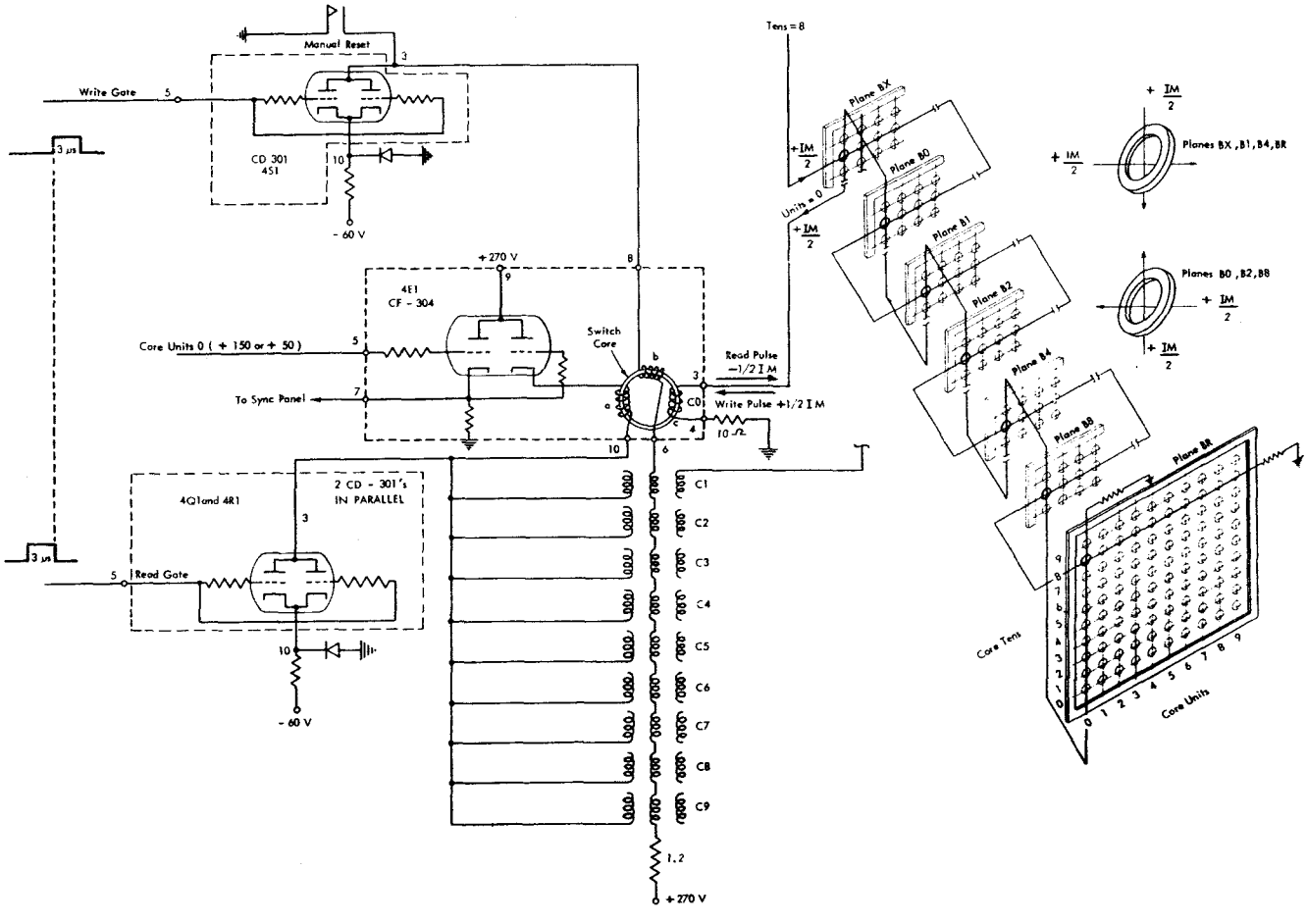


Figure 42. Address Core Buffer Position 80 (4.04.00, 4.05.00)

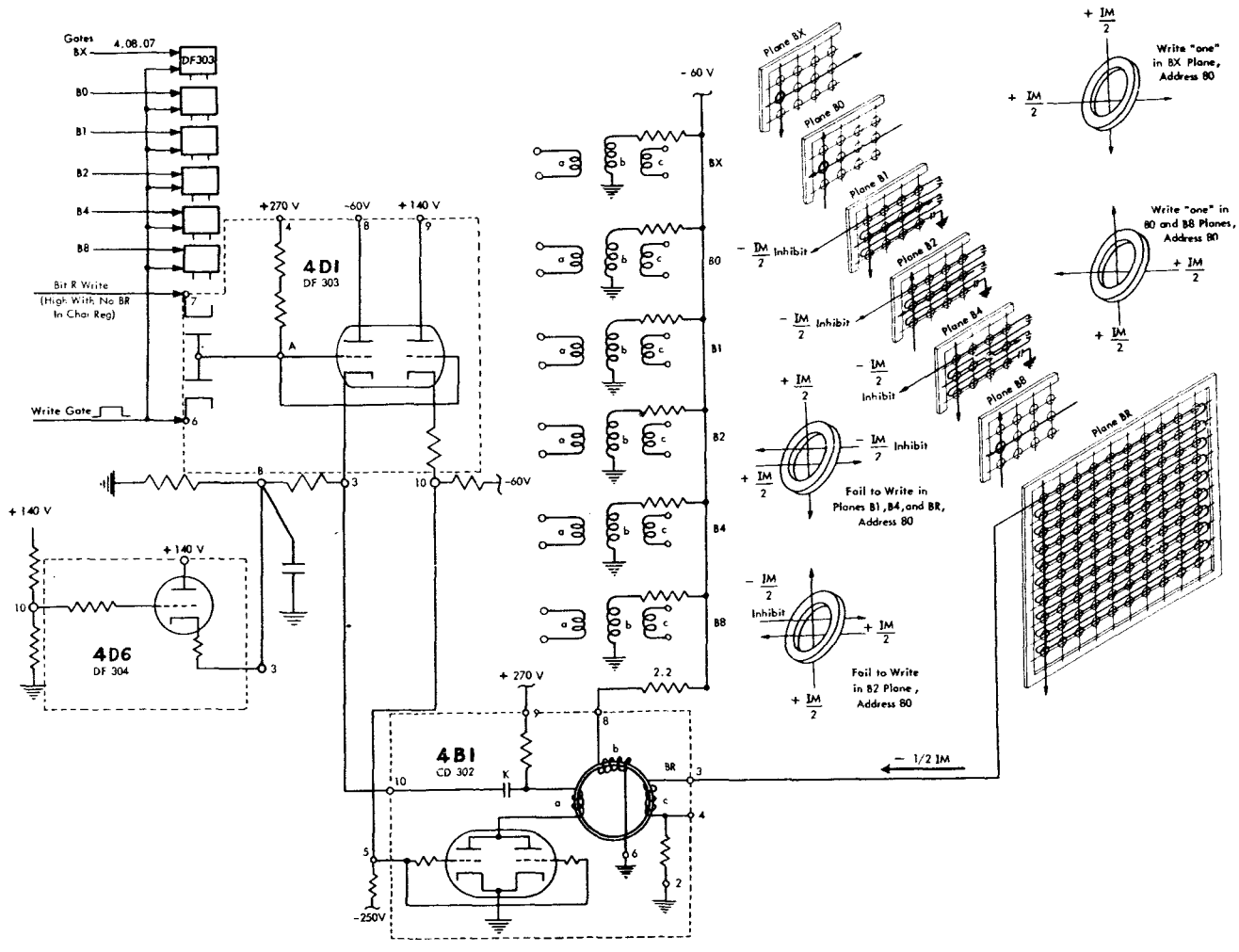


Figure 43. Inhibit Drive Showing BR in Detail (4.07.00)

To select which of the seven cores will be allowed to flip from "0" to "1" the character register triggers will be analyzed and the inhibit lines for those positions with no-bits will pass $-\frac{1}{2}$Im. This is shown in Figure 43 and diagram 4.07.00. To prevent writing a bit we must pass current through winding "a" of the inhibit switch core transformers. The CD 302 will conduct if its DF303 is allowed to conduct. The DF303 will conduct if the core write pulse (write gate) and the bit write line from the respective character register triggers are both high. These lines feed an "and" switch within the DF303 unit.

Following the core write pulse the inhibit switch core transformers have flipped and the next pulse through winding "a" will not result in an output unless the transformer core is flipped back to its original state. To accomplish this a steady current is passed through winding "b", opposite in direction from "a". When the write pulse is finished this current returns the transformer core to its original state.

On 4.02.00 the core units ring is advanced by the core write pulse (write gate). Actually during writing the core position addressed is one higher than the position which receives —Im. In Figure 42 we found that the only switch core transformers affected by the write pulse were those originally flipped by the read pulse.

Core Start (W Cycle). The primary difference in core operation during W cycle as compared to R cycle is the direction of data flow and the timing of the core starts The data is moving from the cores to the character register. From there it moves to the drum on the line labeled "serial data from cores". It is necessary to read out of any core position to the character register, all seven bit positions at once, then scan each character register trigger in sequence: X, 0, 1, 2, 4, 8, and R. This means the core start must occur at the beginning of each character. On 4.11.00 the core start is a BsØC developed at 4G8b and 4G6b. This core start develops a core read pulse and core write pulse as during R

cycle. The read pulse passes −Im through the addressed cores, flipping any core which has a "1" stored in it. A sense line passes through all cores in each plane. The cores which are flipped by the read pulse induce a small signal in one or more of the seven sense lines at each character time (Figure 44). These signals are rectified at the PX units on 4.06.00, then amplified and sent to the respective character register. At the character registers it is anded with core sense, which is a W cycle core read pulse, to turn the triggers 10 pin high. As the core bit ring continues to advance the seven character register triggers are scanned serially to develop ∅A to ∅A data from cores on 4.08.08.

The seven cores which have been read out are reset to a blank. It is necessary before moving on to the next character to rewrite back into this position from the character register. The 3 μs core write pulse, following the read pulse, attempts to pass +Im through all seven cores. However, the inhibit lines on 4.07.00 are once more driven by those character register triggers storing no-bit (bit write line high).

The core units ring is advanced by this same core write pulse.

Example of Core Buffer Operation

Figures 45 and 46 are sequence charts illustrating the core operation during the instruction W53C7402bb.

Transfer Of Data During I Cycle

During I cycle a 10 digit instruction is read from one of 200 drum locations and placed in the instruction register. The 200-step program counter determines which instruction shall be chosen (Figure 47). The hundreds counter determines which of two track groups, numeric (0-9) or 12 zone (&, A-I) will be selected. The tens counter selects the track within the group, and the units counter determines which field of the selected track will be transferred. For example, if the program counter is at level 037, field 7 of track 3 is selected; if the program counter is at 137, field 7 of track C is selected. One exception to the zone selection occurs for the 0 drum track. This is in the 0 zone and both the hundreds and tens counter must be analyzed.

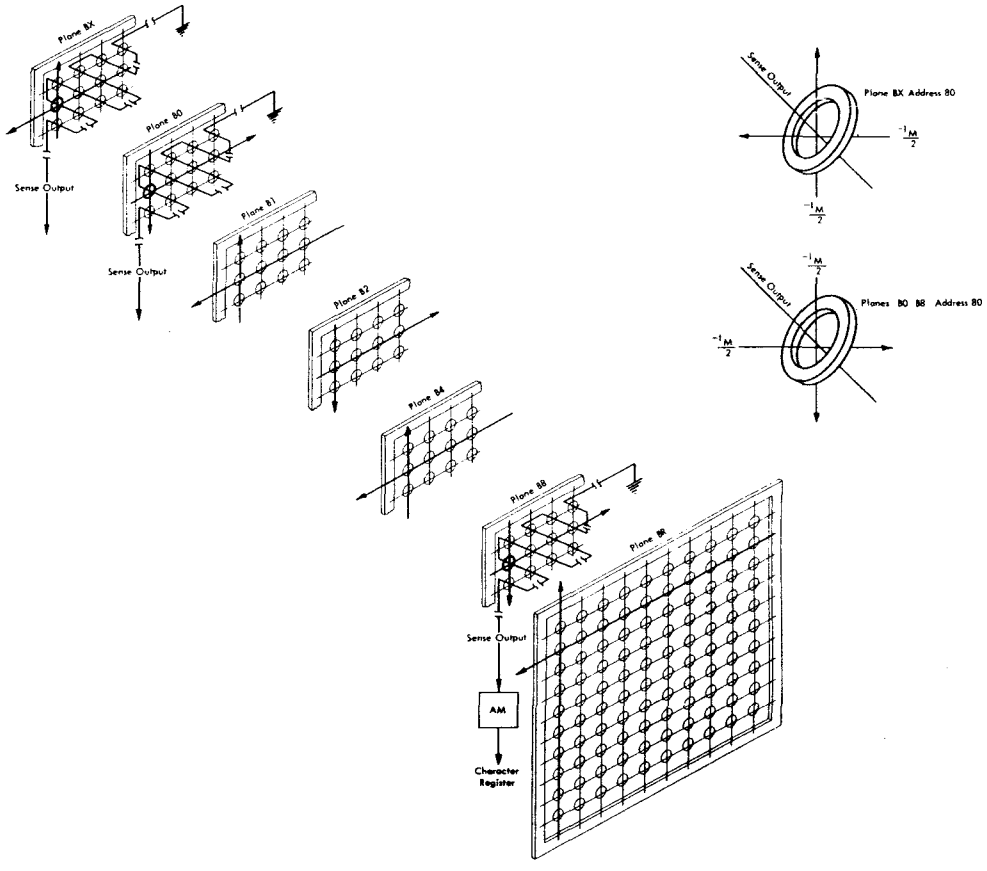


Figure 44. Sensing "H" While Flipping Cores (B0, BX, B8) Back to Zero

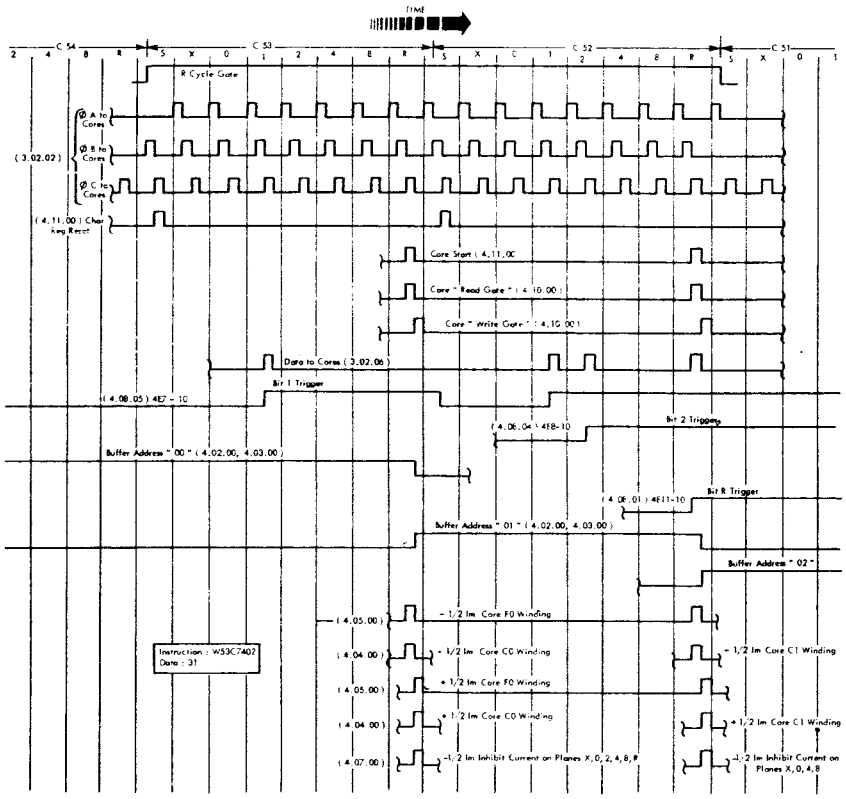


Figure 45. Core Buffer Operation on R Cycle

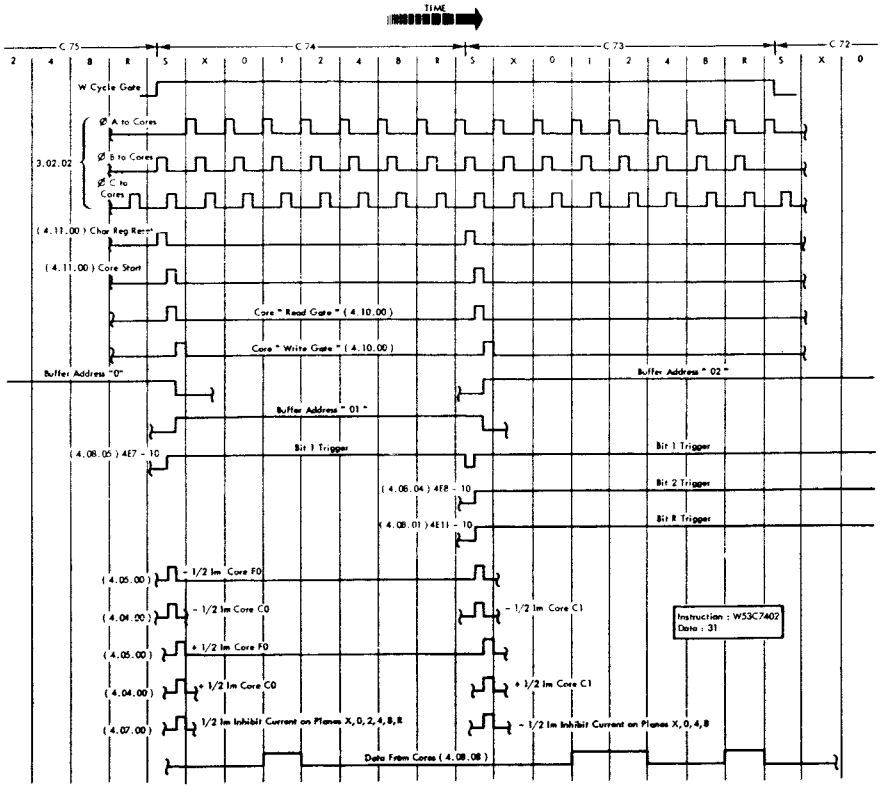


Figure 46. Core Buffer Operation on W Cycle

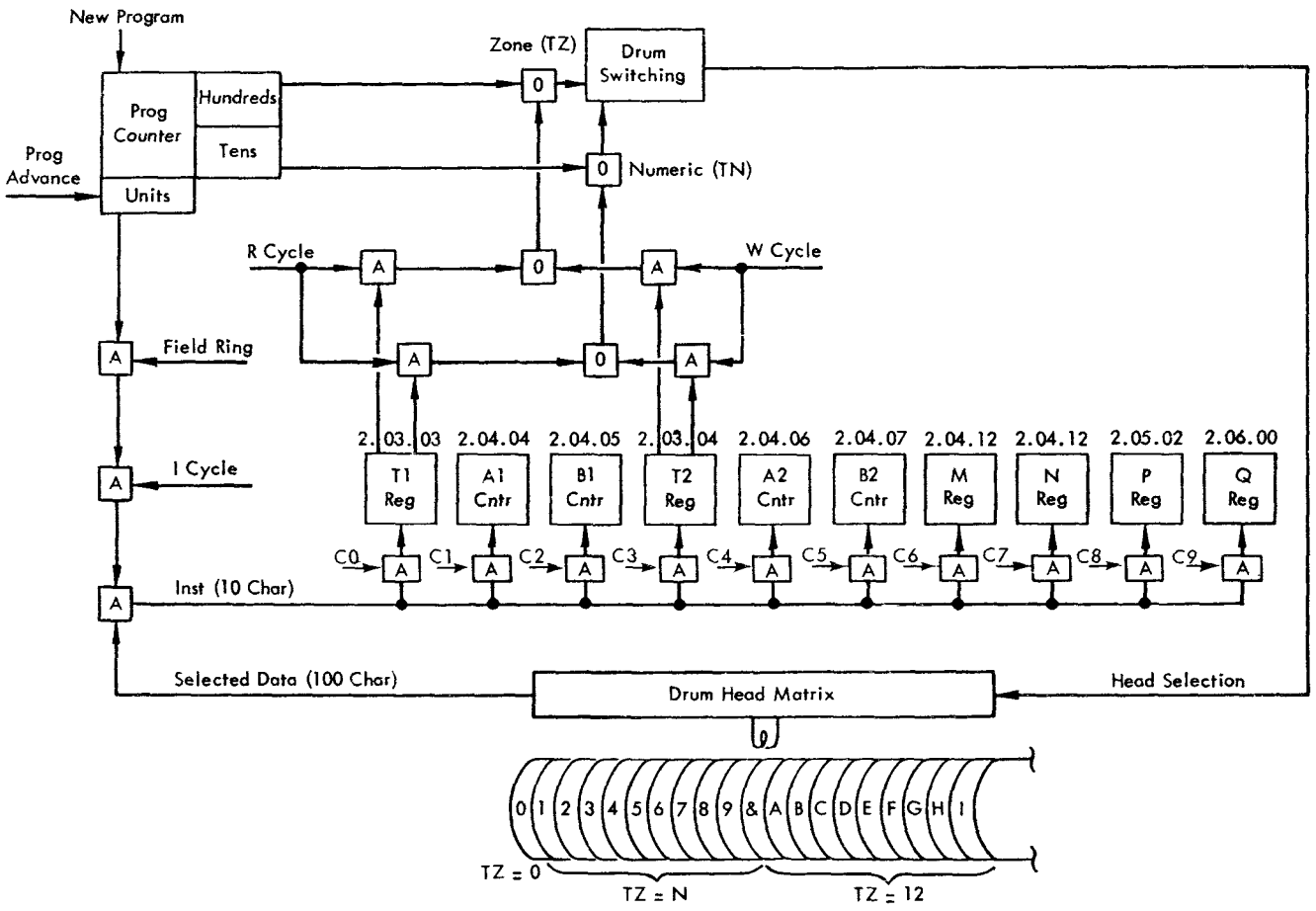


Figure 47. I Cycle Data Flow

Normally the program counter, reset to 000 with the reset key, will advance sequentially at CLBR just before I cycle. An instruction with a P flag interrupts this sequence, requiring control panel wiring to continue. The program exit hubs may be used to impulse the program entry hubs for setting up a new program level, or to impulse the program advance hubs to cause the counter to continue advancing sequentially.

OBJECTIVES:

1. Set the program counter.
   a. Program switches
   b. Program entry hubs
   c. Normal advance BRCL W cycle
   d. Program advance hub (P flag)
2. Select a read head with the value in the program counter, tens and hundreds.
3. Gate one field of selected track data by analysis of the units position of program counter.
4. Reset and read-into instruction register.

Program Counter. Both the program counter units (2.01.04) and tens (2.01.05) consist of ten triggers. The hundreds counter (2T2-2.01.06) is a single trigger, since 199 is the highest program level provided. There are a number of ways to reset the program counters. The manual reset key on the 380 console develops an "X" reset which sets the hundreds trigger (2.01.06-2T2) 3 pin high. The "X" reset places all triggers in the units and tens counters three pin high, resulting in blanks in these counters. This is done by placing 0 volts on the program counter reset line at 2L4 on 2.01.07.

Depressing the program set key picks R153 (2.01.01) and develops a 200 μs reset pulse at the single shot 2P4 (2.01.07) to reset the units and tens counters. Following the reset pulse (R153 still up) the program selector switches (2.01.01) determine which triggers will be turned ON in each of the three counter positions. A third method to reset and set the program counters is used when a P flag is present (2.01.07-2L3). The flag forces the D, P cycle and during the P cycle the counters are reset. Following this reset they will be set with impulses to the program entry hubs (2.01.02) from a program exit hub. The line to pin 6 of 2L3 (2.01.07) coming from the CE sync panel is normally floating. This is the same as a plus voltage on the AI.

The program advance pulse to pin 5 of all the program counter units triggers is a BrCl pulse before each I cycle (2.01.07) following any IRW sequence or when the program advance hubs are impulsed following an IRWDP sequence. The controls for advancement of the counter are developed on 2.01.06 at two triggers, labeled new program and program advance (2N2 and 2M2). Both are reset 10 pin low at I cycle end and remain there until a P flag or T_2=J. The P flag must result in the new program line being high or I cycle cannot begin (1.03.04). 2N2 is turned on by impulsing program entry hubs (units), program advance hubs, or T_2=J when P=blank. 2M2 is turned on by the last two conditions only, not the program entry hubs.

In the counter rings the two AI units (2.01.05-2G5a and 2.01.04-2G5b) are designed to block the rolling of the counter during reset time. This concept is more fully covered in the section on "Core Units and Tens Rings."

Head Selection. The program counter tens conditions the numeric portion of the head matrix (2.03.07) during I cycle ready. At the same time the program 100 trigger selects the zone matrix (2.03.09). This is shown in Figure 37. All of the selected track will appear as the output of the drum matrix read amplifier.

I Cycle Gate. The field of the selected track data to be entered into the instruction register is determined by the value in the program counter units. On 2.02.03 the matrix read data is gated with I cycle and the program gate; the latter being developed while scanning the program counter units with the field ring. The result is ten characters of ⌀C data on the line labeled gated process drum data. The various bits are separated for entry into the instruction registers (2.02.04).

Instruction Register. The program bits are gated with characters 9 through 0, the C9 data entering the Q register (2.06.00), C8 data entering the P register and so on down to C0 data entering the T_1 register. Remember, data from the drum is arriving character 99 first and character 00 last.

The T_1 and T_2 registers (2.03.03, 2.03.05), similar in operation, consist of six triggers. Using T_1 register (2.03.03) as an example, all triggers will be turned off prior to the I cycle gate with the instruction register reset A line. On 2.03.01 this line is high during any "C" reset developed with the manual reset button, check reset button, or program load button. The program set reset line is high when the program set button is pushed. These are static resets. When cycling the reset occurs with the I cycle ready trigger on (ClBr) and lasts until the I cycle begins (RM).

The T_1 register triggers are plate-pulled on in several ways on 2.03.02. During I cycle the matrix read data in the form of I bits "ands" with C0 and is inverted. The T_1 register may also be entered from the 380 Console at the D1302's.

There are 4 modified binary counters in the instruction register; the A_1, B_1, A_2, B_2 counters. Using the A_1, B_1 (204.04, 2.04.05) counters as an example, these counters are reset with a ClBr to RM gate, before an I cycle. The instruction bits from the appropriate character turn on the corresponding triggers.

The MN register (2.04.12) and the Q register (2.06.00) are binary storage units of four triggers. M and N registers are read into on characters 6 and 7 respectively, while the Q register is read into during character 9.

The P instruction register (2.05.02) is a relay storage device, the relays being picked by thyratrons fired by the bits in C8 of the instruction. The relays determine which of the program exit hubs (2.05.03) will emit during P cycle. These relays therefore are held until P cycle through the normally closed points of mercury relay 2 (2.09.10). The pick coils of the P relays will be energized until the plate circuit, P pick, is opened on 2.09.10 when MR-1 picks. MR-1 is picked on 2.09.01 by turning trigger 3M2 10 pin high at F6 of D cycle. The hold coils were previously energized by the dropping of MR2 at R cycle end (2.09.01) until P cycle end. The impulse to the program exit hubs comes from MR7 normally open points. MR7 is energized on every P cycle (2.09.02). The MR relay timings are shown on the sequence chart on 0.09.03.

Figure 48 is a sequence chart illustrating the read in of the instruction register during I cycle.

Transfer Of Data During R Cycle

Using the instruction W53C7402bb, during R cycle the data will move from the drum to cores (Figure 49). T_1=W will select the W drum head from the matrix. The A_1, B_1 counters will tell the machine when to begin reading and the MN register will decide when to stop. If the A_1 B_1 counters, containing 53, are advanced each character time beginning with Br of character early, they will roll from 99 to 00 at Br character 54. The carry thus developed begins read-in to cores. If the A_1 B_1 counters continue to advance they will reach 02, the amount in the MN register, at Br character 52 and the transfer will be stopped.

Objectives:

1. Select the read head with the T_1 register.
2. Develop R/W cycle gate with AB compare to MN compare.
3. Develop AB compare and MN compare.
4. Core start during R/W cycle gate.

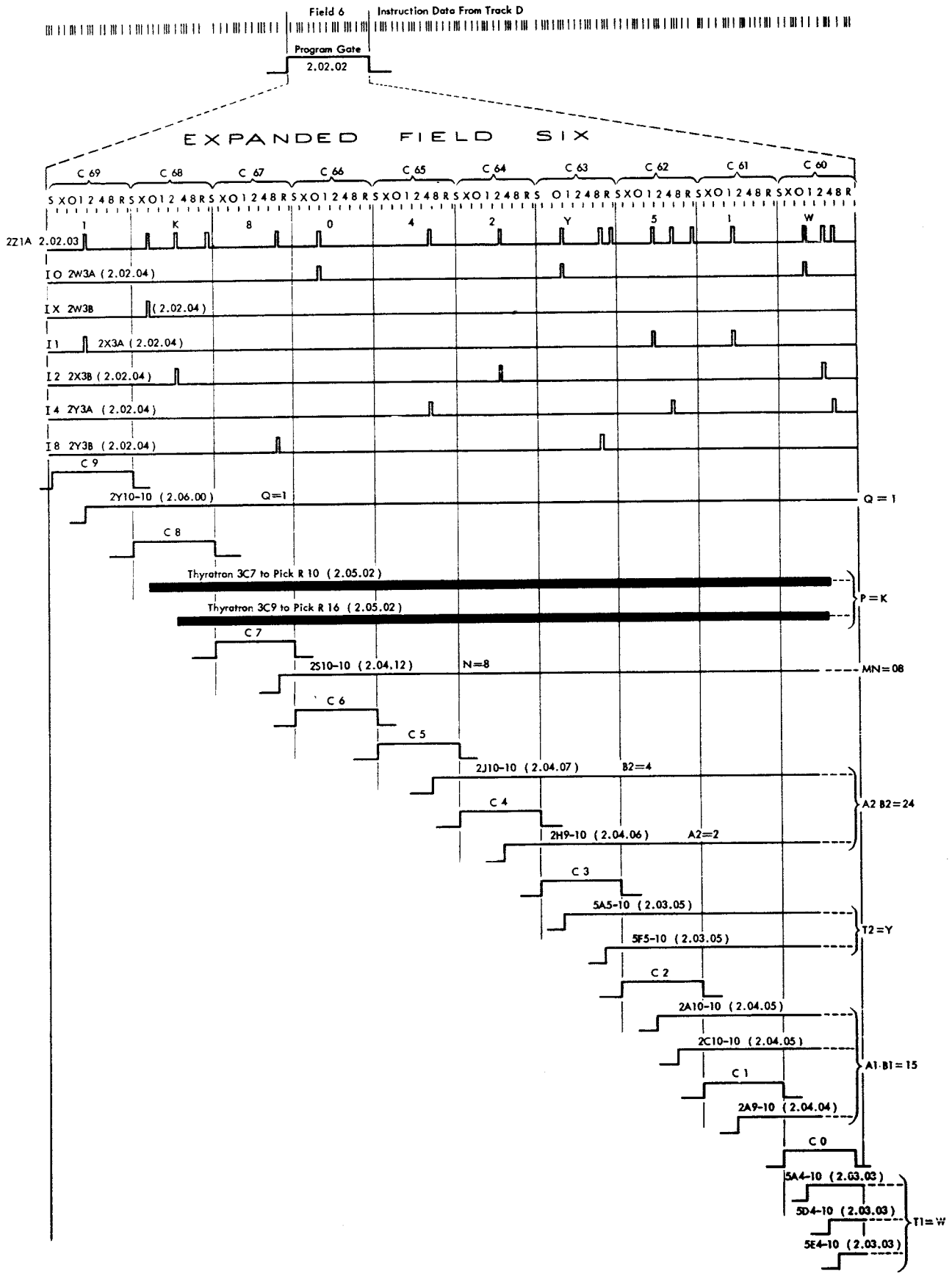


Figure 48. Setup of Instruction Register Program Step 146 (Instruction: W15Y2408K1)

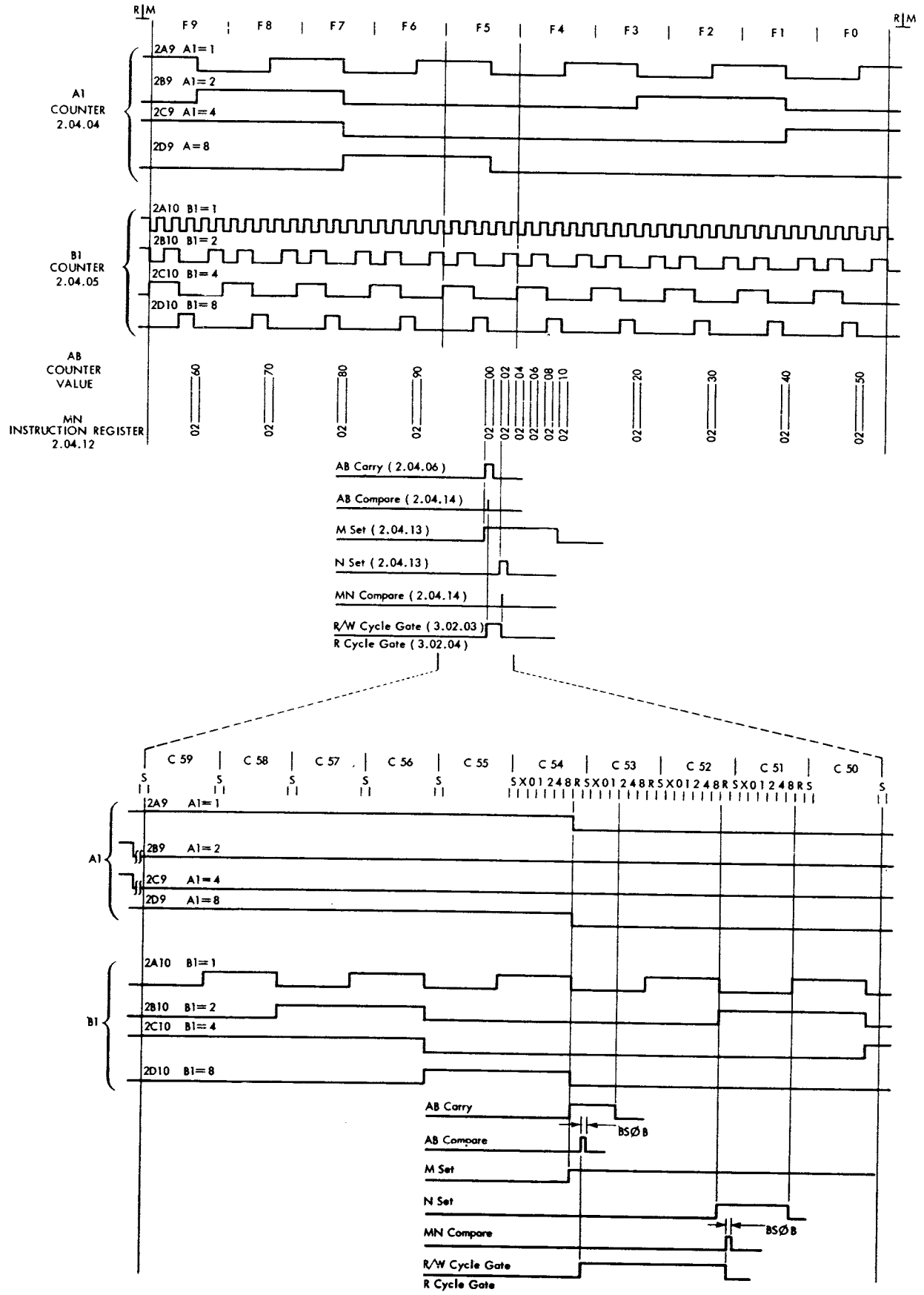


Figure 49. Development of R Cycle Gate (Instruction: W53C7402bb)

Select Read Head from T_1 Register. Analysis of the T_1 register occurs on 2.03.07 and 2.03.09 developing a TZ line and a TN line. If any heads in the matrix are selected, the matrix read gate (3.10.07) will be high. The matrix write gate is low during R cycle. The matrix read data in the form of a 1 volt peak to peak sinusoidal signal enters four stages of amplification (3.10.11). The clipper at 5V11 receives two similar amplified and inverted drum signals, one riding at +15 volts (pin 10) and one at −15 volts (pin 5). Only the top of the signal at pin 5 and the bottom of the signal at pin 10 reach the TR306, blocking any noise appearing on the base line. The trigger at 5U11 follows both plus and minus changes on its grid. The Bs pulse will set the trigger 10 pin low before the next character. Matrix read data is now full bit pulses. The data was written on the drum ∅A to ∅A. Because there is a delay when going to the drum and then from the drum, the data is now approximately ∅B to ∅B.

R/W Cycle Gate. The matrix read data is gated with R cycle gate and ∅C to cores (3.02.06). With the instruction W53C7402bb the R cycle gate should be up for characters 53 and 52 only. On 3.02.04 the R cycle gate will be up when any one of the three AI's conduct if 3T6a is cut-off. 3U3 will conduct during R cycle for the duration of R/W cycle gate from 3.02.03. This is the major gate during track to track transfer, determining when the transfer will begin and end. The trigger at 3T1 will go to 10 pin high at AB compare and 10 pin low at MN compare or CL.

AB Counters. The A_1 B_1 counters are advanced during R cycle with each BR, starting with CEBR. The trigger at 2J6 (2.04.03) does prevent BR of character 00 and CL from advancing them. The B_1 counter carries into the A_1 counter and when the A_1 counter rolls from 9 to 0 an A_1 carry (2.04.04) is developed which becomes an AB carry (2.04.06) from BR to B2. This is "anded" with Bs∅C (2.04.14) to become AB compare and raise the R/W cycle gate.

The MN compare signal used to drop the R/W cycle gate is developed at 2X6 (2.04.14) from N set, M set, Bs∅B and a previous AB carry (2Z6). The M and N set are developed on 2.04.13 in the MN comparator. M set will be high only when the value in the A counters is equal to the figure in the M register. N set is high when the B counter equals the N register. Both lines are devloped in the same manner so we will examine only N set. For N set to be high none of the eight AI on this line can be conducting. Four inverters compare the OFF side of the four N triggers with the ON side of the four B triggers. The other four AI's compare the ON side of the N triggers with the OFF side of the B triggers. Only when all N triggers compare with all B triggers will all eight AI's be cut off.

When MN=00 and A_1B_1=99, 100 characters are to be transferred beginning at character 99. MN compare must be blocked since it will occur at character 99 also. The trigger at 2Z6 (2.04.14) accomplishes this. It must be ON to permit an MN compare at Bs∅B. In this case above the trigger will not come ON until Bx character 99 (2Z7a), too late for MN compare.

Core Start. During the R/W cycle gate a core start (4.11.00) is needed at BR∅C of each character written into cores. The R/W cycle gate was up at the beginning of the first character transferred (Bs∅B). After this character is entered into the character register, the core start (BR∅C) resets core position 00, writes the character and advances the core units ring.

Transfer Of Data During W Cycle

During the W cycle, data flows from cores to the drum. The drum track written on is decided by the T_2 address while the starting character is fixed by the A_2B_2 counters. The MN register determines how many characters will be read out of cores beginning at core character 00. The starting point on the drum and the number of characters will be controlled by the W cycle gate developed from the R/W cycle gate, which was previously discussed. Figure 50 is a sequence chart showing the necessary gates and the data flow.

OBJECTIVES:

1. Select drum head for writing with T_2 register.
2. Core start.
3. Select data specified by A_2B_2 counters and the MN register.

Head Selection. This is accomplished just as it was during R cycle by analysis of T_2. The matrix write gate is up now allowing 65 *ma* to flow through the selected current driver (3.10.13).

Core Start. The first core start pulse will read position 00 of the core matrix into the character register. This will occur in the example W53C7402bb at the beginning of drum character 74. On 4.11.00 the core start pulse, developed at 1H7, is Bs∅C (start of a character) "anded" with W cycle gate and W cycle core start gate. The W cycle core start gate is up every machine cycle from RM to F0C0B2. The W cycle gate, through a number of inversions is actually R/W cycle gate "anded" with W cycle. On 3.02.08 the not W cycle gate is developed at the trigger 3T1 on 3.02.03, up at Bs∅B of the first character and down at Bs∅B following the last character to be transferred.

AB Carry and MN Compare. The R/W cycle gate is started with an AB carry and stopped with an MN

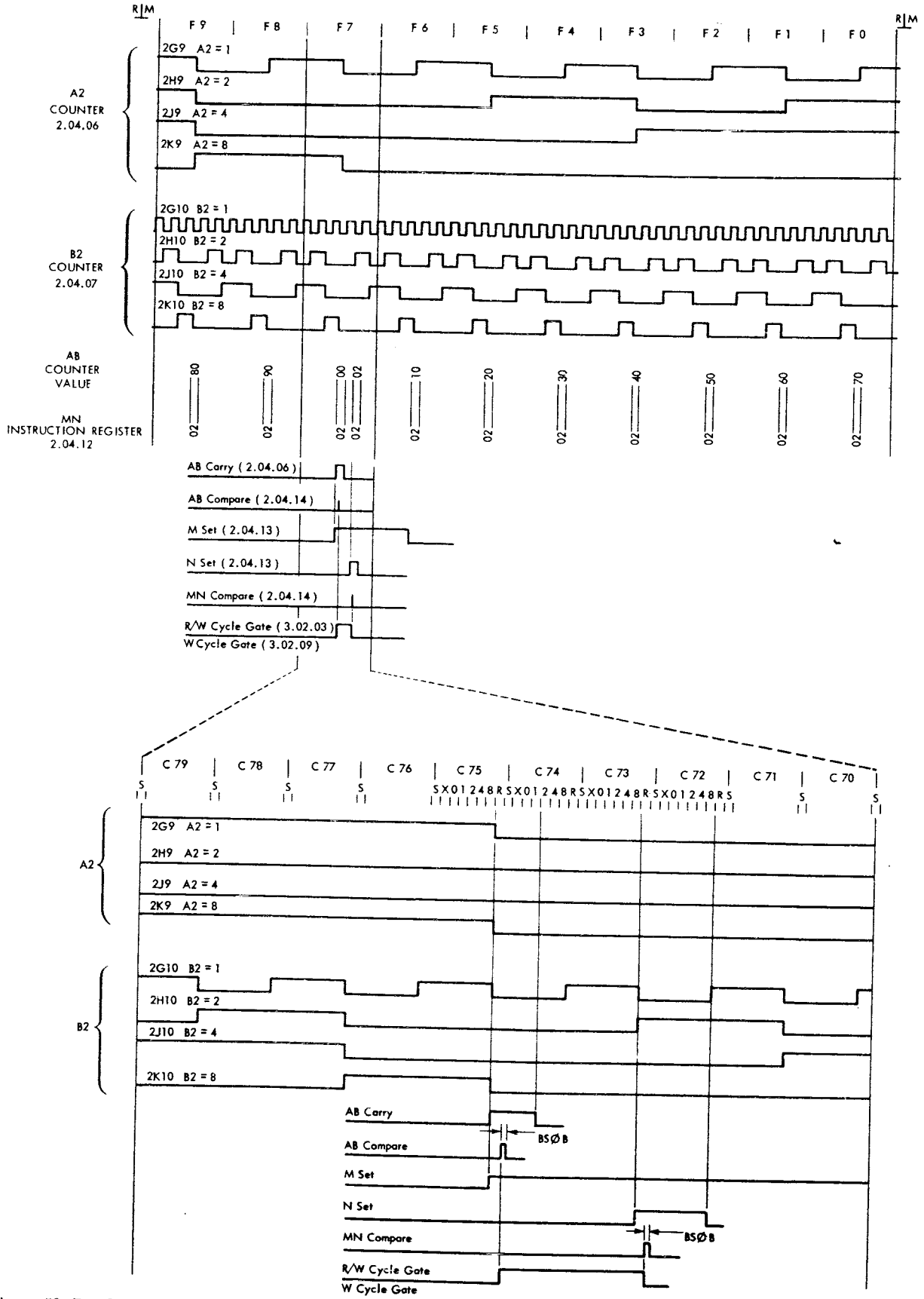


Figure 50. Development of W Cycle Gate (Instruction: W53C7402bb)

compare. During W cycle the B_2 counter is advanced instead of the B_1 counter (2.04.03). Therefore, the AB carry on 2.04.06 is a result of a carry in the A_2B_2 counters. MN compare is developed just as it was during R cycle except M is compared to A_2 and N to B_2.

Parity Checking

All data entering or leaving core buffer is parity checked, i.e., each character transferred must have an odd number of bits. The data moving to the instruction register on I cycle is also parity checked. This can be seen on the data flow diagram, Figure 7. When an error occurs we want the machine to stop processing immediately in the error cycle. The console will indicate the cause of stopping (parity error) and the cycle. Processing may be restarted at the beginning of I cycle in the same program step by depressing the check reset key followed by the program start key.

OBJECTIVES:

1. Count the bits in each character and turn on parity error if the number is even.
2. Stop processing with cycle ready trigger still ON.
3. Reset parity error with check reset key; restart in I cycle with program start.

Parity Error Trigger. Figure 51 illustrates the operation of the parity error trigger (3.02.14-3U5) during I cycle. R and W cycles are similar in operation. When an error is detected 3U5 will be pulled 10 pin high. The actual counter of bits is the parity control trigger 3W4. At the beginning of each character, Bs∅C, it is set 10 pin high. The bits of data comprise a binary input, the first bit after reset flipping the trigger OFF, the second ON. If no bits or an even number of bits are present the trigger will be 10 pin high at the end of a character, Bs∅B. The condition of the trigger is tested each Bs∅B at 3V5 and if 10 pin high, the parity error trigger is turned ON. Notice in Figure 50 the first test pulse (Bs∅B) is blocked and the final one permitted by the slow rise and fall of the I cycle gate.

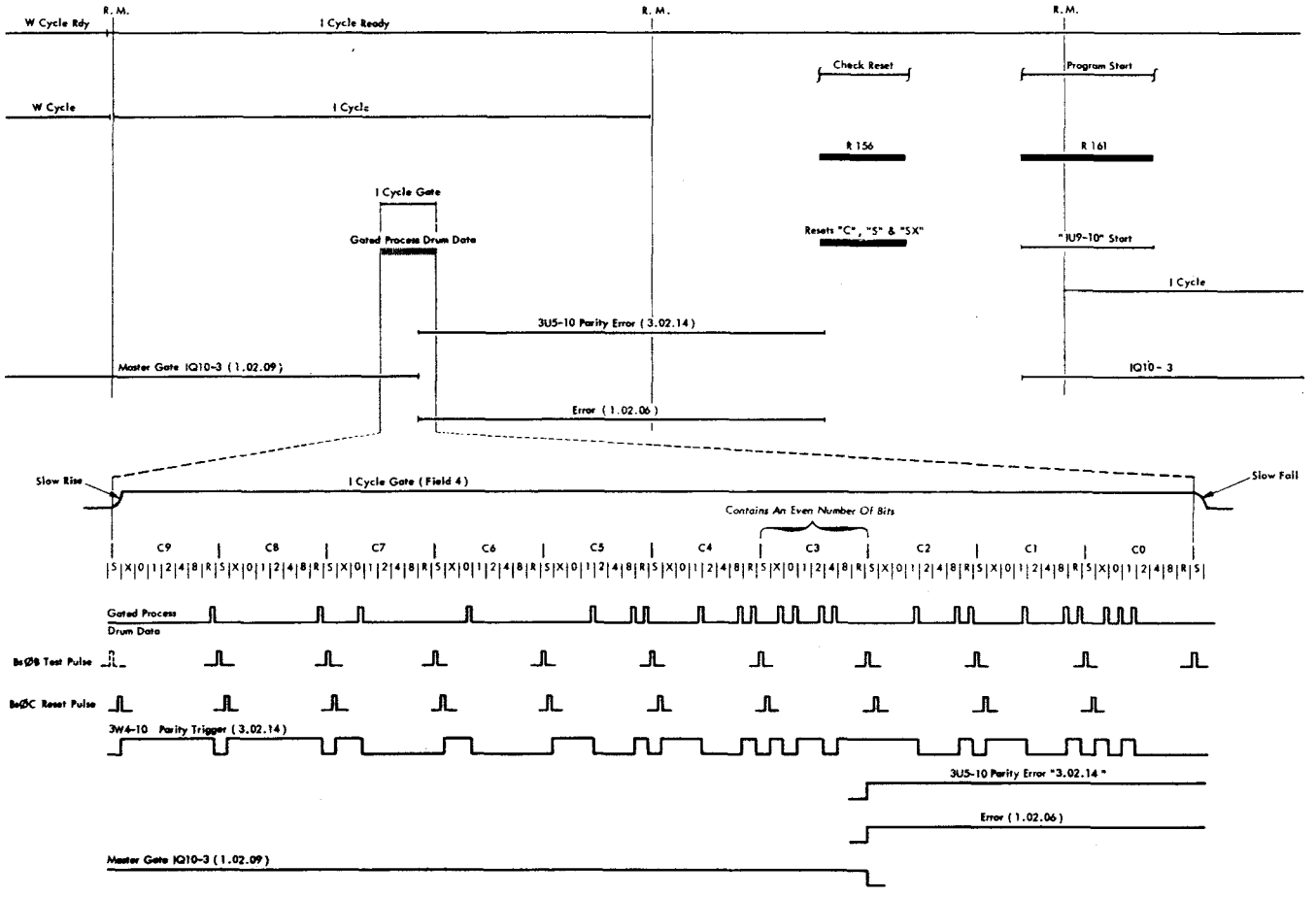


Figure 51. I Cycle Parity Error

Stop Processing. On 1.02.06 the parity error joins the other possible error conditions. Any of them will raise the common error line. This error line turns the master stop trigger 10 pin high on 1.02.09 to block all cycle starts. The error line blocks cycle complete on 1.02.08, and finally it directly turns OFF any of the cycle triggers which may be ON. Blocking cycle complete prevents a cycle end which allows the cycle ready trigger to remain ON. This trigger and the parity error trigger have neons on the console (6.15.07, 6.15.08).

Reset Parity Error Trigger. Depressing the check reset key picks R156 (1.02.03) developing three levels of reset: C, SX, and S. This resets the parity error and parity control triggers 3 pin high, all cycle and cycle ready triggers OFF except I cycle ready. Depressing the program start key will pull the master stop trigger 3 pin high, permitting a cycle start.

Compander (optional)

This optional feature permits the compression or expansion of process drum track fields during a track to track transfer. This is illustrated in Figures 52 and 53. Notice in the compress operation, the portions of each field to be compressed are of the same length and all begin with character 9 (low order) position. The same is true of the expanded fields during the expand operation. Also note that all fields, compressed or expanded, are adjacent.

The compander operation is called for during processing by placing a 7, 8, or 9 in the 10th character of a program instruction. Q=9 calls for compress; Q=8 is an expand operation; Q=7 is a compress-expand operation.

The function of MN characters in the instruction represents the major change in programming. M now tells the machine how many adjacent fields, beginning with the AB address (B must always be 9), are to be compressed or are to be the result of expansion. N now tells the machine how many characters in each field are to be transferred, automatically beginning at character 9. An N of 0 will result in the transfer of 10 characters from each field, a normal transfer operation.

Compress

Of the three operations, compress requires 2 program instructions, the others one instruction.

Using Figure 52, the first instruction L89b9946b9, will transfer four, six digit fields (MN) starting with position 89 (AB) to the first 24 positions of cores.

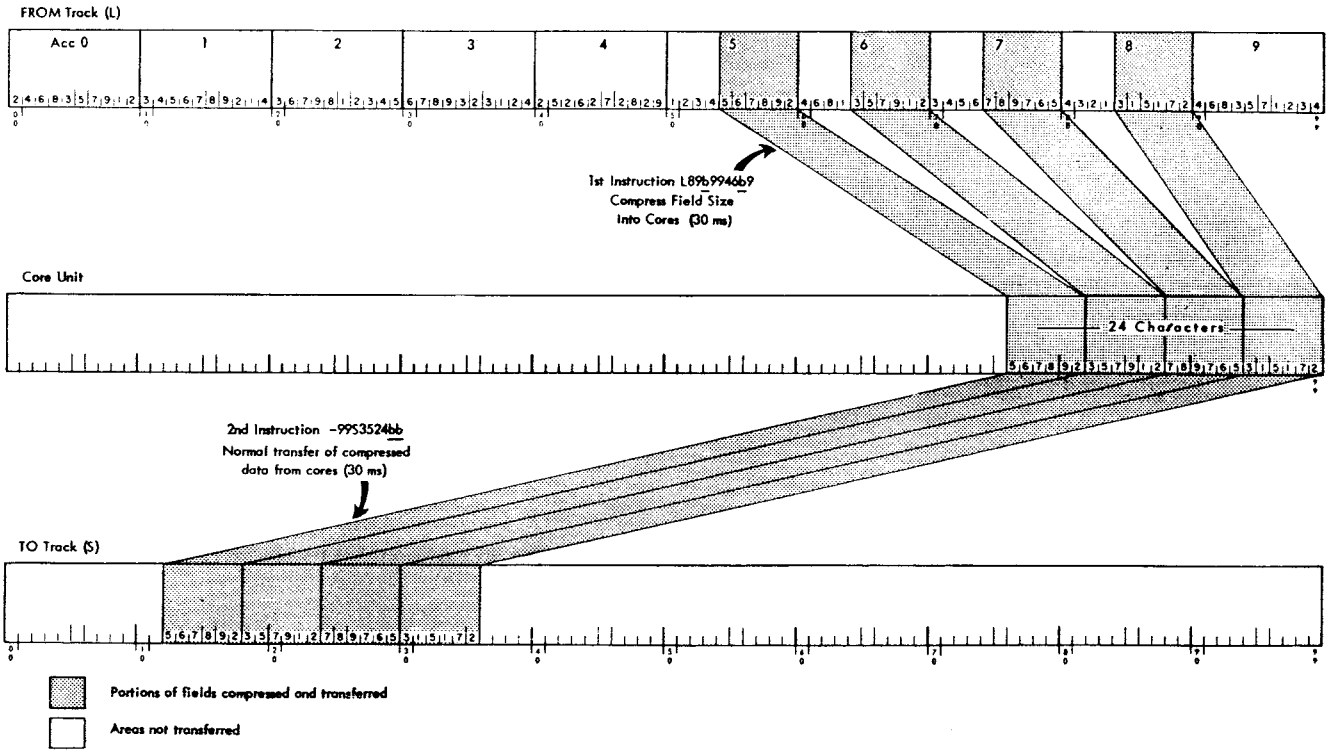


Figure 52. Compress (Q = 9) Function

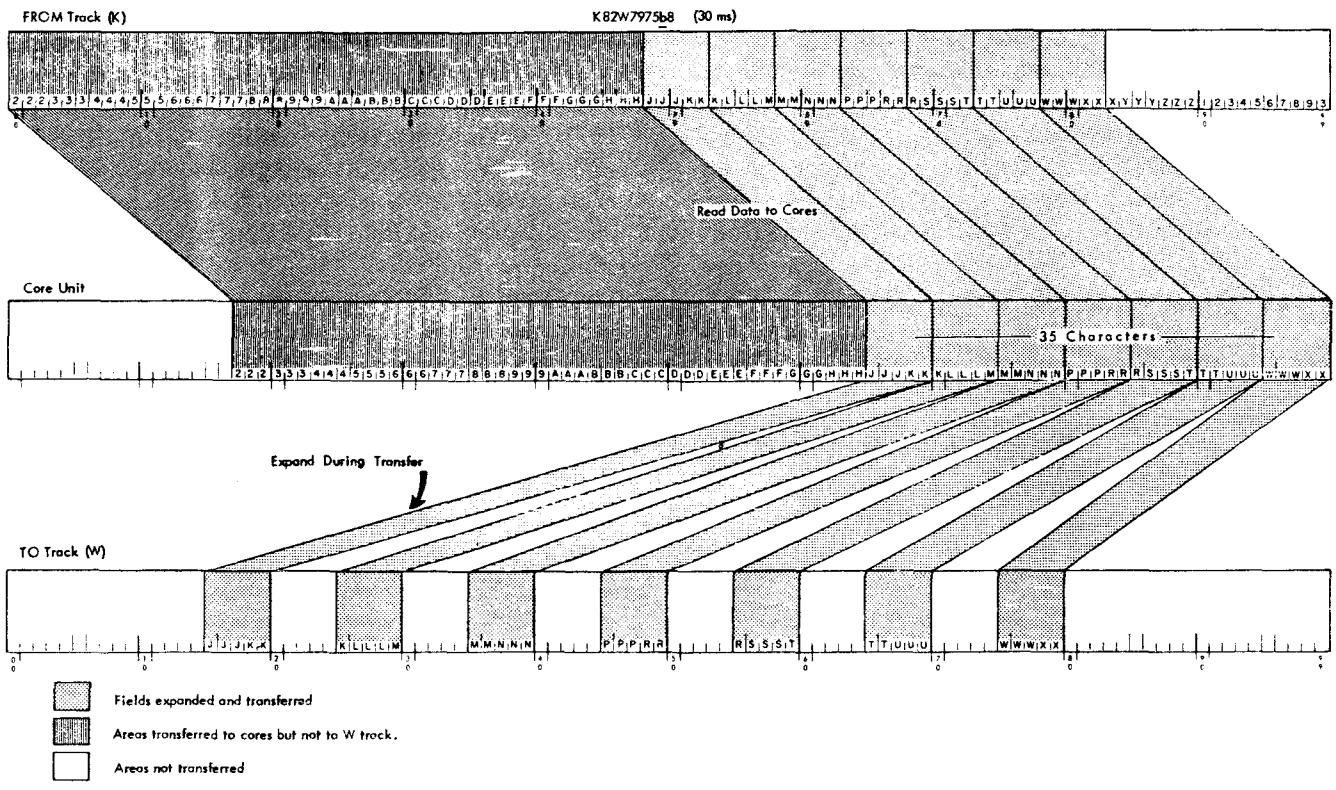


Figure 53. Expand (Q = 8) Function

Since T_2 is blank, no transfer from cores will occur during W cycle. The second instruction then will be –99S3524bb, transferring the first 24 characters in cores to S track, beginning with character 35. If one instruction L89S35346b9 had been used, 46 characters would have been read out of cores to S track on W cycle.

On R cycle the R/W cycle gate will be brought down at character 9 and M set (4N6-3.02.03-optional). This can be seen on the sequence chart in Figure 3. During compander operation MN compare is blocked at AI-4R8a. The read cycle gate is now developed on 3.02.04-optional at AI 3U3 from R/W cycle gate (a C9 to C9 gate), Q = 9 and C9 to N comp. gate. This latter gate, used in all compander operations, is developed on 3.02.08-optional at trigger 3W2. This trigger is always pulled ON at C9 and OFF at N compare (Bs ∅ B) which occurs once during each field. C9 to N comp. gates, 10 per drum revolution, are equal in length to the N in the compress instruction. Switching these gates with R/W cycle gate results in selecting a number of them equal to M (See Figure 54). This becomes the R cycle gate and establishes the core starts.

During W cycle T_2=blank so no head is selected for writing from cores. The W cycle gate will be up for 100 characters and all positions of cores will be read out and then read back in. No data will be destroyed. Cycle complete will occur at CL when the R/W cycle gate goes down (3.02.03-optional).

The second compress instruction, –99S3524bb, is a standard transfer, reading from cores to S track on W cycle. T_1 = – addresses cores during R cycle and is developed on 2.03.11. It causes a cycle complete at CE (1.02.08) and blocks the R cycle gate (3.02.04) so no core starts can occur. A T_1=blank, on the other hand, would raise the R cycle gate and cause BR's to be inserted into cores. This would set the contents of the cores to blanks.

Expand

The expand operation (Figures 53 and 54) requires one instruction of the form K82W7975b8. The R cycle occurs as normal with one exception found on 3.02.03-optional. The R/W cycle gate can not be brought down until CL, which means all information on the FROM track following the AB address will be placed in cores.

During W cycle the R/W cycle gate (3.02.03-optional) is a character 9 to character 9 gate for the number of fields specified by M, in this case seven. The not W cycle gate (3.02.08-optional) is a product of the ten C9 to N comp. gates and the R/W cycle gate "anded" at AI 3Z2. This, in turn, becomes the W cycle gate developing the core starts.

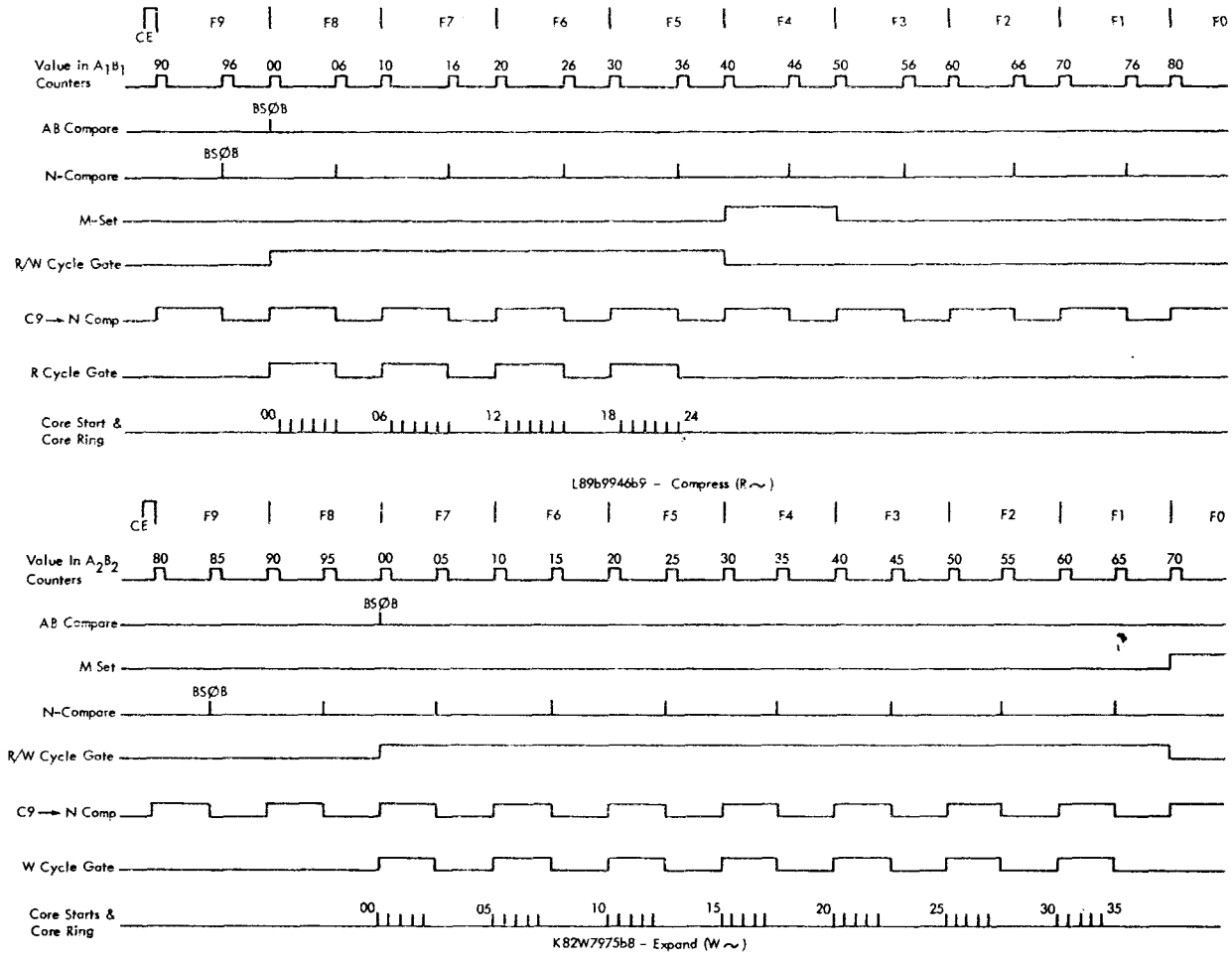


Figure 54. Compander Sequence Chart

Compress Expand

A 7 in character 10 position of the instruction will compress the fields on R cycle, then expand them to the original size on W cycle. The primary advantage of this operation is the ability to change the information in portions of adjacent fields leaving the rest of each field intact. To accomplish compress-expand, the 7 in the Q register will raise both Q=8 and Q=9 lines on 2.06.01-optional from AK 2L6.

Increased Processing Speed (Optional)

IPS is a special feature that may be installed in the RAMAC 305 to reduce the time required to transfer data between process drum tracks. This feature is automatic in operation and requires no special programming nor control panel wiring.

Normal transfer operations require 3 drum revolutions (30 ms) without this feature. I, R, and W cycles always begin and end with a reference mark, even though the actual transfer may take only a few character times. With IPS installed, the system advances to the next cycle as soon as the transfer is complete, without waiting for a reference mark. For example, as soon as the instruction has been placed in the instruction register during I cycle, R cycle can begin. When the data specified by the A_1B_1 counters and the MN register has entered cores, W cycle can begin. As soon as the data from cores has been written in the specified drum location, I cycle can be started. With optimum location of instructions and data, an IRWI sequence may be completed in 10 ms. The only limitation on location of data is that 4 character times exist between the end of one address to the beginning of the next. Any less will cause the machine to take another cycle. This 4 character gap between cycle gates is necessary to allow the drum head selection circuits time to become established.

To aid in servicing the machine, a CE switch has been included which can cripple the IPS feature.

Circuit Operation

At the time of this printing, system diagrams are unavailable. To aid in a discussion of IPS, two simplified circuit diagrams are referred to (Figures 55, 56) and a sequence chart is included (Figure 57).

On a standard machine the cycle sequencing operates similarly in all three types of cycles, I, R, and W. A sequence RM tests all three cycle ready triggers to turn ON one of the cycle triggers. Then a cycle gate is developed from AB compare to MN compare (or program gate during I cycle) to gate the data to and from the drum. At the fall of the cycle gate the cycle complete gate trigger (1H9-1.02.08) is turned ON, then at CLB0 this trigger is sampled to develop a cycle complete pulse. The cycle complete pulse turns ON the next cycle ready trigger which then turns OFF the previous cycle trigger. The next cycle start (sequence reference mark) then begins the new cycle.

With IPS three major circuits need revising. A cycle start pulse must be available at any character time, 4 characters after the actual data transfer of the previous cycle is completed. A cycle complete pulse must be available at any time. Finally, the A_1B_1 counters and the A_2B_2 counters must be corrected after I cycle if we are to use our AB carry to begin a transfer. This correction is necessary to simulate starting the counters at CEBR.

OBJECTIVES:

1. Start a cycle at B0 of any character or at RM.
2. Cycle complete pulse as soon as transfer is complete.
3. Correct A_1 and A_2 counters before R cycle begins.

Cycle Start. Refer to Figure 55. The cycle start pulses, sampling the cycle ready triggers are now conditioned B0's or sequence RM's. I cycle can begin at B0 if I cycle ready is ON and the program gate is not high. The not program gate prevents I cycle from com-

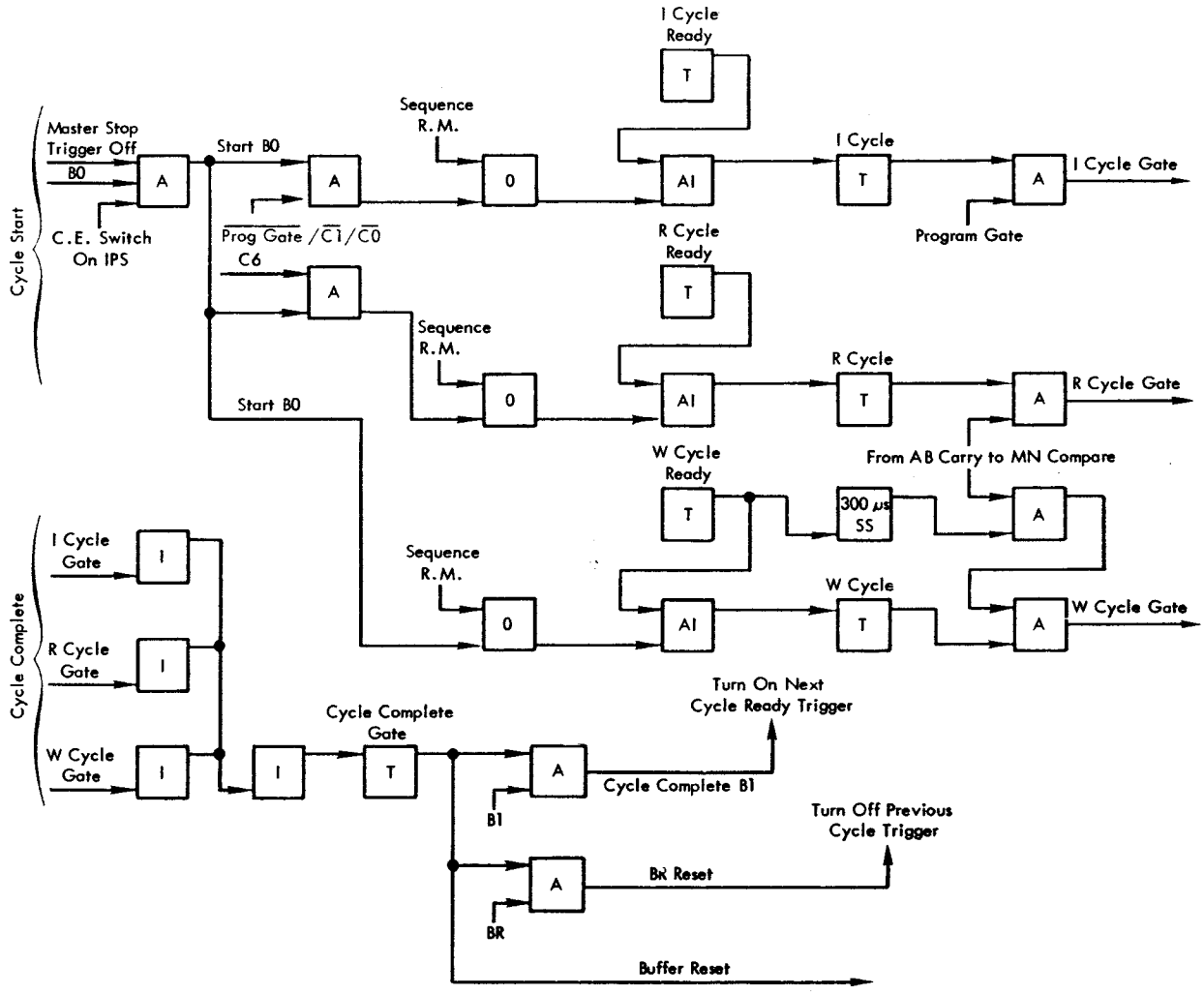
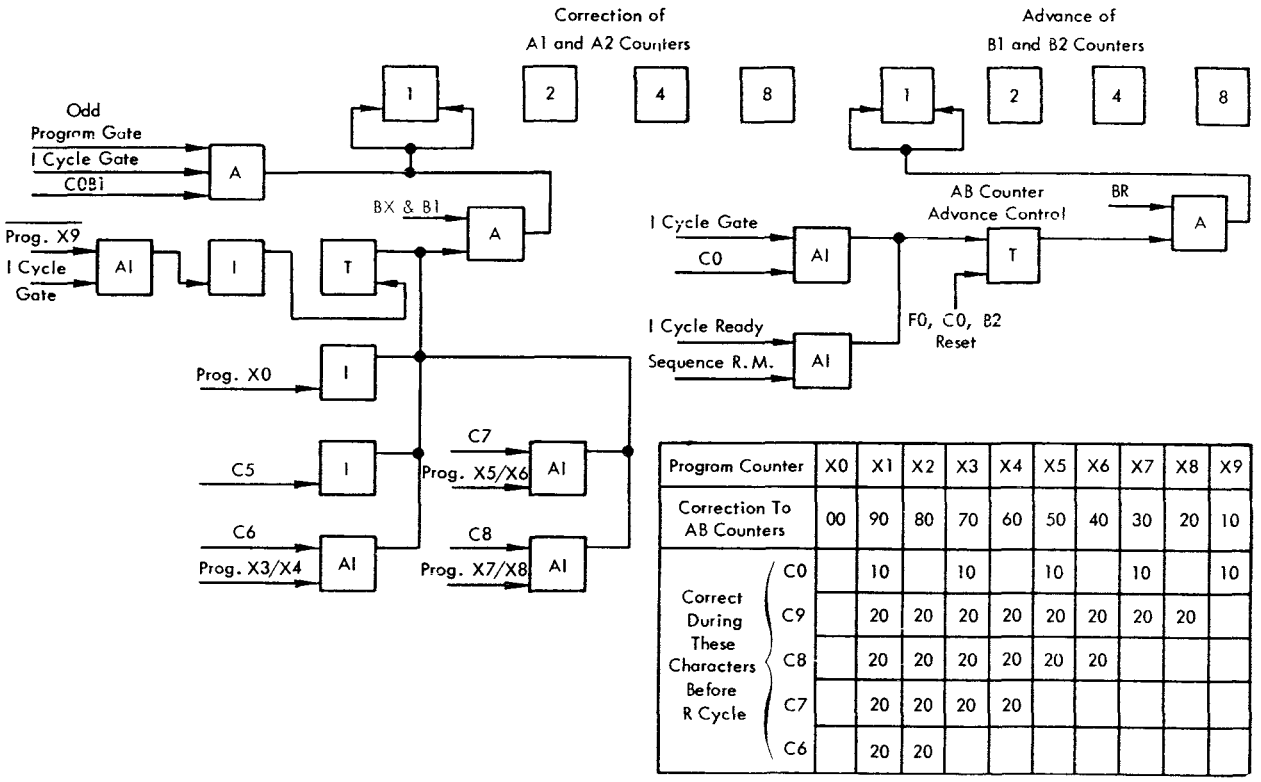


Figure 55. IPS Block Diagram (A)



Program Counter		X0	X1	X2	X3	X4	X5	X6	X7	X8	X9
Correction To AB Counters		00	90	80	70	60	50	40	30	20	10
Correct During These Characters Before R Cycle	C0		10		10		10		10		10
	C9		20	20	20	20	20	20	20	20	
	C8		20	20	20	20	20	20			
	C7		20	20	20	20					
	C6		20	20							

Figure 56. IPS Block Diagram (B)

ing up in the middle of the field in which the next instruction is located. Also I cycle cannot be turned ON during C1 or C0. This prevents I cycle from beginning sooner than 4 characters after W cycle ends and can be more fully understood after cycle complete has been discussed.

R cycle can begin whenever R cycle ready is ON at any C6B0. Since the I cycle transfer of data is always complete at the fall of character 0, the R cycle transfer can begin 4 characters later, at C5 time. R cycle trigger will go ON at C6B0.

W cycle can come ON at B0 when W cycle ready is turned ON. This will occur as soon as the read cycle gate falls. We must delay the actual transfer of data for 4 characters, however. Notice that W cycle ready trigger fires a 285 μs single shot. Until this delay is complete, the A_2B_2 carry cannot develop a Wcycle gate.

Cycle Complete. In each case listed above, the B0 or RM cycle start tested the 3 cycle ready triggers (I, R & W) to turn ON the next cycle trigger. On a standard machine these ready triggers were turned ON by a cycle complete pulse at CLB0. With IPS we will develop a cycle complete pulse at B1 of the character following the last character transferred, turning ON the cycle ready trigger immediately. In Figure 55 the cycle complete gate trigger still comes ON with the fall of the I, R or W cycle gates. This trigger is now sampled every B1 time to develop a cycle complete pulse and turn ON the next cycle ready trigger.

Now let us examine the I cycle start which is blocked every C1 and C0. If the W cycle gate should fall at the end of character 3 of the field preceeding the instruction field, there would be only 3 character times between W and I cycles. In this case, I cycle must be blocked until after the program gate. The cycle complete trigger will be turned ON at Bs$\varnothing$B between character 3 and 2 (MN compare). The I cycle ready trigger will come ON with cycle complete at C2B1. The next B0 start pulse would occur at character 1 time but it is blocked at the "and" switch by the not program gate, not C1, and not C0 line. I cycle will not come ON until C9B0 following the program gate.

AB Counter Correction and Advance. In normal machine operation the A_1B_1 counters were advanced during R cycle beginning at CEBR. As the drum character ring advanced from 99 toward 00 the AB counter value increased until it rolled from 99 to 00, developing an AB carry which started the transfer. The A_2B_2 counters advanced during W cycle, performing the same function. With IPS both counters advance during all cycles except I cycle. On Figure 56, BR's "and" with the ON side of the AB counter advance control trigger. This trigger is intially turned ON at C0 of the I cycle gate and OFF at F0, C0, B2. For all other cycles it is turned ON at RM and OFF at F0, C0, B2, allowing 100 BR's to impulse both counters.

Since these counters may begin advancing at any one of ten fields at C0Br following the I cycle gate, they must be corrected to simulate starting them at CeBr. They will be incorrect by some multiple of ten, determined by the fall of the I cycle gate. This in turn is established by the program gate from the program counters. We find that the A_2 and A_1 counters must be corrected with the tens complement of the value in units position (field location) of the program counter. This can be seen in the chart in Figure 56. By adding these amounts to the A_1 and A_2 counters during the 4 character delay between I and R cycle, these counters will remain in step throughout R and W cycles.

Since we may have to add up to 9 in these positions within 5 character times, we must add 2 each correction character time. This allows us to add 8. Since all four counters (A_1B_1, A_2B_2) have the initial instruction entered by character 1 time of the I cycle gate, we can also use C0 of I cycle for correction of the decimal 1 position if the correction figure is odd. The correction circuit is shown in Figure 56. During the correction time, 2 advance pulses, a Bx and a B1, will impulse the A_1 and A_2 counters, adding 20, each character time. The control trigger determines how many "20's" are added to the counters. It is turned 10 pin high at the fall of the I cycle gate if not in program step X9. It will be plate pulled 10 pin low at C5, C6, C7, or C8 depending on the value in the units position of the program counters. If the program step is X0 the trigger will be prevented from going ten pin high since no correction is needed. Although not shown on the simplified diagrams, the cycle start and cycle complete pulses must be conditioned by a number of other conditions. There are a number of operations requiring a full drum revolution.

Service Aid. The start B0 line is developed at an "and" switch when the master stop trigger is OFF and the CE switch is on IPS. By turning the CE switch to non IPS operation, the start B0 line is low and only the RM can advance the cycles.

Example of IPS Operation. The sequencing chart in Figure 57 illustrates IPS operation with an optimized instruction of A45B4001bb located in field 5.

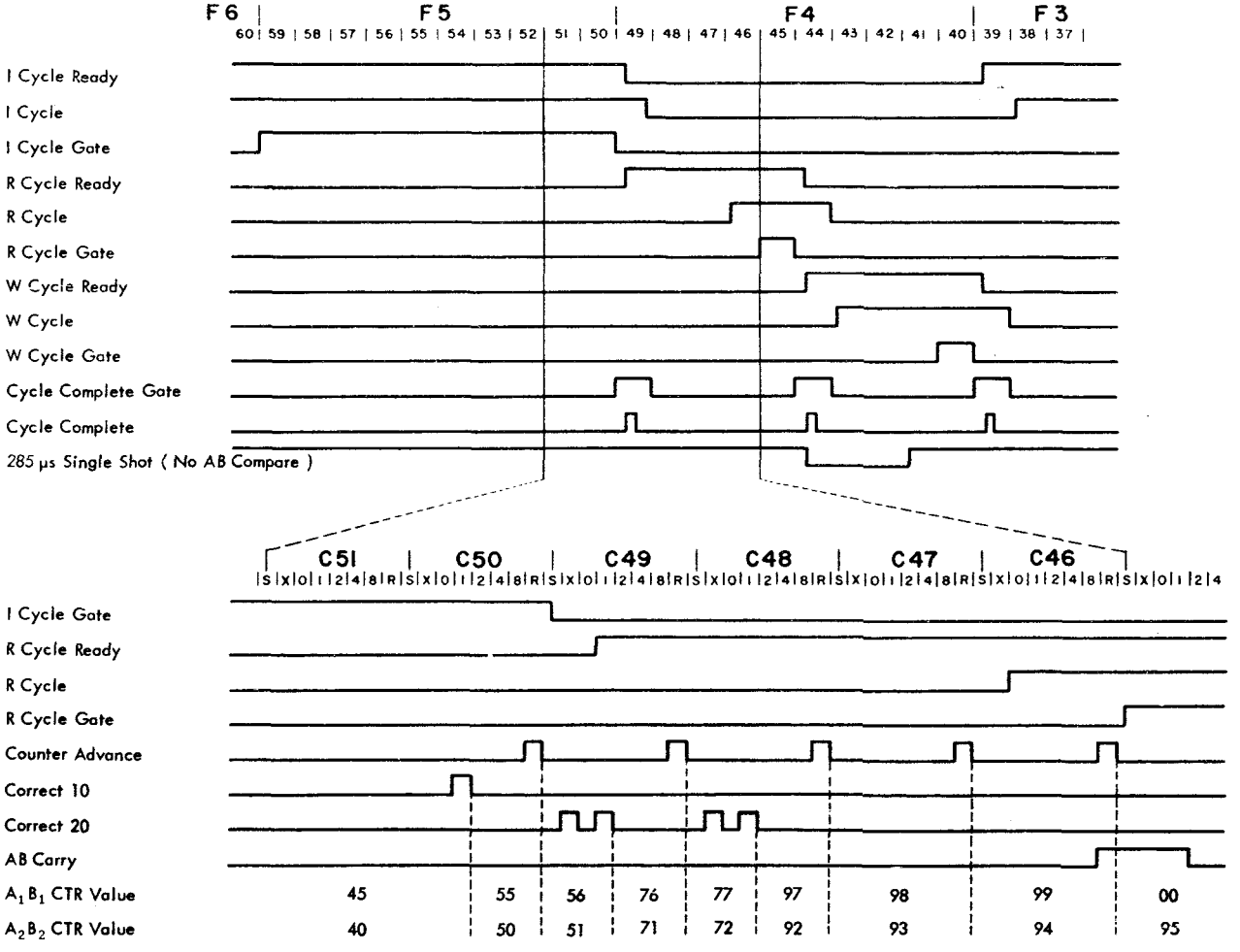


Figure 57. IPS Sequence Chart (Instruction A45B4001bb in Program Step XX5)

File Mechanics

Disk, Track and Record Arrangement

The arrangement of the disks in the file is shown in Figure 58. The file contains 52 disks, however, only 50 of these are used for data storage. The top and bottom disks are dummy disks, used to aid in the regulation of stray air currents within the file. The recording disks are numbered consecutively from top to bottom, 00 to 49. The whole disk array is rotated at a speed of 1200 RPM by a 1½ HP, 220 volt AC motor.

Data is stored on both the top and bottom of each recording disk. There is one read/write head for addressing the top side of the disk and one for the bottom. Both of these heads are mounted in one access arm (Figure 59) which may be positioned to straddle any of the 50 disks.

When the access arm is addressed to any particular disk, it may be moved inward or outward to place the read/write heads at various radial distances from the center. The arm may be detented at 102 different positions. When the arm is detented at any one of its 102 positions, a circular path on the surface of the disk moves past the read/write heads. These circular paths are called tracks. Each track includes the paths both on the top and on the bottom of the disk.

The innermost track and the outermost track on each disk are reserved for use by the Customer Engineer when servicing the file. The 100 remaining tracks, which are used for storage of accounting records, are numbered 00 to 99 from outside to inside.

With the disk rotating at 1200 RPM, each revolution requires 50 ms, which is 5 times as long as a drum revolution. Using a bit frequency in the file approximately equal to the bit frequency of the drum, two complete 100 character records can be stored in each 1/5 of the track circumference, one on the top side and one on the bottom side. Thus, a total of 10 records can be stored on each file track. Record positions 0, 1, 2, 3, and 4 are on the top side of each track; 5, 6, 7, 8, and 9 are on the bottom side.

Disk and Track Selection

In order to select a given track, the arm must be moved from its previous track location to the new track location. This involves one of three types of movement sequences:

1. To move to a numerically higher track address on the same disk, the access arm must move inward only.
2. To move the arm to a numerically lower track on the same disk, the arm must move outward only.
3. To move to an address on another disk; the arm must first be moved all the way out, then up or down to the new disk location, and inward to the selected track.

Since the third movement sequence includes the movements used in the other two, we shall use it as the example for an explanation of disk, track, and record selection.

Access Mechanism

In order to accomplish the necessary movement of the arm, an access mechanism is provided. This consists basically of the following components (Figure 60).

1. A carriage on which the arm is mounted for horizontal movement.
2. A way on which the carriage is mounted for vertical movement.
3. Two access cables, a capstan, two clutches, and a motor to provide movement to the arm and carriage.
4. A disk detent to keep the carriage fixed in place while the arm moves into the disk array.
5. A track detent to fix the arm's position at the correct track.

Carriage and Disk Detent

In order to allow the arm to move vertically, it is held in a carriage that is free to move vertically on a specially constructed way (Figure 60). The arm itself is free to move horizontally within special guides on the carriage. However, the carriage cannot move vertically at the same time that the arm is moving horizontally without damaging the disks. Therefore,

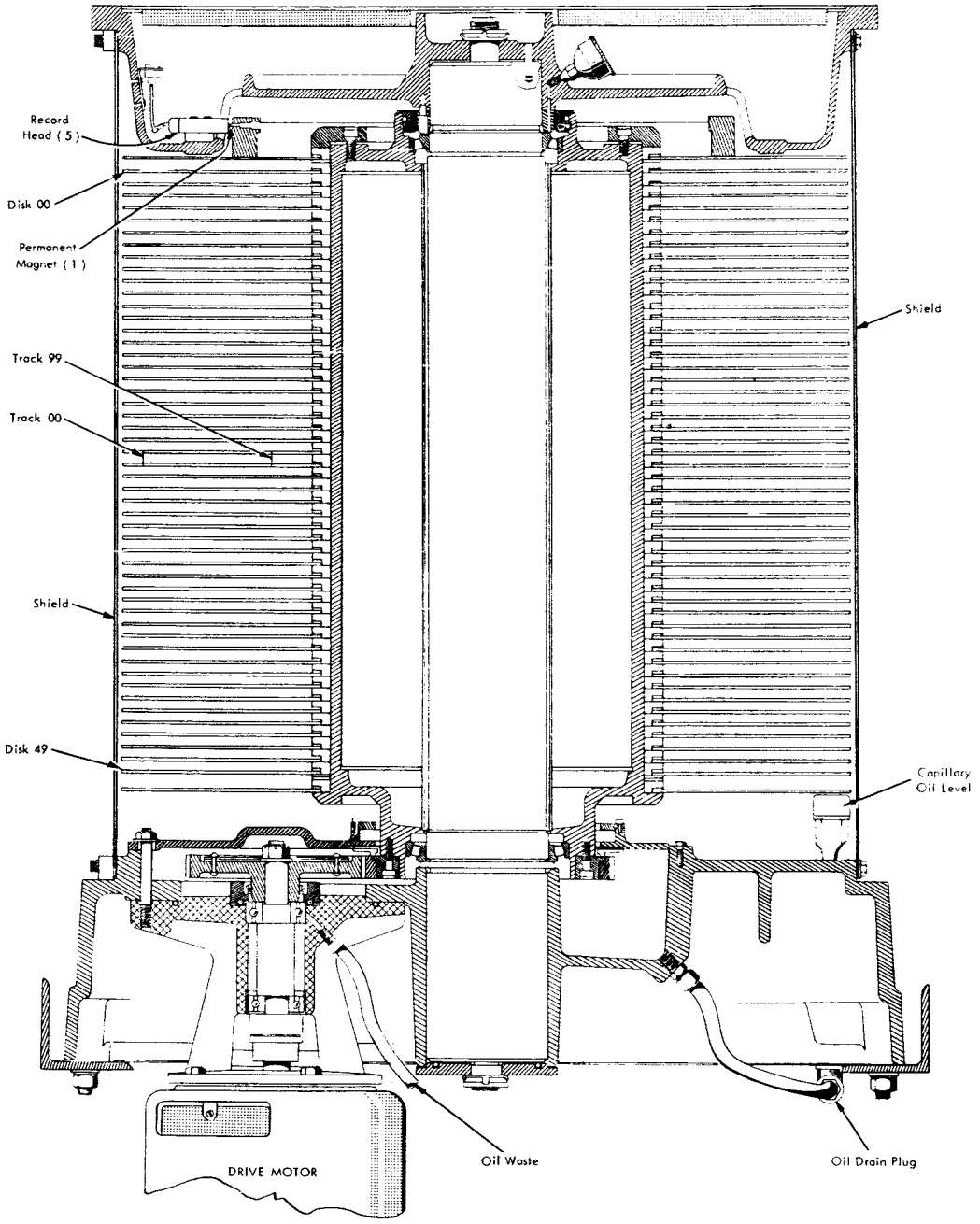


Figure 58. Disk Assembly

a detent is provided to lock the carriage to the way while the arm is extended or retracted. Another detent is provided to lock the arm all the way out, in the home position, while the carriage moves vertically. This disk detent (which locks the carriage to the way) and the fail safe bar (which locks the arm in the home position) are mechanically linked so that one or the other must be engaged at all times. This linkage (Figure 61) is called the fail safe interlock.

When the arm is retracted to the home position, out air pressure is applied to the disk detent piston to unlock the carriage so that it can move. When the correct disk has been located, in air pressure is applied to the disk detent piston to lock the carriage to the way and unlock the arm.

Capstan and Cables

The capstan and cables provide a method of applying power to move the arm and the carriage. The two cables are wrapped around the capstan in opposite directions (Figure 62). One of these cables goes up the far side of the way, over the tension adjusting

pulley, down and through a pulley on the carriage, and is fastened to the front end of the arm. The other cable goes up the near side of the way, through a pulley on the carriage, and is fastened to the rear end of the arm.

If the disk detent has locked the carriage to the way, rotating the capstan clockwise will cause the arm to move in; rotating it counterclockwise will cause the arm to move out.

If the arm is locked in the home position by retracting the disk detent, clockwise capstan movement will cause the carriage to move down; counterclockwise capstan movement will cause the carriage to move up.

Servo Clutches

The capstan may be caused to rotate in either direction by energizing one of two clutches attached to the capstan shaft. Figure 63 shows an exploded view of one of these clutches. The rotor is fastened to the capstan shaft, and the clutch housing is free to move about the shaft. The two clutch housings making up the pair of servo clutches are each driven in the opposite direction by a pinion assembly on the shaft of a 1/3 HP access drive motor. This pinion is shown in Figure 64, along with its clutches. One of these clutches is shown in cross section.

The space between the rotor and the housing is filled with powdered iron and graphite. The application of a direct current to the magnet coil will cause the powdered iron particles to align themselves and form a magnetic bond between the continuously running housing and the rotor.

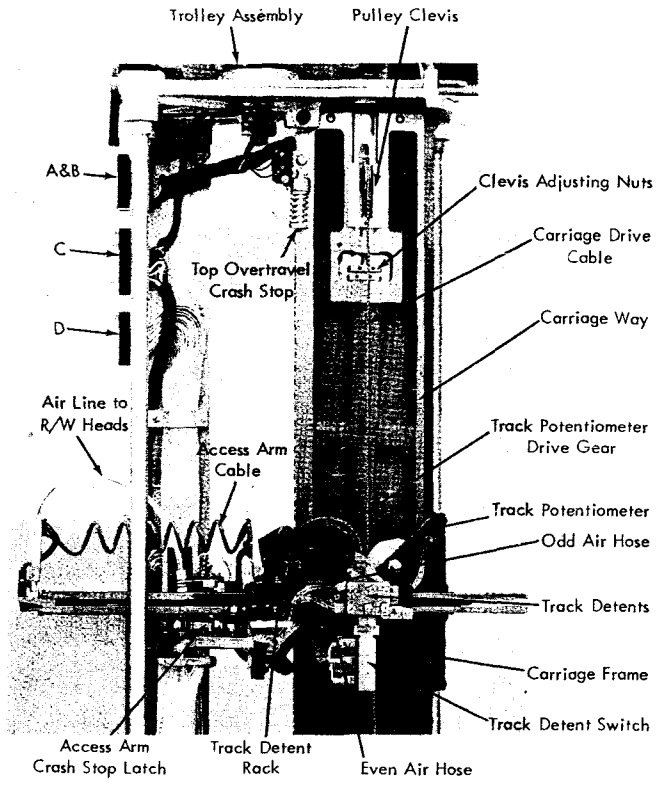


Figure 60. Carriage and Arm Assembly

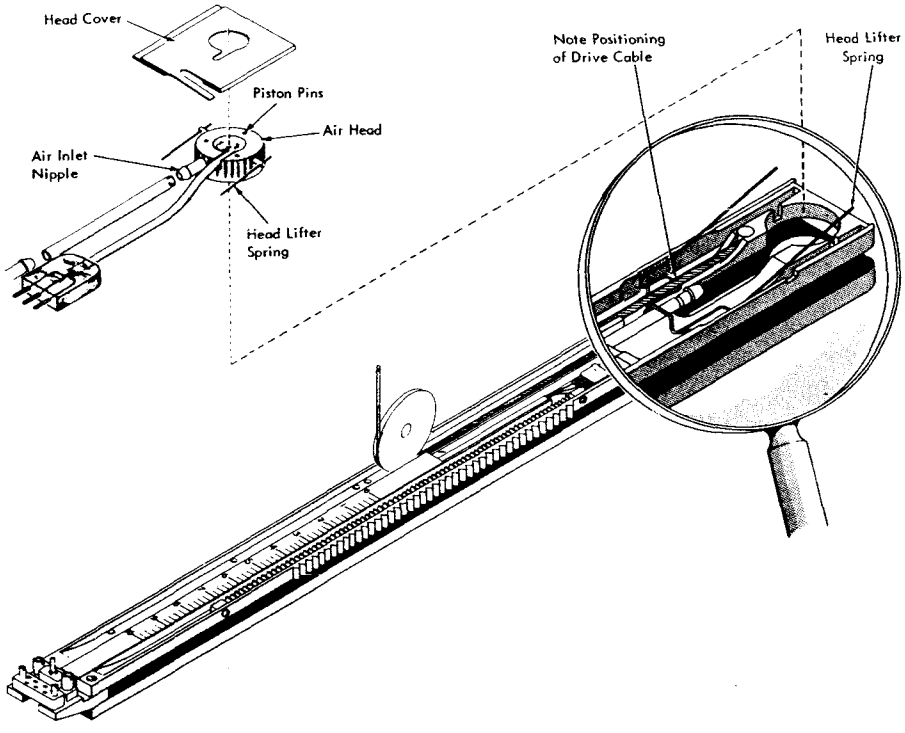


Figure 59. Access Arm

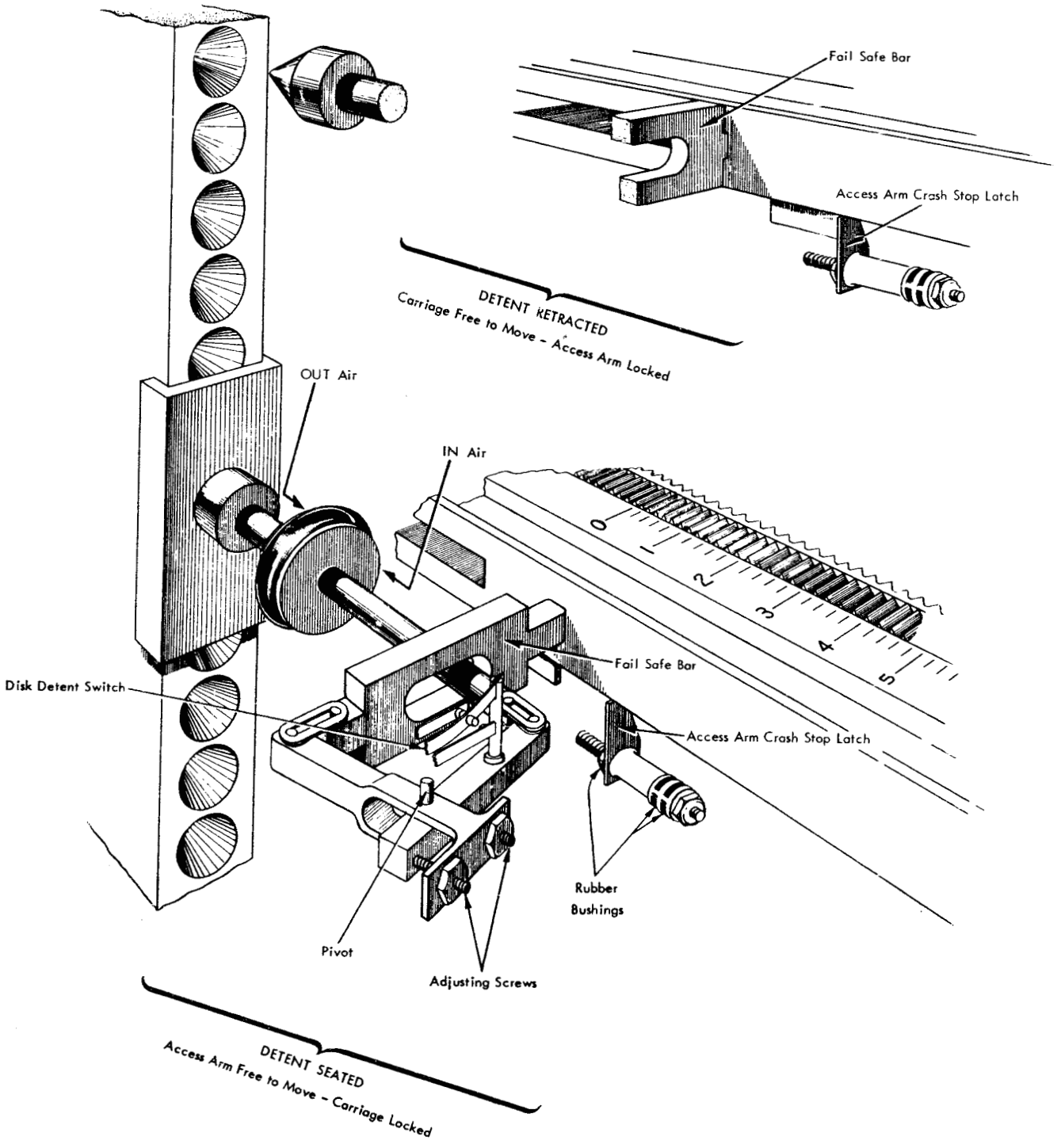


Figure 61. Disk Detent Operation

The servo control circuits are designed so that only one clutch is energized at a time. If one of these clutches is energized to produce the desired movement of the arm or carriage, the other will be energized as the addressed position is reached to cause dynamic braking.

Track Detent

Once the arm has been moved into the correct track, a track detent is driven by air pressure into a land in the rack on the side of the arm (Figure 65). In order to allow the rack to have teeth large enough to effectively hold the arm in place, two detents are

provided, one for even track addresses, and the other for odd addresses. Thus, one arm rack tooth is used to hold the arm for two tracks, depending on which detent is used. Both detents are air operated and spring returned.

Record Selection

When the access arm is detented so that its read/write heads are scanning a particular track, further selection is necessary to obtain one specific record.

The selection between the records on the top side of the disk and those on the bottom is accomplished by the side relay. When normal, this relay connects the read/write circuits to the top head, when transferred, to the bottom head.

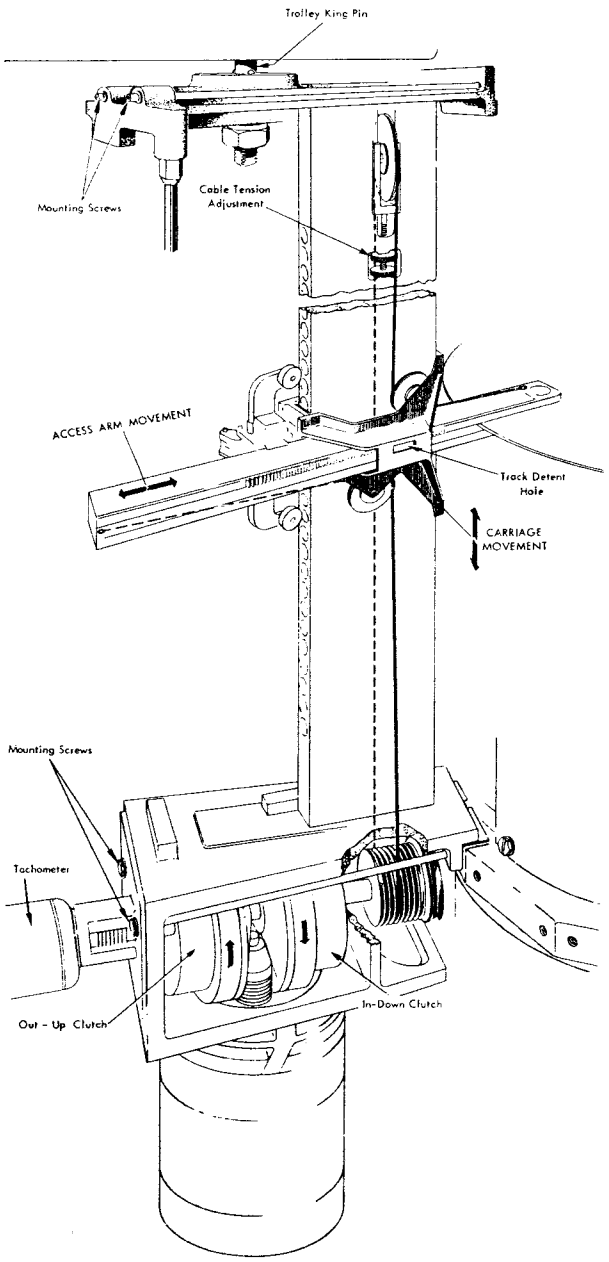


Figure 62. Access Mechanism

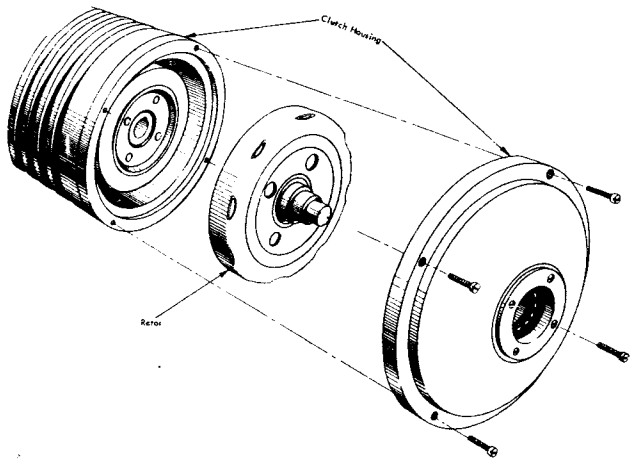


Figure 63. Exploded View of Magnetic Clutch

The selection of one of the five records on the selected side of the selected track is accomplished with the aid of the record heads. These heads are mounted on the top casting at intervals of 72°. A permanent magnet mounted on the top dummy disk moves past one record head every 10 ms. The relays which establish the record address connect the proper head into the record selection circuit to provide a record start pulse at the correct time. The same relays connect a second read head into the circuit to supply a record stop pulse 10 ms after record start. The record stop pulse serves as a safety feature.

Read/Write Heads

The actual reading and writing of a file record is done by the read/write heads. Figure 66 shows the physical arrangement of the coils used for reading or writing on the disk. The read/write coils have a core consisting of 8 laminations, while the erase coil core has 14 laminations. The erasing of a broader path than is used for writing and reading helps minimize extraneous "noise." The read/write head is cast in plastic and mounted in a larger mechanism called the air head (Figure 66).

Figure 59 shows the air heads as they are mounted in the access arm. The purpose of the air heads is to position the read/write head in relation to the disk. When the access arm is advanced from a position clear of a disk to a position straddling a disk, the read/write heads must be in a retracted position to avoid striking the edge of the disk. When the arm is detented at a track address, the read/write heads must be positioned close to the disk for reading and writing.

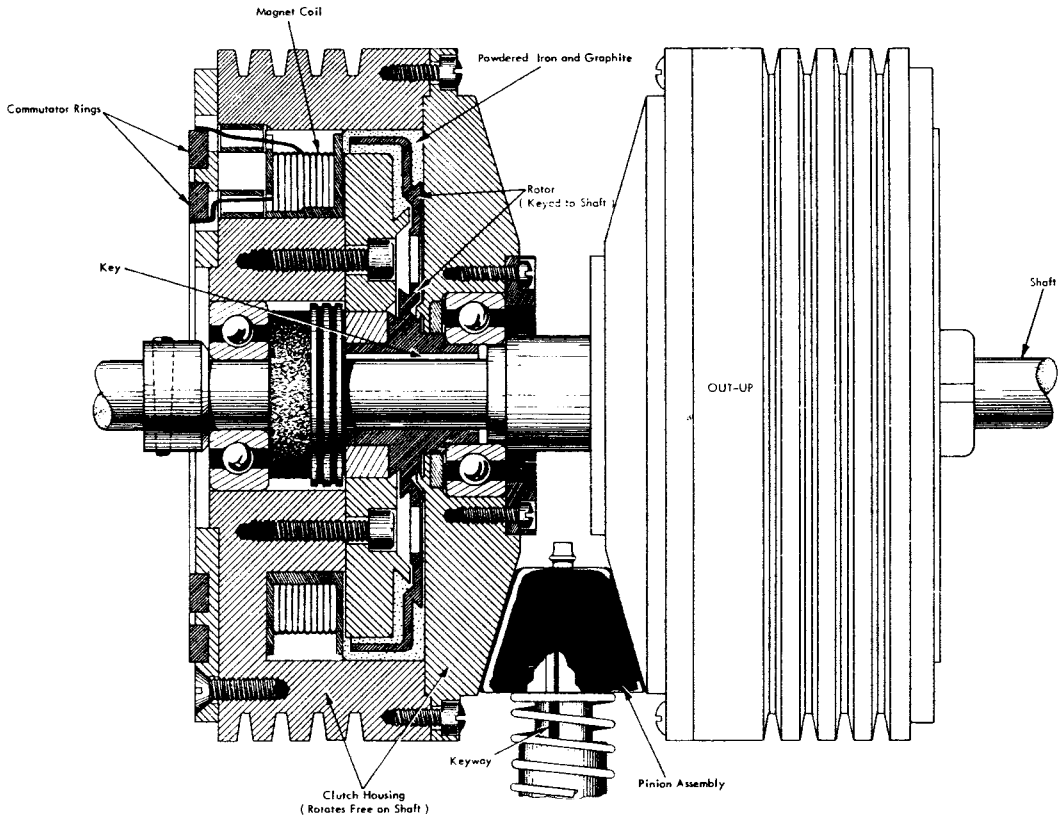


Figure 64. Magnetic Clutch Assembly

The positioning of the air head (and the read/write head which it contains) is controlled by the application or removal of air pressure. If no air pressure is applied to the head, the springs act against the gimbal pins to hold the head against the head cover. When air pressure is applied to the air head, the three pistons are forced to protrude from the head against the head cover. The stationary head cover limits the movement of the pistons, forcing the head away from the cover and toward the disk. To keep the head from scraping the disk, air is expelled against the disk from six small orifices in the head. The applied air pressure thus causes two distinct forces to impel the head in opposite directions. The point at which these forces balance allows the head to ride about .0003" from the surface of the disk. When air is applied, the heads are said to be down, even though the bottom head is moved upward to reach its active position.

Servo Control Mechanism Logic

The preceding material has explained the mechanisms required to move the read/write heads from one address to another. Since the various actions involved in a servo operation are controlled electronically, some means of translating the positions of the access arm and carriage into electrical signals and controlling their movement is required.

Track Potentiometer Logic

The track potentiometer provides a means of indicating electrically the distance and direction that the access arm must be moved to reach the addressed track. This potentiometer is mounted on the carriage as is shown in Figure 60. The wiper is geared to the access arm. As the access arm is moved from it's home position, the wiper moves from one end of the potentiometer resistor strip toward the other.

The upper part of Figure 67 shows the logic of the track potentiometer operation. A 150 volt floating power supply is connected across the extremes of the potentiometer. The position on the potentiometer resistor strip corresponding to the newly addressed track is grounded. However, since the track potentiometer is not physically large enough to permit a separate tap for each track position, taps are provided for track positions 00, 20, 40, 60, 80, and 100 only. Intermediate track positions are addressed by grounding a point on a voltage divider network connected between two adjacent taps. The selection of the grounding point is accomplished by the track ad-

dress relay tree (8.02.02). Ground potential is provided through the disk null relay N/O points which are transferred when the carriage is detented at the correct disk.

If the wiper receives a positive signal, as is the case in Figure 67, this voltage is taken through the home relay N/C points (the home relay is down when the carriage is detented) to the differentiating clutch amplifier. A positive voltage causes the in and down clutch to be energized. This moves the arm in.

A negative wiper signal follows the same path to the clutch amplifier, but energizes the out and up clutch.

A zero wiper signal causes neither clutch to be energized. However, it does cause an output from the track null detector, which is used to apply air to the correct track detent.

Disk Potentiometer Logic

The disk potentiometer provides a means of indicting electrically the direction and distance that the carriage must be moved to reach the addressed track. It operates on the same principle as the track potentiometer; however, the disk potentiometer resistor strip is actually mounted on the side of the way. The spacing of the disks is sufficient to allow a separate tap on the disk potentiometer strip for each disk position. The disk potentiometer wiper is mounted on the carriage.

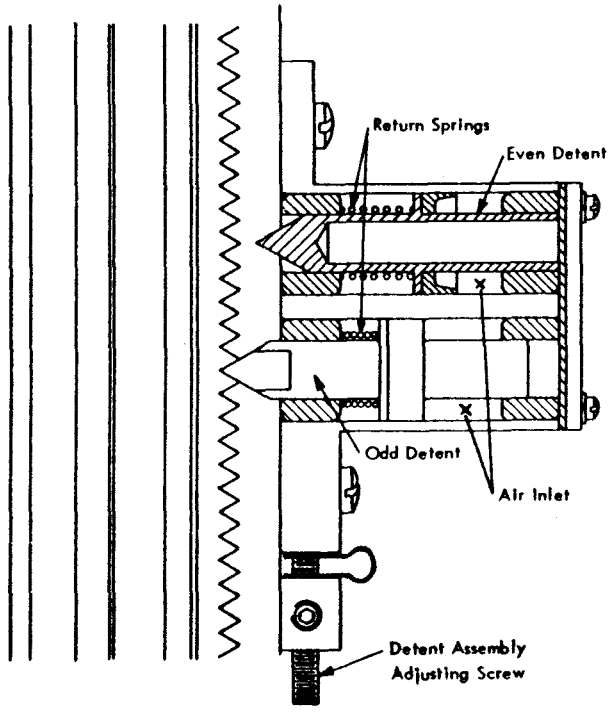


Figure 65. Track Detent

The output at the disk potentiometer wiper is fed to the disk null detector and a N/O point of the home relay. If the home relay is up (disk detent not engaged), this signal is fed to the clutch amplifier to control the movement of the carriage.

The output of the disk null detector controls the disk detent air and the disk null relay (top of Figure 67).

Disk Detent Switch

When the disk detent is disengaged, the disk detent switch is transferred to pick the home relay (8.04.03). Since disengaging the disk detent also frees the carriage to move, the control of the clutches is given to the disk potentiometer when the home relay is picked, as was seen in the discussion of the disk potentiometer.

Tachometer Logic

The tachometer provides a means for controlling the speed of movement and deceleration of the arm or carriage during a servo operation. It is essentially a DC generator, which is mounted on the clutch shaft.

As the clutch shaft gathers speed, the tachometer supplies a potential that builds up to a maximum of approximately 25 volts. The tachometer signal has the same polarity as the potentiomenter signal which has energized the active clutch, but the two signals oppose each other in the differential clutch amplifier. As the carriage or arm approaches the addressed position, the wiper signal becomes less than the tachometer signal. This causes the opposing clutch to be energized to provide dynamic breaking. With proper adjustment, the carriage or arm will decelerate to a smooth stop without oscillation or overshoot.

Air Valve Solenoids

The air valve solenoids are provided to control the air used to position the read/write heads and to operate the two track detents and the disk detent. These are located at the lower part of the access mechanism, on the side away from the disks. From top to bottom, these solenoids control the following: odd track detent, even track detent, head, disk detent in, disk detent out.

Air Compressor

Compressed air is supplied to the air valve solenoids from a piston type compressor currently located in its own cabinet. Previous models were located under the file. A schematic of the remote air compressor is shown in Figure 68. One or two compressors may be used depending on the requirements of the system. Air is delivered from the tank to the file through flexible hose. A solenoid operated vent valve will

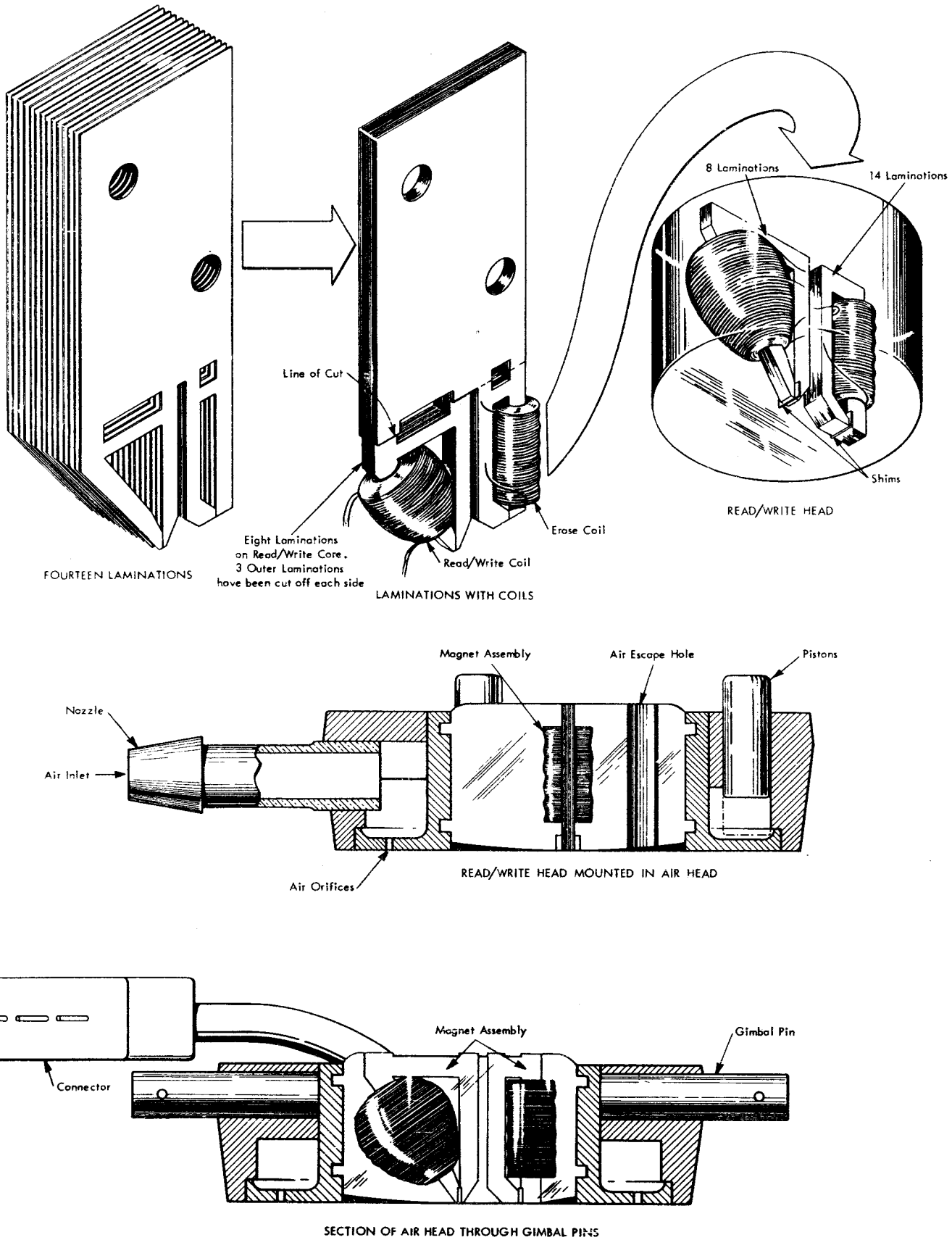


Figure 66. Read/Write Head and Air Head

open the file air lines to atmosphere if the file is taken off line. Water from the tank and lines accumulates in the automatic drain valve. From there it passes to trays to evaporate. A pressure switch will de-energize a dump valve solenoid if the line pressure exceeds 80 PSI. This will direct the compressor output to the atmosphere until the pressure in the tank is reduced to 60 PSI by file operation or bleeding.

Each of the two compressors has a three position control switch in the sequence control box. With the switch set to OFF, the unit under control of that switch is inoperative.

When set to LOCAL, the compressor can be controlled with the start and stop buttons on the control box. On 8.40.04, the compressor motor is excited through the motor control switch and the three points of switch C1 to the line. C1 coil is energized from L2, through the thermal points; then, through the remote-local switch terminal 33 (8.40.03) to the start switch on 8.40.04. When the control switch is set to REMOTE the motor control is through time delay point 7 (8.40.03). This point closes after the timer motor has been started by a signal from the 305.

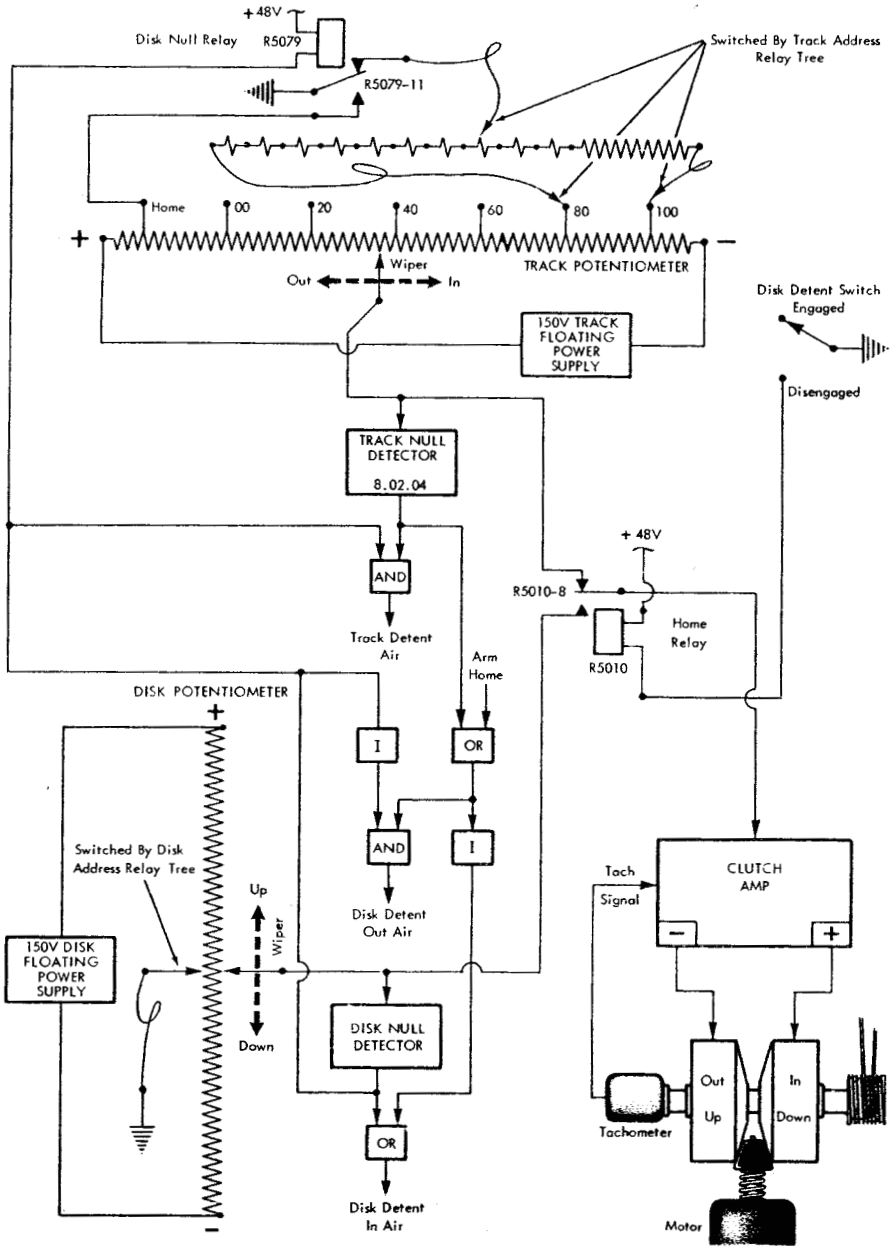


Figure 67. Logic of Access Servo System

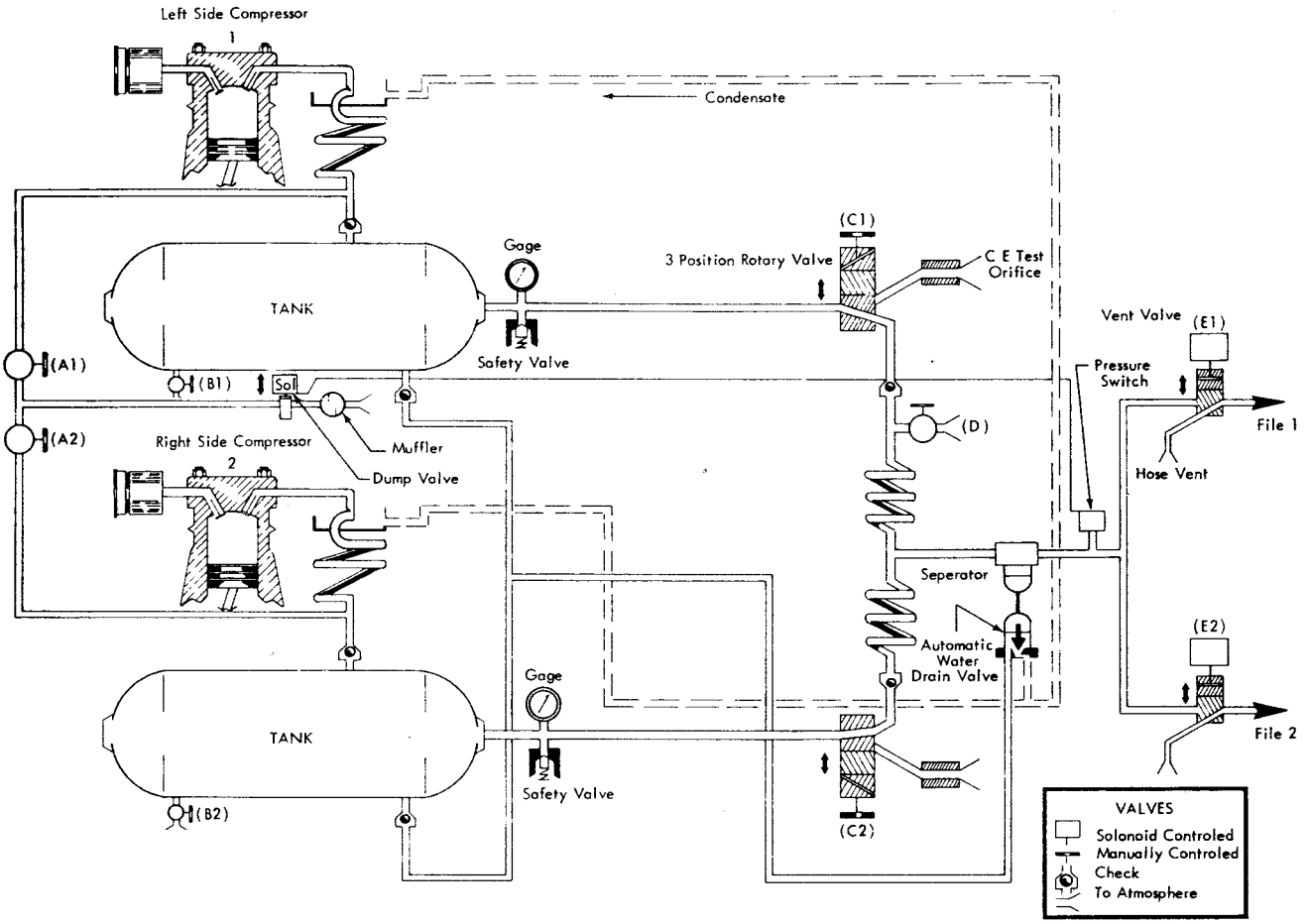


Figure 68. Remote Compressor

Basic File Servo Circuits

In order to follow the circuits involved in a complete $T_2 = J$ operation, it will first be necessary to consider the following basic servo circuits: safety circuits, null detectors, differential clutch amplifier.

Servo Safety Circuits

Great care has been taken in the design of the 350 circuits to protect the records that are stored in the file. A number of safety circuits must be properly conditioned before the file can be operated as a component of the RAMAC. Two safety relays are involved in these safety circuits, and both must be energized. These are the logic safety relay, and the bias safety relay.

Logic Safety Relay

The logic safety relay, R5116 (8.06.01), can be picked only by meeting the requirements of the interlock chain in series with the coil. Even if all of the interlocking conditions are fulfilled, R5116-2 N/O must be shunted in order to pick the relay initially. This shunt may be provided by either the safety reset switch (8.06.01), or by R160-1 (1.02.02). R160 is energized by the reset switch at the supervisory console (1.02.03).

If either reset switch is depressed, R5116 (8.06.01) will be energized, provided the following conditions exist:

1. The carriage is not at its extreme upper or lower limit of travel on the way. This permits the disk drive overtravel safety switches to be closed (8.06.01).

2. A number of critical relays must be in the machine. A normally open and a normally closed point of each of these relays are paralleled, so that any one may be either energized or not energized and still complete its portion of the interlock (8.06.01).

3. The pressure supplied by the air compressor must be greater than 45 PSI in order to close the air pressure switch (8.00.06).

Even though the logic safety relay is picked with the above conditions satisfied, the bias safety relay, R5007, must be picked to establish a hold circuit through the R5007-3 N/O points.

Bias Safety Relay

Figure 69 has the circuit for the pick of the bias safety relay, R5007 (8.06.02).

This relay is to be energized only if all of the following conditions and voltages are present:

1. Logic safety relay is energized.
2. +48v, +140v, −250v and −60v are present.
3. Regulated voltages −210v, +215v, +140v are present.
4. Pluggable unit B8b is present.
5. Track and disk ground fuses are intact.
6. Track and disk power fuses are intact.
7. Track and disk floating power supplies voltages are present.

Normally the left hand grid of the DE304 is at approximately ground potential causing the left hand section to conduct, picking R5007. If the disk or track ground fuses, the regulated 140v or regulated 215v power goes out, the left hand grid will be pulled down cutting this side of the tube off. If the −250v or regulated −210v were not present, the right hand grid would go plus, raising the common cathode potential and cutting off the left hand side again. The relay points of R5055 and R5056 in the plate circuit will be closed only if the two floating power supplies are operating correctly. The logic safety relay, R5116, must be up due to the fact that either the reset key or the safety reset key are depressed. R5116 has no hold until R5007 has been picked; therefore, the key must be held until 5007 picks.

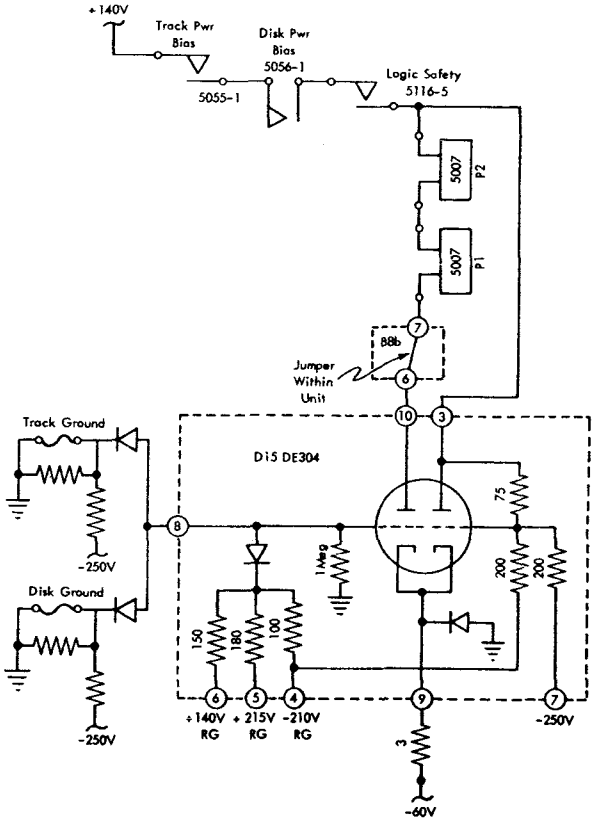


Figure 69. Bias Safety

Null Detectors

The disk and track null detectors are almost identical. We shall consider the disk null detector first, then the differences between the disk null detector and the track null detector.

Disk Null Detector

Figure 70 is a redrawing of the disk null detector (8.01.04) to include all the components within the pluggable units.

Servo logic requires that the disk null relay, R5079, be energized only when the carriage is located at the disk to which it is addressed. This relay is picked through the normally open points of MR3. MR3 is picked only when the disk wiper signal is within ½ volt of ground level.

The input to pin 4 of C10a must be high to allow this unit to draw current to energize MR3. This requires that both halves of A10 be cut off; that is, both grids must be about 10 volts negative with respect to their cathodes. As the left cathode and the right grid are both connected to ground, B11a must supply −10 volts from pin 6 and +10 volts from pin 3 to achieve a null. The circuit components are such that the required levels will be available if the input to D10 is within ½ volt of ground level.

If the input to D10 rises, the increased conduction through the left triode causes a lower level at the cathode of C11a. C11a draws more current to lower the grid of B11a. The input to the right cathode of A10 becomes negative, allowing current to flow through that triode, which lowers its plate output. C10a is thus blocked and MR3 is dropped.

A negative input to D10-5 causes the left triode to conduct less, raising the cathode of C11a. C11a draws less current to raise the grid of B11a, causing greater conduction. Pin 6 of B11a is thus raised, causing the left triode to A10 to conduct. This lowers the plate output of A10. As a result, C10a is blocked and MR3 is dropped.

The potentiometer in the cathode circuit of D10 controls the bias at the right grid. Since the voltage level of the common cathodes of D10 is determined by the total conduction of both triodes, the grid bias at the left triode is also controlled in part by the potentiometer adjustment. The sensitivity and balance of the disk null detector are therefore functions of this potentiometer adjustment.

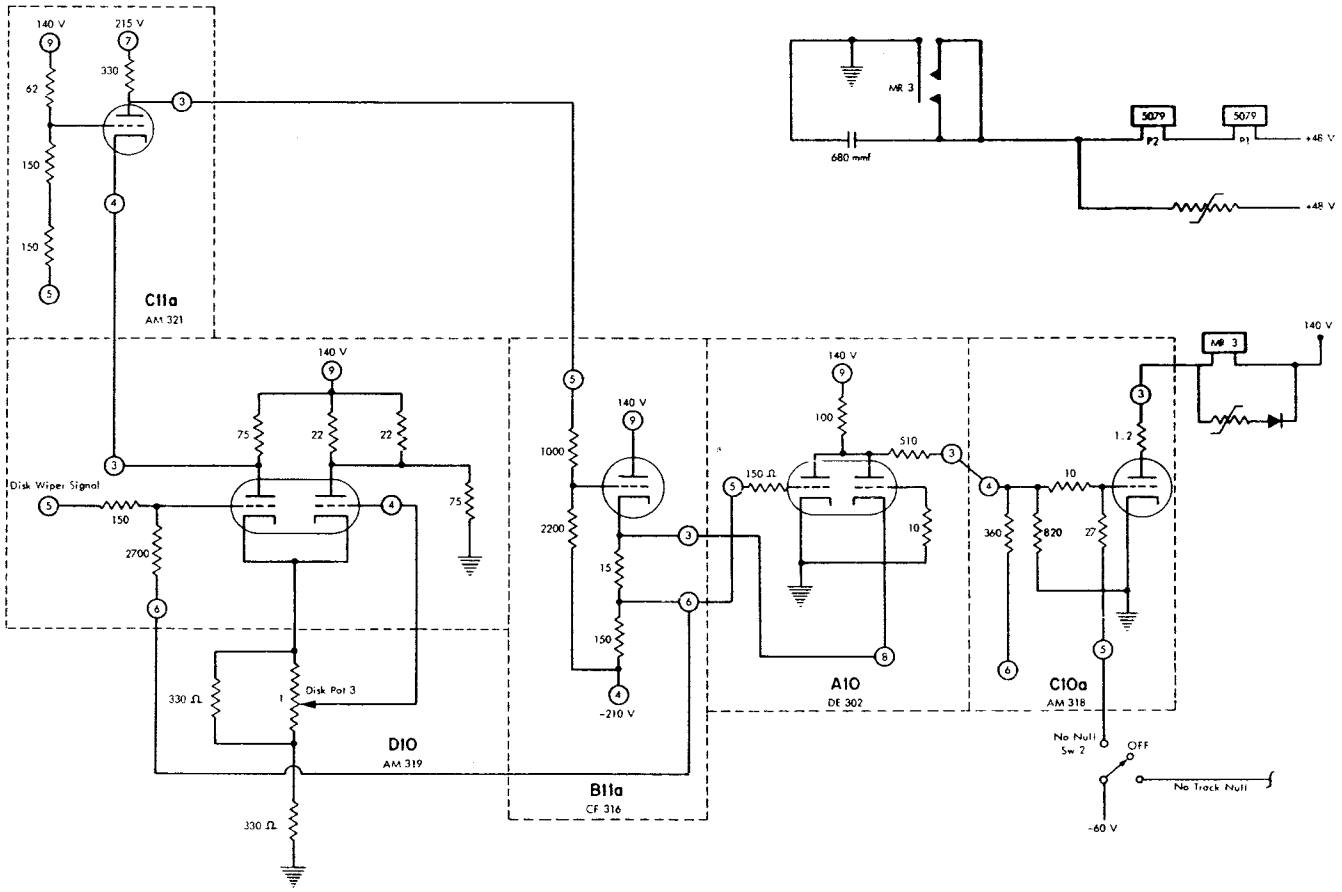


Figure 70. Disk Null Detector (8.01.04)

TRACK NULL DETECTOR

Servo logic requires that the track null relay (R5082 on 8.02.04) be energized only when the access arm is positioned at the track to which it is addressed, or when it is at home position if there is no disk null. R5082 is energized by the N/O points of MR2. With disk null relay (R5079) energized, MR2 is picked in a manner identical to the pick of MR3 by the disk null detector. This may be seen by comparing Figure 70 with Figure 78 (8.01.04 with 8.02.04). The operation of the track null detector when the arm is at the home position will be considered later.

Clutch Power Amplifier

Figure 71 shows the differential clutch amplifier (8.05.01) with the components of all the pluggable units drawn in. The input to pin 5 of A14 is taken from either the track or disk potentiometer wiper, depending on the status of the home relay (GR5010). The input to pin 8 is the tachometer signal.

If a positive signal is applied to pin 5 of A14, the in and down clutch will be energized, assuming that R5116 and R5035 are energized. The positive signal to A14-5 increases conduction through the upper triode. This raises the cathode level, causing less current to flow through the lower triode. Thus, the level of A14-3 becomes more negative while A14-10 becomes more positive. These two levels applied to B14 cause less current to flow through B13's upper triode, and more current through the lower triode. Thus, B14-3 becomes more positive while B14-10 becomes less positive. The inputs to pin 5 and 8 of C14 cause the output from pin 3 to rise and that from pin 10 to fall. The halves of the CD 308's which drive the out and up clutch are cut off, while greatly increased current is drawn through the in and down clutch.

Similar analysis will show that a negative wiper signal causes the out and up clutch to be energized.

As the clutch shaft gains speed, a signal is supplied from the tachometer to pin 8 of A14. This signal has the same polarity as the wiper signal applied to pin 5, but its maximum value is about 25 volts. As the wiper signal becomes less than the tachometer signal, the differential amplifier becomes unbalanced in the other direction. This causes the opposite clutch to be energized to provide dynamic braking.

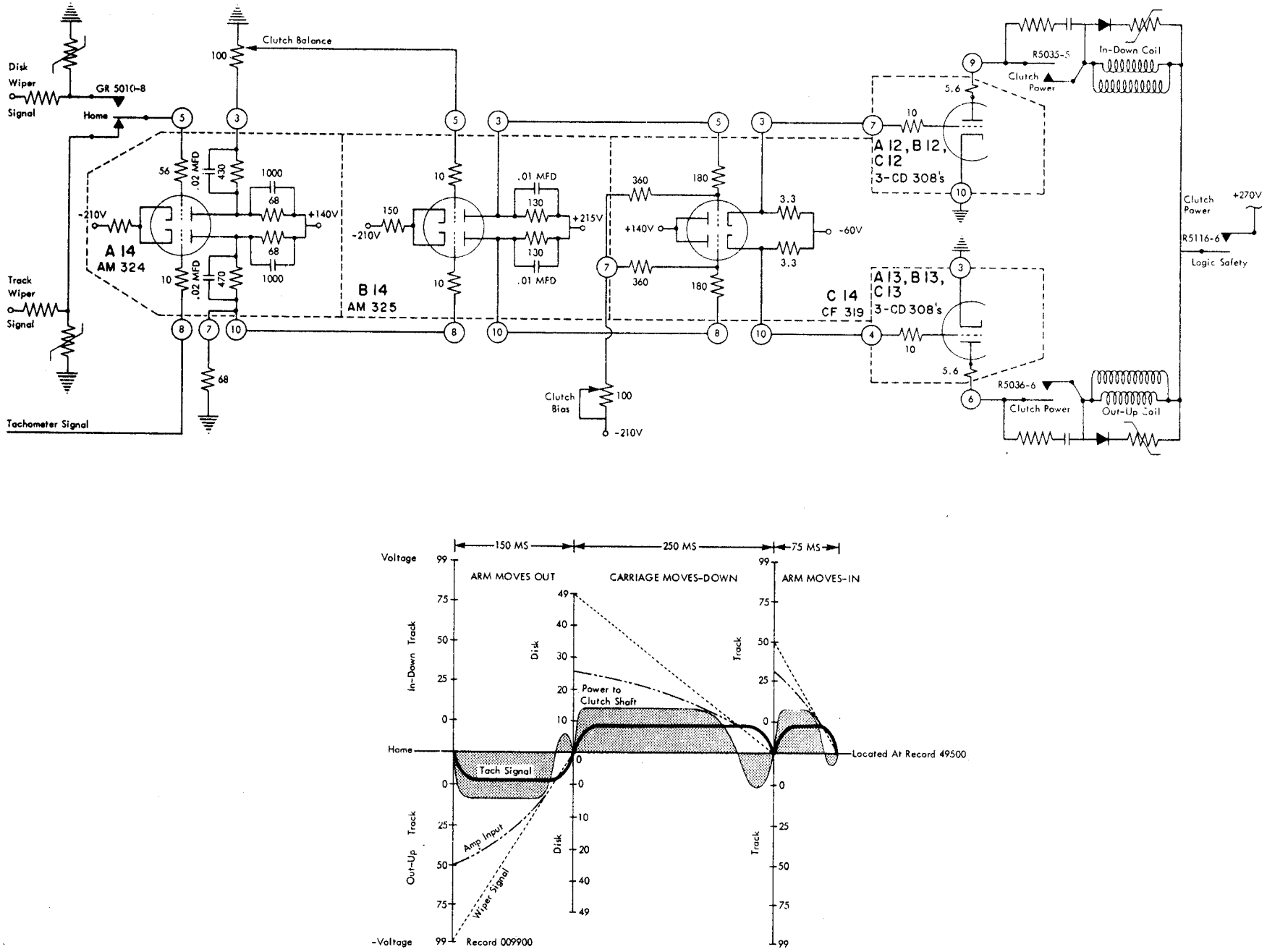


Figure 71. Clutch Power Amplifier (8.05.01, 8.05.02) with Theoretical Voltages and Waveforms

File Servo Circuit Operation

In order to facilitate the explanation of file circuits, we shall assume that a servo from address 01451 to address 49955 is being executed from the instruction W04J9905bb. Figure 72 is the data flow diagram.

OBJECTIVES:

1. Cause IRWDP cycle sequence.
2. Place new address in file address register relays.
3. Start mechanical servo operation.
   a. Retract air heads.
   b. Move arm out (track detent was released during R cycle).
   c. Retract disk detent, causing fail safe mechanism to lock arm all the way out.
   d. Move carriage down to new disk.
   e. Engage disk detent, causing fail safe mechanism to free arm.
   f. Move arm into new track.
   g. Engage track detent.
   h. Extend air heads.
4. Notify process unit servo is complete with track located gate.
5. Select addressed record for reading or writing.

IRWDP Sequence: The $T_2 = J$ line causes D cycle to follow W cycle. It also blocks I cycle ready trigger until P cycle end. On 2.01.06, $T_2 = J$ forces a program advance and a new program if P = blank. New program must be up to allow P cycle end to initiate an I cycle (1B2a – 1.03.04).

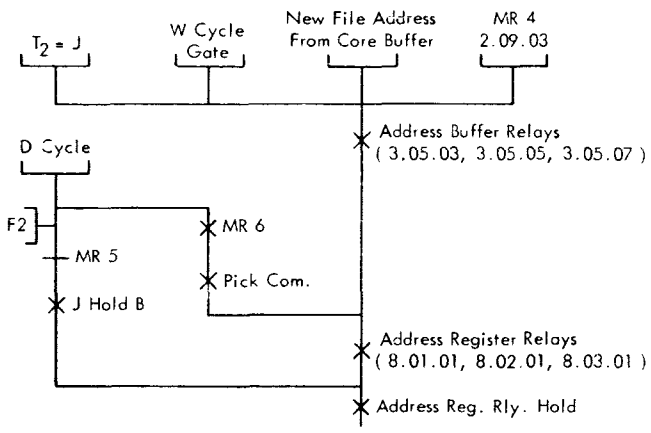


Figure 73. Pick and Hold Address Register Relays

Address Register Relays: The data flow chart for a servo operation (Figure 72) illustrates the path of the file address data. During R cycle the 5 specified characters are read into core buffer. On W cycle they are read out of cores as data to J and stored in the thyratron controlled address buffer relays. MR4 provides plate voltage for these thyratrons on a $T_2 = J$ operation. When MR6 makes, the address buffer relays are sampled to pick the address relays in the file. Just prior to reading the address out of cores, MR5 picks,

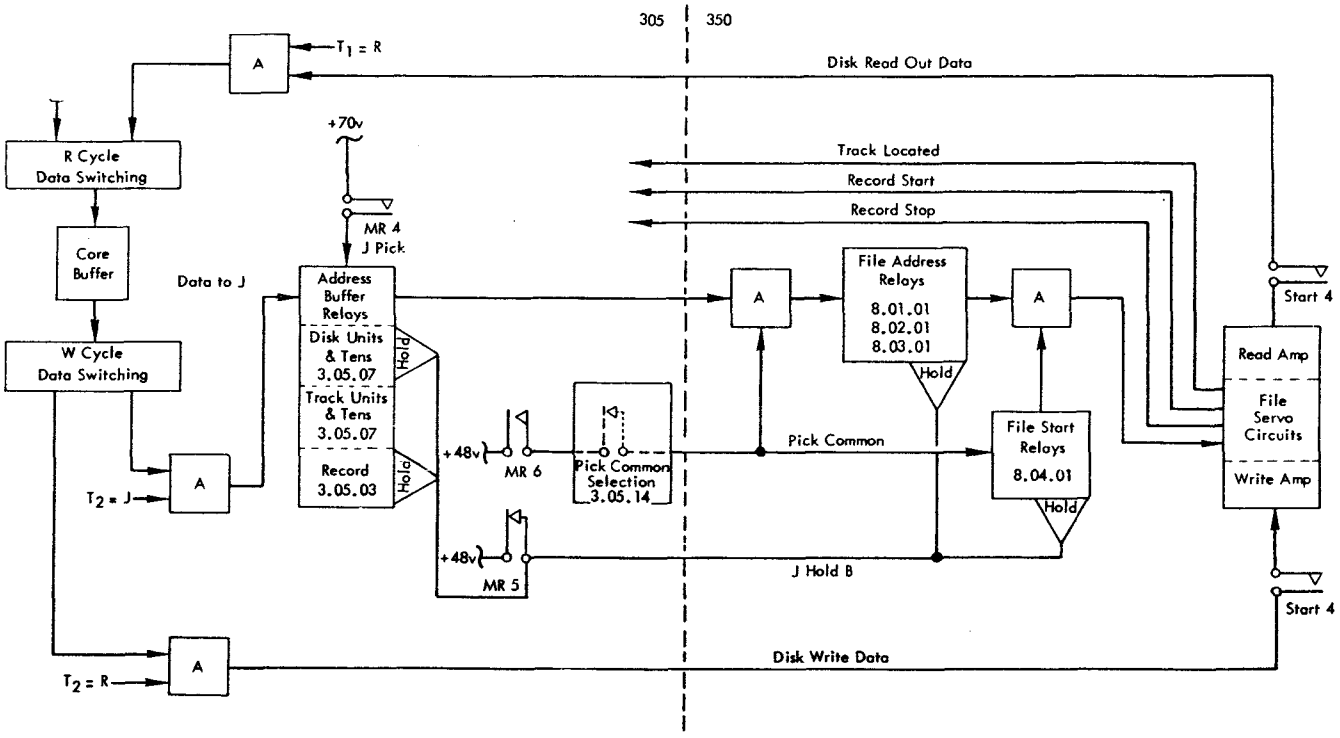


Figure 72. File Data Flow and Servo Control

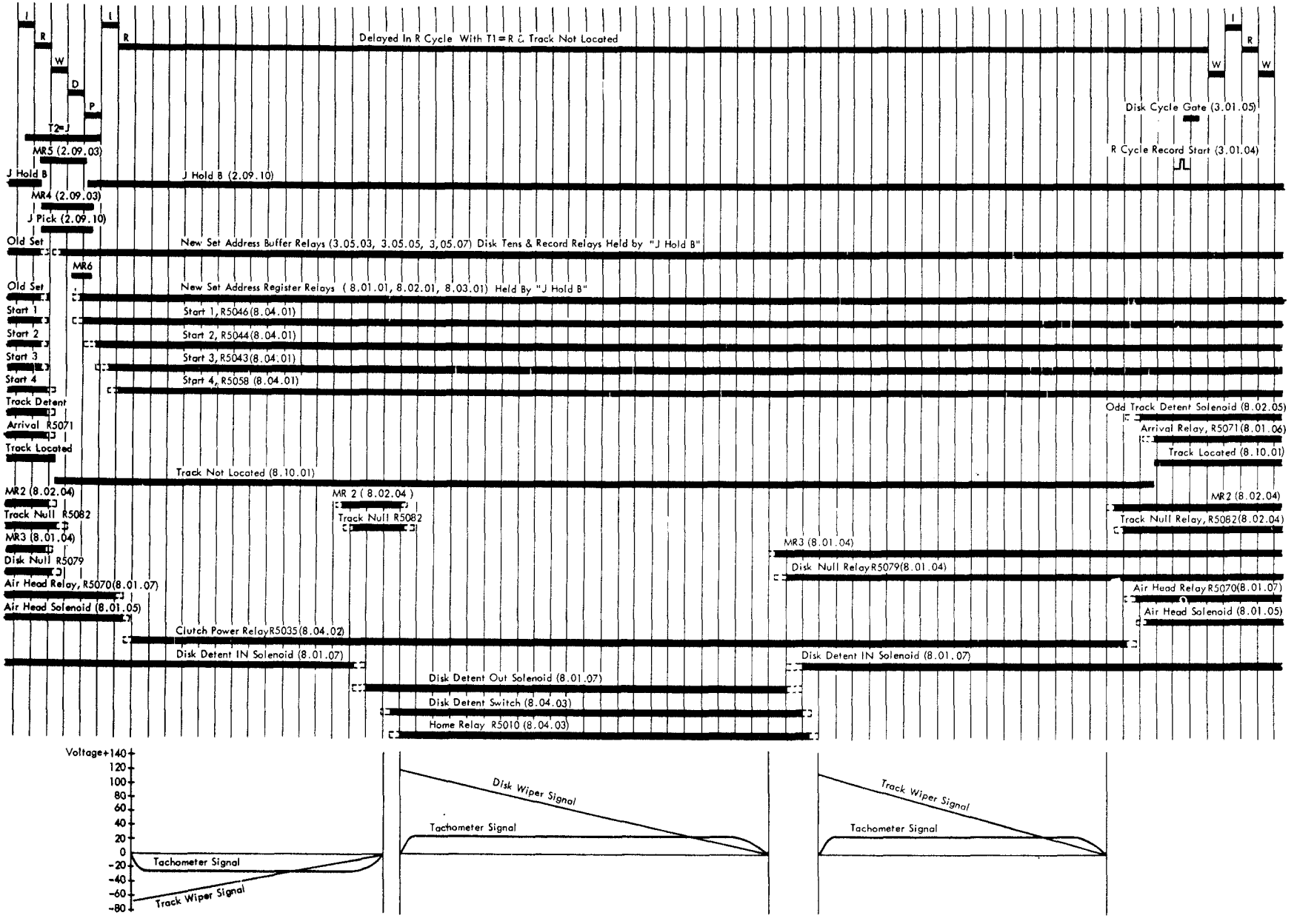


Figure 74. Sequence Chart of Servo Operation From Address 01451 to 49955 Followed by $T_1 = R$

dropping the hold on all file address relays, file start relays and some of the buffer relays. After the new relays have been picked MR5 will drop out establishing a hold until the next servo instruction. The only address buffer relays held are the record relays (for record advance purposes), and the disk tens relays (for dual file purposes).

The timings of these MR relays for a $T_2 = J$ operation are shown on System Diagram 0.09.05. MR5 will pick on 2.09.03 at the start of R cycle (3F3a), and drop out at F2 of second D cycle (same as D cycle). This lowers the J hold B line on 2.09.10, dropping the address buffer relays (3.05.03, 3.05.07). All file address relays (8.01.01, 8.02.01, 8.03.01) are dropped since their hold lines become J hold B on 3.05.11.

MR4 picks at the same time MR5 does on 2.09.03 but holds up longer, until D cycle end. This raises the J pick line on 2.09.10 to provide +70 volts to all the address buffer thyratrons (3.05.03, 3.05.05, 3.05.07). During W cycle the core data appears as data to J from C99 through C95 ($A_2B_2 = 99$ and $MN = 05$). On 3.05.01 this data is separated into 4 bit lines which feed the associated thyratrons of the address buffer relays. The units position of the core buffer appearing at C99 time is gated to the record address thyratrons (3.05.03). The next two characters, track units and track tens, are gated to the track address thyratrons (3.05.05). The disk address characters go to the disk address thyratrons (3.05.07).

To transfer the address from the process unit to the file address register, on 8.01.01, we must ground the proper pick line and place + 48v on the pick common line. The pick line grounding is accomplished on 3.05.12 and 3.05.3 by the points of the previously energized address buffer relays. The pick common line passes through 8.00.07 on one of eight common lines, depending upon the file configuration. For a single 5 million character file installation, pick common access 0/3 disk 00-49 would be used. This particular line is connected to +48v through MR6 N/O points (3.05.14). MR6 will be up during D cycle (2.09.03). The pick common selection circuits on 3.05.14 will be more fully explained under "350 Optional Features."

During D cycle MR5 dropped out, establishing a hold on all file address relays. The points of these relays have now set up new ground points on the disk potentiometer (8.01.03) through the relay tree on 8.01.02, and on the track potentiometer (8.02.03) through the relay tree on 8.02.02.

The following table will aid in tracing the pick circuits for the address 49955:

	Address Register Relay		Address Buffer Relay Point	
Disk 40	R5137	(8.01.01)	R355-5	(3.05.13)
Disk 8	R5121	(8.01.01)	R347-2	(3.05.12)
Disk 1	R5130	(8.01.01)	R342-2	(3.05.12)
Track 80	R5166	(8.02.01)	R339-2	(3.05.12)
Track 10	R5152	(8.02.01)	R335-2	(3.05.12)
Track 4	R5156	(8.02.01)	R330-2	(3.05.12)
Track 1	R5134	(8.02.01)	R327-2	(3.05.12)
Record 4	R5163	(8.03.01)	R308-3	(3.05.12)
Record 1	R5157	(8.03.01)	R305-3	(3.05.12)

Start Servo Operation

The initiation of the servo operation is controlled by the start relays on 8.04.01. These relays are picked and held along with the file address relays with MR6 and MR5 (de-energized) respectively. The start hold access line becomes J hold B on 3.05.11, while the pick common line goes to MR6.

Retract Air Heads: The air head solenoid on 8.01.05 is de-energized as soon as the head relay (R5070) drops. This is only necessary if the disk address has been changed, so on 8.01.07, R5070 is dropped only if the disk null points (5079-5) are open after the start relays repick. For our example, the disk null relay (R5079) on 8.01.04 will be down. A positive disk null signal is applied to the null detector from the disk potentiometer through the start relay points, G5046-7 N/O on 8.01.03. The disk wiper is located at disk 01 while the new ground point is at disk 49, through the address relay tree on 8.01.02.

While the start relays are de-energized, and the new address is being transferred to the file, the disk null relay was dropped by applying −60v to the null detector through G5046-7 N/C points on 8.01.03. The head relay (R5070) on 8.01.07 is held at this time by the normally closed start relay points.

Move Arm Out: To accomplish this objective the carriage must still be detented, the track detent must be released and the out-up clutch energized. The track

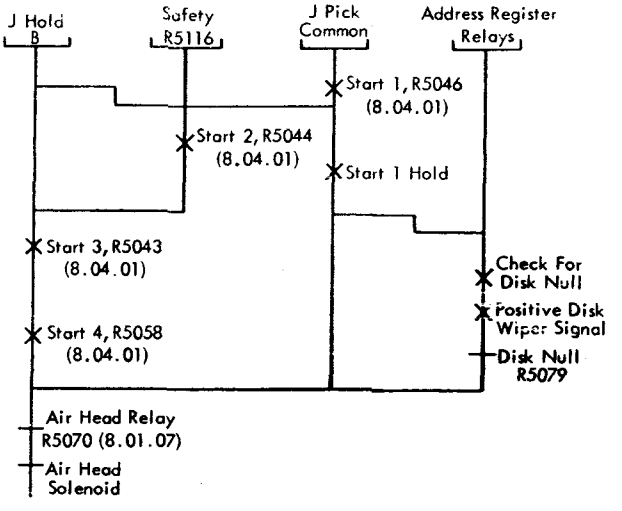


Figure 75. Retract Air Heads

detent solenoid (8.02.05) was de-energized when the start relay (R5046) dropped during R cycle. The disk detent in solenoid (8.01.07) is still energized through the home relays points (R5010-1 N/C) and track null points (R5082-2 N/C).

The out-up clutch is energized by applying a negative track signal (clutch) to the clutch amplifier on 8.05.01 and closing the clutch power relay points (R5035) on 8.05.02. The negative track signal from the track potentiometer on 8.02.03 is provided by grounding the home position. The de-energized disk null relay indicates the arm must be completely retracted to facilitate a shift to a new disk, so a disk null point (G5079-11 N/C) places ground potential at the track potentiometer plus end, beyond track address 00.

The clutch is actually energized when R5035 on 8.04.02 is picked. With no disk null (R5079 normal), R5035 picks when the air head begins retracting (R5070 normal) and the track detent is out. The CD cathode is grounded through the track detent switch on 8.01.06. If the read/write heads are already near the edge of the disk due to a previous track address of less than 20, we must delay arm movement until the air heads are fully retracted. In this case the clutch delay relay (R5006) will be energized and holding. The R5006-1 N/O points place a negatively charged capacitor on the grid of the CD, which must discharge through the R5070-4 N/C points before the clutch power relay is picked.

Retract Disk Detent: When the arm is fully retracted, a track null is developed. The track null points (R5082-4 N/O on 8.01.07) close to energize the disk detent out solenoid. At the same time the disk detent in solenoid is de-energized with the opening of R5082-2 N/C. When the disk detent is disengaged the home relay (R5010) on 8.04.03 will be energized.

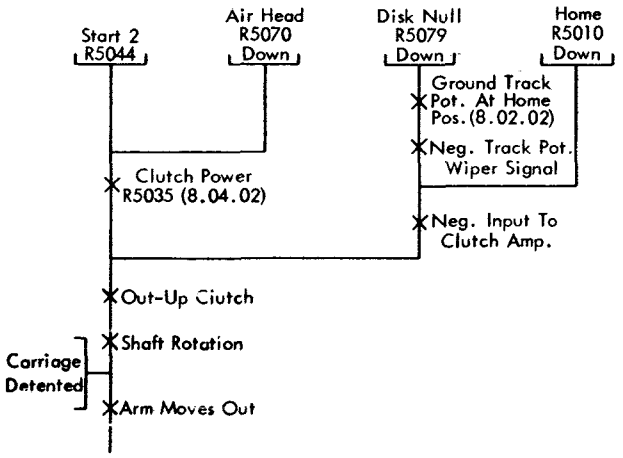


Figure 76. Move Arm Out

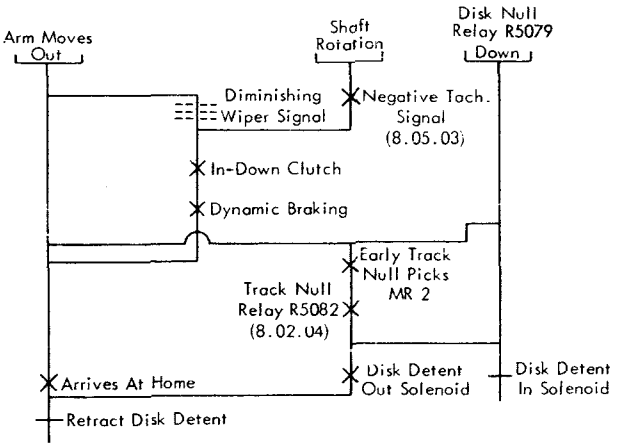


Figure 77. Retract Disk Detent

In order to save time when transferring from track drive to disk drive the track null circuits are designed to pick MR2 early (8.02.04) when moving to the home position. Figure 78 shows the disk null points in the grid circuit of the left hand section of A11b. When R5079-8 is normal the grid is tied to a more negative point on the cathode resistors of B11b. This cuts off the right hand section of A11a before the track signal actually reaches zero volts.

Move the Carriage Down: The fail-safe mechanism locked the arm in the home position when the disk detent was retracted. Energizing the in-down clutch on 8.05.02 will move the carriage down until a disk null is detected. A positive disk signal (clutch) is applied to the clutch power amplifier on 8.05.01 through the transferred home relay points (G5010-8). In our example the carriage is at location 01 (8.01.03) while the disk potentiometer is grounded at location 49 through the address relay points on 8.01.02.

Engage Disk Detent: When the disk null is detected the disk detent in solenoid is energized through the R5079-4 N/O points.

Move the Arm In: Energizing the in-down clutch will now move the arm in until a track null is detected at the addressed track. A positive track signal can be applied to the clutch power amplifier (8.05.01) when the home relay (G5010) drops. This occurs as soon as the disk detent is engaged on 8.04.03.

The track potentiometer (8.02.03) will be grounded at position 95 by placing the 10 one ohm resistors and then the ten ohm resistor on 8.02.02 in parallel with the markite strip from position 100 to position 80. This is done through the following N/O points on 8.02.02: from position 100, G5166-5 N/O, G5152-7 N/O, the ten one ohm resistors, G5152-6 N/O, the 10 ohm resistor, G5152-8 N/O, G5166-6 N/O to position 80. The fifth one ohm resistor down will be grounded through the units track address relay points.

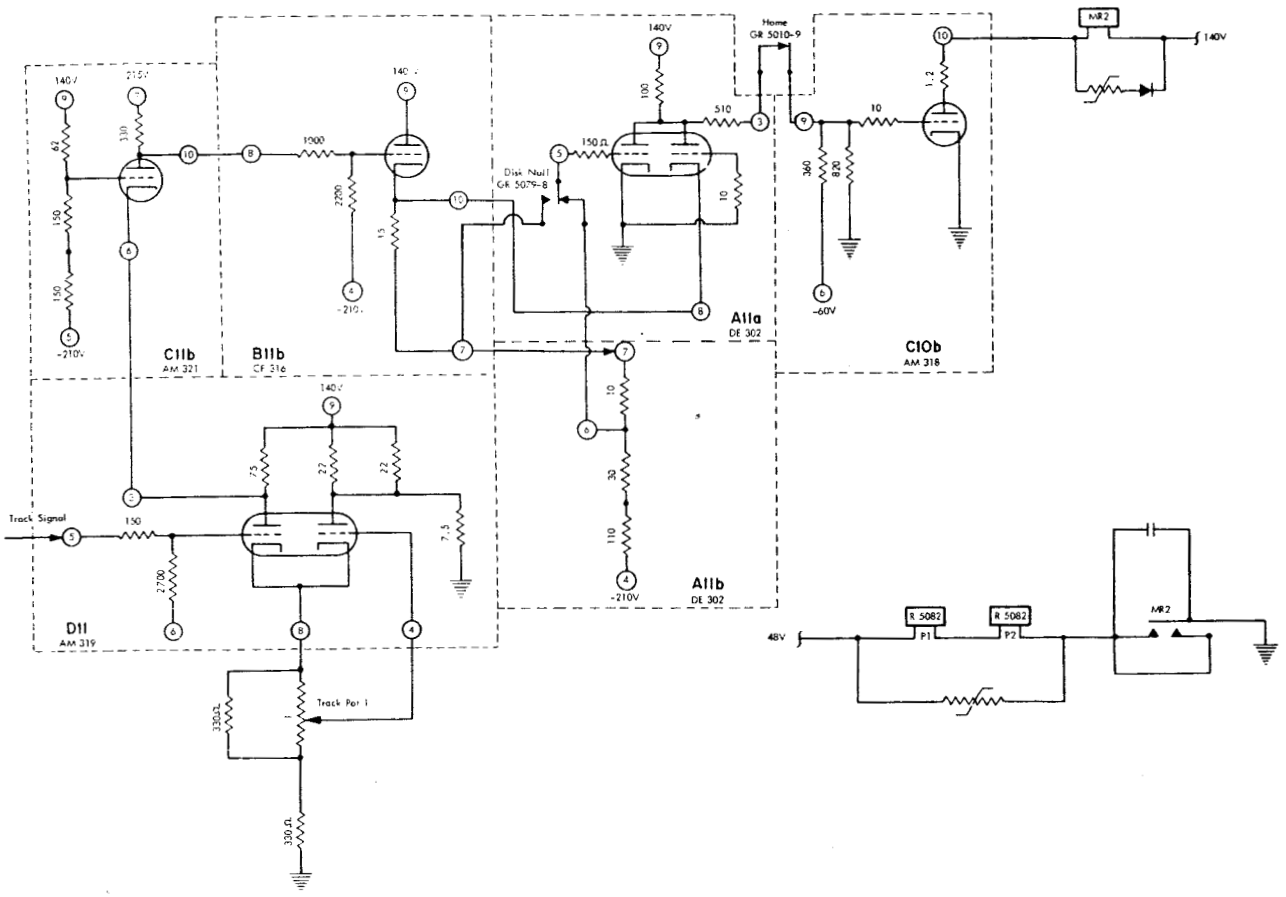


Figure 78. Track Null Detector (8.02.04)

The full application of the postive track signal (clutch) to the power amplifier on 8.05.01 will be delayed following a carriage movement until the carriage settles down. Accerelator limiter points, R5004-1 N/C and R5005-1 N/C will open, sequentially, after the carraige reaches the addressed disk. On 8.04.03, R5004 picks when the disk detent switch transfers and R5005 picks shortly later when the 10 μfd condenser has charged.

Engage Odd Track Detent: When the wiper on the track potentiometer reaches the addressed position, the track signal decreases to zero volts. This picks the track null relay (R5082) on 8.02.04 which will energize the odd track detent solenoid on 8.02.05.

Extend the Air Heads: The air head relay (R5070) on 8.01.07 is picked through the track null relay points, R5082-2 N/O. This energizes the air head solenoid on 8.01.05.

Track Located Signal: This signal, developed on 8.10.01 by the closing of the arrival relay points (R5071-2 N/O), informs the 305 process- unit that the servo is complete. The arrival relay on 8.01.06 picks as soon as the track detent switch transfers if a track null exists and the air head relay is picked.

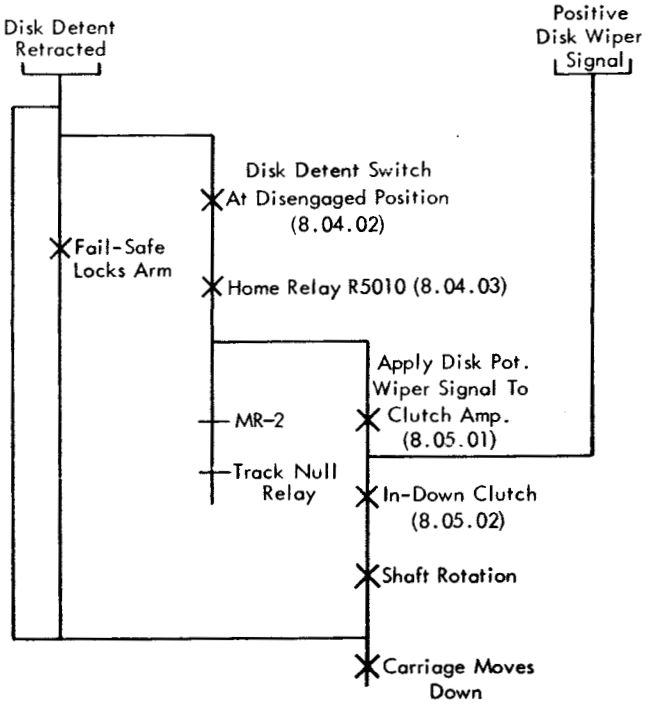


Figure 79. Move Carriage Down

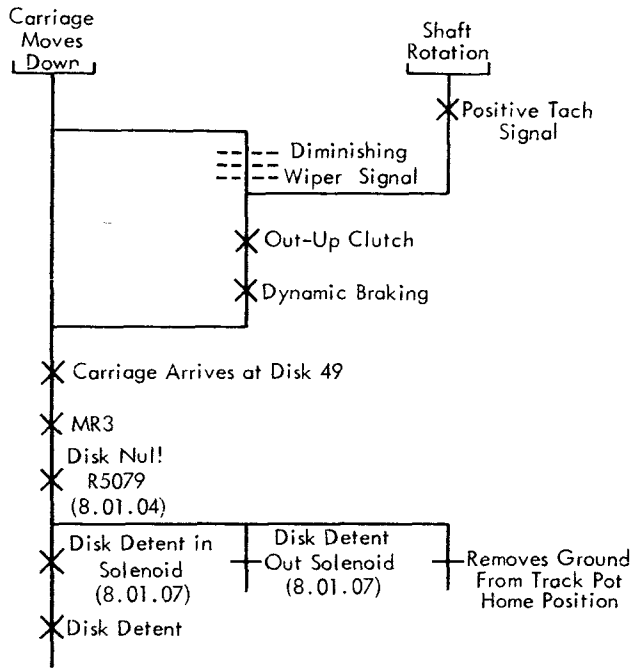


Figure 80. Engage Disk Detent at Disk 49

Record Selection: The record address relay points are used to select the correct record head through the network on 8.03.02. In our example, address 49955, record address relays 1 and 4 provide a record start pulse from the 0/5 head and a record stop pulse from the 1/6 record head. These pulses will tell the process unit when to start reading or writing record 5.

The bottom head on the access arm will be selected by energizing the side relay (MR1) on 8.10.03.

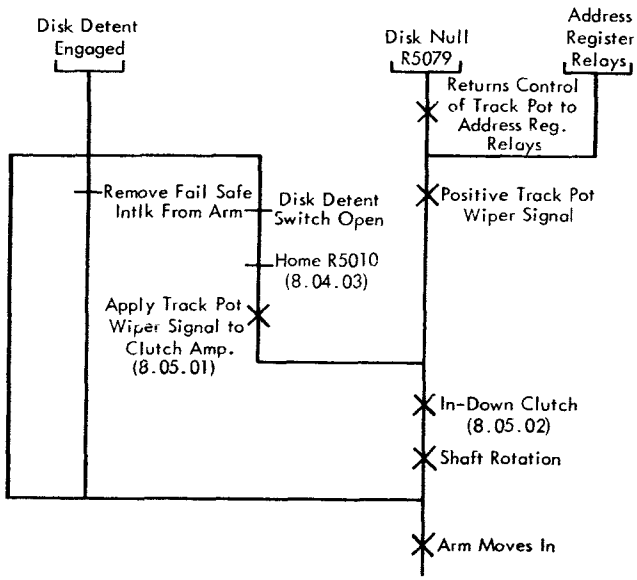


Figure 81. Move Arm In

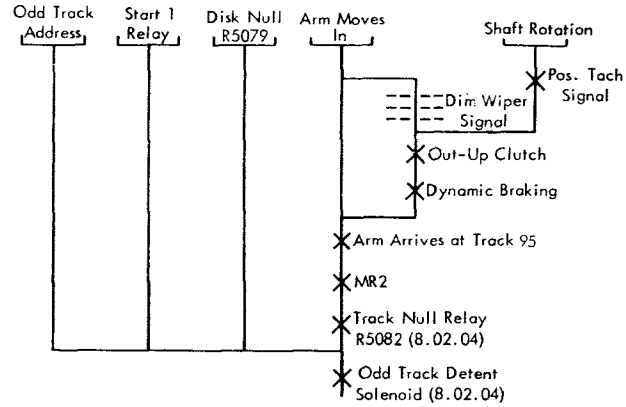


Figure 82. Engage Odd Track Detent at Track 95

Figure 74 is a sequence chart of the entire servo operation.

Customer Engineering Track Selection

One of the two customer engineering tracks (inner or outer) on an addressed disk is selected automatically when the test lock switch is ON and $T_2 = J$ operation is initiated. If the record address is an odd number, the outer track is selected. If the record address is even, the inner track is selected.

The test run relay, GR5119 (8.11.01) is energized when the test lock switch is ON (6.15.04). With GR5119 energized in addition to GR5079, control of the track address is exercised by GR5134-12 (8.02.02). The entry of an even track address will leave GR5134 down, and will apply ground to the 100 (inner CE track) tap of the track pot. The entry of an odd track address will cause GR5134 to be picked, and will apply ground to terminal "B", which is a point on a voltage divider connected between the 00 tap and the positive input to the track potentiometer. This will establish ground level at a point one track from the track 00 position.

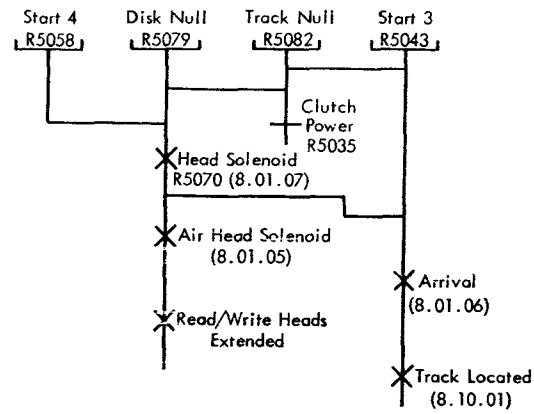


Figure 83. Extend Air Heads; Obtain Track Located Signal

File Read/Write

Basic Circuits

The method used to record information on the RAMAC file differs from that used on the process drum. On the drum one polarity of flux indicates a bit while the opposite polarity indicates no bit. On the disk an NRZI (non return zero IBM) system is used where a change in flux represents a bit while no change represents no bit (see Figure 86). One additional difference is the fact that all space bits (Bs) are inserted and written for each character. This is done only to stabilize the file read circuits.

The physical arrangement of the read/write coil and the erase coil are shown in Figure 81. The coil wiring is shown on System Diagram 8.10.02. Notice that the read/write coil is centertapped with the erase coil feeding the tap. One of the two heads (top or bottom) will always be selected by the points of the side relay, MR1. This is picked by analysis of the units position in the file address relays (8.10.03). When writing on the disk, the write relay 5057 will be energized and the arrival relay 5071 will be up. Electrons will flow from the head ground through the top head erase coil (assume MR1 is normal). At this point it will flow through either half of the read/write head, depending on which write amplifier (A or B) is conducting. One of the two will always be conducting during a file write operation and a bit of information coming in will cause the other to conduct. The resultant flux pattern laid down on the disk will change polarity only when a bit of information is written.

WRITE AMPLIFIER (8.10.05)

A detailed drawing of the write amplifier is shown in Figure 84. The three CD308's will conduct on either the left or the right side to pass write current one way or the other through the read/write head. The condition of trigger D8, determines which half of these CD's conducts. The two outputs of the trigger feed two inverters at B8a, and the output of the inverters goes to the grids of the CD308's.

The start 1 relay R5058 will be energized any time the arm is not in a servo operation. When a file write operation takes place the disk write data line will have ∅C data pulses from the core buffer, plus inserted Bs ∅C pulses on it. These pulses are inverted and

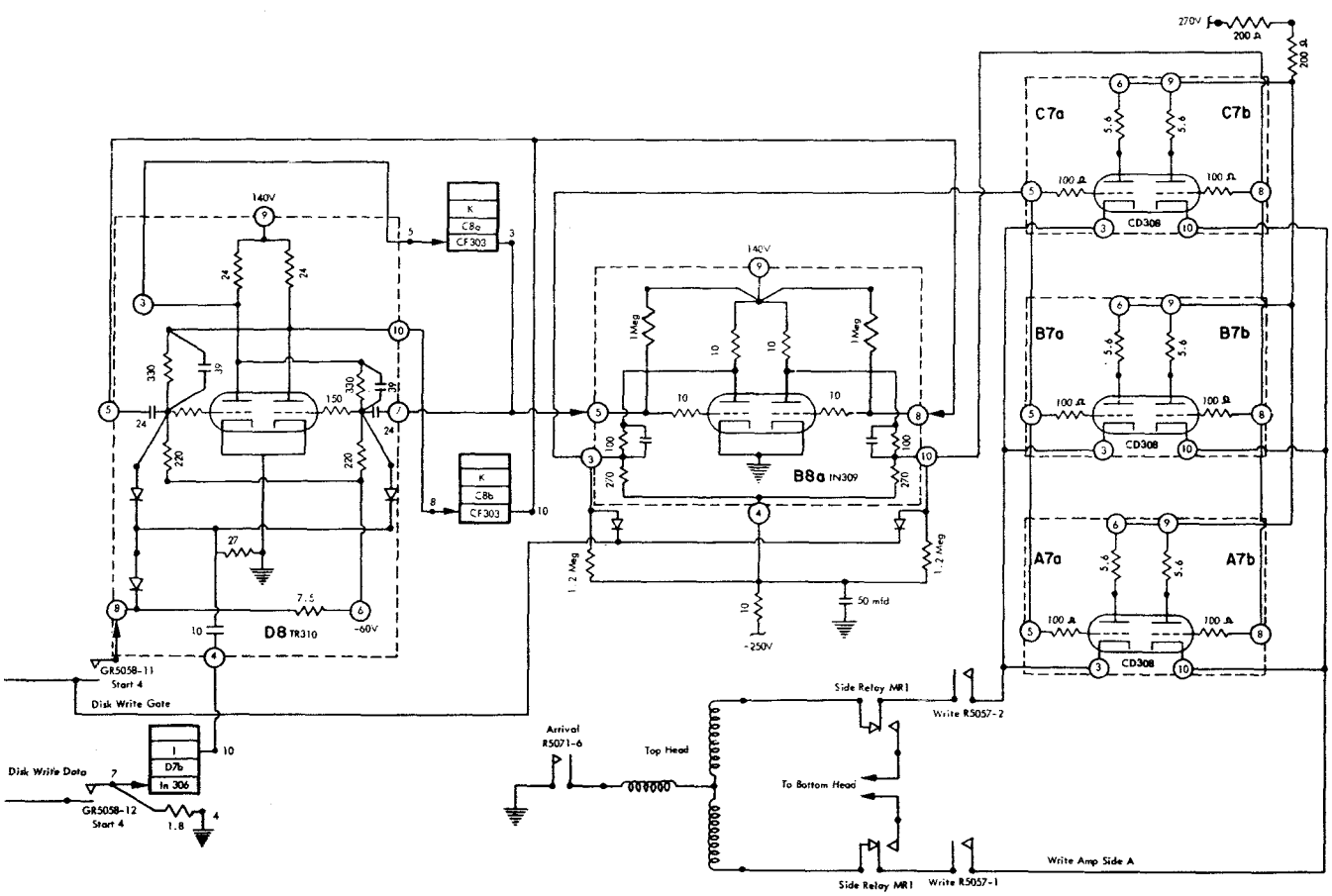


Figure 84. Write Amplifier (8.10.05)

fed to the trigger D8 through a binary input, each one flipping the trigger to the opposite condition. The CD308's will follow the trigger, one side conducting with the other side cut off, until the trigger changes its status.

Because the writing of the data must occur at a specific time in the revolution of the disk, there must be some way to prevent either side of the CD308's from conducting until ready. The disk write gate will be low until the desired sector on the disk is reached. This low on pin 8 of the TR310 keeps both halves of the trigger cut-off. The two outputs will be high and are inverted to lows on all grids of the CD308's. So we can say the disk write gate determines the starting and stopping time of current flow through the read/write head.

The erase coil, with current always flowing through it in the same direction, is necessary to eliminate any peripheral flux from the previous record. The width of its field is greater than that of the read/write head.

Read Amplifier (8.10.04)

Once the data has been stored on the disk in the form of flux reversals, the read/write head can be used to read these changes. The read amplifier is shown in Figure 85. When a change in flux passes the head, a small current will flow through the head coil. This places a pulse of one polarity on one grid of the AM306 (D4), and a pulse of the opposite polarity on the other grid. This 2 phase signal will be amplified through the four stage differential amplifier. One advantage of the push-pull amplifier is the elimination of noise picked up in the head leads. These noise pulses will generally appear on only one input to the amplifier and the degenerative feedback between the two halves of the amplifier will eliminate them.

The outputs of the amplifier A4, will have alternate positive and negative pulses representing data. The plus pulses from first one output and then the other are combined at the OR cathode follower A5, then shaped at the Schmitt trigger C5 to provide disk read out pulses.

Automatic Gain Control

Because of the difference in surface speed between the inside and the outside of the disk, signals from the inside track will vary from 11 to 14 millivolts while signals from an outside track will vary from 26

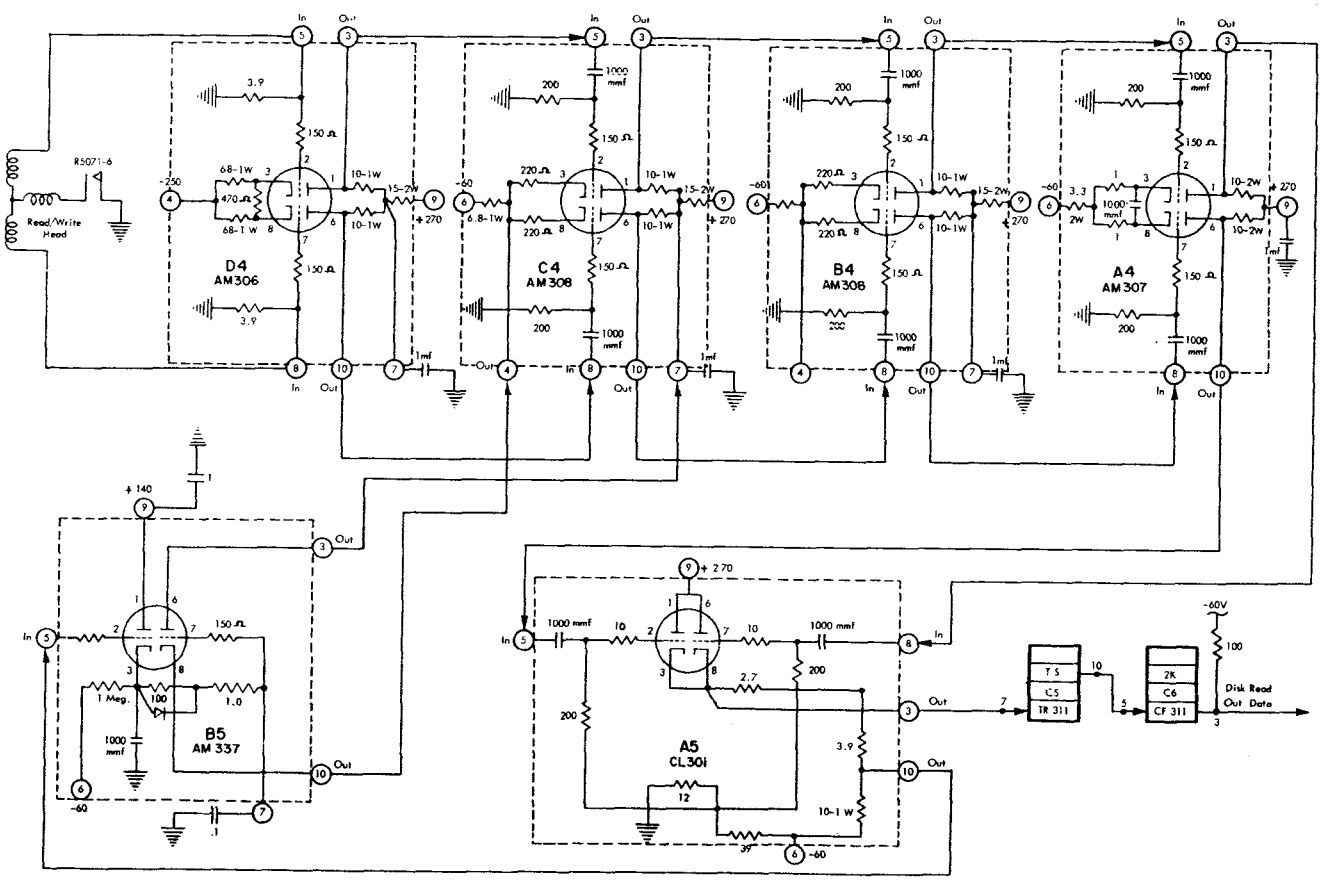


Figure 85. Read Amplifier (8.10.04)

to 40 millivolts. The read amplifier must be able to accommodate signals between these extremes. To accomplish this an automatic gain control circuit (B5-8.10.04) samples the output pulses and varies the amplification of the second stage at C4, accordingly. For example, if the output signals increase in strength it would be desirable to reduce the amplification of C4. This can be done by lowering the plate voltage and raising the cathode voltage. The signals are sampled at pin 10 of A5 and cause the left hand section of B5 to conduct more heavily, increasing the charge on the .1 μf capacitor between pin 7 and ground. This raises the voltage on pin 7 causing the right hand section of B5 to conduct more heavily. This in turn raises pin 10 and lowers pin 3, which has the desired effect on C4.

Prior to dual access and double density files, the first few bits of the record were (when reading) used to set the level of amplification. To prevent any possible distortion of the first few bits, a series of ∅C AGC pulses are now written ahead of the data portion of each record. These pulses are written each time the record is altered and are used when reading to establish the charge level of the .1 μf capacitor.

Disk Clock

The only pulses generated by the file itself are the five record start pulses for each revolution. These are developed by a permanent magnet, fixed to the top dummy disk,as it passes each of the five equally spaced record start heads fixed to the file housing (8.03.04).

The record start heads are numbered 0 to 4, or 5 to 9, depending upon whether the top read/write head or the bottom read/write head on the access arm is selected. Since the disk is revolving at 1200 RPM, a start pulse occurs every 10 milliseconds. These pulses tell the 350 file when to start writing (or reading) a record and when the record should have been finished.

Between two start impulses 100 characters must be written or read (with a gap before and after). This requires a clock to control the character rate and to identify each character and bit (or no bit). A clock track written on the disks would not be feasible because of the inability to predict the exact position of the read/write head from one servo to the next. On the drum, the heads are permanently fixed but not so in the file. For this reason the disk clock must be generated by an external oscillator during a write operation. On a read operation the data being read will control the clock.

When writing on the disk the spacing of the data bits is determined by the speed of advancement of the core buffer bit ring. On a track to track transfer, the core bit ring was driven by ∅A pulses from the process drum clock. On 3.02.02 it can be seen that the ∅A pulses to the cores come from the disk clock instead of the process drum clock when T = R (file read or write). These disk clock pulses are developed on 3.01.02 from three single shots. The rise of the disk clock, a square wave signal of approximately 12 μs in duration, triggers the ∅A single shot. The fall of the 2¼ μs ∅A pulse initiates the 2¼ μs ∅B pulse. The ∅C single shot will be triggered by the fall of ∅B or the fall of the disk clock, whichever occurs later.

The disk clock square wave is generated by an oscillator on 3.01.01. When writing into the file, one oscillator (consisting of pluggable units 2D6 and 2F6a) determines the frequency of the clock. It is adjusted to step through 100 characters plus a 1200 μs gap during the interval between two consecutive record starts. Because the records stored on the file must be retained permanently while the speed of the disks and the oscillator frequency may vary, some method is required to keep the disk clock frequency synchronized with the rate of the data bits being read from the file. To accomplish this there are two oscillators used when reading. The bits on the disk read out line switch one oscillator, then the other, to the disk clock line. This can be seen in Figure 82. Notice that when the oscillators are switched, the active oscillator always begins its sine wave at the midpoint and proceeds to the lower half of the oscillation. Raising pin 5 of the CF302 portion of the oscillator to ground level prevents it from oscillating.

When writing, the oscillator at 2D6 and 2F6a will conduct continuously in the following manner. Pin 5 of 2F6a drops below ground level because 2D7a is not conducting. This is due to the high at pin 10 of the clock switching trigger 2E7, which will be held 10 pin high. At the same time the low at pin 3 of this trigger is inverted, causing conduction at 2D7b, blocking the second oscillator at 2F6b. The clock switching trigger is held 10 pin high by raising the write clamp line (access 0/3).

When reading from the file the write clamp line will be down. The disk read out data pulses are inverted and binarilly fed to the trigger at 2E7, alternately switching it ON and then OFF. This alternates the oscillators through the two AK's, 2D7a and 2D7b. During both reading and writing the clock control trigger at 2B6 is 10 pin high and has no effect on the oscillator operation. When it is desirable to stop both oscillators, this trigger is turned 10 pin low by a negative shift on the clock set line. This causes both AK units to conduct, stopping the oscillators.

Figure 86 illustrates the operation of the oscillators, the clock and the phase generating circuits for reading and writing. To assure that the oscillators will switch

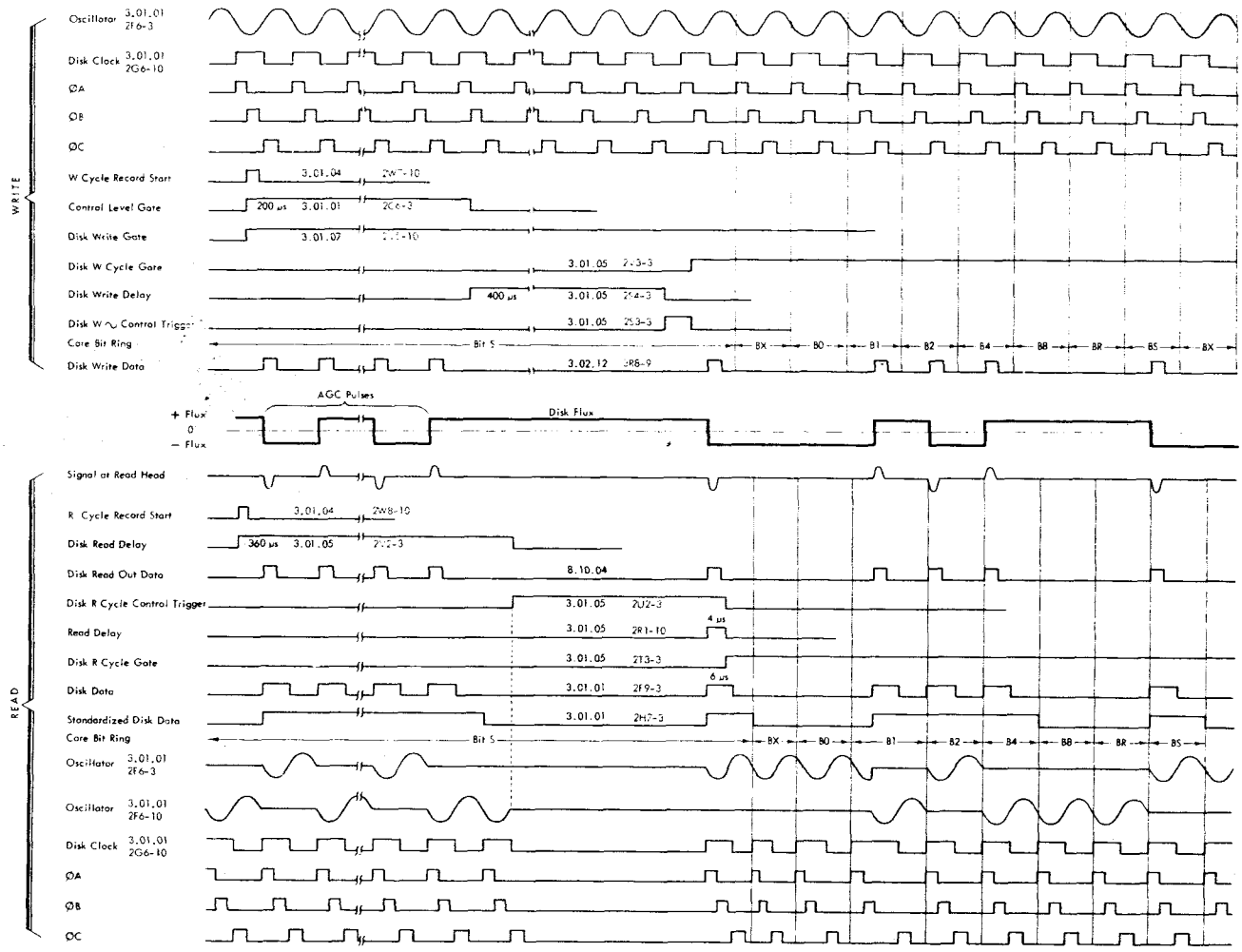


Figure 86. File Write and Read Waveforms

at least twice every character, the space bits are inserted. Notice in the diagram that one oscillator is tending to speed up on the read operation. This increases the duration of the B1 clock cycle. The ØA and ØB pulses have been advanced; however ØC, which is initiated by the fall of the clock pulses, is still in time with the disk data out. This is important since ØC's are used later on to sample the disk data.

File Write Operation ($T_2 = R$)

Two data flow charts in Figure 88 and a sequence chart Figure 87 are provided to supplement the write-up. The file write operation, for example X99R9900bb, can begin when the track has been located. This instruction will transfer X track (100 characters) to core buffer on R cycle. On W cycle the data in the core buffer is transferred to the file location specified by the address relays. As a check, a second RW cycle will follow the first W cycle. On the second W cycle the data just written will be read from the file and compared, character by character, to the data from X track which is placed in cores during the second R cycle. Any variation in the two records will stop the machine.

OBJECTIVES:

1. $T_2 = R$ causes an IRWRW sequence.
   a. Pick up the write relay R5057.
   b. Store check trigger differentiates first Wcycle from second.
2. During first W cycle data flows from core buffer to addressed record position in the file.
   a. Record start.
   b. Write AGC pulses (ØC) for 200 µs.
   c. Write core character 00, 600 µs after record start.
   d. Insert Bs for each character.
   e. The disk clock controls core ring advance and core starts.
   f. Stop file write after core character 99 is written.
   g. Check file speed and write speed.

3. On second R cycle re-read selected drum track into cores.
4. On second W cycle data flows from file record just written to comparing circuits and data from cores flows to comparing circuits.
   a. Record start.
   b. Block AGC pulses from data line.
   c. Develop standard disk data, ØA to ØA, to compare circuits.
   d. Disk clock advances cores and reads out of cores to compare circuits.
   e. Stop machine and turn on file check light if a comparing error occurs.
   f. Stop file read after core character 99 is compared.

IRWRW Cycle Sequence: A T_2 character of R will command the machine to begin a file write operation by picking R5057 on 8.10.01. This relay is energized by firing the thyratron (3A11) on 3.01.06 with I cycle end and $T_2 = R$. Notice that the file hubs on the 305 control panel must be jackplugged. The relay will remain energized until the thyratron is cut-off by firing a second thyratron at 3B11. This occurs at the end of the first W cycle.

The store check trigger (2T4) on 3.01.05 controls the special cycle sequence for $T_2 = R$. It also identifies the first W cycle and the second. Every I cycle it is turned ten pin high. The trigger remains ten pin high until the fall of the disk write delay (2S4). This occurs just prior to writing the record on the first W cycle. It will then remain 3 pin high throughout W cycle, the second R cycle and into the second W cycle. Then it is turned ten pin high by the fall of the disk read delay, 2V2, just prior to reading the record for comparing. The read delay is initiated by W cycle record start and store check switching at "and" inverter 2S5a. This can be seen in Figure 87.

On 1.03.05, R cycle ready trigger will be turned ON with W cycle end and store check for the second RW cycle. Both I and D cycle will be blocked at this time.

First W Cycle: The data flow during this cycle is shown on Figure 88. The core buffer contains 100

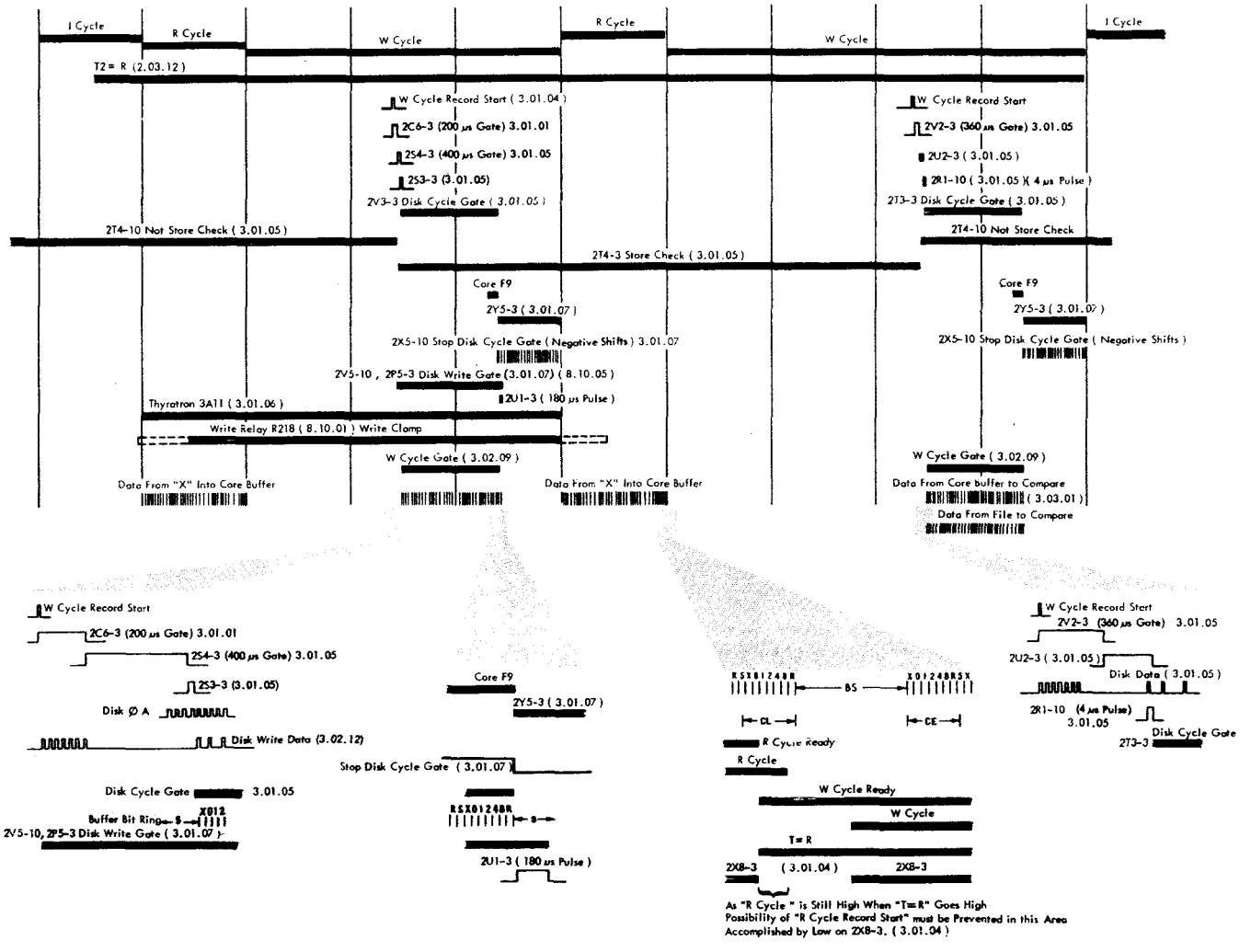
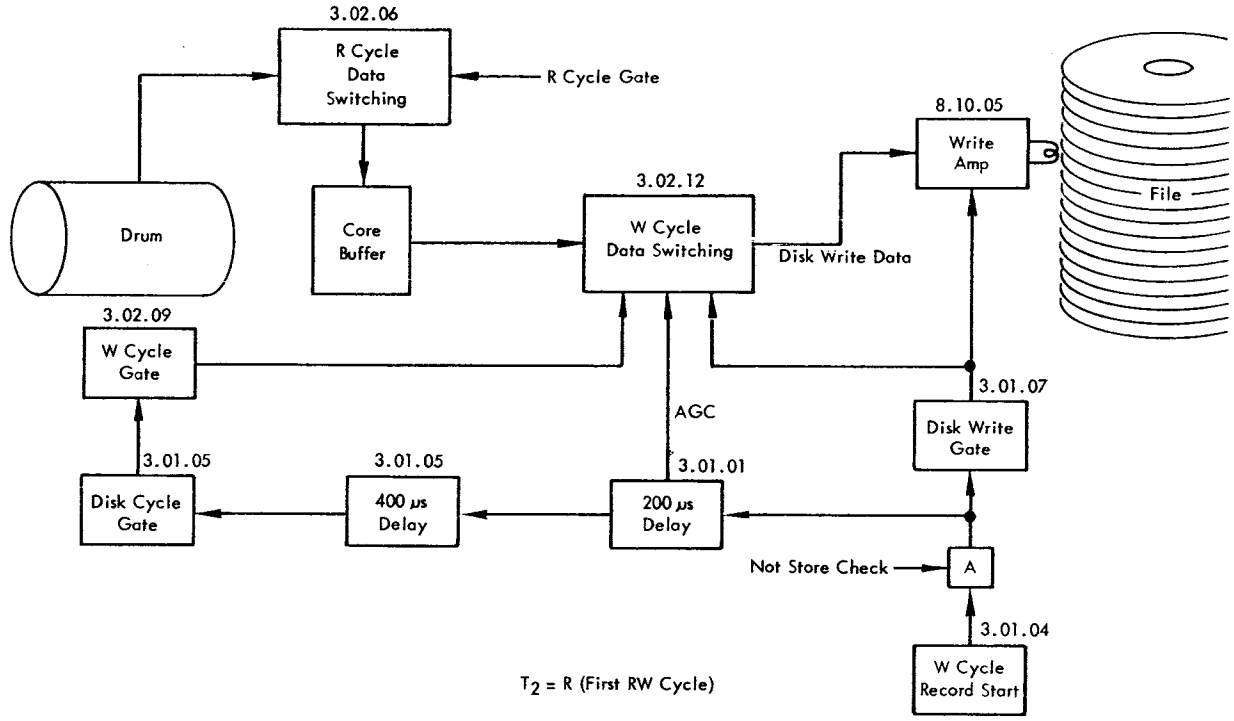


Figure 87. Store Data into File (X99R9900bb)



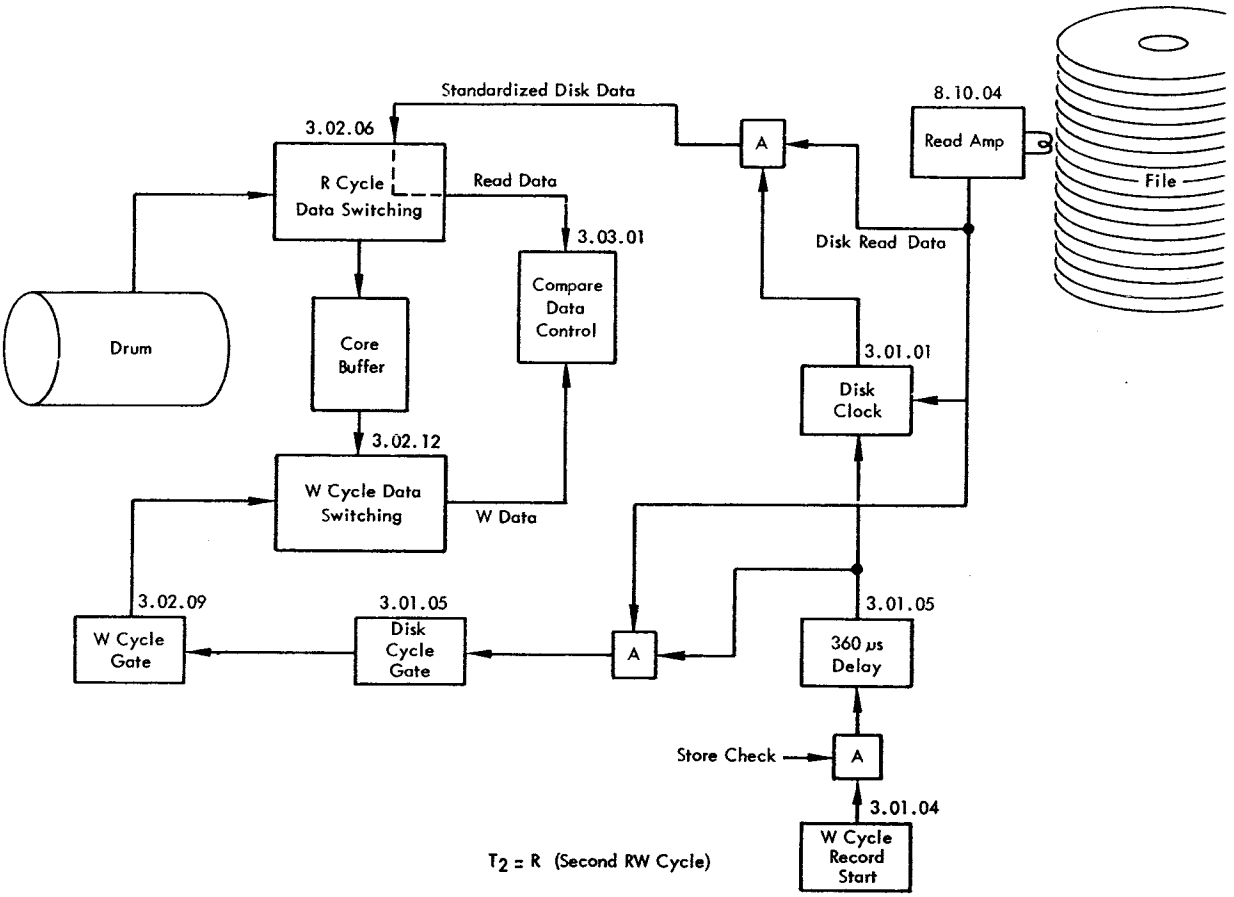


Figure 88. Data Flow and Controls, $T_2 = R$

characters to be written on the disk. Once W cycle begins, the machine will wait for the proper record start pulse; then, after a 600 μs delay, begin writing.

The record start pulse originates on System Diagram 8.03.04. For example, if the record address is 49995, the record start pulse selected will be from the 0/5 record head. As the permanent magnet passes the head a pulse is generated. On 8.03.02 this 0/5 pulse will be selected since the record 1 and record 4 address relays are up. After amplification and shaping on 8.03.03 the start pulse will become R cycle or W cycle record start on 3.01.04. The W cycle record start is conditioned by W cycle, T = R, and track located signal (2W7). T=R will be high while W cycle ready is high, if $T_2 = R$, as in our case. This means T = R will also be up while R cycle is still up (from CLBI to CLBR). To block a possible R cycle record start at this time the "and" inverter at 2Y8b will be conducting.

During the first W cycle (not store check still high) the record start pulse is inverted at 2S5b on 3.01.05 and its leading edge triggers the 200 μs single shot, 2C6 on 3.01.01. The rise of the 200 μs gate from pin 3, labeled control level gate, is placed on pin 7 of the AI at 3R8 on 3.02.12. If disk write gate is high at this time we will place AGC pulses (∅C) on the disk write data line. The disk write gate trigger (2V5 – 3.01.07) will be set 10 pin high by the leading edge of the 200 μs delay, labeled start record write delay. The disk write data on 3.02.12 is inverted on 8.10.05 and used to alternate conduction through the two halves of the read/write head.

The 400 μs disk write delay (2S4 – 3.01.05) is initiated by the fall of the disk W cycle delay gate, which is the 200 μs delay gate. During this 400 μs nothing is written on the disk, however the gap is being developed. At the fall of the 400 μs disk write delay the store check trigger, 2T4, and the disk W cycle control trigger, 2S3, are turned 3 pin high. The fall of the next ∅A sets the disk W cycle gate 3 pin high, raising the disk cycle gate line. This gate, 600 μs after record start, signals the machine to start reading out of core buffer to the disk write amplifier. On 3.02.08 it will drop the not W cycle gate, which inverted becomes the W cycle gate. On 3.02.02 we can now send phase pulses to the cores, each ∅A advancing the core bit ring, and every eighth bit time (Bit S) the ∅C will develop a core start on 4.11.00 at 4H7. This start reads out of the cores to the character register and 3 μs later advances the core units ring. Because the W cycle gate does not come up until the fall of ∅A, the bit ring is still at bit S when ∅C arrives. This reads out of core character 00 and advances the units ring to character 01.

The data from cores, ∅A to ∅A, is sampled on 3.02.12 with ∅C at 3R8. At the same time core space bits are being inserted for each character at 3S8. Since the core bit ring is reset to Bs, the first bit in any file record following the AGC pulses will be a space bit (Refer to Figure 86).

To stop writing after core character 99 has been written it is necessary to drop the disk cycle gate on 3.01.05 at 2V3. This blocks the core starts. The stop disk cycle gate line has a negative pulse at this time developed on 3.01.07. Two "and" inverters feed this line, one for W cycle and one for R cycle. During W cycle 2X5b will have Bs pulses on pin seven. Pin eight will go up when the write gate control trigger goes 3 pin high at the fall of core field 9. At the same time a 180 μs delay is initiated at 2U1 on 3.01.07. The fall of this delay gate will turn off the disk write gate 180 μs after the last character is written.

The record must be written within one sector on the disk. If the disk write gate remains "up" into the next sector, the AGC pulses for the next record will be erased. To detect this condition, the record stop pulse (record start for following record) samples the disk write gate trigger at 2V10b on 3.01.07. A write gate stop failure will turn on the file check trigger on 1.02.06. The fall of the record stop pulse, 40 μs later, is inverted at 2T5b on 3.01.07. It is capacitively coupled to the inverter at 2F10b, where it plate pulls the disk write gate 10 pin low.

When writing on the file a check will be made to ascertain that the file is up to speed. If the file is below speed, writing may be completed long before the end of the sector (record stop). On 3.01.08 the fall of the disk write gate will trigger the single shot at 4Y2. The negative single shot gate should appear at pin 5 of the AI at 4Y1a when the record stop pulse is on pin 6. In this case no file speed check will be detected. Notice that the check will be made only if a write operation has just been performed. The trigger at 4X2 will be pulled 10 pin low each file revolution with the record start. Only the fall of the disk write gate can raise pin 10 and allow the check. The duration of the single shot is adjusted after the file has reached full speed as outlined in the RAMAC Reference Manual.

Second RW Cycle: The store check line, being high at the end of the first W cycle, demands another RW cycle. The second R cycle will be accomplished in the normal manner, re-reading the selected drum track into the core buffer.

During the W cycle the 100 characters in the core buffer are entered into the compare circuits (3.03.01) as W data and the file record is entered into the compare circuits as read data. (Refer to the data flow on Figure 88.) The two sets of data flow must be syn-

chronized with the file clock. The file clock in turn will be controlled by the data coming from the disk.

A W cycle record start will be developed in the same manner on 3.01.04. ON 3.01.05 the disk read single shot 2V2 will be turned on, since store check is high. At the end of 360 μs pin 3 will go low, turning the disk R cycle control trigger 3 pin high and the store check trigger 10 pin high. The disk R cycle control scans the disk data line at the AI at 2U3b looking for the first bit written (after the AGC pulses). The first bit, a space bit, arrives and triggers a 4 μs read delay at 2R1. At the fall of pin 10 the disk cycle gate will be brought up by turning the trigger at 2T3, 3 pin high. The disk cycle gate will again become the W cycle gate on 3.02.09. This will provide core phase pulses to drive cores, and also develop W data on 3.02.12 at 3Q2b.

The disk clock on 3.01.01 was started with the first Bs on the disk read out data line by setting the clock control trigger at 2B6 10 pin high. This trigger had been previously set 10 pin low at the fall of the 360 μs disk read delay, appearing on the clock set line. It was previously explained how the clock control trigger kept both oscillators from operating when 10 pin low. Each data bit from the disk on 3.01.01 will flip the clock switching trigger, 2E7. The write clamp, which previously kept it 10 pin high, is down since the write relay 5057 on 8.01.01 dropped out at W cycle end of the first W cycle.

The disk read out data pulses are arriving at disk ∅A time since they are switching the clock. These pulses are developed into 6 μs pulses at the disk data single shot on 3.01.01 at 2F9. This is the disk data line which brings up the disk cycle gate on 3.01.05. This data is also fed to pin 8 of the standard data trigger 2H7, the plus shift turning this trigger 3 pin high. The next ∅A will flip 2H7 trigger 3 pin low resulting in a ∅A to ∅A standard data pulse. In the case of 2 consecutive data pulses, both ∅A's will be blocked at 2K7b resulting in a 24 μs data gate out. The standard disk data has the space bits removed on 3.02.06 at 3P4 (since there are no Bs in cores) and becomes read data.

W data and read data are now compared on 3.03.01. Two AK's at 3G7a and 3F4b are fed by both data lines. If both sets of data are identical neither one conducts. Any discrepancy causes one of them to conduct resulting in a ∅C pulse on the compare failure line to the file check trigger. This trigger raises the error lines and stops the machine in the same manner as a parity error, described in section 4, except the file check light will be on.

The reading and comparing operation will be stopped on 3.01.05 by dropping the disk cycle gate with a negative pulse on the stop disk cycle gate line at the first Bs after the fall of core field 9 (after character 99).

The file writing and reading operations are shown on the sequence chart in Figure 86. Notice how the two oscillators are out of phase during bit one time. ∅A and ∅B are early in relation to the data pulse but ∅C, initiated by the fall of the clock, is back in time.

Read Record From File ($T_1 = R$)

With the instruction, R99X9900, the RAMAC cycles through I, R, and W cycles, during which it transfers the record from the established file address into the core buffer on R cycle and to track X on W cycle. As the transfer from the core buffer to track X is a typical W cycle operation as covered in Section 4, we need to give attention only to the R cycle operation .

The earlier discussion of the second W cycle operation with $T_2 = R$ has developed all of the concepts necessary to understand how data may be read from the file. In the second W cycle operation with $T_2 = R$, the standardized disk data was passed through 3.02.06 to become read data which was entered into the compare circuits on 3.03.01. With $T_1 = R$ the read data is gated into the core buffer circuits by the R cycle gate (3.02.06). Refer to Figure 89.

The R cycle gate is provided by gating the disk cycle gate against R cycle at 3V3a (3.02.04). The disk cycle gate is developed in the same manner as was used to develop it for the second W cycle with $T_2 = R$, except that the single shot, 2V2, is triggered with the R cycle record start applied through 2W2a (3.01.05).

It will be recalled that on R cycles the core buffer waveform generator is not activated at any character time until BR∅C, after all bits for that character have been entered into the character register. Because of this, the core units and tens rings do not advance until the end of each character time. When the rings advance from 99 to 00, the last character has been transferred and the disk cycle gate can be turned off immediately. The fall of core F9 is inverted into a positive shift at 2Y4a (3.01.07). This is gated by R cycle to cause a negative shift on the stop disk cycle gate which flips the trigger 2T3 (3.01.05) to lower the disk cycle gate.

Record Advance

There are certain types of ledger accounts which normally require the capacity of two records to store the required data. A RAMAC user may, for example, reserve two records for each of his customer accounts.

One of these records would normally contain such

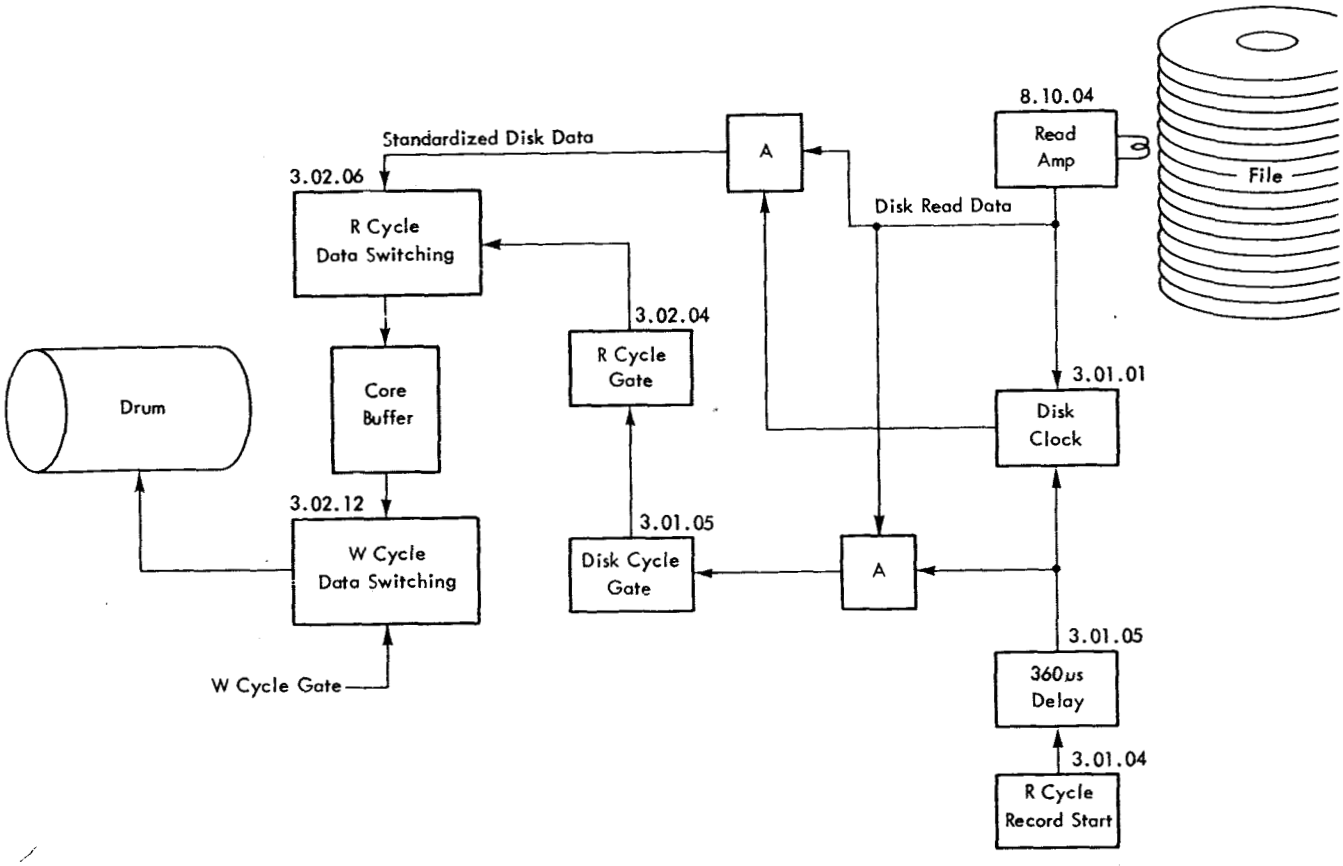


Figure 89. Data Flow and Controls, T, = R

information as name, address, and shipping instructions, whereas the second would contain the accounting data related to that customer. The two records required by ledger accounts of this type are normally stored in two consecutive file addresses. The record advance feature permits both of these records to be made availabe without requiring a second servo instruction.

For example, the ledger account of a particular customer is stored in file addresses 25242 and 25243. Record 25242 contains customer name, address and shipping instructions. Record 25243 contains the accounting data. When it is necessary to process a customer order, the following instructions transfer the customer's records to the processing track:

1. K05J9906 causes a servo to file address 25242.
2. R99W9900 &
   a. Transfers record containing customer name, address, and shipping instruction to track W.
   b. PROGRAM EXIT & is wired into RECORD ADVANCE IN. This causes the file address to advance from 25242 to 25243. RECORD ADVANCE OUT is wired to PROGRAM ADVANCE.
3. R99X9900 transfers record containing accounting data to track X.

Immediately prior to record advance the access mechanism is established at file address 25242. The address register relays are holding on the J hold B line. The record relay which holds is R5160, for record 2 (8.03.01). The disk tens relays and the record relays of the process unit address buffer are holding to J hold B. These relays are:

1. R354	disk tens = 2	3.05.07
2. R306	record = 2	3.05.03

OBJECTIVES:

1. Drop record 2 relays in address buffer and address register.
2. Pick record 3 relays in both groups.
3. Provide record advance out impulse during second P cycle. Drop old record relays.

Drop Old Record Relays: The program exit & hub emits an MR7 impulse during the first P cycle. This is wired to the record advance in hub on 3.05.02, picking R290 and R295 through the R306-2 N/O points. This will cause the 305 to go through an IRWDPDDP sequence. These relays hold through MR9 until character 48 of the second D cycle (2.09.02). The R290-4 points will open the hold to the record relays in the address buffer and address register by picking R311 on

3.05.01. The address buffer relays are on 3.05.03 and the address register relays are on 8.03.01. This occurs at F7 of the first D cycle following P cycle.

Pick New Record Relays: After dropping the record relays it is necessary to pick new relays, increasing by one the previous address. R295 has stored the information that the previous record address was 2. On 3.05.03 the address buffer relays 305 and 306 are picked through the 100 Ω resistor and the normally open points of R290 and R295 to ground. The other side of these relays goes to + 70 volts on the J pick line, through MR4 during the double D cycle. On 8.03.01, R5157 and R5160 (the record 1 and 2 relays) will pick through the normally open points of 305 and 306 on 3.05.12. The common side of the address register relays goes to + 48v on the pick common line. Normally this circuit is through MR6, which picks on servo operations. For record advance, however, we will place MR7 on the MR6 line. On 2.09.11 the circuit will be through the R289-3 N/O points to MR7 to +48 volts. R289 will pick on 3.05.02 through the 290-2 N/O points.

P, D, D, P cycle sequence will be required to complete the record advance routine. To continue the program a control panel impulse to the program advance hubs or the program entry hubs is required. This impulse will be available during the second P cycle from the record advance out hubs on 3.05.02. When the record address is advanced from 9 to 0 it may be desirable to change the track address. In this case the record advance overflow hub (3.05.02) emits instead of the record advance out hub.

Skip to Record

This feature operates very similar to record advance. A P flag wired to one of the 10 skip to record hubs (3.05.02) will change the record address, the track and disk addresses remaining unchanged. Any one of the 10 possible record addresses may be selected. A skip to record out hub provides an impulse to continue programming on the second P cycle.

For example, a P flag wired to SKIP TO RECORD 8 on 3.05.02 will pick relays 278 and 284. The 278-2 N/O points will pick R277 during the double D cycle. On 3.05.10, R311 will be energized through the 278-4 N/O points to drop both address buffer relays (3.05.03) and address register relays (8.03.01). Relay 309 on

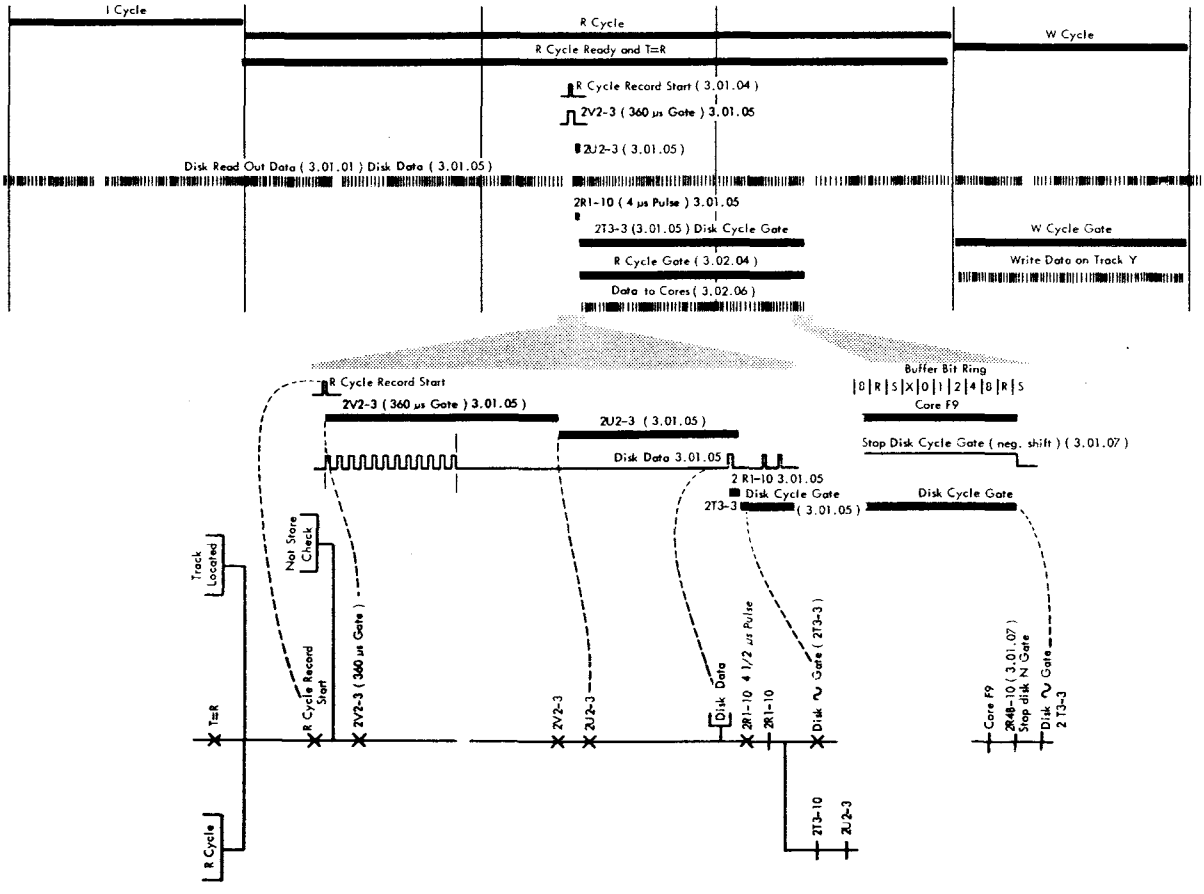


Figure 90. Read Record From File (R99Y9900bb)

3.05.03 will be picked through the 284-2 points to ground, when J pick (MR4) is made. On 3.05.12 record 8 pick line will be grounded through 309-3 N/O points. This will pick the record 8 relay R5164 on 8.03.01 because the pick common line is returned to + 48 volts by placing MR7 on the MR6 line. The skip to record out hub provides a control panel impulse on 3.05.02 through the 277-2 N/O points.

350 Optional Features

In this section the various combinations of files, process units and accesses will be discussed. This covers dual access, dual file, dual process and also the 10 million character file. Figure 93 illustrates the location of the various access arms available, the location of the shoe connectors, fuse boxes and relay gates. The M and S refer to MASTER and SLAVE 305's, the slave processing unit being the second 305 on a dual process system.

Access 0 is used on the standard single access machine and is connected to the 305 through shoe connector E (M). For dual access, 0 and 2 are used through SCE (M). For dual process, accesses 0 and 3 are used through SCE (M) *and* SCE (S) respectively. If dual access is included with dual process, all four accesses are used, 0 and 2 for the master 305 and 3 and 5 for the slave. A dual file system with single access uses access 0 for both files. The second file is connected to the 305 from its SCE (M) to the first file's SCH (M). Nearly all the SCH terminals are jumpered to the corresponding positions on the first file's SCE (M). This

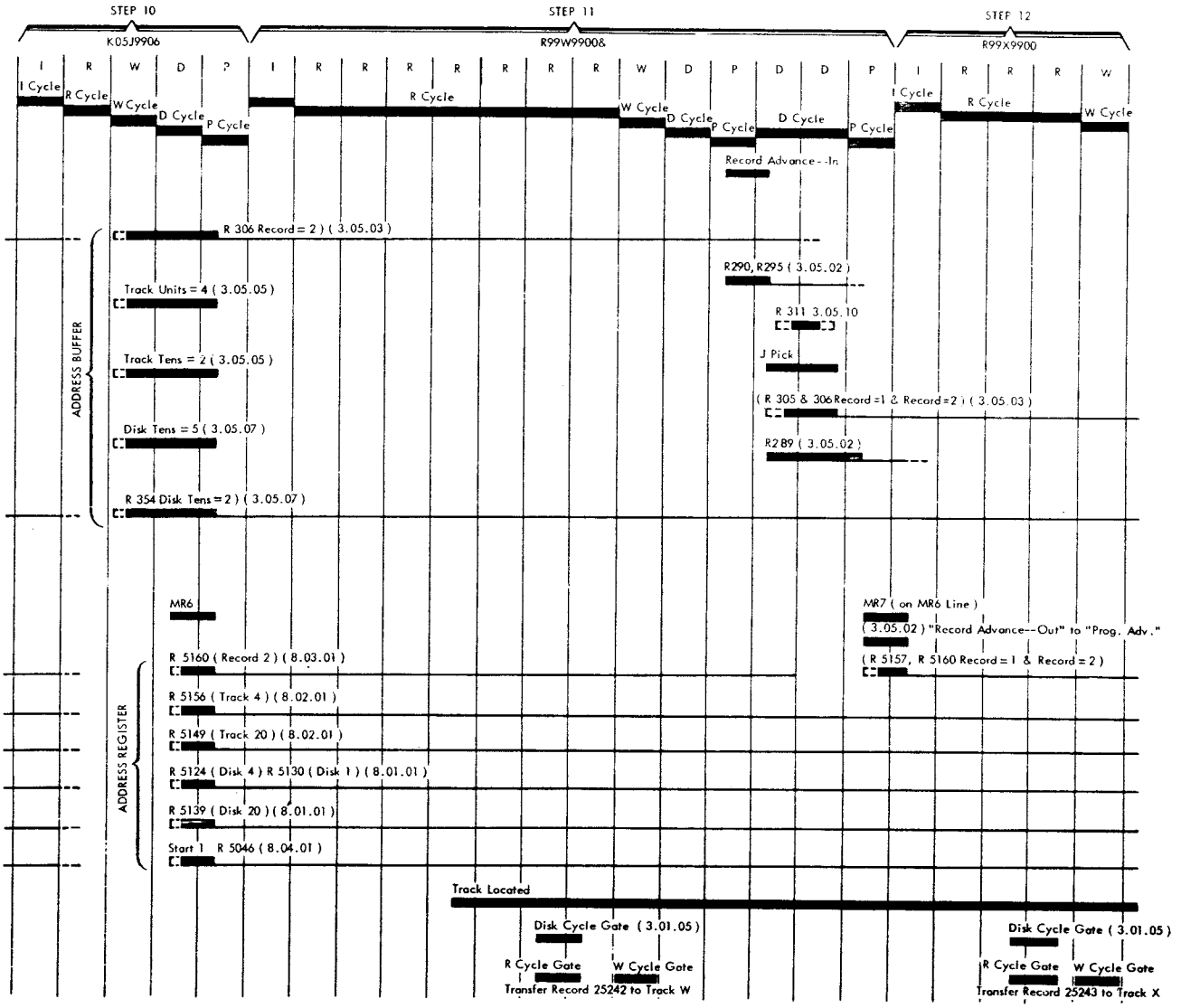


Figure 91. Record Advance

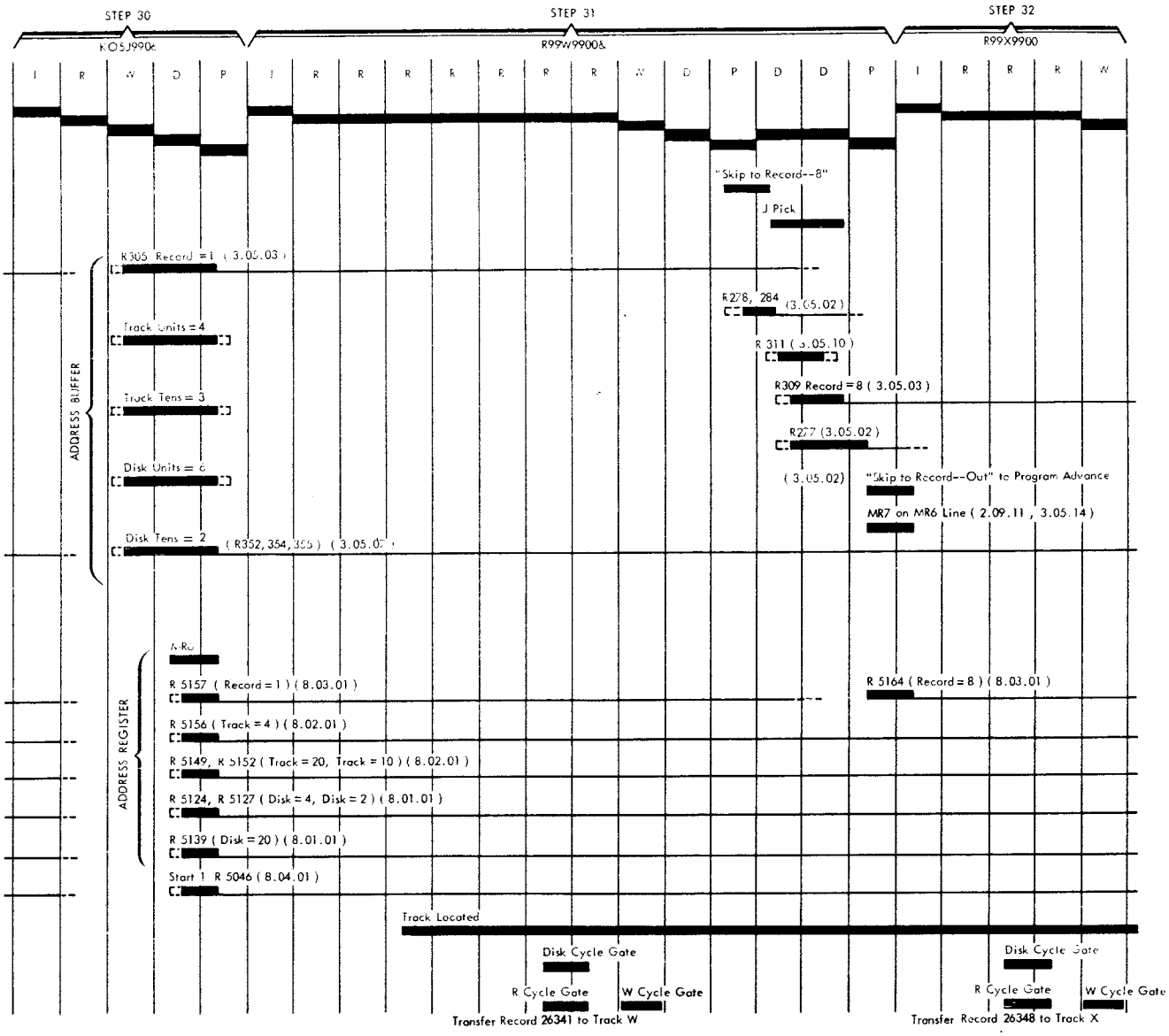


Figure 92. Skip To Record

can be seen on 8.00.07. The SCE (M) on the first file goes to the 305. Dual access can also be included on a dual file system using access 2 through the same cable arrangement.

A dual file system as well as the 10 million character file will augment the standard file addresses. For a dual file the second file will use addresses 5000 to 99999. With a 10 million character file the addresses will run from 00000 to 99999 for one file. If a 10 million and a 5 million character file are used on a dual file system the 10 million character file uses addresses 00000 to 99999 and the 5 million character file will use 100000 to 149999. Two 10 million character files use 00000 to 99999 and 100000 to 199999.

It is important to note that all operational information and control panel hubs refer to access 0 and access 1 on a dual access system. In the system diagrams access 0 and 3 correspond to the control panel access 0 while access 2 and 5 correspond to the control panel access 1.

Dual Access

To reduce the time required for servo operations and to allow processing to begin sooner, two access arms may be installed on a single file. Mechanically, the second access operates like the first and is located in position 2 (Figure 93). All circuits in the file are duplicated for the second access. These are mounted in a second relay gate below the first with identical numbering for the relays and pluggable units. The input, output and control lines to the 305 from access

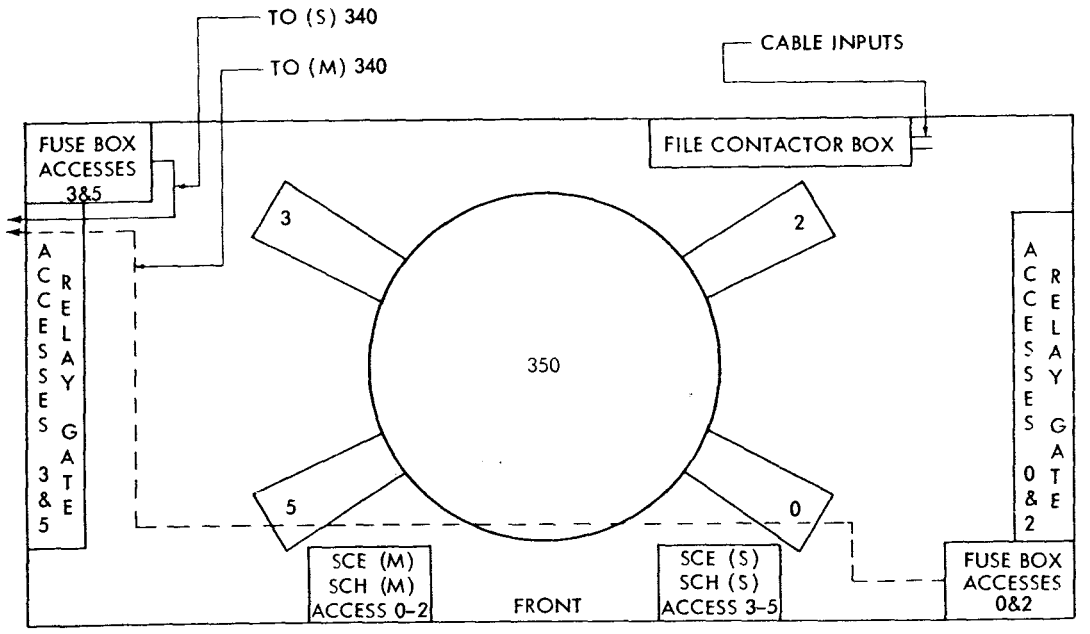


Figure 93. Models 3 and 4 Relay Gate File

2 circuits pass through SCE along with lines from access 0. To trace these lines physically the System Diagrams contain small charts showing the plug connections in shoe connector E for access 0/3 and access 2/5.

Functional Operation

There are two modes of operation for a dual access file:

1. Automatic sequencing.
2. Select Mode.
   A. Using one access only.
   B. Using either access, selected through the control panel.

Automatic sequencing occurs without any special control panel wiring. Following a machine reset, a $T_2 = J$ instruction will cause access 0 to servo. This same instruction switches all file input and output circuits to access 2. Any later instructions or commands to the file will be directed to access 2. This includes another $T_2 = J$, a $T = R$, or an inquiry. A second $T_2 = J$ will activate access 2 and at the same time alert access 0 to any file commands following. This means all programs using automatic sequencing will begin with two $T_2 = J$ instructions conditioning access 0 for the first file read or write operation.

The switch of the control circuits, when in automatic sequencing, may be prevented by including a Q of 4 in the $T_2 = J$ instruction. The following file commands will refer to the access which received this servo instruction. Another $T_2 = J$ without a $Q = 4$ will resume the sequencing.

In the select mode of operation the operator must choose the active access with control panel wiring. Five hubs, shown in Figure 94, have been added to the 305 control panel. A wire from the dual access common hub to SEL places the machine in the select mode. Program exits may be wired to either the dual access 1 or 0 hubs, through selectors if desired, to alert access 2 or 0. The selected access remains so until a new selection takes place. To use only one access for the entire program, a wire from the common hub to the 1 or 0 hub can be used.

Dual Access Logic

In Figure 95 the control of the two access arms as well as the data flow is illustrated. The condition of three relays, R426, R429, and R432 determines which access will be active. Let's assume these relays are all picked, conditioning access 2. During W cycle of a $T_2 = J$ operation the file address (data to J) picks the access 2 buffer relays, disk tens and record, through the N/O points of R432. The other buffer relays are common to both accesses. Pick common is directed to access 2 address relays through R426-1 N/O. This line also initiates the pick of the start relays for access 2.

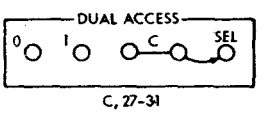


Figure 94. Dual Access Hubs

The result is a servo of access 2. The address relays and start relays will hold through N/C MR5.

This same operation will drop out (Figure 95) the 3 selection relays at the end of P cycle. R426-5 N/C conditions the 0 access write amplifier, while R426-6 N/C conditions the 0 read amplifier. Another $T_2 = J$ instruction will pick the access 0 address and start relays through the R432 N/C and R426-1 N/C points. Notice that during this $T_2 = J$ operation MR5 will open to drop the old access 0 address and start relays. The access 2 address and start relays will hold through R429-8 N/C points at this time.

Circuit Description

Access Selection: An "X" reset will set the alternate access trigger (3Y8-3.05.09) 10 pin low. This allows the manual reset line to fire the three blowout thyratrons and drop the three access selection relays. This trigger will be flipped from one state to the other every W cycle during $T_2 = J$ and $Q = \overline{4}$. Its output alternately conditions the relay pick thyratrons, then the blow out thyratrons which will be fired at P cycle end.

In the select mode a control panel wire from DUAL ACCESS C to SEL blocks the binary input to the alternate access trigger. It can be flipped only by an impulse to the 0 hub or the 1 hub.

Servo: The servo operation on dual access is performed in the same manner as on a single access file. When tracing circuits the condition of the three select relays must be known.

A modification in dual access interlocking does exist on 1.02.10. Normally a servo operation cannot begin if the access arm is still engaged in a previous servo, i.e., track located is low. An exception to this is following an "S" or "X" reset. Any time DC is turned OFF the file address relays will drop. This means the first servo must be made with track located down. On a dual access system the first two servos will be made

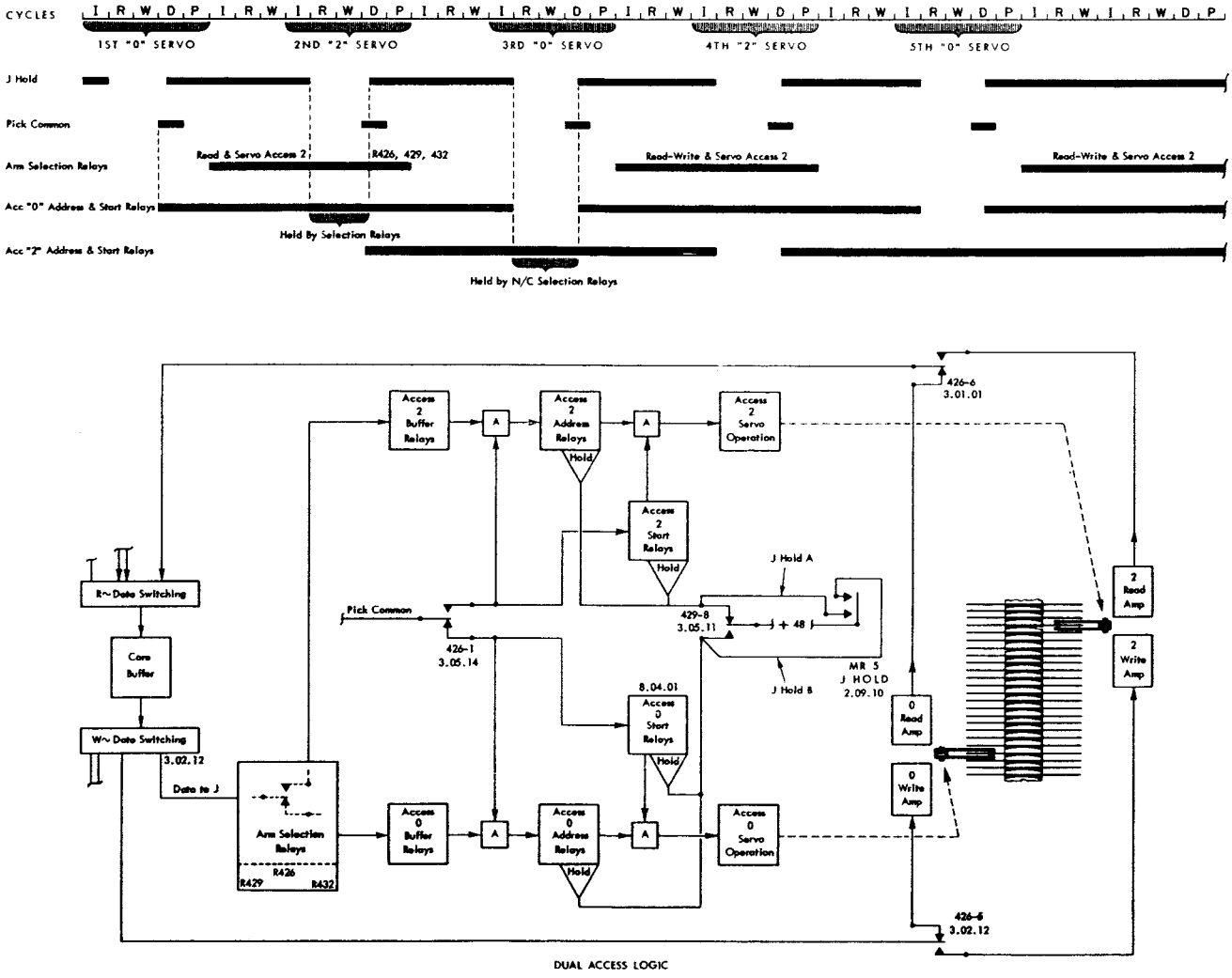


Figure 95. Dual Access Logic

with track not located. On the first servo the R cycle control trigger (1R11-1.02.10) will be 3 pin high allowing a start R cycle. P cycle of $T_2 = J$ will pull 1R11 3 pin low, but the next $T_2 = J$ instruction for access 2 will turn trigger 1K9 3 pin low. This returns the R cycle control trigger 3 pin high, allowing another start R cycle without a track located gate. Both triggers will remain 3 pin low for the remainder of the operation requiring a track located signal for an R cycle start during $T_2 = J$.

Dual File

Functional Operation

There is no change in the operation or programming of a RAMAC when a second 350 Disk Storage Unit is added to the system. The 305 Process Unit automatically decides which 350 will servo, this action depending upon the tens value of the disk address. When performing an instruction in which T = R, the system will read or write at the last servo address. The file which contains this address will be referred to as the active file in this discussion. The 5 million character file added to a basic system is referred to as file 2. It will contain records whose addresses range from 50000 to 99999. A 10 million character file in a dual file system becomes file 1 with addresses from 00000 to 99999. The 5 million character file contains addresses 100000 to 149999. This requires an additional character position in the disk address circuits (3.05.07) which is analyzed for a 1 bit to select file 2 as the active file.

A separate set of system diagrams will show the circuits for file 2. Input and output signal lines go from SCE on file 2 to SCH on file 1. From there many terminals on SCE and SCH of file 1 are common. AC power to both files comes from the remote compressor. The "power on" sequence is controlled by a timer in the remote compressor cabinet and is covered in the "340 Power Supply" section of this manual.

Circuit Operation

The block diagram of Figure 96 shows the modification to the circuits when two files are used. During any $T_2 = J$ command, the J hold B line opens and drops any address relays and start relays in either file. The file address is entered into the common address buffer relays. To select the active file, the high order position of the file address is analyzed and the pick common line is directed to file 1 or 2. The pick common also picks the start relays for the active file. The start relays will hold until the next servo, alerting the active file's read/write circuitry for a T = R operation. Notice that the inactive file's start and address relays will be down. The only neons indicating on an inactive file are logic safety, bias safety, head relay and disk solenoid.

On 3.05.14 there are 4 pick common lines available for a dual file system with single accesses. Two of these will be used, determined by the file configurations (5 or 10 million character files). The address buffer relays in the 305 will direct the MR6 pick common line to one or the other. On an inquiry operation the first digit of the address keyed at the console will select one of the four common lines coming from 6.05.02.

Dual Process

Functional Operation

Dual system control allows two RAMAC systems to share the same disk storage unit or units. To enable each system to operate independently, an access mechanism is provided for each in the shared file (s). Each system may use dual access in the shared file. The master system uses accesses 0 and 2 while the slave system uses accesses 3 and 5. Figure 93 shows the arrangement of accesses within a shared file. Each access has its own relay gate, with 0 and 3 being the top gate in the left and right end of the file, respectively. Two additional shoe connectors, E and H, are added for accesses 3 and 5. The symbol (s) signifies slave components and the symbol (M) master.

The only reason to prevent the two systems from operating completely independently would be an attempt of both systems to process the same record simultaneously. No restriction is placed on both files servoing to the same address; however, dual process interlock circuits prevent a track located signal to the second file to servo to a common address. The first file to reach an address has precedence. Whenever a file servos it compares the contents of its address relays to the contents of the other file's address relays. With dual access, two comparisons must be made. If both comparisons are unequal, a track located signal is allowed. These same checks are made following a record advance or a skip-to-record operation.

Dual process interlock can be suppressed by control panel wiring on either or both of the 305's. However, when a system picks interlock suppression it cannot write on the file. When dual process interlock suppression is active a neon glows on the originating system's console, just above the file check light (8.25.01).

With dual accesses on a shared file a double interlock condition can arise preventing either file from receiving a track located signal. For example:

Access 0 to address A
Access 3 to address B
Access 2 to address B with a Q of 4
Access 5 to address A with a Q of 4

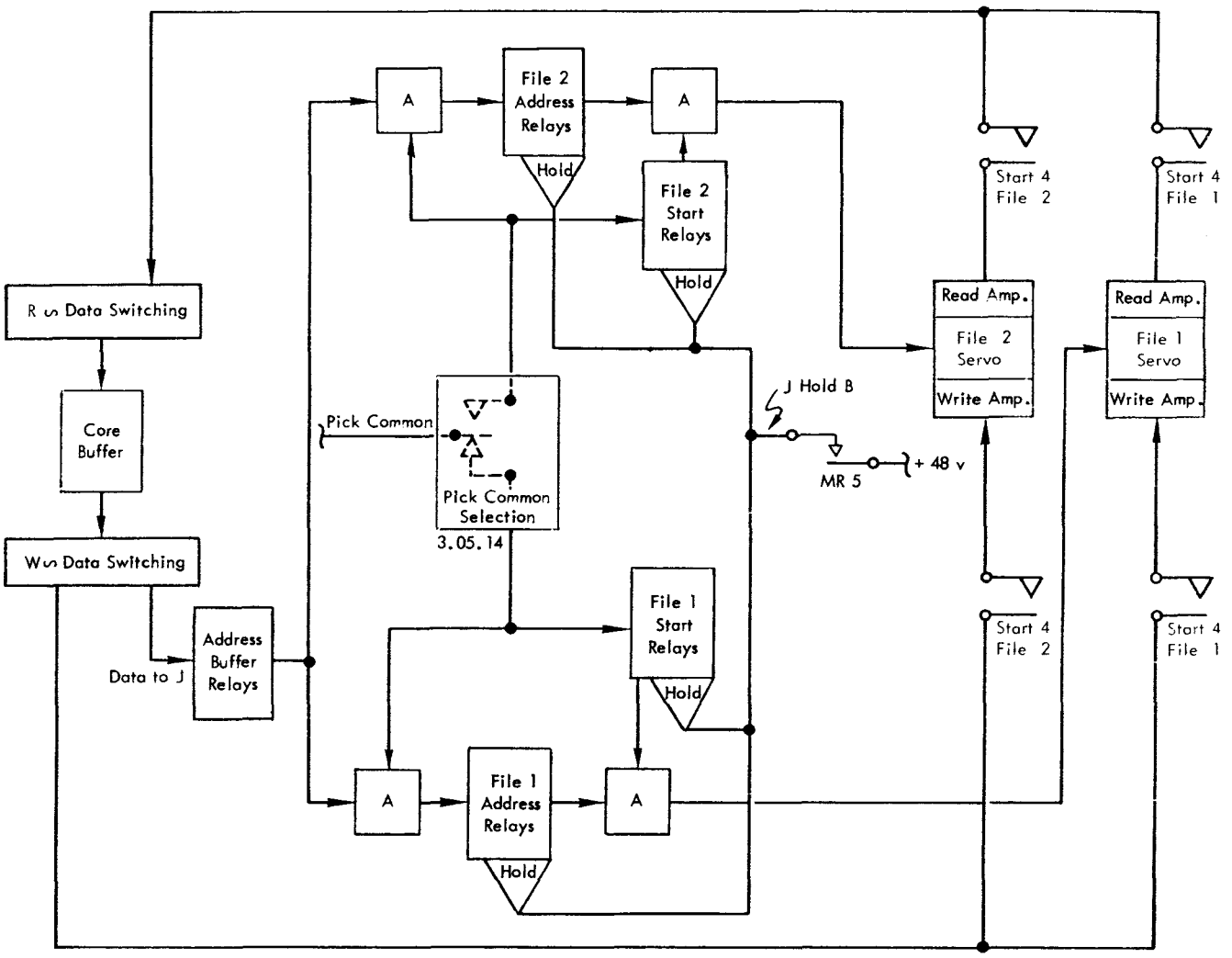


Figure 96. Dual File Logic

Dual process double interlock release circuits will allow the master system to receive a track located signal in this case.

Either system can operate with the other off. Depressing the power on switch on either console will cause the timer motor in the master compressor cabinet to sequence the file (s) power on (8.40.03). A slave compressor cabinet will be used only if the capacity of the two compressors in the master cabinet are insufficient. The slave cabinet will have only additional compressors in it. The control of file power is still in the master cabinet. When using a slave cabinet, the air supplies are in parallel. With dual access, dual file, dual process systems, connect master cabinet file 2 hose vent valve to the slave cabinet file 1 hose vent valve. The master cabinet file 1 hose vent valve supplies file 1 and the slave cabinet file 2 hose vent valve supplies file 2.

Circuit Operation

The dual process interlock circuits for access 0 checking the addresses at which arms 3 and 5 (on a dual access file) are located, are on diagrams 8.25.01 and 8.25.05. Each of the other three accesses will have similar circuits. A number 3 or 5 in parenthesis following a relay point indicates a relay in one of the other gates. All other relays and points are in access 0 gate. The objective is to develop a track located signal on 8.10.01 as soon as the access 0 servo is completed if access 3 and 5 are not at the same address. Plus 48 volts will be placed on the track located line through R5034-2 N/O and R5067-2 N/O on 8.25.01. These relays are picked by the J hold B line when an unequal condition exists in the compare circuits on 8.25.05. They will hold through their own 1 points until J hold B is broken by another servo instruction.

An impulse to the dual process interlock suppress pick (DPISP) hub on the master 305 control panel (3.05.11) will latch pick relays R5093 and R5094 bypassing the compare points in the track located signal line. File writing cannot occur from the system which has suspended interlocking because R5057 cannot pick (8.10.01). The interlock suppress will exist until the drop out hub on the master 305 is impulsed, latch tripping R5093 and R5094.

On a record advance or skip-to-record operation the J hold B line itself does not drop, however, it is modified before reaching 8.25.01 and 8.25.05. On 3.05.11 R289 or R277 points will open dropping the compare relays and allow a retest of the comparing circuits. The dual process double interlock release circuit is on diagram 8.25.09. All four arrival relays (R5071) must be picked. If there is no track located signal in either the slave or master 305 at this time, a double interlock exists. A high from 2Z1b in the master system will force a record start for the master system on 3.01.04.

In the event both systems servo to the same address simultaneously, preventing an access 3 clear signal (3.25.05) and an access 0 clear signal (8.25.06), the master system clear relay, R5034 on 8.25.01, will pick through R5034-3 (3) N/C points on 8.25.01 with J hold B. The slave system clear relay, R5034 on 8.25.02, will be unable to pick.

10 Million Character File

The track density has been doubled on this file increasing the addressable locations to 99999. Fifty single thickness disks are used which means 4 disk addresses per disk. This can be seen in Figure 6. All even disk addresses servo to the outer 100 tracks while odd disk addresses move the arm to the inner 100 tracks. There is an outer and one inner CE track, separated by 200 processing tracks.

The track detent assembly is shown in Figure 97. There are four detents numbered 1, 2, 3, 0 from outside to inside. Detent 0 operates for track addresses 00, 04, 08, 12, etc., detent 1 for addresses 01, 05, 09, 13,

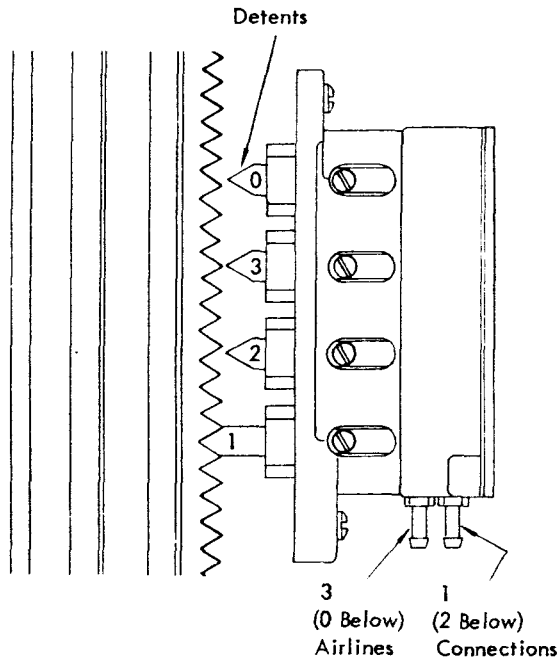


Figure 97. Track Detent, 10 Million Character File

etc., detent 2 for 02, 06, 10, etc., and detent 3 for 03, 07, 11, etc.

The address register for a single 10 million character file is not changed. However, the bit 1 relay of the units position of the disk address is now used in the track address relay tree to determine whether the track address is for an odd or even disk. For the disk markite all we need is the disk 10's relays and the 2, 4, and 8 bit relays of the disk units position. This can be seen on diagrams 8.01.02 and 8.02.02 for a 10 million character file.

The 5 and 10 million character gate files are identical in most areas. Any area that is different is easily identified. Each System Diagram covering a changed circuit has the title "10 million character file."

The single thickness disks used on this file require a different access arm, head spreader, read/write head, and head air pistons.

Card Reader

For normal processing the only input available to the RAMAC is through the card reader. The data read from the cards is translated from Hollerith into binary code, checked for accuracy, and stored on the input track of the process drum.

Mechanical Principles

Card Feed

A 402 type card feed is used to transport the cards from the hopper, past two sets of reading brushes to the stacker. The upper brushes are called write brushes, and the lower brushes are called check brushes. To recognize the presence of cards there is a card lever contact ahead of each set of brushes. There is also a hopper card lever contact.

The cards are placed in the hopper face down, 9 edge toward the throat, and are moved past the brushes by a series of feed rolls. The feed rolls are gear driven from the card feed clutch. At a fixed time in each feed cycle, a pair of feed knives move a single card from the hopper through the throat to the first set of feed rolls.

As a card moves past a reading station the 80 individual brushes scan the 80 columns, searching for punched holes. When a brush locates a hole, a + 140 volt signal is applied to that brush line. The identity of a punched hole is determined by the timing within the machine cycle when that hole is read. Signals from the write brushes are used to write card data on drum track K1. Check brush signals write card data on K3 track. K3 data is compared with write brush data to verify the reading accuracy of the write brushes.

Mechanical Drive

Figure 98 shows the relationship of the card feed unit to the 380 mechanical drive. The card feed clutch ratchet receives its drive from the motor, through a series of idler pulleys. The feed unit, the feed circuit breakers, and the index are driven by the card feed clutch through the horizontal shaft. The horizontal shaft is driven whenever the card feed clutch pawl and arm are engaged in the 10 tooth ratchet. The clutch latches at 320° of the index on systems equipped with K3 track. It latches at 288° on systems without K3 track.

Card Feed Clutch

The card feed clutch is similar to the 402 card feed clutch. Once the armature is attracted the pawl engages the first tooth of the ten tooth ratchet to pass by it. The safety pawl guarantees that once unlatched, the clutch pawl cannot be relatched by the armature until it has engaged with the ratchet and has been driven through a cycle. The clutch lever yoke spring absorbs the shock when the clutch pawl arm latches up and returns the arm to the 320° position if there is any movement beyond this point.

Card Feed Control

To start the feeding of cards, a single depression of the reader start key causes three card feed cycles. The process unit controls feed cycles after run in. Each PROGRAM EXIT impulse received at the card feed hubs causes one feed cycle. When the feed runs out of cards, several operations can take place. They are described below under "Last Card Operation," "Last Card Routine," and "Automatic Last Card Routine." Feed check circuits allow feeding, provided cards feed in correct order and do not jam. Read check circuits allow card feeding as long as the data read from the card is written correctly on the input track.

Run In Circuits

OBJECTIVES:

1. Three successive pulses to the card feed clutch (7.22.03).
2. Keep the feed check relay up (7.22.04).
3. Keep the read check relay up until read check time (7.22.04).

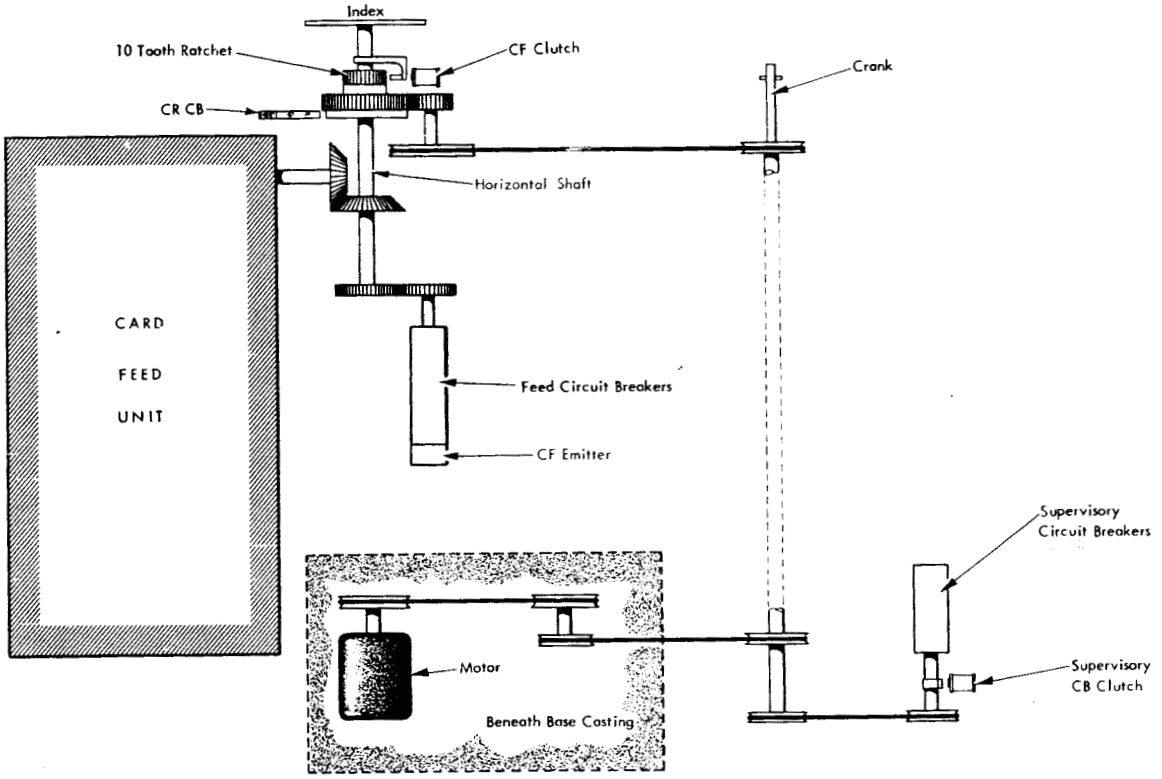


Figure 98. 380 Mechanical Drive

One depression of the start key will feed 3 cards, the first card passing the check brushes on the third feed cycle. The sequence chart in Figure 99 illustrates the relay operation. Relays 8035, 8036, and 8037 are up before striking the key and will remain up unless a feed failure occurs. R8027, the run relay will pick 3 times through the R8004-2 N/O points on 7.22.03, then R8004 will drop. This directs control of R8027 to the select relay, R170, on 2.07.03.

Process Unit Control

OBJECTIVES:

1. Energize card feed clutch once (7.22.03).
2. Latch pick R170 (2.07.03).

When R170 is up the reader not ready line is high (2.07.03). This line blocks an R cycle gate (3.02.04) or a W cycle gate (3.02.08) if T = K. R170 LT is picked by FCB 19 at 253°.

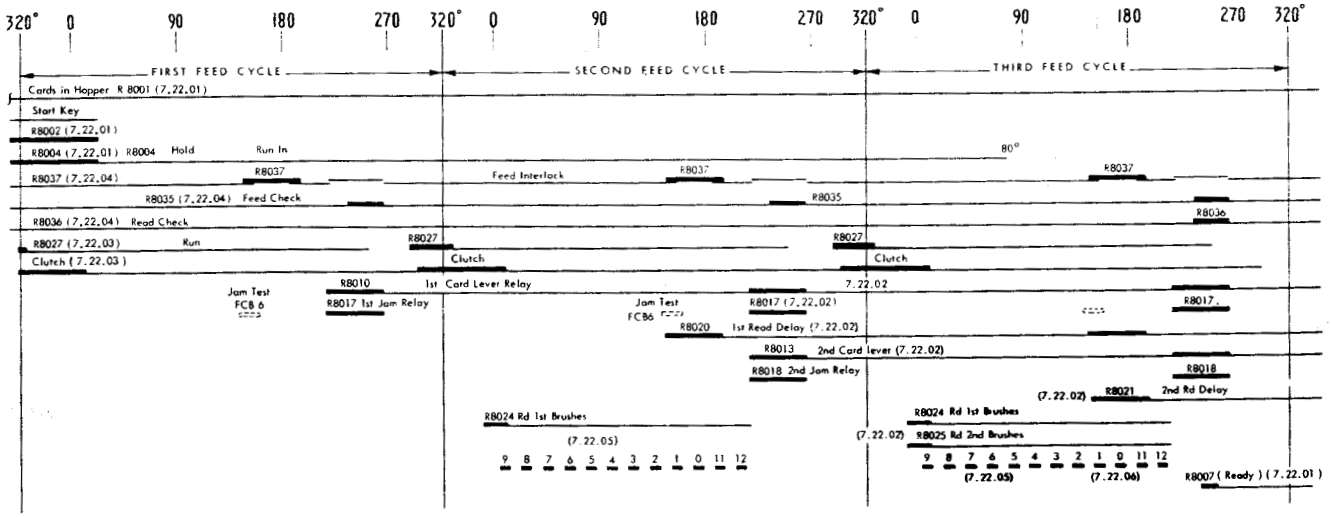


Figure 99. Reader Run-in Clutch Control

Last Card Operation

After the run in, the card feed will operate for each impulse received at the feed card hubs until the last card has passed the check brushes. The opening of R8013-10 N/O points (7.22.03) blocks the pick of R8027. If there are more cards to be processed, place them in the hopper and depress the start key. The cards will feed in and then processing will proceed as if there were no interruption. If there are no more cards to be processed, the last card may be fed to the stacker by depressing the start key. R8027 will be picked through the R8002-3 N/O points.

Last Card Routine

Many programs will include a special routine to be executed after the last card has been processed. This last card routine (ALC hubs not wired) should be used whenever the amount of cards to be processed is more than one hopper full. The set of last card hubs is used to indicate when this routine should start. The last card relay, which controls these hubs, is energized during the first card feed cycle after the last card has passed the check brushes. An example of this condition is shown in Figure 100.

When the feed runs out of cards the last card routine will be suppressed by placing cards in the hopper. An example of this operation is shown in Figure 101.

OBJECTIVE:

Energize the last card relay (7.22.03).

In Figure 100 the program loop is short so that the card feed is kept in continuous operation. Transfers from the input track are accomplished by the instruction, K99W9900Fb. After the last card has passed the check brushes, the program instruction that transfers last card data to W track is accomplished, but a card feed operation does not take place. R170 picks, but with the second card lever relay down, the run relay does not pick. Processing continues until the program loop returns to R cycle of the same instruction. Depressing the reader start key allows a card feed cycle. The last card relay picks during this cycle. This latch trips R170 and programming resumes, branching into the last card routine.

Automatic Last Card Routine

When the amount of cards to be processed is less than one hopper full, the last card routine can be started automatically. Bottle plugging the ALC hubs on the control panel allows one additional card feed following the cycle that the last card passed the check brushes. The last card relay picks during this cycle allowing the last card routine to start.

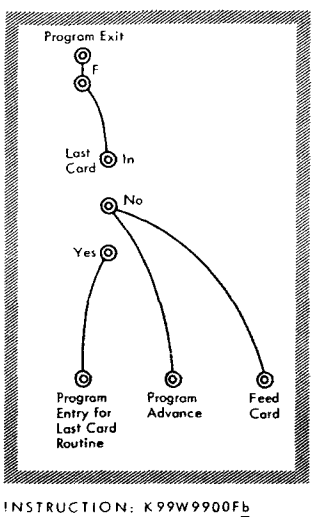
OBJECTIVES:

1. One additional automatic feed cycle after last card passes check brushes (7.22.03).
2. Pick last card relay (7.22.03).

The additional cycle occurs when R170 is picked. The circuit that picks the run relay on 7.22.03 goes through R8007-5 N/O to the ALC hubs on 3.05.11.

Feed Interlock

The feed interlock circuitry is designed to stop card feed operation whenever cards feed incorrectly. When cards are feeding correctly the feed check and feed interlock relays are up throughout each feed cycle.



INSTRUCTION: K99W9900Fb

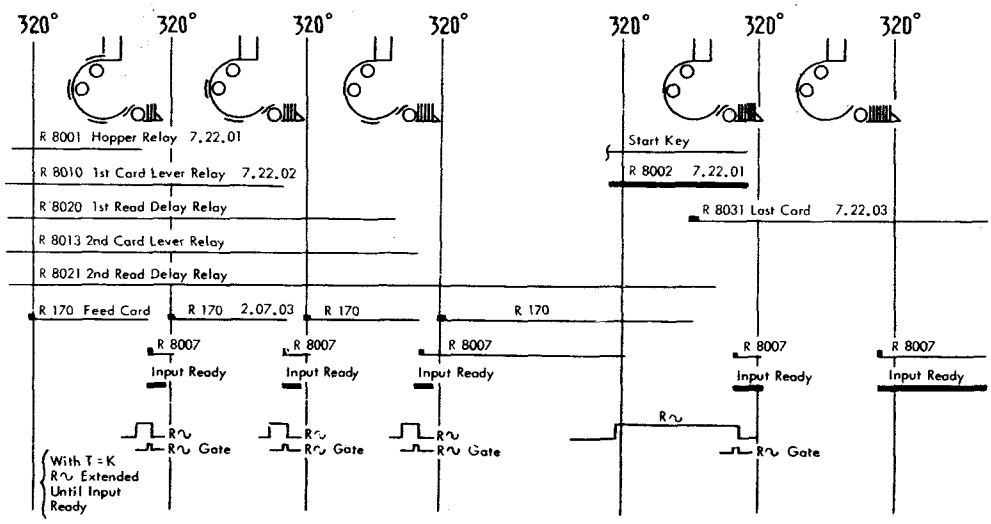


Figure 100. Last Card Routine

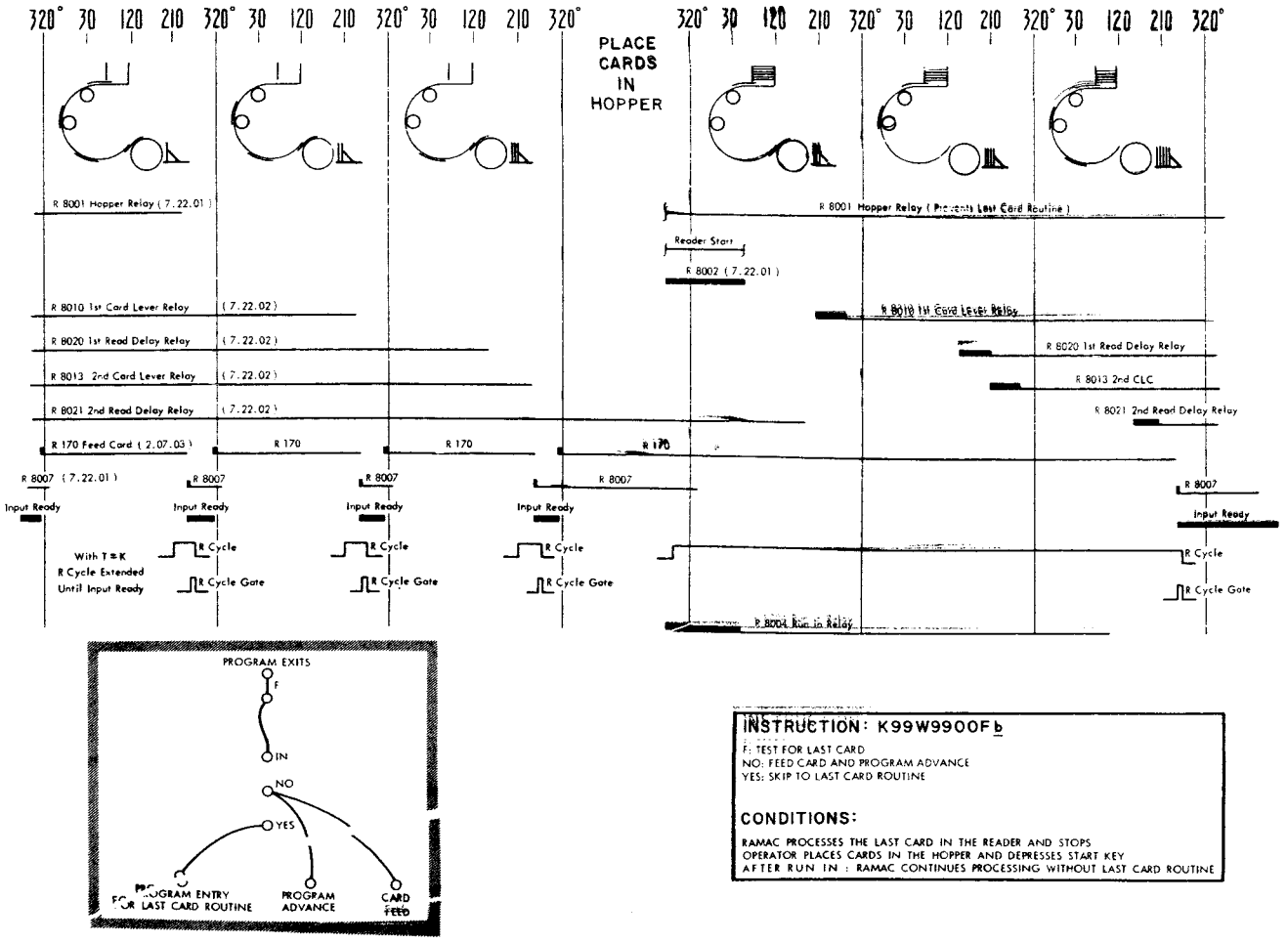


Figure 101. Run-in Sequence After Reader Runs Out of Cards

OBJECTIVES:

1. Keep feed check relay up (7.22.04).
2. Keep feed interlock relay up (7.22.04).

The feed interlock relay must be up to keep the feed check relay up. The hold coil of the feed interlock relay, R8037, picks twice each cycle through FCB's 4 and 9 in series on (7.22.04). R8037 pick coil is impulsed to bridge one gap between the FCB 4 and 9 impulses. This impulse is received as long as no card jam occurs. R8037 hold receives an impulse from FCB 5 to bridge the second gap in the FCB 4 and 9 impulses as long as cards are feeding in their proper order.

Data Flow

There are three different input tracks, K1, K2, and K3. Card data read at the write brushes is written on K1. K1 data is transferred to K2 without going through the core buffer. This transfer occurs at the beginning of the cycle when the card containing the data passes the check brushes. Data read at the check brushes is written on K3. As soon as all K3 data has been written, a bit by bit comparison of K2 and K3 data is made. If this data compares favorably, transfer of K2 data to the core buffer is allowed. This describes the card reader operation for normal processing conditions. The K test-K run switch on the console is set to K RUN for this operation. That is the normal position for this switch. With it so set, a T = K operation addresses K2 track.

To assist a Customer Engineer to analyze read check problems the K test-K run switch may be set to K TEST. When this is done a console read K operation reads K3 track. The card feed will not run continuously with the switch in this position. It forces a read check. This switch is not present on early production models. Early models use a bit count system of read checking.

Writing on K1 and K3

Card data is written in character positions 00 to 79 of K1 and K3 tracks. Card column one data is written

in C00; column two in C01; etc. Character positions 80 through 99 of K1 and K3 never receive data. As the card is read, all the 9 punches are read simultaneously, then all the 8 punches, etc. The process drum makes 1⅓ revolutions during each read time impulse. This allows each card column to write into its particular character position on the drum. Each hole develops its own write character gate to allow writing on K1 and its own check character gate to allow writing on K3. Any brush reading a hole at 9 time will have the read impulse decoded into B0 and B4 pulses, because data is stored on K1 and K3 one bit early. Writing one bit early allows data to be transferred to K2 from K1 without going through the core buffer.

Since the character in the card may be composed of more than one Hollerith punch, the bits recorded within a particular character position during a digit impulse time may be supplemented by additional bits at a later digit time. The intervals between the recording of bits cannot be occupied by write 0 current because this would erase the bits which were written at an earlier digit time. The technique used is to erase the track completely, prior to card reading time. Then ØC bits are recorded without interspersing write 0 current. This is called the discrete pulse method of writing.

OBJECTIVES:

Writing on K1 objectives follow. Writing on K3 objectives are similar.

1. Erase K1 (3.10.21).
2. Develop the write character gate (7.21.05).
3. Decode emitter output (7.25.00).
4. Write on K1 (3.10.21).

The following describes the achievement of the above objectives while writing a "7" on K1 track from card column 14 (brush 13). The description refers to Figures 102 and 103. At the beginning of the card feed cycle, FCB 25 provides current to completely erase (write 0) K1 track. Then, when the 7 punch is sensed, the impulse is "anded" with C14 and BR to plate pull the write character gate trigger (7X3 – 7.21.05). This trigger develops a gate for each punch that is sensed in the card. It allows decoder impulses to be written on

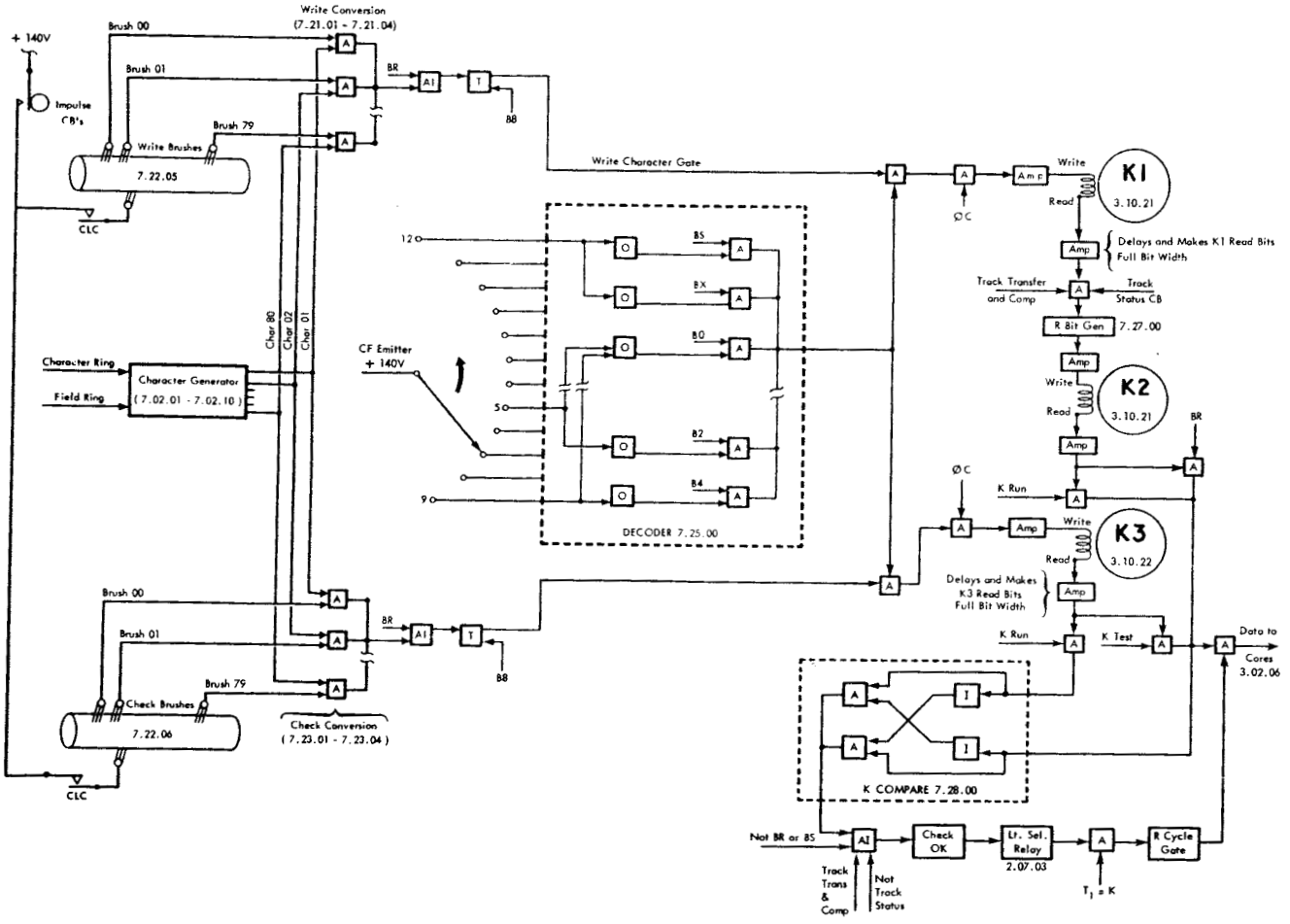


Figure 102. Input Read and Check Logic

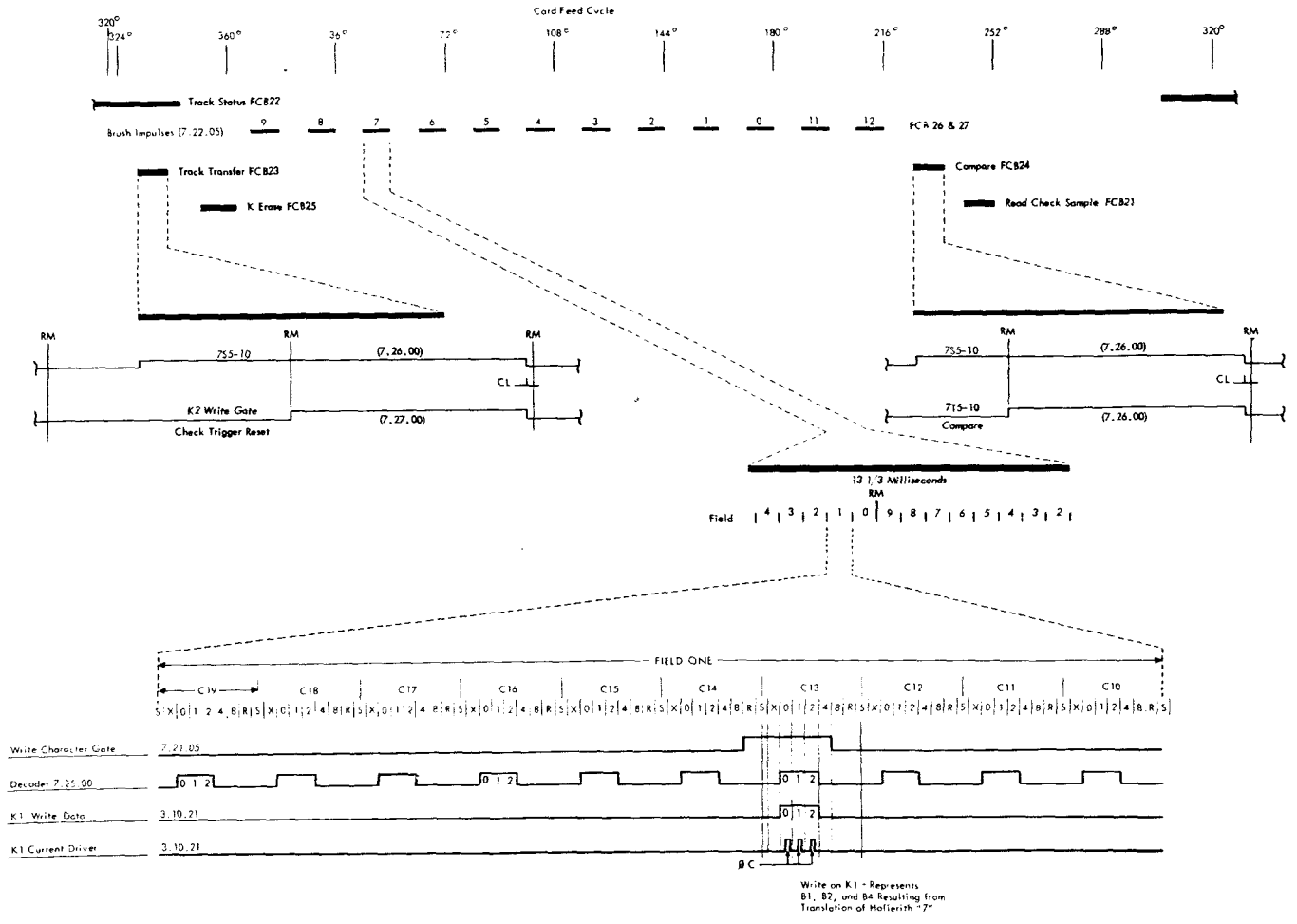


Figure 103. Card Read and Check Sequence Chart

K1. B8 of C13 lowers the write character gate. At the time that the 7 punch is sensed, the emitter (7.22.01) is made on the 7 segment. The decoder emits B0, B1, B2 pulses all during this time. B0, B1, and B2 represent a 7 when written one bit early. One group of these pulses "ands" with the write character gate, then is strobed with a ØC. These pulses then become write one pulses at the write head. BR's are not written on K1 and K3.

Transfer K1 to K2

Refer to Figures 102 and 103. The track transfer CB controls when data is shifted from K1 to K2. This occurs very early in a feed cycle just before K erase time. Data transferred must be delayed one bit and have BR's added where needed.

OBJECTIVES:

1. Delay K1 read data (3.10.20).
2. Add BR's where needed (7.27.00).
3. Write data on K2 track (3.10.21).

K1 read data delay occurs on 3.10.20. Figure 104 is a sequence chart showing an example of signals present when a "P" is read from K1 track.

BR's are inserted into K1 read data on 7.27.00.7J7 counts the number of bits present in each character. 7J7-10 is high whenever the count is even. This output "anded" with the R bit gate inserts BR's into K2 write data.

K2 write data is gated by the K2 write gate. The sequence of developing this is shown in Figure 103.

Read Check

Read check consists of comparing K2 and K3 track data bit by bit to see if the data is the same on both tracks. K3 data has to be delayed one bit and expanded to full bit width before entering the comparator so that it will be similar to K2 read data. On a $T_1 = K$ operation if the two tracks contain the same data, R cycle gate is allowed. This allows the process unit to read K2 track. If the data does not

compare, the R cycle gate is not allowed, a read check is indicated, and the card feed will not operate.

OBJECTIVES:

Equal comparison.

1. Delay K3 read data (3.10.22).
2. Compare OK (7.28.00).
3. $T_1 = K$ R cycle gate (3.02.04).

The delay of K3 read data is accomplished the same way K1 read data is. Figure 104 shows a sequence chart of K1 read data delay.

The comparator has no output if each input is equal, so the ATH 7Z7 conducts on 7.28.00. On 7.22.04, the read check relay, R8036, picks when the thyratron fires. This allows the reader select relay, R170, to be latch tripped.

A $T_1 = K$ R cycle gate is allowed on 3.02.04 after the reader select relay is tripped. This is indicated when the reader not ready line is low.

OBJECTIVES:

Unequal comparison.

1. Fail to pick read check relay (7.22.04).
2. Interlock reader (7.22.01).
3. No $T_1 = K$ R cycle gate (3.02.04).

The read check relay is not picked when there is an unequal comparison.

Reader interlock results from not tripping the reader select relay. R8036-3 N/O on 7.22.01 prevents tripping.

No $T_1 = K$ R cycle gate is allowed when the reader not ready line is high.

Console Read K3 Track

OBJECTIVES:

1. K3 data to cores (7.28.00).
2. Add needed BR's (7.27.00).

K3 data "anded" with K-test allows K3 data to cores. K2 data "anded" with BR's, inserts BR's where needed on the K3 data line.

Program Load

It is possible to load programs from the card reader to the program tracks. This is accomplished by automatically performing the instruction K9919900 as soon as the data read is checked on the input track. The instruction also has a special automatic program exit, which is labeled COPY OUT. This exit is usually used to start a program to transfer the I track data to other program tracks and then program load another card.

A program load operation may be started two ways. One way is to place the program load cards in the feed hopper and then depress the program load button. This causes 3 card feed cycles and then the auto-

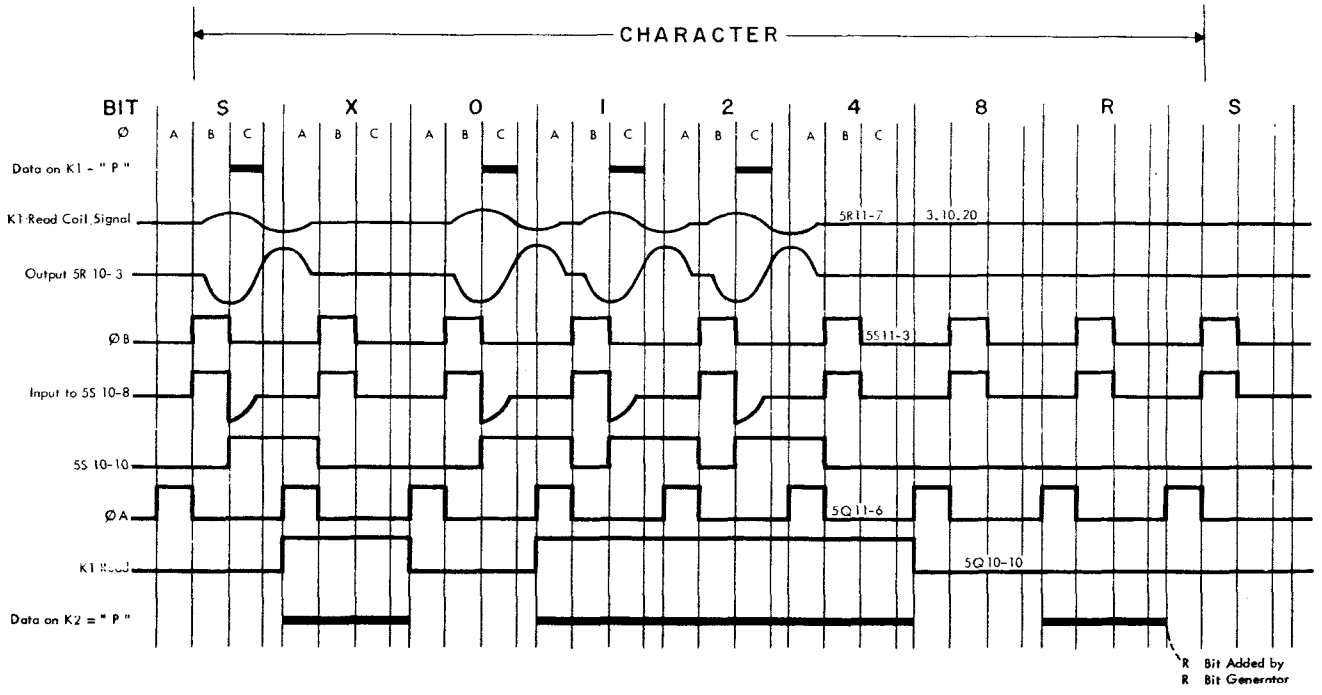


Figure 104. Delay and Expansion of K1 Read Data (3.10.20)

matic transfer of K track data to I track, and a COPY OUT EXIT. The other way is to wire the control panel from the start hub to the copy in hub and then depress the reader start key. This will cause the feed operation, then the transfer to I track, and COPY OUT EXIT.

Additional program load card operations may be initiated by wiring a PROGRAM EXIT to the copy in hub.

Program Load Button Operation

Figure 105 shows the sequence of operations when the program load button starts the operation.

OBJECTIVES:

1. 3 card feed cycles (7.22.01).
2. Copy line high (2.07.01).
3. Master stop trigger 3 pin high to begin processing (1.02.09).
4. $T_1 = K$ (2.03.03).
5. $T_2 = I$ (2.03.05).
6. IRWDP cycles (1.03.04 to 1.03.08).
7. Copy out impulse (2.07.01).

The 3 card feed cycles are normal run in card feed cycles. They are started by the program load switch parallel to the start button on 7.22.01.

The copy line high signals the system that a program load operation is taking place. The copy trigger is turned ON by R175-3 N/O on 2.07.01. R175 latch picks on 1.02.03 when the program load switch is depressed.

The master stop trigger pin 10 is plate pulled as a result of R161 on 1.02.03 picking. R161 is picked through the R175-2 N/O points when R175 is latch tripped. This occurs when the R8021-4, 2nd read delay

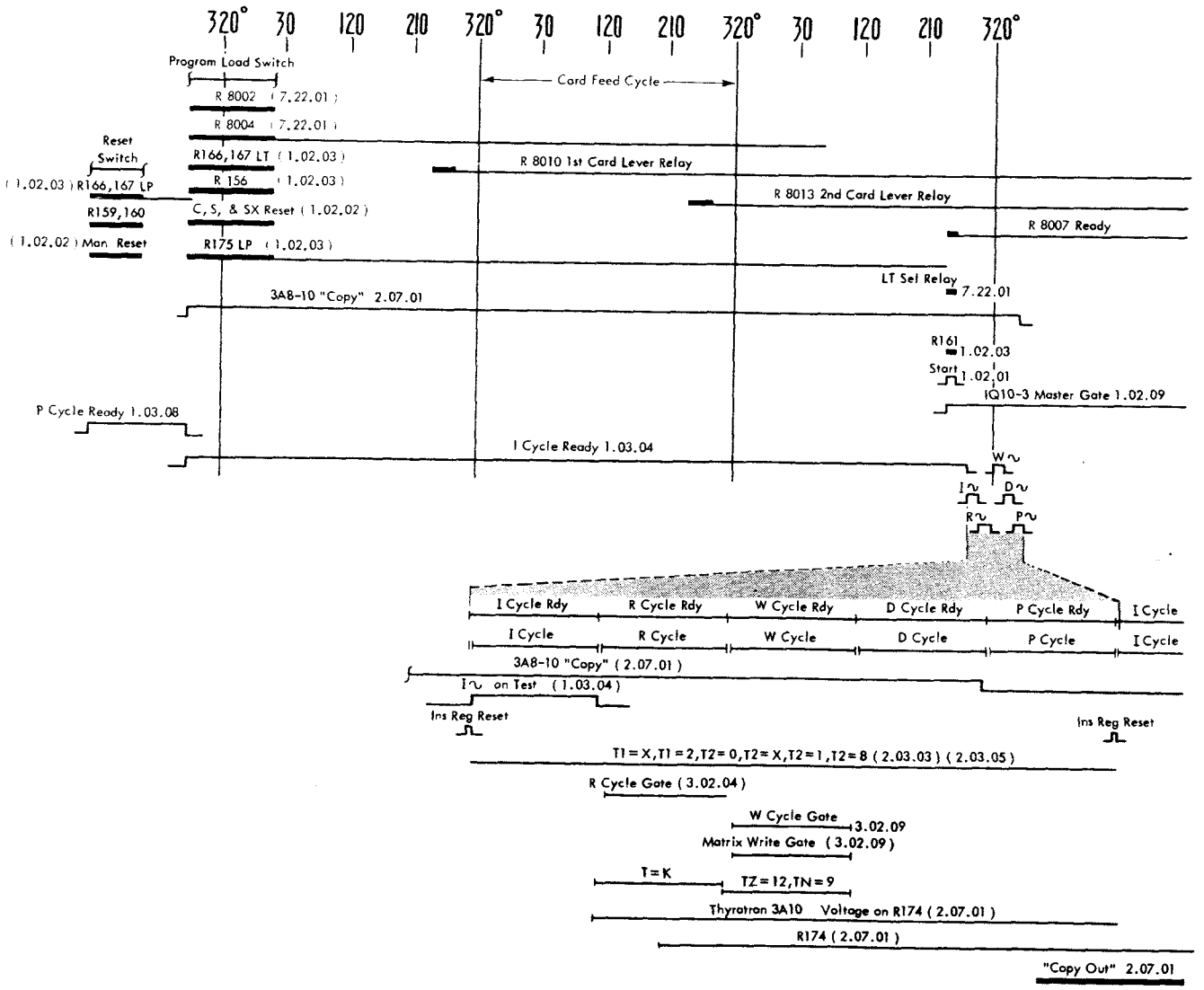


Figure 105. Program Load

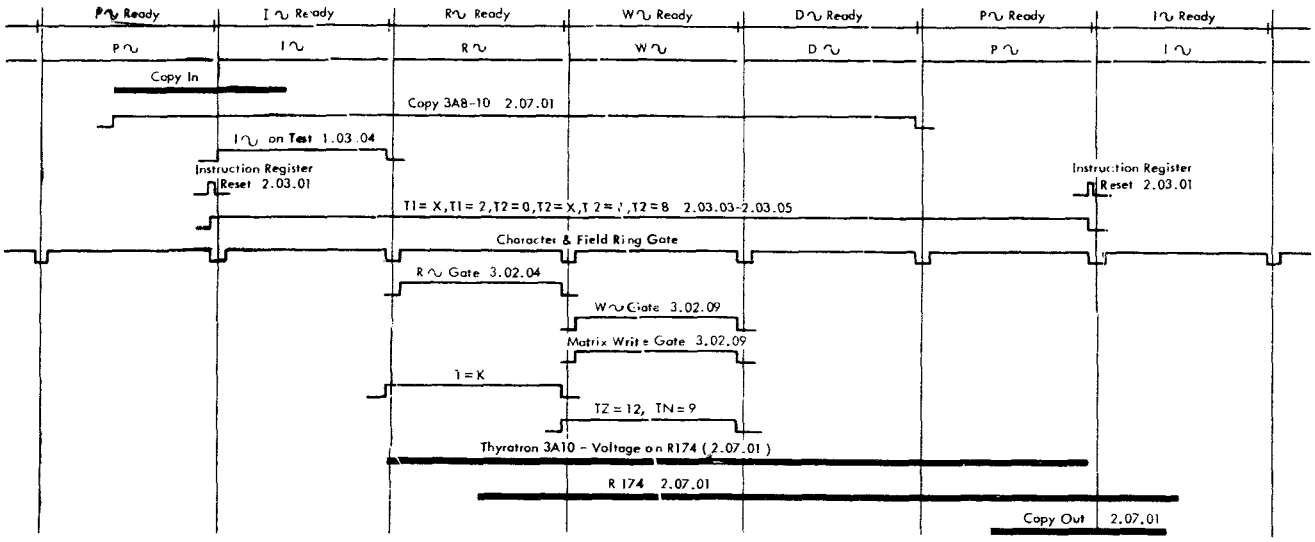


Figure 106. Copy Operation

relay is up, indicating the third feed cycle is nearly complete.

$T_1 = K$ is set in the instruction register as a result of $T_1 = X$ and $T_1 = 2$ on 2.03.03. Turn on $T_1 = X$ and turn on $T_1 = 2$ are developed with I cycle on test. I cycle on test is developed on 1.03.04 with the copy line high.

$T_2 = I$ is developed by copy and I cycle on test on 2.03.04, similar to the development of $T_1 = K$ above.

IRWDP cycle details are found in the Basic Machine Timing Section. I cycle ready is initiated by depressing the program load button. Refer to Figure 101.

A copy out impulse originates from the MR-7 line. MR-7 picks every P cycle on 2.09.02.

Copy in Operation

At the completion of the run in card feed cycles, the start hub emits an impulse. This impulse when received at the copy hub, plate pulls the copy trigger ON. This sets up an automatic K99I9900 operation with a copy out impulse. Any program exit impulse into the copy in hubs initiates this automatic program also.

OBJECTIVES:

1. Three card feed cycles (start button).
2. Start hub impulse (1.02.02).
3. Copy line high (2.07.01).
4. $T_1 = K$ (2.03.03).
5. $T_2 = I$ (2.03.05).
6. IRWDP cycles (1.03.04 to 1.03.08).
7. Copy out impulse (2.07.01).

All of the above objectives except the start impulse are described under the program load operation. The start impulse is a MR-7 impulse coming from 6.11.04. The impulse passes through R167-1 N/O, and R8006-2 N/O. R167 was latch picked on 1.02.03 when the reset button was depressed. R8006 is latch picked on a run in operation on 6.11.04. The MR-7 impulse is present during P cycle. The reset button placed the machine in P cycle ready. The master gate, going high after the third card feed cycle, starts P cycle. This is illustrated in Figure 106.

Input Data Rearrangement (Optional)

The control panel hubs associated with this feature may not be wired to any other area of the panel. The control panel mask is bright orange to define this restricted area.

Rearrangement

Data rearrangement is accomplished by controlling the location on K track in which data from each card column will write. 100 input track control exit hubs and 80 card column control entry hubs on the 305 control panel allow this control. By wiring from any track hub to any card column hub, the information contained in the card column will be written on K1 and K3 tracks in the character position wired. The control panel wiring "ands" the character to be written with the brush from which it is read. A BR is written in all unwired positions on K2 track. Figure 107 is a block diagram showing how the rearrangement feature operates.

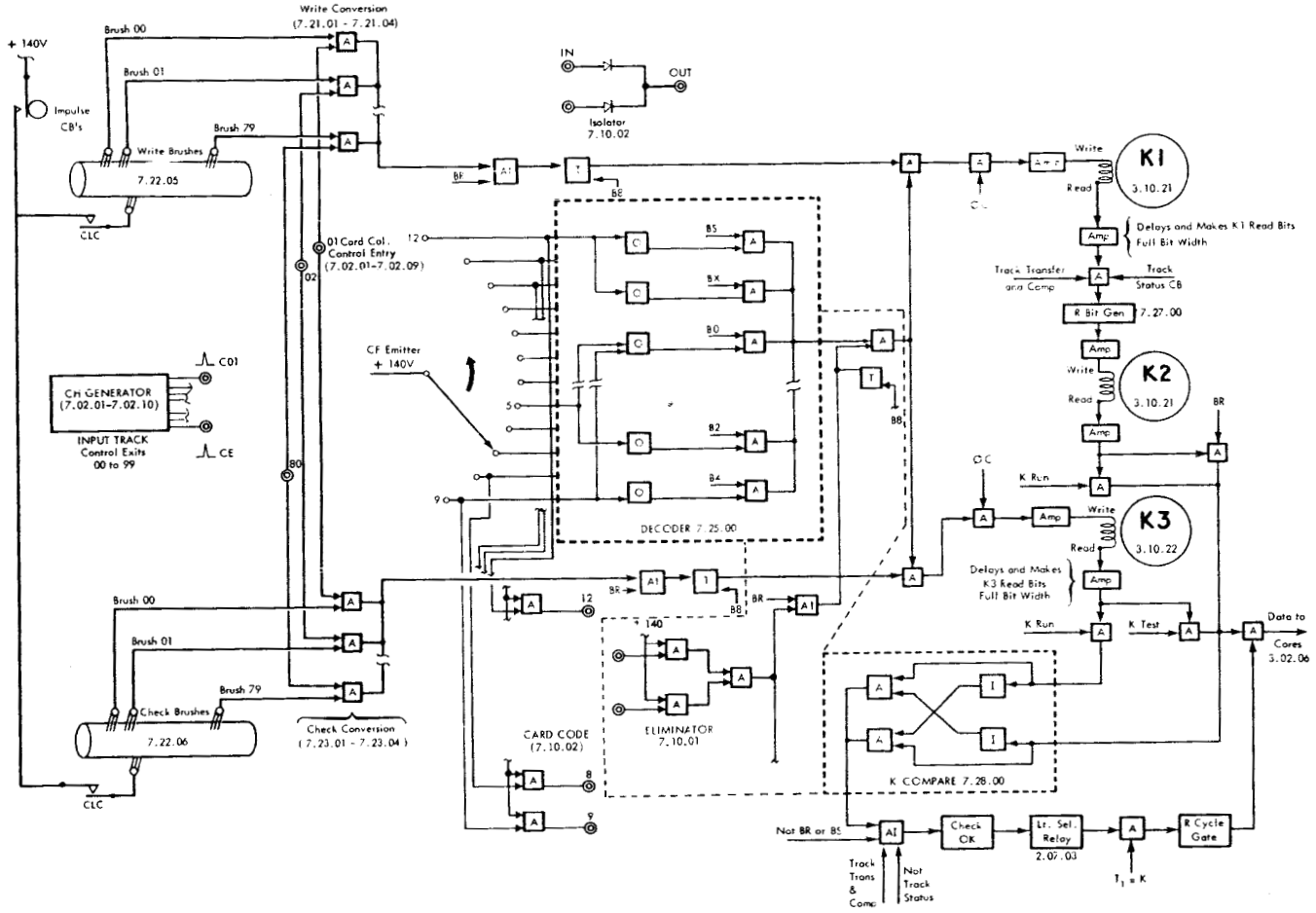


Figure 107. Input Data Rearrangement and Check Logic

Eliminators

An eliminator permits any card code to be eliminated from any character which is to be written on the input track. The card code to be eliminated is determined by one input to an eliminator. This input comes from one of the card code hubs. The card column from which the code is to be eliminated is determined by the other input to the eliminator. This input comes from a card column control entry hub. A card code is removed from a character by eliminating the decoder output for the card code at the time that the character is to be written.

OBJECTIVE:

Eliminate decoder output (7.10.01).

The elimination occurs at the AK 7P9a on 7.10.01. 7P9a-5 is always high unless 7S8-3 is plate pulled. Plate-pulling is done at BR of any character when there is a coinciding input to both hubs of any eliminator.

Analysis Selectors

The prerequisite to this feature is Input Data Rearrangement. Analysis selectors are used to analyze a character for card code content as it is being written on K track. Only data that is being written on K track can be analyzed. Analysis selector PU hubs are in the orange section of the 305 control panel. They may be wired from other hubs in the orange section only. Both PU hubs must be impulsed at the same time to pick up a selector. One PU hub must be wired from a card code hub. The other must be wired from a CARD COLUMN CONTROL ENTRY.

Once a selector is energized, it remains energized until 335° of the next card feed cycle through FCB-31 on 7.10.03. The analysis selector test point hubs are on the 305 control panel. These hubs may be tested with program exits only between a $T_1 = K$ instruction and the next card feed instruction. Testing an analyzer must wait until a $T_1 = K$ instruction is permissable, i.e., reader ready, so that an analyzer is not tested during a card feed cycle. The $T_1 = K$, card feed and analyzer testing may occur on the same instruction.

370 Printer

Mechanical Principles

The sole purpose of the 370 is to serve as an output printer for the RAMAC; thus, all of the mechanisms in this unit are related either to the positioning of forms or to the selection and printing of characters in the proper positions on these forms.

Print Element

Figure 108 shows the relationship of the form to the print element, ribbon, and hammer. These comprise the essential elements for printing.

Only one print element and one hammer are needed because the 370 prints serially. The print element, or print stick, is a hollow aluminum tube with 8 sides and 7 divisions lengthwise. A particular character is engraved in each of the 7 divisions on each side. With the various combinations of fixed increments of horizontal and/or rotational movement, any one of the 56 characters may be placed in the printing position, opposite the hammer.

The positioning of the print stick to print a character is controlled by the identity of the bits within a character on the output track. Each bit value is translated into a number of units of horizontal or rotary motion of the print stick. The table in the lower left corner of Figure 108 shows that bits X, 0, and 2 impart rotary motion of 4, 2, and 1 units, respectively. Bit 1, 4, and 8 impart horizontal motion of 1, 2, and 4 units, respectively. The table in the lower right corner shows the combinations of horizontal and rotary motion necessary to position the print stick for the printing of any character.

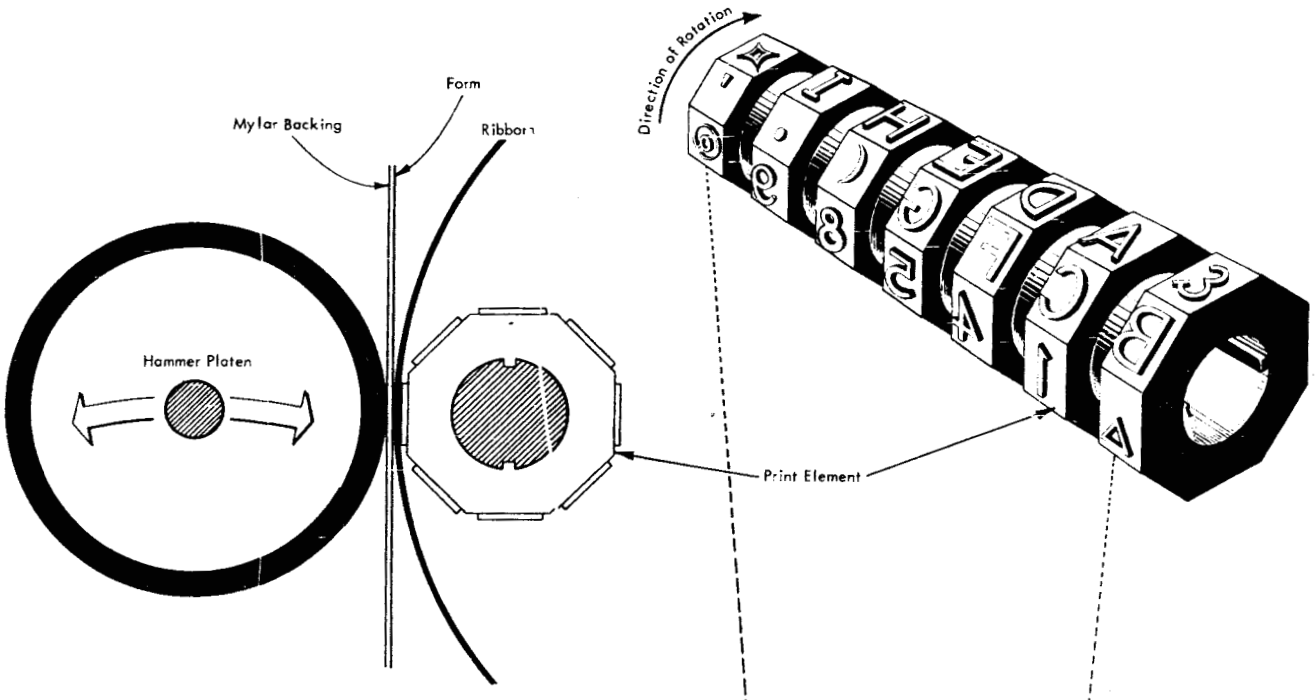
Figure 109 shows a top view of the printing mechanism. The print stick has two internal keys, which ride in splines on the print element shaft. It is free to slide horizontally on the shaft, but rotation of the shaft causes rotation of the print stick also.

The left end of the print element shaft is geared to a pulley, which is operated by the rotary control tape. A block, welded to the tape, fits into a slot of the pulley to provide a positive action. Tension is applied to one end of the tape by a spring operated lever. Rotary motion is imparted to the print stick by pulling the rotary control tape a fixed distance in increments of 1 to 7 units. Exact rotary alignment of the print stick at print time is accomplished by the aligner, which is spring operated and cam returned.

The ends of the print stick are held between two plates, which are fastened together by three rods. This is called the basket. The print stick is free to rotate within the basket, but moves horizontally along the print element shaft as the horizontal position of the basket is moved. The horizontal position of the basket is under control of the horizontal control tape and the horizontal return spring. Horizontal motion is imparted to the print stick by pulling the horizontal control tape a fixed amount in increments of 1 to 6 units. Exact horizontal alignment of the print stick, at print time, is obtained by a cam operated aligner or comb. The seven-tooth aligner is spring driven against the basket at print time. The end plate of the basket is held between the teeth of the aligner.

In addition to the horizontal and rotary motion of the print stick, the complete print carriage and hammer carriage move from left to right past successive printing positions. These carriages return to their extreme left positions between the printing of lines. In order to keep the print control tapes taut without stretching or breaking them, and to prevent imparting false horizontal or rotary motion to the print stick, these tapes are looped over pulleys of the half speed carriage instead of coming directly from the print set-up unit. The half speed carriage is so named because it moves at half the speed of the print and hammer carriages. The methods of driving these mechanisms will be explained later.

The aligner mechanism and ribbon feed are operated through a gear which rides on the aligner and ribbon drive shaft. The gear has an internal key which rides in a groove of the shaft. The gear is free to slide along the shaft, but must turn with it. The aligner and ribbon drive shaft turns at 1500 RPM, but the gear ratio causes the aligner mechanisms to operate at twice that speed, thus permitting a printing speed of 3000 characters per minute.



PRINT ELEMENT CODE AND MOTION VALUES

Binary Code	Motion Values	
X	+ 4	Rotary
0	+ 2	
2	+ 1	
1	+ 1	Horizontal
4	+ 2	
8	+ 4	

@	9	8	5	4	1	Home Δ		
11	#	10	7	6	3	2	1 R	2
%	Z	Y	V	U	/	Zero 0	2 R	0
Degree	,	+	X	W	T	S	2-1 R	0-2
*	R	Q	N	M	J	—	4 R	X
"	$	)	P	O	L	K	4-1 R	X-2
¤	!	H	E	D	A	&	4-2 R	0-X
'	.	(	G	F	C	B	4-2-1R	0X-2
4 2 H	4 1 H	4 H	2 1 H	2 H	1 H	PRINT MAGNETS		
4 8	1 8	8	1 4	4	1	BINARY CODE		

Shaded Characters Are Not Obtainable With Valid Data Coding

Figure 108. Print Element Positioning

Print Setup Unit

Bit values are translated from electrical impulses into increments of motion to the control tapes within the print setup unit. Figure 110 illustrates the method by which motion is imparted to the horizontal and rotary control tapes, and from the tapes to the print stick. One end of both the horizontal setup tape and the rotary setup tape is attached to the setup unit frame. Each of the setup tapes is looped over its three setup pulleys and is linked with its corresponding control tape. The print stick may be caused to move to the left by moving the upper or lower horizontal setup pulley to the right or by moving the middle pulley to the left. Likewise, rotary motion may be imparted to

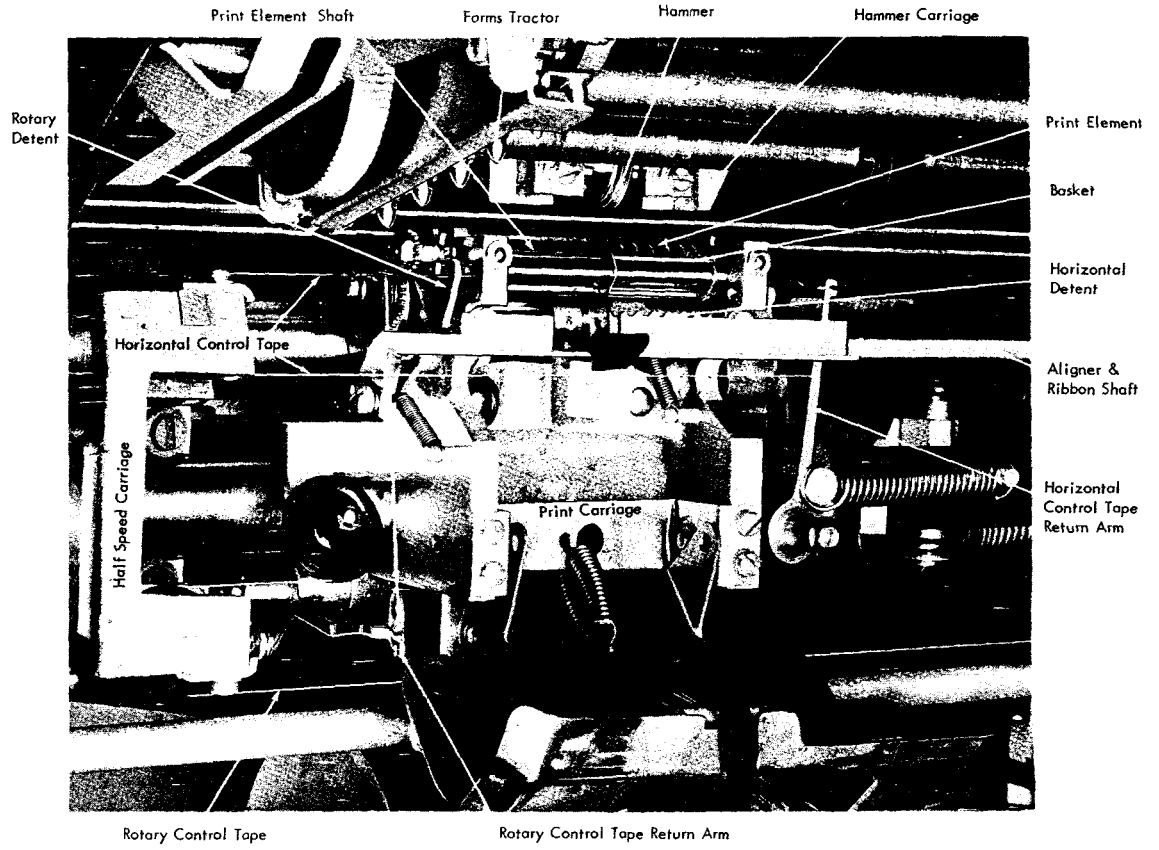


Figure 109. Print Assembly

the print stick by moving the upper or lower rotary setup pulley to the right or the middle pulley to the left.

Figure 111 illustrates schematically how one of the two groups of setup pulleys may be operated to provide the desired increments of motion to its setup tape. The directions of motion indicated by this figure are applicable to a rear view of the mechanism. As the setup bail moves to the right, it will engage with any setup pawl which has been raised into its path. It can be seen that two of the setup pulleys would move to the left and one would move to the right as the result of inter-action between its pawl and the bail. The increment of motion resulting from the operation of any one of these setup pulleys is determined by the distance from the pivot point of the arm to the pivot of the pulley.

Figure 112 shows an exploded view of one position of the print setup unit. Each setup position includes two setup pawls and a repeat pawl. Each of the setup bails has seven teeth, one for operating a setup pawl at each position of the print setup unit. Although the lower bail is beneath the upper bail, its teeth are shorter so that the operating edges of the two sets of teeth are at the same level. The teeth of the lower bail operate between the teeth of the upper bail so that each bail has a tooth directly above a setup pawl at each position. Each of the setup bails oscillates left and right at a speed of 1500 cycles per minute, but since they operate 180° out of phase, the effective speed of operation is 3000 cycles per minute.

If the setup magnet is energized, its armature is attracted to permit the latch arm to follow into the low dwell of the reset cam. The operating ear on the right end of the latch arm operates against the lower side of both setup pawls to move them upward.

One of the bails will be in a retracted position at the time of the impulse to the magnet, but it will then move to the left and engage its pawl. The setup pawl will be moved to the left by the bail until it operates against the motion pulley stud, moving to the left also. The upper end of the motion pulley arm will be moved to the left and the setup pulley will move to the right, thus imparting motion to the setup tape, the control tape, and to the print stick.

The reset cam turns at 1500 RPM. However, it has two high lobes and thus operates 3000 times per minute to reset the latch arm onto the setup magnet armature, if it has been unlatched.

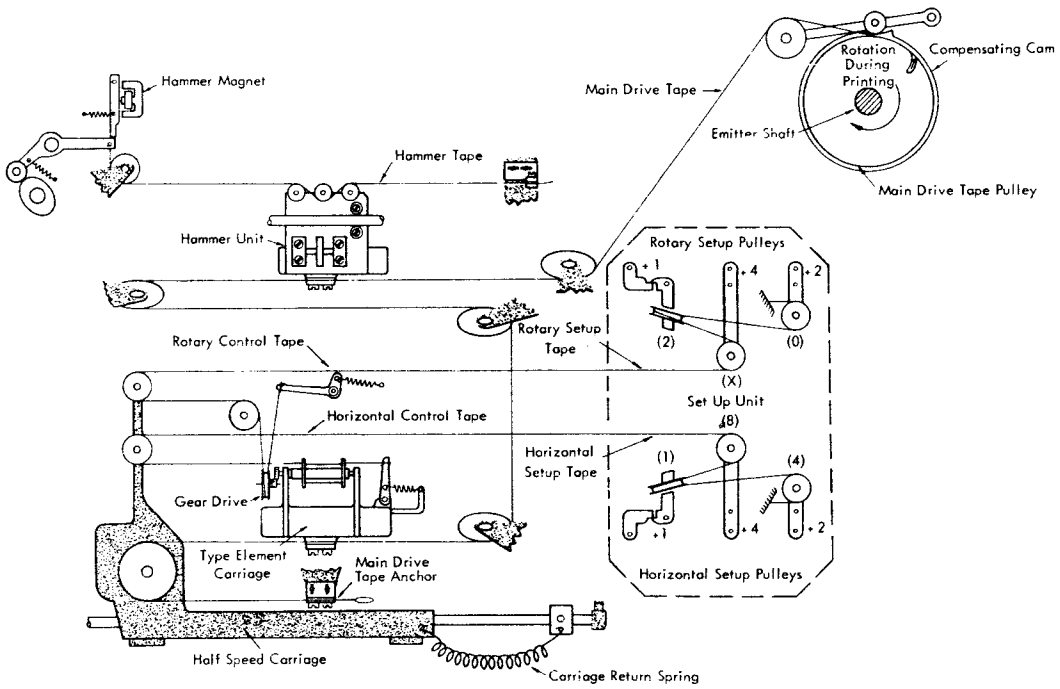


Figure 110. Schematic of 370 Printing Mechanics

If a second consecutive impulse is received by the setup magnet, one of the setup pawls and the repeat pawl will already be in an advanced position. The operating ear of the latch arm will move the retracted pawl upward into the path of the retracted bail, and it will also cause the repeat pawl to move upward and latch onto the repeat pawl latch block. This will cause the setup pulley to remain in its operated position as one bail is retracted and the other advanced. The advancing bail will give slight additional movement

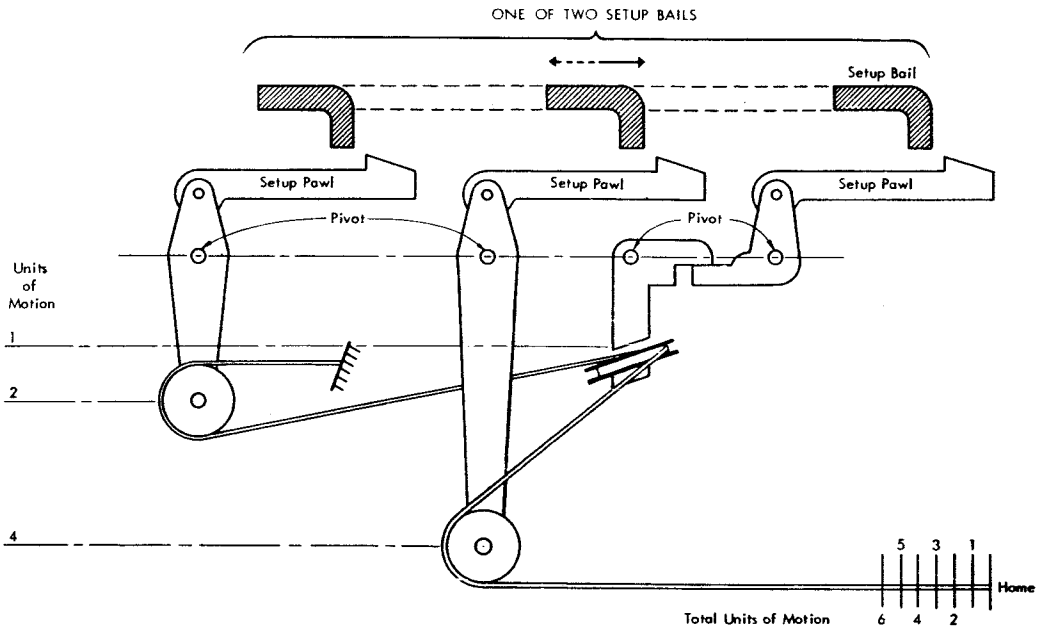


Figure 111. Functional Operation of Motion Pulleys

to the repeat pawl as it reaches the setup position, thereby allowing the repeat pawl to be unlatched from the repeat pawl latch block.

In order to permit a parity check of characters which are set up for printing, each setup position operates a pair of setup contacts as shown in Figure 112. The BR setup position does not operate a setup pulley, but does operate its pair of setup contacts.

Since there is only one latch to operate two setup pawls within each position of the print setup unit, the latch must be reset onto the setup magnet armature before printing time. There also must be some arrangement to prevent the setup pawl from dropping off the bail when the latch is reset. This is the function of the locking bar. As a pawl, which has been operated by the latch, is moved by the bail into its setup position, the step on the underside of the pawl reaches a position above the locking bar before the latch is reset. The locking bar will then prevent the pawl from dropping off of the bail until after the bail and pawl are retracted (see Figure 112).

If, due to some malfunction, the latch should fail to hold the pawl high enough to clear the locking bar, the locking bar would be pivoted against its spring tension. This arrangement is to prevent breakage in the event of a mechanical failure.

Figure 113 shows a top view of the print setup unit mounted in the 370.

Hammer Unit

A rear view of the hammer and its associated mechanism is shown on Figure 114. The hammer drive shaft turns at 1500 RPM. However, the gear ratio results in 3000 RPM operation of the hammer cam shaft. This permits the hammer to be fired at the same frequency, as the print stick is positioned for printing.

The hammer platen, hammer arm, hammer cam shaft, hammer latch, unlatching lever, tension adjustment mechanism, and the three trip tape pulleys just to the rear of the unlatching mechanism are all parts of the hammer carriage. The inner surface of the 1500 RPM gear which drives the hammer cam shaft has a key which rides in a groove of the hammer drive shaft. This gear, being a part of the hammer carriage, is free to move along the hammer drive shaft, but turns with it.

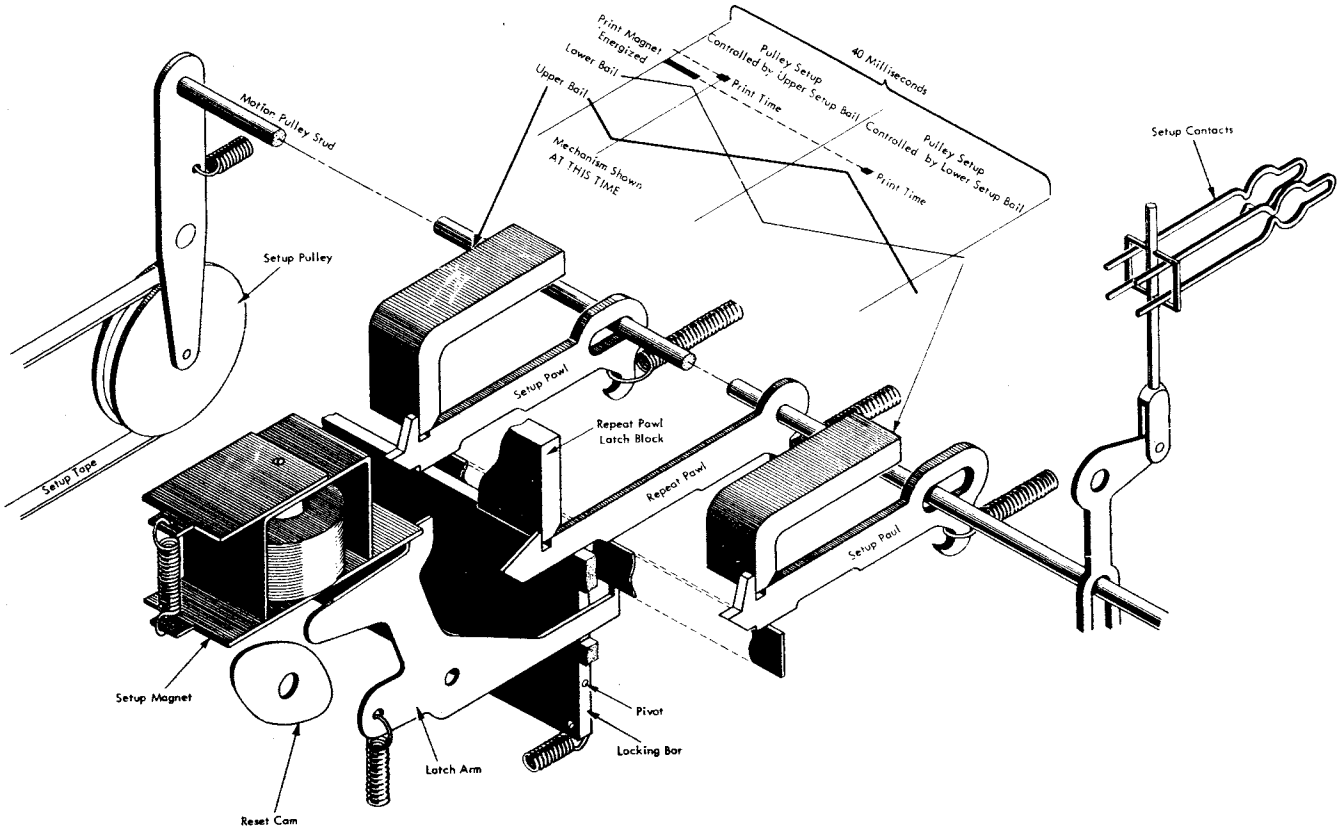


Figure 112. Exploded View of One Bit Position of Print Setup Unit

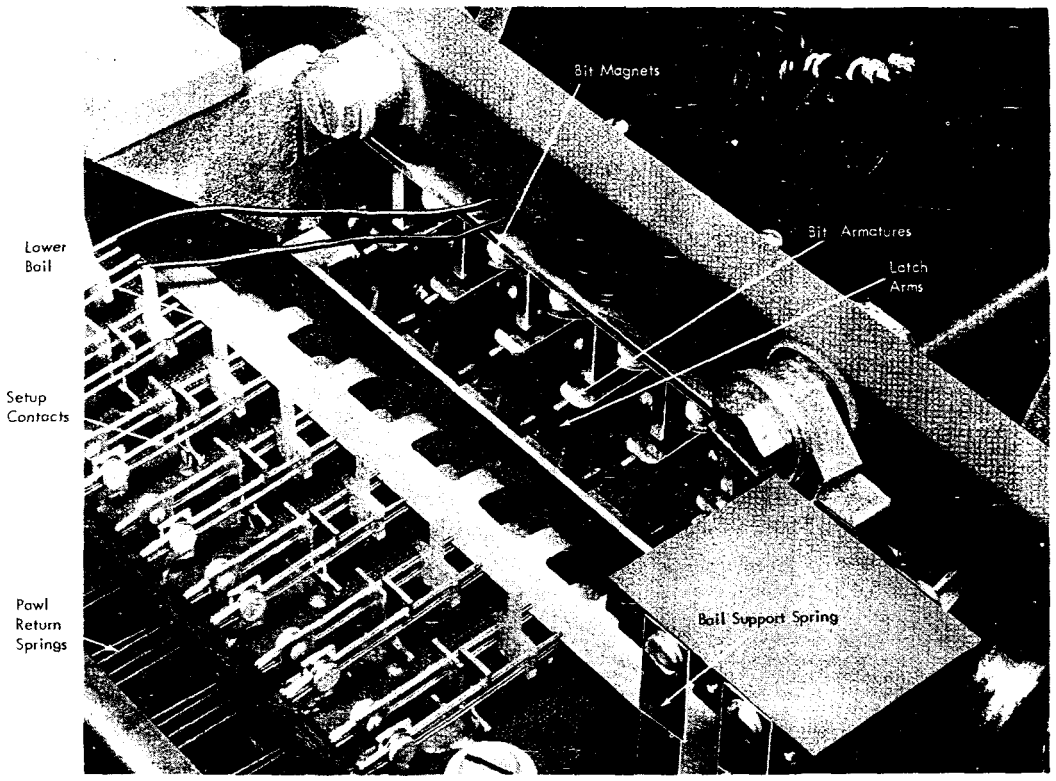


Figure 113. Print Setup Unit

In the normal position, the hammer arm is held clear of the hammer cam by the hammer latch. The 370 must anticipate when a character is to be printed and must energize the hammer magnet while the hammer latch cam is at its high dwell. The hammer latch cam follower will then follow the cam to its low dwell, causing the trip tape to be pulled. The tightening of the trip tape causes the unlatching lever pulley to move downward, which causes the left end of the unlatching lever to move upward. This lifts the hammer latch clear of the hammer cam follower, which is then free to follower the hammer cam down the gradual slope to its low dwell. As the hammer cam continues to turn, the sharp rise as it approaches its high dwell imparts sufficient momentum to the hammer arm to throw the hammer against the paper, ribbon, and print stick.

If the hammer magnet is not energized again for printing the next character, the hammer latch cam follower will be relatched by the hammer magnet armature and the hammer latch and unlatching lever will be returned to their normal position by spring tension. The hammer latch then holds the hammer cam follower clear of the hammer cam. The rebound lever insures against double impression resulting from bounce of the hammer.

As the hammer cam follower is operated against the tension of its return spring when it is thrown forward to print a character, the printing impact may be adjusted by positioning the tension adjusting lever to alter the tension of the spring. This permits adjusting the hammer impact for printing on multipart forms.

Main Tape Drive

The preceding discussion has shown how the print stick is positioned for printing the various characters and how the hammer is fired. It has also been stated that both the print carriage and the hammer carriage must move from left to right past the successive printing positions as a line is printed, and that they must move back to their home position after each line. As the 370 prints a maximum of 80 characters at ten characters per inch on one line, total movement of the carriage is slightly more than 8 inches.

Figure 110 illustrates the manner in which the hammer carriage, print carriage, and half speed carriage are driven. The hammer and print carriages are attached to the main drive tape and are pulled to the right at tape speed when the tape drive pulley is caused to rotate clockwise. The half speed carriage

moves at half tape speed because of the block and tackle arrangement.

The tape drive plley is mounted on the emitter shaft, which will be explained later. The emitter shaft is positively driven in its clockwise direction, but is returned by the carriage return spring action through the half speed carriage and the main drive tape.

Figure 115 provides a front view showing the print carriage, half speed carriage, part of the main drive tape, and the carriage return spring.

Emitters

As the print and hammer carriages are moved from left to right across the form during the printing of a line, individual characters are read from the output track to impulse the bit magnets within the print set-up unit. Wiring on the 370 control panel determines the character position of the output track from which a character will be selected for printing in each of the 80 print positions. The machine must have some means of determining, electrically, when the print carriage reaches each printing position.

Figure 110 shows that there is a definite relationship at all times between the horizontal position of the print carriage and the angular position of the emitter shaft, to which the tape drive pulley is attached. This provides a means of indicating electrically when printing positions are reached.

Figure 116 shows two emitter plates positioned to be wiped by brushes mounted on the emitter shaft. Each emitter plate has 80 spots, 40 on each side. Each wiper assembly includes two sets of brushes, one set to wipe the spots representing print positions 1 through 40 located on one side of the emitter plate, and a second set to wipe the spots representing print positions 41 through 80 located on the opposite side of the emitter plate.

The emitter closest to the front of the machine is the print position exit emitter, and that closest to the rear is the print control exit emitter. The actual function served by these two emitters will be explained later.

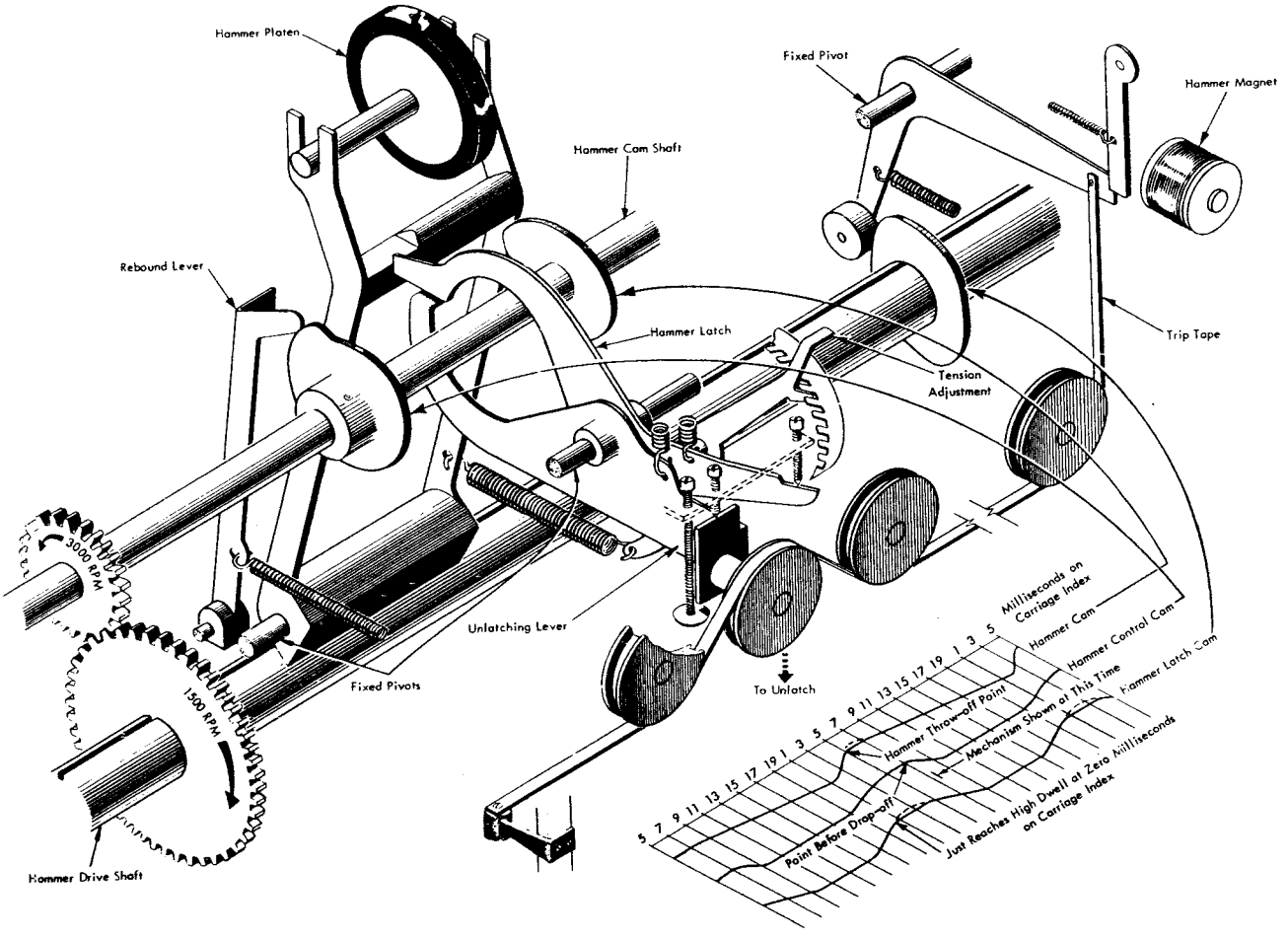


Figure 114. Hammer Carriage

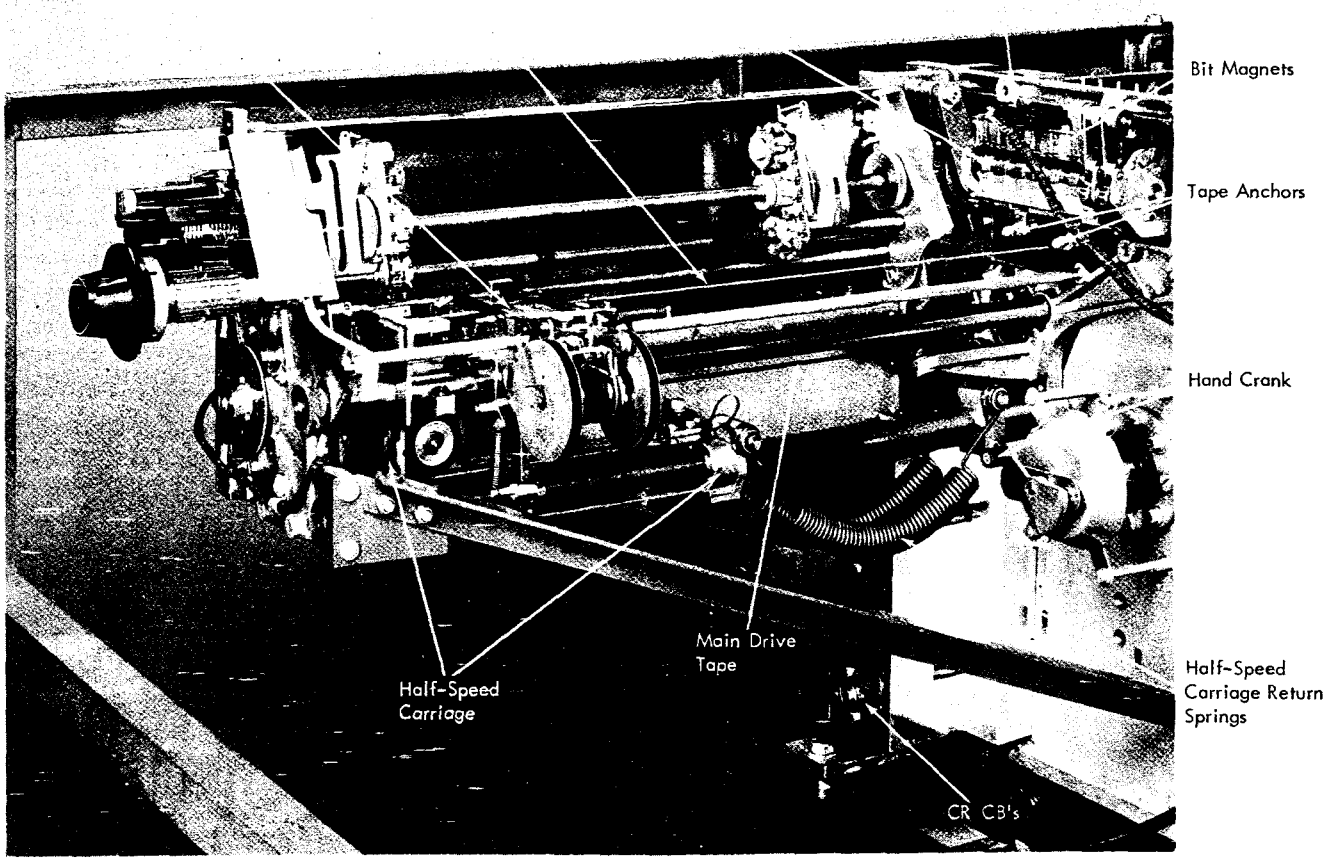


Figure 115. Carriage and Print Mechanism

Three circuit breakers, called E1, E2, and E3, are also mounted on the emitter shaft. Two of these are closed when the print carriage is in its home position, and the other closed when print position 80 has been passed.

After the 370 receives a signal to cause it to print a line, the driving mechanism for the emitter shaft is engaged. This causes the shaft to turn through a part of a revolution, pulling the print and hammer carriages past the successive printing positions, and causing the emitter brushes to wipe the emitter spots. When the last position to be printed has been passed, the emitter shaft is disengaged from its driving mechanism, allowing the carriage return spring to force the carriage and the emitter shaft back to their home positions. The actual mechanism which drives the emitter shaft will be discussed later.

Program Shaft

The 370 control panel permits a very flexible arrangement of data in printing each line. The format may be varied from line to line under control of code characters in certain character positions of the output track. In order to accomplish the selection of the desired format for each line, some time must be allowed between the signal to initiate a printing operation and for the engagement of the emitter shaft drive. A set of timed impulses must be available during this time for the purpose of testing code characters and picking selectors. These impulses are provided by the program shaft circuit breakers.

When the 305 program directs the 370 to print, the first result is to energize the program shaft clutch magnet (Figure 117). This permits the program shaft to turn through one 320 *ms* cycle, at the end of which the clutch latches. The program shaft operates the cam contacts that can be seen mounted on the upper right corner of Figure 116. The emitter shaft engages after 130 *ms* of the program shaft cycle.

Program Shaft Clutch

The program shaft clutch (Figure 117) contains the following basic elements: a magnet and armature, a

latching mechanism, a clutch pawl, an eight-tooth ratchet, and a restoring device. The clutch drive gear and the clutch ratchet are continuously running and ride free on the program shaft.

When the clutch magnet attracts the armature, the latch is rotated in a clockwise direction by spring tension, thus releasing the pawl. The pawl then pivots in a counterclockwise direction and engages in a tooth of the ratchet. The pawl and pawl arm then turn with the continuously running ratchet. Since the clutch pawl arm is pinned to the program shaft, the program shaft CB's are operated through one cycle.

The clutching mechanism is restored to normal during the program shaft cycle in the following manner. The restoring cam operates against the roller to pivot the knockoff arm in a counterclockwise direction. The knockoff arm pulls the adjusting screw plate to the right by spring tension. Since the adjusting screw plate is attached by two screws to the latch arm, the latch arm is pivoted in a counterclockwise direction to relatch on the armature. As the upper end of the latch arm moves to the left, it operates the knockoff bell crank, which knocks the armature free from the magnet cores.

Emitter Shaft Drive

The emitter shaft drive is engaged directly as a result of the operation of the program shaft clutch. The emitter shaft starts turning when the program shaft has turned for 120 *ms* of its 320 *ms* cycle. The emitter shaft drive may be explained with reference to Figures 118 and 119.

A sector gear is attached to the rear end of the emitter shaft; it is driven by the sector drive gear. The sector drive gear is continuously running, but it normally does not mesh with the sector gear.

In order for drive to be transmitted to the emitter shaft, the sector drive gear must slide approximately ¼-inch on its shaft, toward the front of the machine, to mesh with the sector gear. This is accomplished under control of the face cam mounted on the rear end of the program shaft.

As the program shaft turns through its cycle, the face cam follower rides from a high dwell to a low dwell. A strong compression spring forces the face cam follower and the cam follower operating plate toward the rear of the machine. The cam follower operating plate causes the sector drive gear operating lever to pivot so that the sector drive gear is moved toward

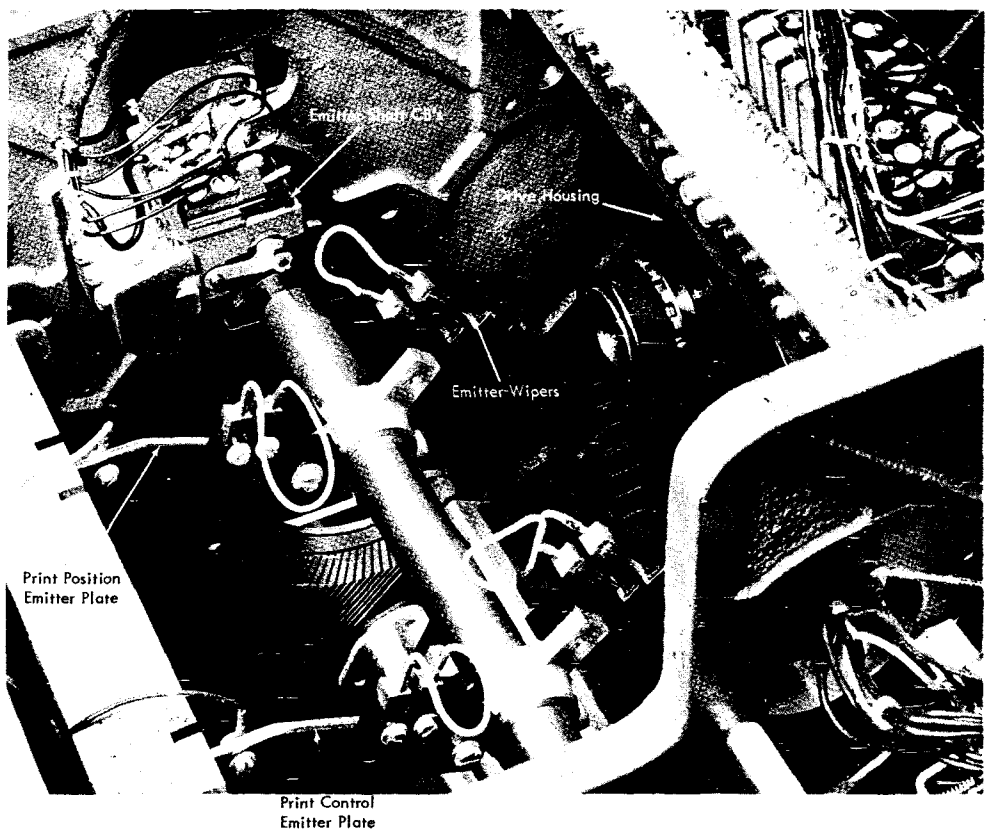


Figure 116. Print Position Exit and Print Control Exit Emitters

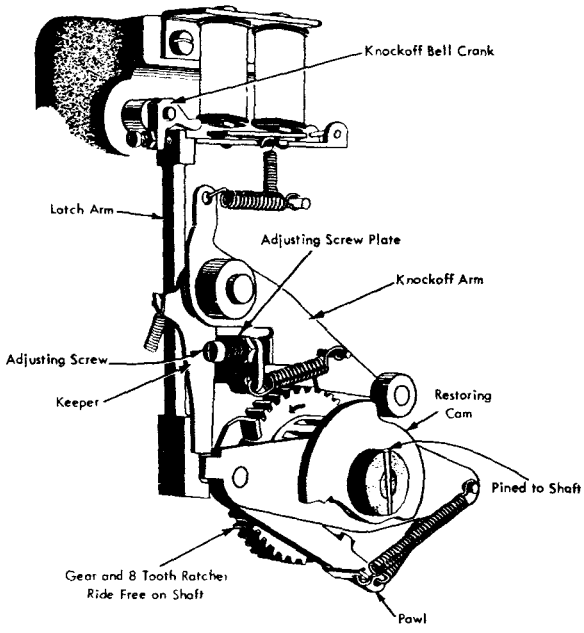


Figure 117. Program Shaft Clutch

the front of the machine to mesh with the sector gear. The pivoting of the sector drive gear operating lever causes it to be latched in its operated position by the line stop magnet armature. This keeps the sector drive gear meshed with the sector gear even after the face cam follower has returned to its high dwell.

When printing on a particular line is complete, the line stop magnet must be operated to unlatch the sector drive gear operating lever and permit the sector drive gear to de-mesh. To prevent any possibility of overdriving the mechanisms operated by the emitter shaft, the sector gear has only enough teeth to be driven through a safe arc. In addition, a knockoff stud on the side of the sector gear will operate a lever to unlatch the line stop magnet mechanically if there should be electrical failure. This may be seen in Figure 119.

Viewed from the rear of the machine, as in Figure 119, the emitter shaft, sector gear and carriage return control cam turn counterclockwise during the printing of a line. As they turn, the follower for the carriage return control cam rides to a lower dwell, permitting the cam follower spring to lift the dash pot plunger. When the line stop magnet is energized to de-mesh the sector drive gear, the emitter shaft is pulled clockwise by the main drive tape back to its home position.

The follower for the carriage control cam returns to its high dwell, pushing the dash pot plunger downward. The dash pot thus absorbs the shock as the emitter shaft and the print, hammer, and half speed carriages reach their home position.

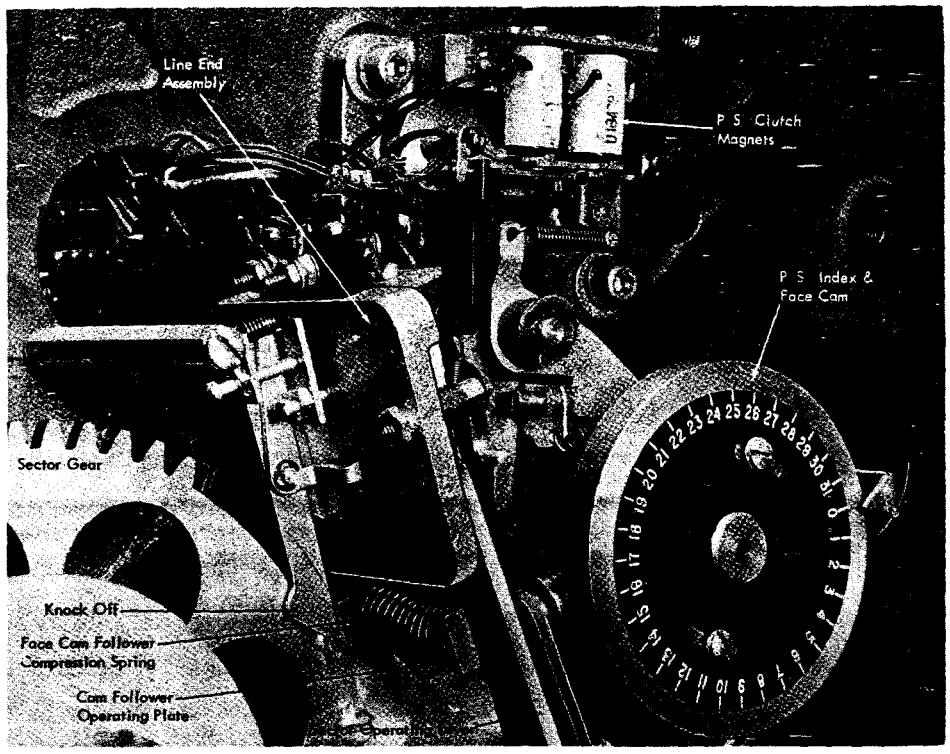


Figure 118. Face Cam, Cam Follower, and Sector Operating Lever

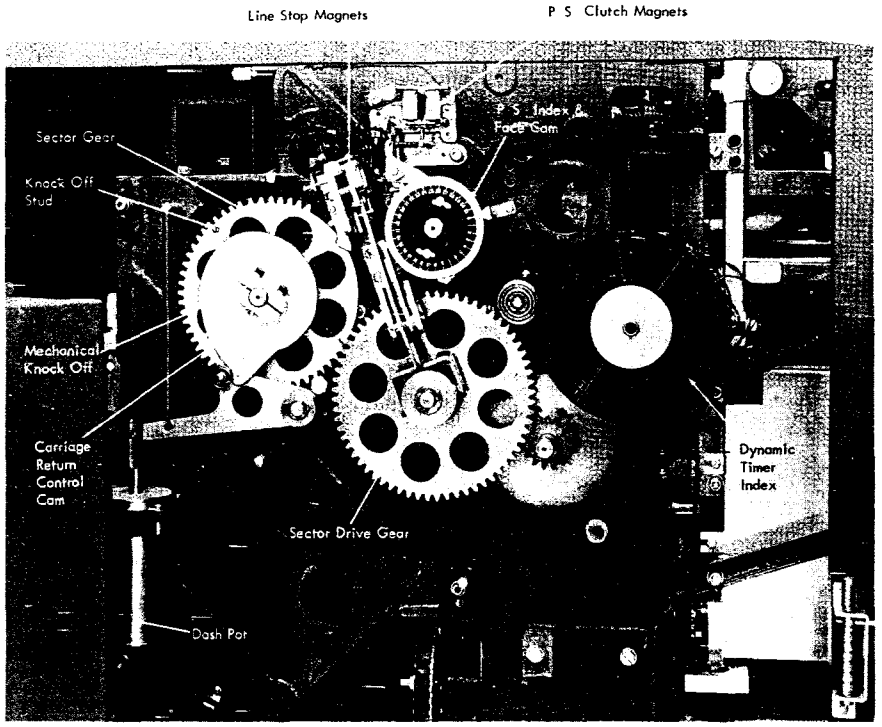


Figure 119. Printer Drive and Clutch Mechanism

Mechanical Drive

Figure 120 shows how mechanical power is transmitted from the motor to the various units within the printer.

The following continuously running mechanisms operate at 1500 RPM: the CRCB's, the hammer drive shaft, the aligner and ribbon drive shaft, and the print setup unit cams. All of these units are involved in the printing of characters. Even though all these units operate at 1500 RPM, 3000 characters per minute (within a line) are printed. This is accomplished through the use of double cams and 1 to 2 gear ratios.

All of the moving parts within the 370 which are not continuously running are under either direct or indirect control of the program shaft clutch. All of the non-continuously running parts, except the program shaft itself, are driven by the sector drive gear and returned by the carriage return spring operating against the half-speed carriage.

Timing Relationships

All continuously running mechanisms are timed to the CRCB index which is mounted on the hammer drive shaft. This index (Figure 121) turns at 1500 RPM; hence, it requires 40 *ms* per revolution. It is divided into two halves, A and B, each of which is graduated in milliseconds, 0 to 20.

The program shaft index (Figure 119) is attached to the face cam, which is mounted on the rear of the program shaft. As this index requires 320 *ms* for a cycle, it is graduated in increments of 10 *ms*, 0-32. The index is at zero when the program shaft clutch is latched. The program shaft clutch itself may engage or latch only when the CRCB index is at A10.

The sector drive gear meshes with the sector gear to set the emitter shaft and the hammer, print, and half speed carriages in motion when the program shaft index indicates 13 (130 *ms*). The timing of the emitter spots must then have a definite relationship to the CRCB index.

These timing relationships are shown on system diagram 0.09.50 and Figure 122.

Form Feeding Mechanism

The 370 Printer employs a forms tractor mechanism to feed forms by lifting at the marginal pin holes. This is the only provision for feeding, therefore forms must have marginal pin holes. The tractor mechanism is driven from the shaft operated by the form feed ratchet shown in Figure 121.

Units of single, double, and triple spaces are obtained by repetitive single spaces. Skipping also uses the repetitive single space method.

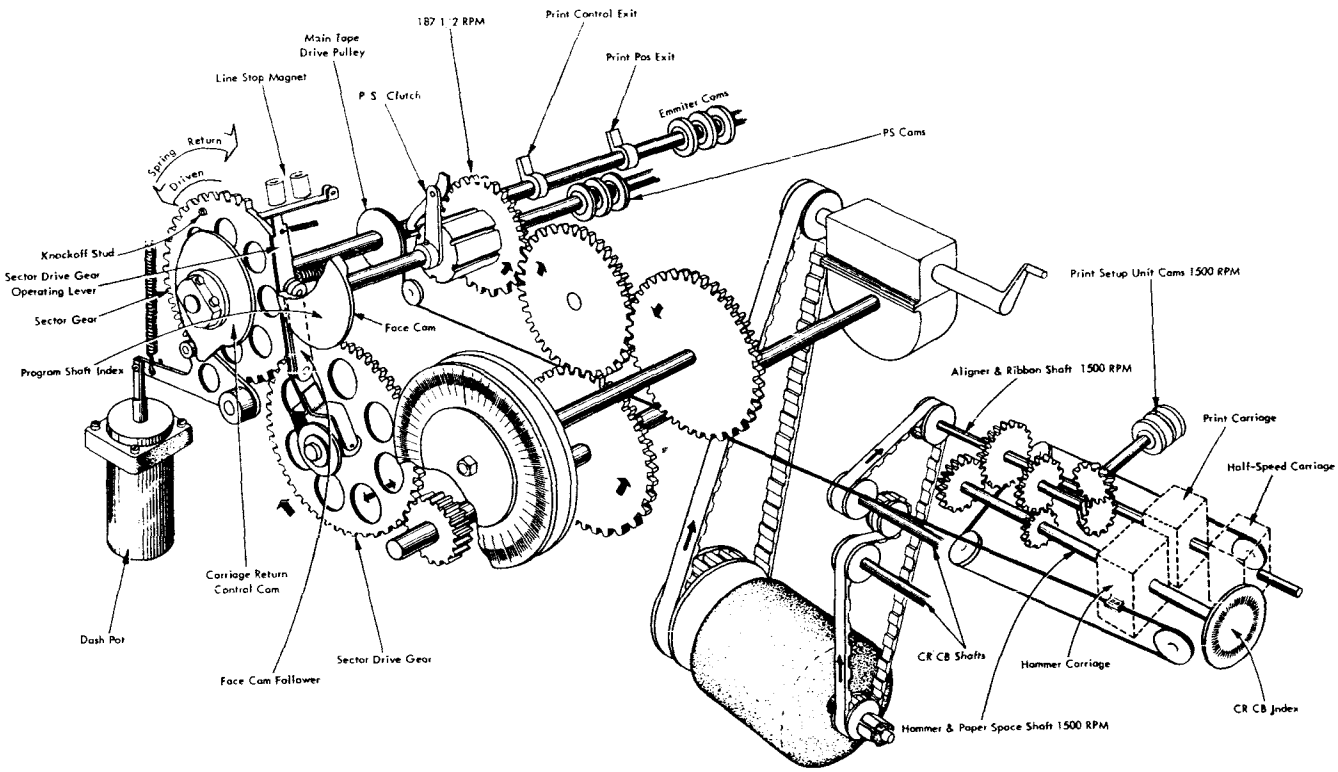


Figure 120. 370 Mechanical Drive

Line space drive is obtained through two cams on the left end of the continuously running hammer drive shaft. The function of the line space drive is to give an oscillating motion to the line space pawl. The pawl is normally held clear of the form feed ratchet by a disengaging arm. Impulsing the line space magnet allows the disengaging arm to cam forward and drop the line space pawl into the form feed ratchet by spring tension, as the pawl is at its maximum forward position. The pawl and ratchet are then pulled back an amount equal to one space by the line space drive cam, after which the disengaging arm lifts the drive pawl clear of the ratchet. The ratchet is held in position by a spring loaded detent roller.

On repetitive spacing, the line space disengaging arm is not relatched, but allows the drive pawl to drop into the next rachet tooth for another space.

The form feed employs a 12 channel tape to control the positioning of forms for skipping and overflow. Five of these channels, numbers 7 through 11, are inoperative on a standard machine. The tape channels are read by star wheel contacts (Figure 121).

Selection Circuits

The only function of the 370 is to serve as a document printer under control of the 305 program. An automatic print operation is initiated by an impulse into the print hub on the 305 control panel. As a result of this print signal, the program shaft clutch is operated to provide a program shaft cycle. At 13 of the PS index the sector drive gear starts to drive the emitter shaft, which causes the operation of the print and hammer carriages. As the carriages move across the form and the print position exit emitter spots are wiped, characters for printing are selected from the output track by wiring on the 370 control panel. The 370 checks the parity count of each character printed, as it is read from S track. It also makes a parity check of the setup magnets energized for each character printed. The controlling circuits for each function of the 370 are described below.

Print Ready

Before a 370 can start to print a line, it must be in a ready status. The ready light on indicates that the 370 main line switch is on, forms are in the printer, and that S track is not interlocked. S track becomes interlocked whenever the printer is printing data, after a setup error has occurred, or after an S track parity error is detected.

The ready light on 7.74.12 glows whenever R1 and R2 are up. R1H is picked on 7.74.11 through the start key, R40-3 N/O, and R41-2 N/O. R40 is the print

setup check relay. Its control is explained under "Setup Check." Control of R41, the track check relay, is explained under "Track Check." R2H is picked through emitter cam E1 on 7.74.11. E1 indicates that the carriage is in the home position. The names of the other points in the pick of R2H indicate other conditions that prevent a ready condition.

Printer Not Ready

Printer not ready is a signal to the process unit that the printer is unable to start a print operation or accept new data on S track. This signal exists whenever the printer is printing, or after a setup error or track check error have occurred.

OBJECTIVES:

1. Printer not ready line high (2.07.03).
2. Prevent $T_2 = S$ program (3.02.08).
3. Prevent print start (7.74.11).

The printer not ready line is high whenever the print select relay is up. It is latch picked to begin a print operation. It is latch tripped after the last character in the line has been printed. However, R1-4 N/O on 7.74.12 prevents tripping if a setup error or a track check error occurs during the printing of a line.

To prevent a $T_2 = S$ transfer the not W cycle gate is developed from printer not ready and T = S on 3.02.08.

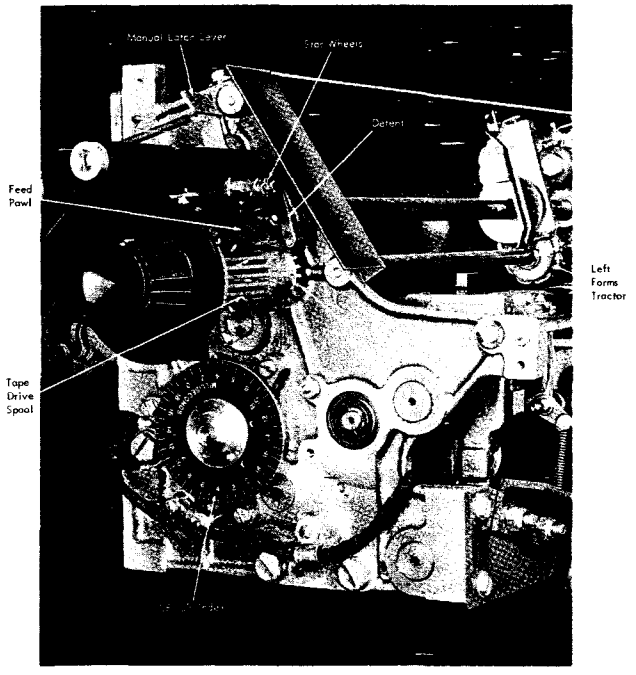


Figure 121. CRCB Index and Carriage Tape Assembly

Printer start is prevented by R2-1 N/O on 7.74.11. R3 cannot pick. By referring to Figure 122 you can see that R2 drops early in a print operation.

Printer Start

Energizing the PS clutch magnet causes the print stick to start moving across the line to be printed. The PS clutch magnet is picked whenever the printer is ready and a PROGRAM EXIT impulse is received at the print hubs. Figure 122 shows the relays needed to pick the PS clutch.

Line End

The movement of the carriage is terminated by impulsing the line stop magnet after all characters for a particular line have been printed. A line end operation is started automatically by emitter shaft CB E3 after character 80 is printed. If less than 80 characters are to be printed, printer operating time can be saved by wiring from the print control exit hub after the last character to be printed into the line end hub. However, *line end must not be impulsed before print control exit 10.* This exception allows sufficient time for the carriage to return home before the program shaft clutch is reenergized, when the 305 is interlocked with $T_2 = S$. The cut of the program shaft face cam will not allow the carriage to return before print position 10 time.

The line end operation also removes the printer interlock and re-establishes the printer ready condition. Figure 122 shows a sequence chart of line end operations.

OBJECTIVES:

1. Energize the line stop magnet (7.74.42).
2. Remove printer interlock (2.07.03).
3. Printer ready (7.74.11).

The line stop magnet is energized through CR13 after R5 is picked. The pick of R5 is initiated on 7.74.42 by E3 or the line end hub.

Printer interlock removal is accomplished by latch tripping the print select relay. The printer not ready line goes low when the print select relay is tripped. The print select relay is tripped through R5-2 N/C, R14-2 N/O on 7.74.12 from CR-17.

Printer ready indicates that the printer is ready to begin printing a new line. It is indicated when R2H is picked through E1 on 7.74.11. If a long line is printed R2 is picked when position 20 is passed on the carriage return. This is the time when E1 makes. In the example of Figure 122, E2 never opened; so R2H picked when CR19 made after R14 was tripped.

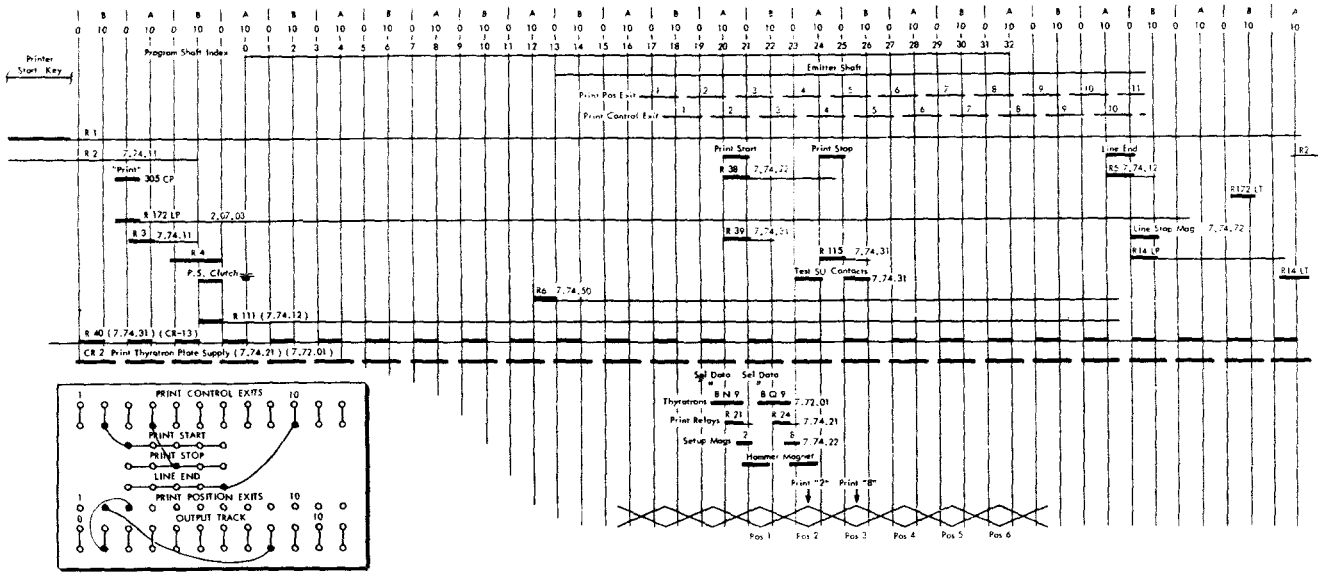


Figure 122. Printer Operation

Print Start

Format control of a printed line is accomplished by wiring the print start and print stop hubs. The COLUMN CONTROL EXIT of the first position of each field to be printed should be wired to PRINT START. This allows the hammer to be fired, and a set up check to be made. Figure 122 shows the sequential operation of print start.

OBJECTIVES:

1. Fire hammer (7.74.22).
2. Setup check (7.74.31).

The hammer magnet picks through R38-1 N/O. R38 picks on 7.74.22 when an impulse is received at a print start hub. The print position and print control hubs emit impulses as long as R6 is up.

A setup check is made whenever R38-2 N/C is open on 7.74.31. R39-2 N/O keeps R40 up for one print cycle after R38 picks until a setup check can be made (see Figure 122).

Print Stop

Wiring print start and print stop hubs allows format control. They are wired from COLUMN CONTROL EXITS. PRINT STOP prevents hammer firing and nullifies set up check. These objectives are accomplished by picking R115 and dropping R38. Refer to Figure 122 and the objectives under "Print Start" for further amplification.

Printing Circuits

Print Setup

Once the carriage has started across the copy and PRINT START has been impulsed, it is only necessary to set the print stick and fire the hammer to print. The set of the print stick depends upon analysis of a character on S track. The character to be printed depends upon control panel wiring (see Figure 122). The print stick can be set up whenever the print position emitter makes. It sets up when a control panel wire allows an emitter impulse to an output track hub. The hammer fires when a printable bit is detected in the OUTPUT TRACK position wired.

The print stick is set up by motion pulley movement. The setup magnets are energized through print relay points. The proper print relays are picked when the character to be printed (selected data) is analyzed. Selected data is developed by "anding" S track data with the selected character gate. The selected character gate is determined by control panel wiring. Figure 123 is a block diagram showing the logic of print setup. It combined with Figure 122 shows the printing of a 2 in print position 3.

OBJECTIVES:

1. Selected character (7.71.03).
2. Pick print relays (7.74.21).
3. Set print stick (7.74.22).
4. Fire hammer (7.74.22).

The selected character is a "gate" that allows only one character of S data to be analyzed for each print

position exit impulse. The character analyzed depends upon the output track hub wired. The development of this "gate" can be seen in Figure 123. The 6 *ms* print position exit impulse passes through the F0, and C8 diode OR switches, and then is lengthened to 13 *ms* using condensors and a discharge CB. The condenser and discharge CB at the F1 AK of Figure 123 are typical of the circuit connected to all 20 AK units. The actual condensors are the twenty .047 μf units connected to the AK's on 7.71.03 and 7.71.04. CR21 is the discharge CB. The F0 and C8 AK units develop a field 0-9 pulse during F0 time and a CH0-9 pulse during C8 time. These two pulses "anded" develop the selected character.

The print relays energized depend upon the thyratrons fired on 7.72.01. The thryatrons fire through CR2 on 7.74.21. Then the appropriate print relays pick through CR3 on 7.74.21. The thyratrons fired depend upon the bit structure of the selected data character. The "anding" of selected character and S read data develops selected data. S read data is always present since S read data does not pass through the read matrix.

The print stick is set after the setup magnets are energized. They are energized through print relay N/O points and CR10.

The hammer magnet is energized through one or more print relay N/O point and CR20. Notice on Figure 122 that the print position exit emitter wiper will be making on the 5 spot before the character selected by the 3 spot is printed.

Checking Circuits

Two separate parity checks are made of each character printed. The first, a track check, verifies the parity count of each character printed as it is read from S track. The second, a setup check, verifies the parity count of the setup magnets energized for each character printed. The check light glows and the 370 stops when an error is detected, or the control panel can cause either a "△" to print then stop the 370, or continue to print succeeding lines. Each checking circuit condition is discussed below.

Track Check

R41 energized indicates a track check error. This relay picks whenever the thyratron 8D10 on 7.75.01 fires. The pin 8 input to the thyratron is the selected char-

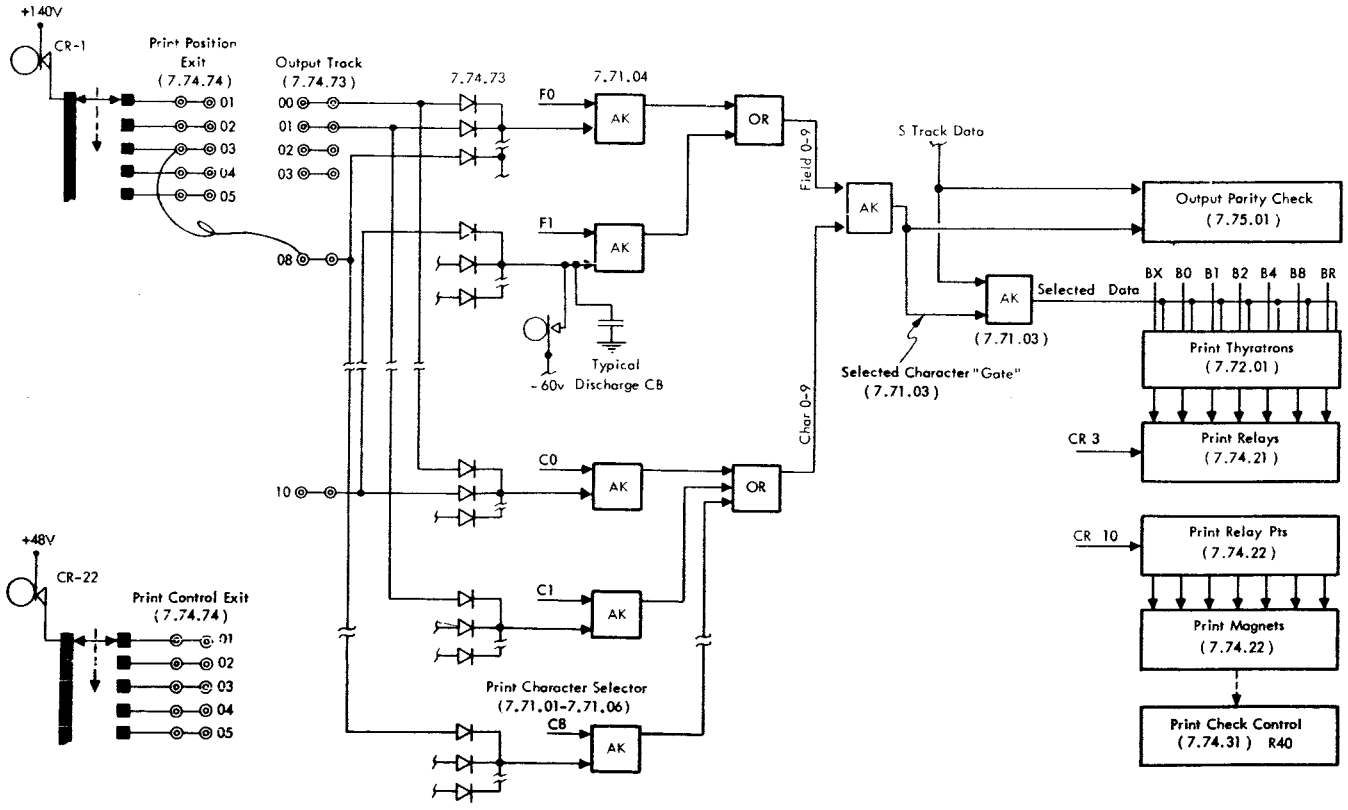


Figure 123. Print Setup Logic

acter. This permits the thyratron to fire only for characters that are printed. The .02 μf condenser and 7.5K resistor at pin 8 delay the selected character at least 4 μs so that the Bs∅B test pulse can fire the trigger just after the bit count of the character has been made. The test pulse checks the condition of the S parity control trigger. 8E8a-5 low, when the test pulse is present, indicates an odd number of bits has just been detected.

Track Check Error

R41 picks when a track check error occurs. When a track check error occurs, the 370 completes the line it is printing before it stops. The track check error relay holds until R45 on 7.74.32 picks. The printer check reset switch picks R45. As long as the track check error relay is up, it prevents re-establishment of the ready condition by preventing the pick of R1 and R2 on 7.74.11. The printer not ready line is also kept high.

After the print carriage returns to its home position R58 picks on 7.74.32. This lights the check light on 7.74.12. Operating the check reset button, then the start button, re-establishes printer ready.

Setup Check

R40 up indicates a successful setup check. R40 up is necessary for printer ready, therefore, a means of keeping it up is needed whenever a setup check is not being made. This means is through R38-2 N/C on 7.74.31. This circuit must be opened in order to test the setup contacts when a character is printed. If an odd number of setup magnets are energized, there is a circuit through the setup contacts.

A study of the picks and holds of relays 38, 39 and 115 in Figure 122, reveals how these 3 relays control the time that setup checks are made. R39 up picks R40 for the cycle between R38 pick and the first setup check. R115 up allows the last character printed to be setup checked.

Setup Check Error

The setup check relay, R40, drops when a setup check error occurs. The 370 finishes printing the line and then stops in a not ready condition with the printer check light ON. The setup check relay is prevented from repicking by the setup check interlock relay, R48, on 7.74.31. R48 drops when the check reset button is depressed. This allows a repick of R40. Depressing the start key then re-establishes printer ready.

Error Print—Delta Stop

Improper control panel wiring can cause setup errors. When testing for this condition on a machine malfunction, it may be desired to print a delta left of any line which includes an error. Jackplugging the delta stop or delta non-stop hubs causes this.

When delta stop is wired the printer prints a delta left of the line in error after the carriage returns to its home position. Then the printer stops in a not ready condition. Depressing the start key re-establishes printer ready in this case. However, the check light remains ON. It may be extinguished by depressing the printer check reset button.

Figure 124 shows the sequence of circuit operation. When the print stick is in its home position a delta prints if the hammer is fired. The hammer magnet is energized through R43-3 N/O on 7.74.22. R43 and R58 are picked through the delta stop hubs as the carriage nears its home position. R58 staying up keeps the check light ON. R45 picks to drop the error interlock condition, R48 up. If the error had been a track check error, R41 would have indicated the error condition.

Error Print—Non-Stop

When the △ non-stop hubs are jackplugged the 370 prints a △ to the left of any line with an error and continues operating without any interruption. This is accomplished by failing to destroy the printer ready condition. If an error occurs the check light turns ON and stays ON.

Bottleplugging the △ non-stop hubs keeps R44 up constantly. This allows the R44-2 N/O points on 7.74.11 to keep the ready 1 relay held. Therefore the ready condition is re-established when the carriage returns home in the normal manner.

Other than the fact that the ready condition is not destroyed this operation is the same as error print — delta stop.

Print Control Circuits

Print control circuits increase the flexibility and usefullness of the 370. The function and operation of each circuit is described below.

X-Eliminate

In a numerical field a Bx in the units position digit indicates the complete number is negative. If such a Bx were allowed to to enter into the setup of a character for printing, an alphabetical character would

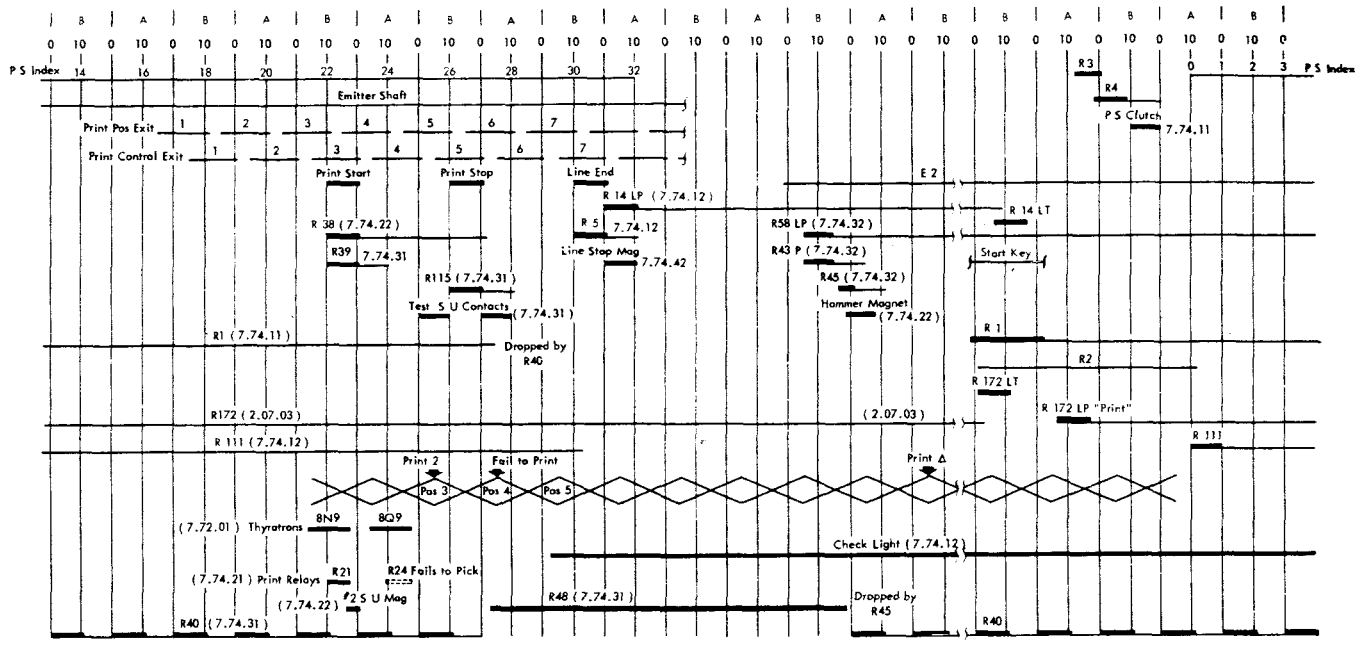


Figure 124. Error Print — Delta Stop

print. The X-eliminate feature is provided to prevent this. The wire from PRINT CONTROL EXIT 20 to X-ELIM in Figure 125 operates the feature.

If a Bx is suppressed by the X-eliminate relay, R34 on 7.74.22, a print setup error indication will occur unless there is a modification in the pick of the BR setup magnet. The table below indicates how this circuit is modified.

CHARACTER CONTAINS	SETUP MAGNET BX	BR
Bx, BR, Etc.	Suppress	Suppress
Bx, No BR, Etc.	Suppress	Pick
No Bx, Etc.	No pick	Picked Normally (R25)

The above conditions are accomplished in the pick of the bit R setup magnet.

NX-Eliminate

The 370 may be wired to print a minus sign to indicate a negative number. The two wires labelled A in Figure 125 accomplish this. This control panel wiring allows the Bx setup magnet only to be energized if there is a Bx in the units position. It picks only the BR setup magnet if there is no Bx in the units position. R35 on 7.74.22 controls this operation.

Zero Suppression

In the numeric field it is often desirable to suppress the printing of zeros to the left of the first significant digit. This may be accomplished by a PRINT CONTROL EXIT wired into the zero suppress start hub to pick R37 (7.74.22). The R37-1 point prevents the hammer magnet from being energized if only the B0 relay, R16 is picked. The first character containing any bit, other than a B0, will provide a circuit to the hammer magnet and will pick R31 through R37-1 N/O. R31-3 then opens the R37 hold circuit. R31 can also be picked by a print control exit impulse wired into the zero suppress stop hub. Figure 125 shows proper control panel wiring.

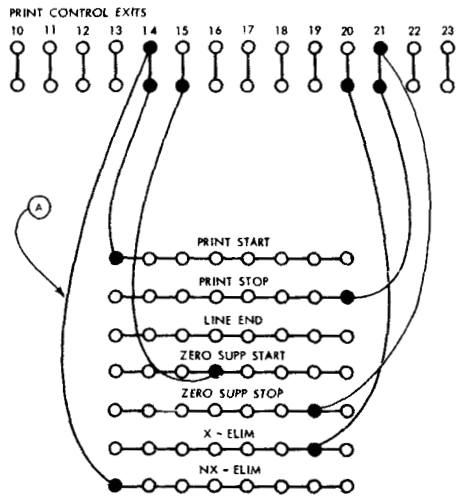
Print Space

If PRINT START is wired from PRINT CONTROL EXIT 10 and PRINT STOP from PRINT CONTROL EXIT 21, then every print position exit hub from 10 through 20 should be wired. If any print position exit hub within this field is left blank, no setup contacts will transfer causing a setup error. To prevent this, wire into the print space hubs from each print position exit hub which is not otherwise wired.

An impulse into the print space hub (7.74.22) is taken to 8H8a (7.72.01) where it gates BR pulses onto the selected data line at 8J9b, where they are strobed with ØC. These BRØC pulses cause thyratron 8R9 to be fired. Thus, the BR relay and the BR setup magnet are energized to prevent a false error indication.

Special Character Hub

A special character hub on 7.74.21 may be wired from a print control exit hub to cause the character thus selected to be printed. The print position exit hub



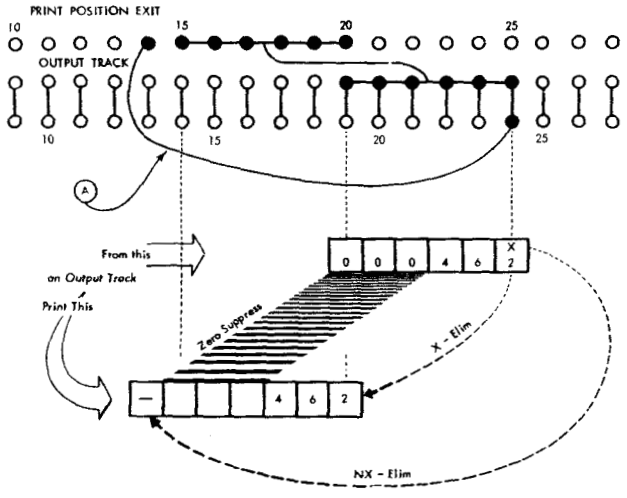


Figure 125. Numeric Field Wiring

should be left blank for a printing position where a special character is to be printed.

Analyzers

An analyzer determines the Hollerith code of any character on the output track. It then emits an impulse from a combination of its exit hubs to indicate the code content determined. An analyzer operates during the early part of the program shaft cycle before the emitter shaft drive engages. There are four analyzers.

An analyzer reads a character on S track in the same manner that a character is read for printing. The same circuit is used and the print relays are picked. This is done because the circuit is not needed for printing early in the program shaft cycle.

Figure 126 is a block diagram showing how the analyzer relays are picked. The character to be analyzed is determined by the output track hub wired. The ACI hub determines which analyzer will do the analyzing. The analyzer relays are picked through the appropriate print relay points and the program shaft CB associated with the analyzer.

Figure 127 shows the sequence of operation when selecting character 51 to set up analyzer A, and of selecting character 13 to set up analyzer D.

Analyzer A detects a Bx. Analyzer D detects a B8.

Multiple Line Printing

The 370 can print up to 4 lines each time the print select hubs are impulsed. This operation is called multiple line printing, or MLP. Normally a different line program selector is energized for each line to control format. Each of the MLP out hubs, 1, 2, 3, and 4, emits an impulse during the early part of the program shaft cycle preliminary to the printing of its corresponding MLP line. Usually an MLP start hub is

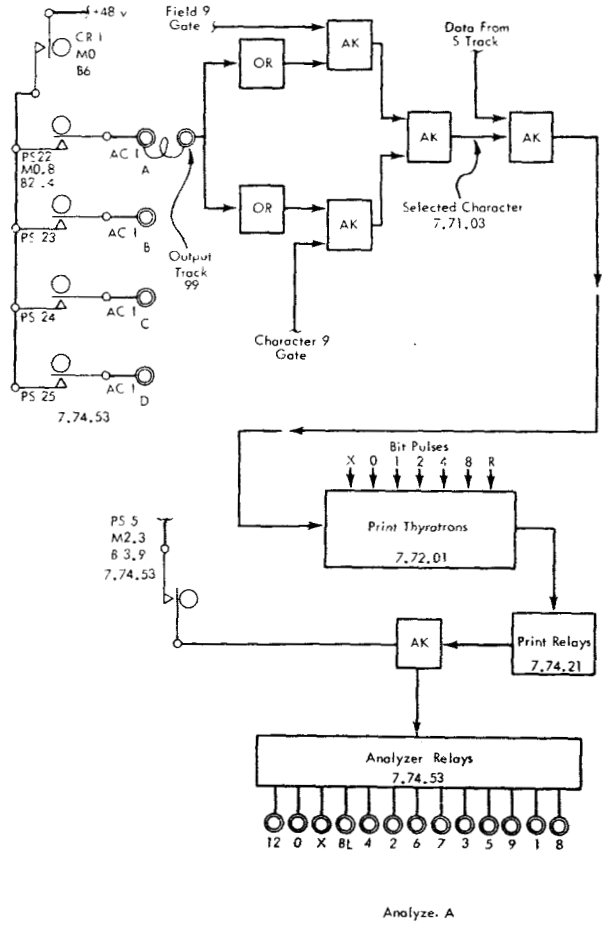


Figure 126. Analyzer Logic

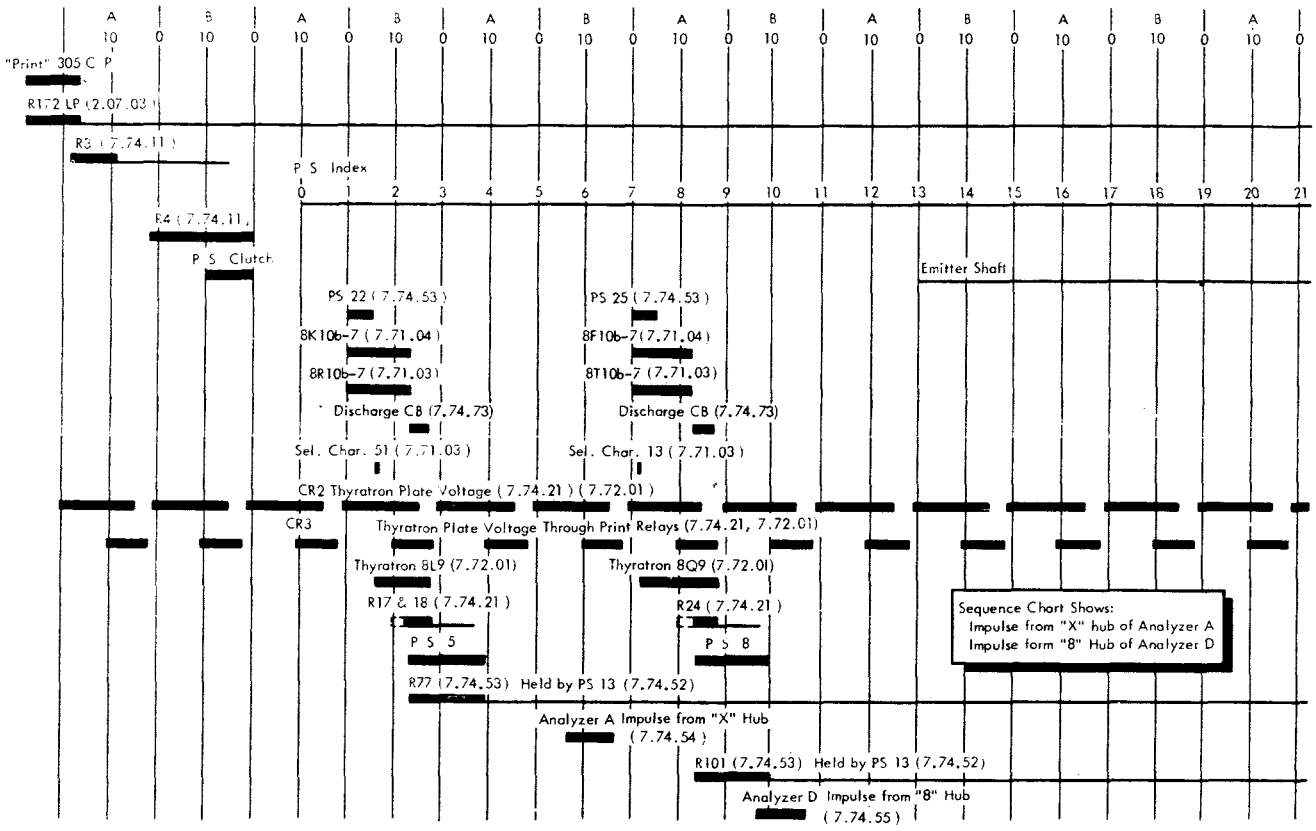


Figure 127. Analyzer Operation

impulsed after analyzing a character on the output track. Figure 128 shows control panel wiring for a 4 line MLP operation.

Once an MLP operation starts, the output track must remain interlocked until the last line has been printed. The program shaft clutch magnet must be energized for each line to be printed. The appropriate MLP out hub must emit an impulse for each line printed.

OBJECTIVES:

1. Interlock output track (7.74.12).
2. Successive PS clutch picks (7.74.11).
3. MLP OUT impulse (7.74.51).

The output track remains interlocked as long as the print select relay, R172, is not tripped. R54-5 N/C on 7.74.12, an MLP interlock relay point, prevents this. It serves to latch trip R14 instead. R54 was picked on 7.74.50 and remains held until the last line of print is initiated.

PS clutch picks occur each time R3 on 7.74.11 picks. R3 picks, whenever the carriage returns home, through R2-1 N/O. E1 makes, as the carriage returns home picking R2. The last time the carriage returns home, R3 does not pick because R172 has been tripped.

The appropriate MLP out impulse is present through a program shaft CB and the appropriate MLP start relay. For example, during an MLP 4 operation the MLP 3 out impulse passes through R51-2 N/O on 7.74.50 at the beginning of the third MLP line. R51 holds until late in the third program shaft cycle.

Line Program Selectors

Each line program selector has eleven sets of hubs. One set of hubs from each selector is grouped together above the print control hubs. The other 10 sets are grouped together in the lower half of the control panel. Each set of hubs is connected via relays so that only two of them are common at one time. The C and N hubs are common normally. The C and 1 hubs are made common if the 1 PU hub is impulsed. The C and 2 hubs are made common if the 2 PU hub is impulsed, etc. Once a PU hub is impulsed the hubs so controlled remain common until line end.

Figure 128 shows control panel wiring for a line program selector application. The machine wiring for these selectors is shown on System Diagrams 7.74.61 through 7.74.63.

Selectors

Twelve selectors of the conventional type are cataloged on 7.74.72. A sample set of hubs with the asso-

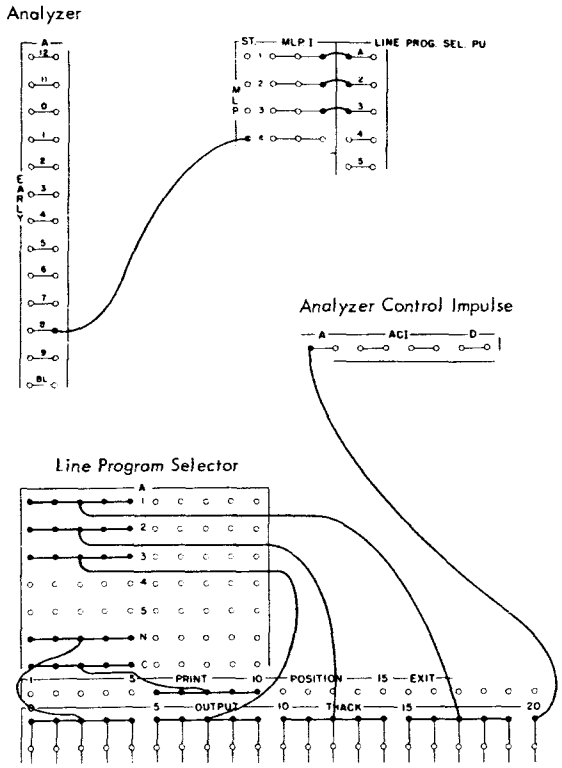


Figure 128. MLP Line Program Selector Application

ciated relay point is shown at the top of the page. The location of all hubs and identification of all relay points are shown in the table.

The pickup hubs for these selectors are shown on 7.74.71. An impulse into the 5 hub picks R139, which holds until R11 picks at line end. This transfers all five points of selector 5.

Form Feeding Circuits

Paper Space Control

The 370 may be wired for single, double, or triple spacing. The line space magnet (7.74.42) must receive a CR17 impulse for each space to be taken. If the single, double, or triple space hubs are jackplugged, PS1, PS2, or PS3, respectively, will be placed in the circuit to the line space magnet. The timing chart (0.09.50) shows that PS1, PS2, and PS3 overlap one, two, and three CR17 impulses respectively. Spacing occurs after the program shaft clutch magnet is impulsed, but before printing begins.

Once the form is positioned at the desired line by a skip, normal line spacing is suppressed before printing that line. This is accomplished by R7 (7.74.42). R7 is picked as R73 holds. R7 holds until PS 17 makes after printing begins, and opens the circuit from the space hubs to the line space magnet.

Carriage Tape Control

The 370 form feed carriage employs a standard IBM 12 channel carriage tape to control the positioning of the forms for skipping and overflow. Five of these channels, numbers 7 through 11, are inoperative except as an optional feature. A hole in channel 1 of the tape is normally used to stop the carriage at the first line of a form. A hole in channel 12 is used to initiate an overflow to a new form. Holes in channels 2 through 6 are used to stop a form at one of 5 intermediate positions after skipping has been started. The holes in the tape channels are sensed by star wheel contacts.

The form feed mechanism is caused to take repetitive spaces for all movements of the form. Except for form spacing operations, the form feed may not be advanced while a line printing operation is in progress. The repetitive impulses to the line space magnet (7.74.42) for a skip or restore action are provided by a circuit through the selected SKIP TO channel relay points and the skip start relay point, R73-2 N/O from CR17. This circuit is opened by the selected SKIP TO channel relay point as that relay is latch tripped when the selected channel is reached.

Programmed Skips

In order to skip before printing, a skip to hub on the 370 control panel must be impulsed before the print hub on the 305 control panel is impulsed. If SKIP TO is impulsed after the print cycle has started, skipping will take place after printing.

A 370 print operation is normally initiated during a program step having $T_2 = S$. If it is desired to have the skipping take place before printing, the PROGRAM EXIT impulse is wired through a communication channel to the appropriate skip to hub. The same impulse is wired to CYCLE DELAY-IN. CYCLE DELAY-OUT is then wired to PRINT and to PROGRAM ADVANCE or PROGRAM ENTRY.

If it is desired that skipping take place immediately after printing, either of two control panel wiring methods may be used. The first requires that the PROGRAM EXIT impulse be wired into print hub and the cycle delay-in hub. The resulting CYCLE DELAY-OUT impulse is wired through a communication channel to the desired skip to hub. This same impulse is wired to PROGRAM ADVANCE or PROGRAM ENTRY. The second method makes use of an impulse at the 370 control panel, such as an ANALYZER EXIT impulse, to cause skipping.

It is possible for a 370 to receive a signal to skip while it is in the process of skipping. So that the 370 can remember where to skip to, and to prevent a process unit interlock, it has a second set of skip to relays. The two sets of skip to relays take turns being the relays to store skip information. The function of the skip buffer control relays is to control when the skip to relays store data. One set is prepared to be picked for every other print operation.

Figure 129 shows sequential relay operation for a skip to 2 before printing, printing, and a skip to 3 after printing. The printer receives the skip to 3 impulse while the skip to 2 is in operation. The program that causes this operation is W99S9900&b. Cycle delays are used in the wiring of the & PROGRAM EXIT. Notice that the skip buffer control relays, R152, and R153, pick every other time the print select relays pick. Also skip buffer relays, R177, 178, and 179, pick every other time the program shaft clutch is energized. The figure shows R152, 153, 177, 178, and 179 as latch tripped at the beginning of the sequence. They are tripped whenever the 370 reset button is depressed.

OBJECTIVES:

1. Pick skip to relay (7.74.41).
2. Skip start (7.74.42).
3. Interlock 370 (7.74.11).
4. Skip stop (7.74.41).

A skip to relay is latch picked to remember what carriage tape channel hole stops the form movement. It stays up until the hole is sensed.

Skip starts occur when R73 on 7.74.42 is picked. R114-2 in the pick of R73 prevents a skip start whenever a printer is already skipping. R73-2 N/O allows

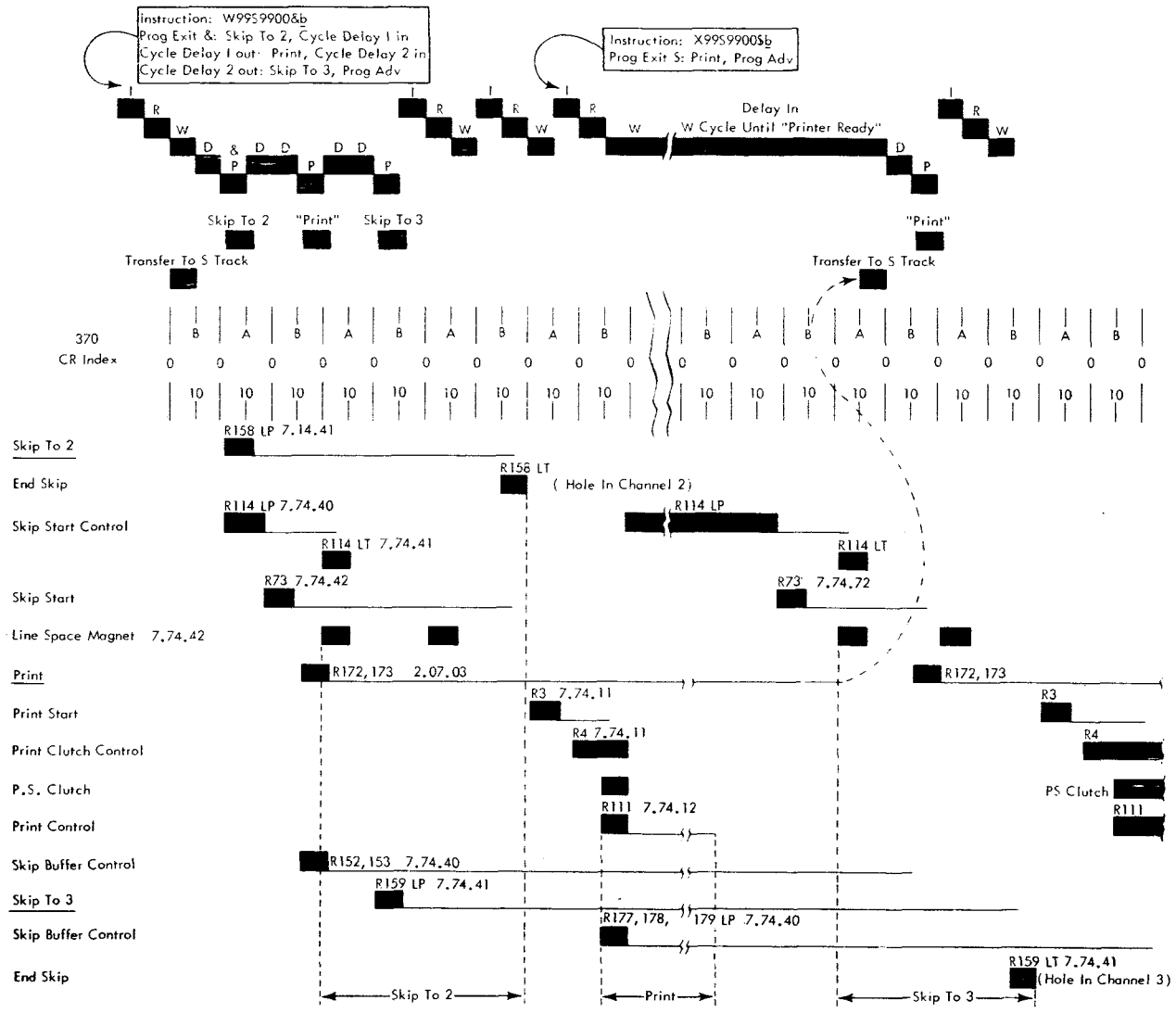


Figure 129. 370 Skipping

CR17 impulses to the line space magnet.

Printer interlock is accomplished by dropping R2 on 7.74.11. R73-5 N/C does this.

Skip stop is accomplished by dropping R73. R73 is held through a N/O skip relay point. Skip to relays are latch tripped when the skip to hole is sensed on 7.74.41.

OBJECTIVE:

1. Pick a skip to relay during a skip (7.74.41).

To pick a skip to relay during a skip it is necessary to use the set of skip to relays not concerned with the present skip. R152 and R153 points accomplish this. These relays are latch picked every other print operation on 7.74.40. R177-1 N/C controls this. Referring to 7.74.40 you see that R177 is latch picked every other PS clutch pulse under control of R152-3 N/O. Refer to Figure 129 to see the timing of these relay operations.

Overflow

The overflow hubs (7.74.41) emit a PS17 impulse after printing starts if the channel 12 contact is closed. The OVERFLOW impulse is wired to a skip to hub to cause a skip to a hole in the desired channel after printing of the line is complete.

Restore

Depressing the restore switch causes a skip to 1 operation. When you operate the restore switch on 7.74.42, one of the skip to one relays, R155 or R156, picks. R114 on 7.74.40 latch picks. When the restore switch returns to normal, the skip start relay, R73, picks on 7.74.42. The circuit then operates as a normal skip to 1 skip.

If the channel 1 star wheel contact is already reading a hole when the restore switch is operated, the skip takes place nevertheless. This is insured by R114-1 N/C on 7.74.41, which holds open the circuit to latch trip R155 or R156. The first impulse to the line space magnet also latch trips R114.

Optional Features

MLP Repeat

Up to 8 lines of MLP may be printed by using this feature. It consists of relays and control panel hubs to permit extended control of MLP. MLP and MLP repeat control panel hubs are shown in Figure 130. The wiring in this figure also shows an example of wiring to cause a 6 line MLP operation. The MLP repeat in hub must be impulsed before analysis time of the last standard MLP line called for has passed (line 3 in Figure 130).

Impulsing the MLP repeat in hub picks R56 on 7.74.50 to allow a hold for R54 through R56-2 N/O until PS-16 makes again on 7.74.51. With R54 up the printer select relays may not be tripped, so the printer proceeds into repeating MLP. The MLP repeat out hub emits an impulse during the first MLP repeat program shaft cycle. This impulse is directed by control panel wire to an MLP in hub. The MLP in hub selected determines the number of MLP repeat lines of printing. In Figure 130 the number of additional MLP repeat lines of printing is 3. R59 remains up throughout the MLP repeat operation to activate the MLP 5, 6, 7, and 8 hubs.

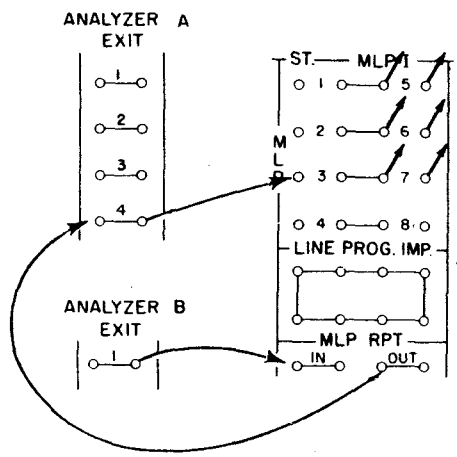


Figure 130. MLP Repeat Control Panel

The 323 Punch serves as one of the output devices for the RAMAC 305. Its operation during automatic processing is under control of the 305 program, supplemented by control panel wiring on the punch itself. When a program exit impulse is received at the punch hub on the 305 control panel, the 323 takes a cycle. During this cycle, data is selected from the output track, translated into Hollerith code, and punched into a card.

Mechanical Principles

Feeding Mechanism

The feed knives feed one card through the throat into the first set of feed rolls for each revolution of the punch clutch. The feed rolls then carry the card past the punch station and the brush station to the stacker. The knives are driven back and forth by gear sectors which mesh with the knife racks. The gear sectors are pinned to a shaft which moves back and forth under the control of complementary cams mounted on the punch clutch shaft as shown on Figure 134.

When a card is fed from the hopper, it is fed between the first pair of feed rolls. The feed rolls operate intermittently under control of the geneva. The feed knives are timed to carry the card up to the first feed rolls while the feed rolls are stationary. To insure that the first feed rolls will pick up the card, the knives buckle the card slightly just before the feed rolls start turning.

The upper feed rolls are mounted in fixed bearings. The lower feed rolls are provided with pivoted bearings to allow separation of the rolls when a card is fed between them. Feed roll tension is provided by a pressure bracket consisting of four bearing shoes held against the feed roll shaft by compression springs.

The card also passes a set of brushes and a contact roll. The brush assembly consists of 80 individual brushes mounted in a brush holder so that they are insulated from each other.

Figure 131 shows a schematic diagram of the punch feed. Cards are placed in the hopper, face down, 12-edge toward the throat. During the first feed cycle, the bottom card is fed from the normal hopper location to a position where its leading edge is just entering the die and stripper. At the end of the first feed cycle, the die card lever contact has been closed in addition to the hopper card lever contact.

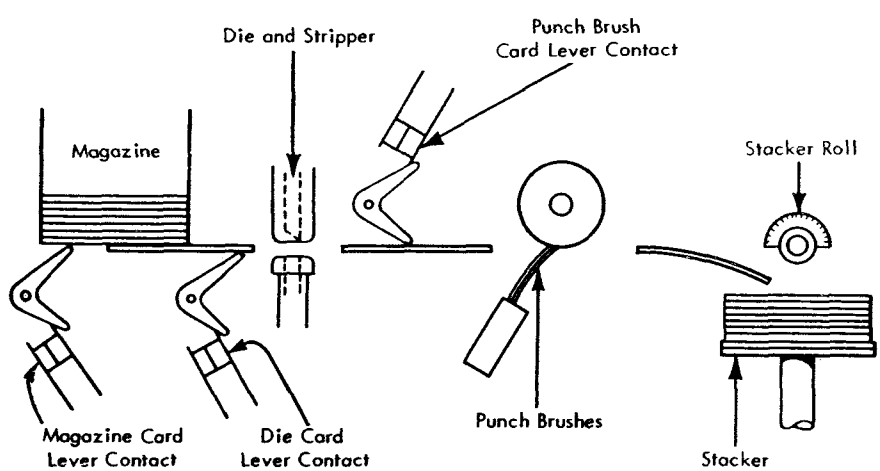


Figure 131. Punch Feed Schematic

During the second feed cycle, the first card is advanced past the die and stripper to a position where its leading edge has just reached the brush station. The second card is advanced to the position where its leading edge is just entering the die and stripper. At the end of the second cycle, the brush card lever contact has been closed in addition to the die card lever contact and the hopper card lever contact.

During the third feed cycle, the first card moves past the reading station, the second card moves past the die and stripper, and the third card is advanced from the hopper. Punching may be performed on this and on all subsequent feed cycles.

Drive Mechanism

Power to drive the 323 Punch is provided by the drive motor. A diagram of the drive mechanism is shown in Figure 132.

When the drive motor is energized, the following mechanisms operate continuously:

1. Motor, V-belt, and drive pulley.
2. Geneva disk.
3. Eccentric shaft.
4. Oil pump.
5. Punch clutch ratchet.

All of the other mechanisms are under control of the punch clutch. The feed rolls, contact roll, and stacker roll are under further control of the geneva clutch. Operation of the punch clutch causes the geneva clutch to engage mechanically in a manner which will be described later.

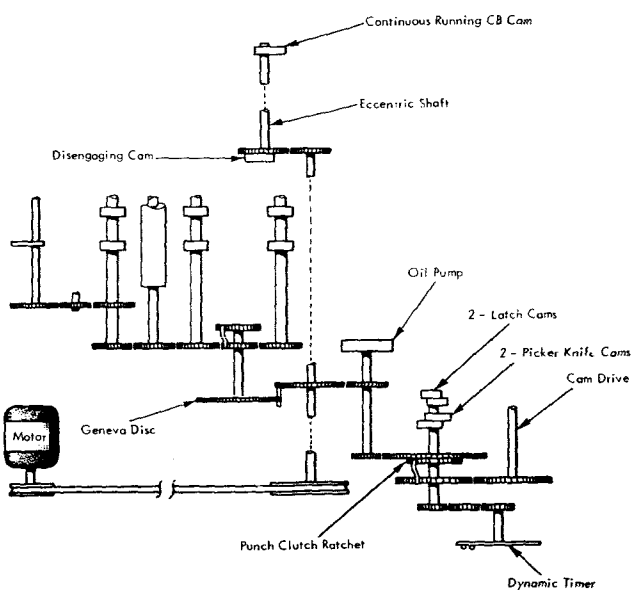


Figure 132. 323 Mechanical Drive

When the motor is in operation, but with neither clutch engaged, the drive pulley turns the drive pulley shaft to which the pulley is keyed. Attached to this shaft inside the gear housing are two gears, the geneva drive gear and the eccentric shaft drive gear.

The eccentric shaft drive gear operates the eccentric shaft, which in turn transmits motion to the punch bail. The geneva drive gear operates the geneva, the geneva ratchet, and also the punch clutch idler gear and shaft. Pinned on the outside of the idler gear shaft is a small gear which drives the intermediate index gear (Figure 133). The punch clutch 14-tooth ratchet is a part of the index gear assembly and rotates continuously as long as the motor is in operation. The intermediate index gear and ratchet rotate on the punch clutch shaft, but are not pinned to it.

In order to place the other machine units in operation, it is necessary to unlatch the punch clutch pawl from its armature so that it will engage in the continuously running 14-tooth ratchet. When the pawl engages, the punch clutch shaft turns with the ratchet. One of the gears mounted on the punch clutch shaft drives the P-cam shaft. The gear on the outside end of the punch clutch shaft drives the dynamic timer, which is the index for the 323.

Within the gear housing, pinned to the punch clutch shaft, are two sets of complementary cams. One set of cams operates the feed knives, and the other controls the engaging of the geneva clutch pawl with its ratchet.

The geneva pawl and pawl arm are normally stationary, but when the pawl engages with the geneva ratchet, they are driven by the geneva disk, which imparts an intermittent motion to the pawl and pawl arm. Welded to the geneva pawl arm is the pawl gear, which serves as the drive gear for all feed rolls, the contact roll, and the stacker roll. Because all of these rolls are driven from the geneva, they all turn intermittently. The intermittent movement is necessary so that the card will be stationary when punching occurs. Only the upper feed rolls and the contact roll are driven by the gear train in the housing. The lower feed rolls are driven by their corresponding upper rolls through gears at the front of the machine. The stacker roll is driven by a gear train from the last feed roll.

Punch Clutch

The punch clutch has a 14-tooth ratchet similar to the one-tooth ratchet commonly used on IBM equipment. The principal parts of the clutch include the continuously running 14-tooth ratchet, a clutch pawl, a latching mechanism, and a magnet. The magnet provides a means of electrically controlling the operation of the clutch. The clutch magnet armature serves

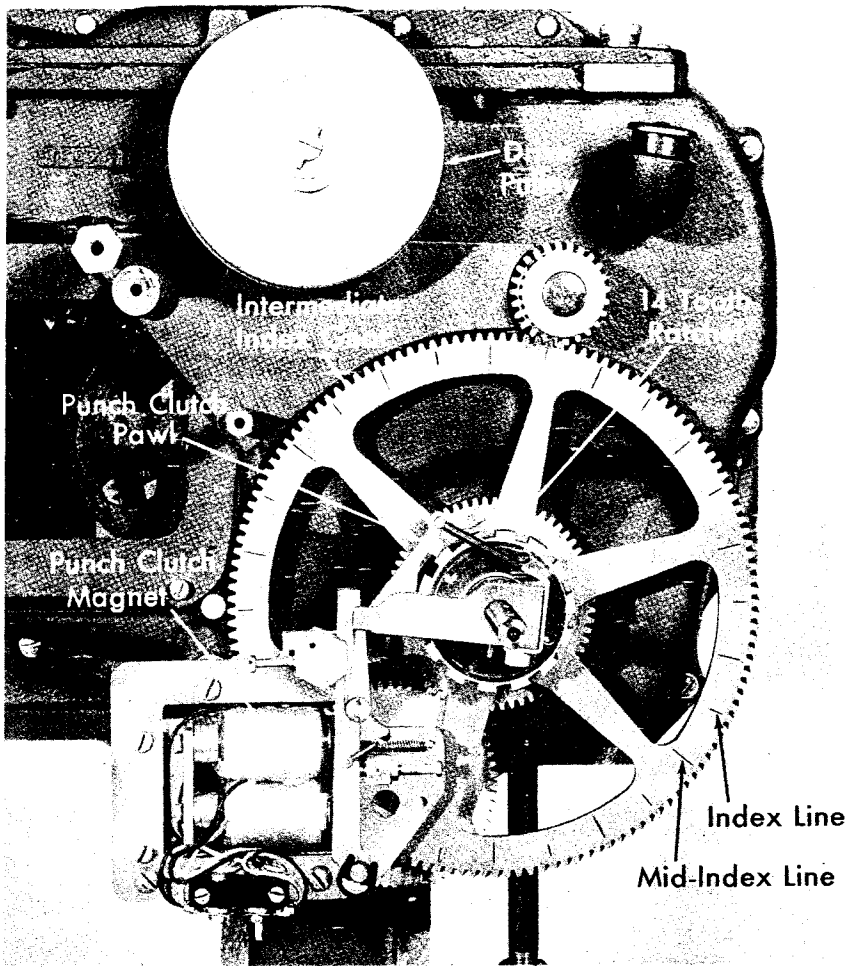


Figure 133. Punch Clutch

as the latching mechanism to latch the pawl and keep it from engaging in the ratchet.

When the magnet is energized, the armature is attracted and the pawl is unlatched. The pawl spring causes the pawl to pivot in a clockwise direction to engage the 14-tooth ratchet when the next ratchet tooth reaches the pawl. The pawl pivots on a stud fastened to the clutch pawl arm, which is pinned to the punch clutch shaft. Thus, when the pawl turns with the ratchet, the shaft must also turn.

Once the pawl is unlatched, it must make one complete revolution before it can be relatched, because there is but one latching point. For this reason, it is necessary to keep the armature attracted only long enough to allow the pawl to engage the ratchet.

When the pawl reaches the end of its cycle, the armature has been returned to its normal position by the return spring, and the tail of the pawl will strike the armature, causing the pawl to be cammed out of mesh with the 14-tooth ratchet. When the pawl has been cammed out of mesh, the keeper drops behind the clutch pawl arm and prevents the clutch shaft from turning backward. Without the keeper, the shaft might turn backward because of the rebound, and the pawl could drop against and catch on the 14-tooth ratchet. This nipping action would have a tendency to round off the edges of the ratchet teeth.

The latch point of the punch clutch is 14.5 on the index.

Index and Cycles

Since all of the mechanical and electrical actions in the 323 must be synchronized with each other, it is necessary to have a common index to which all machine timings may be referred. The dynamic timer serves as the index for 323 operations.

For convenience in measurement, one cycle is divided into units called cycle points. The most logical unit of division is the distance between successive punching positions on the card. The distance from the 12 punching position to the 11 punching position

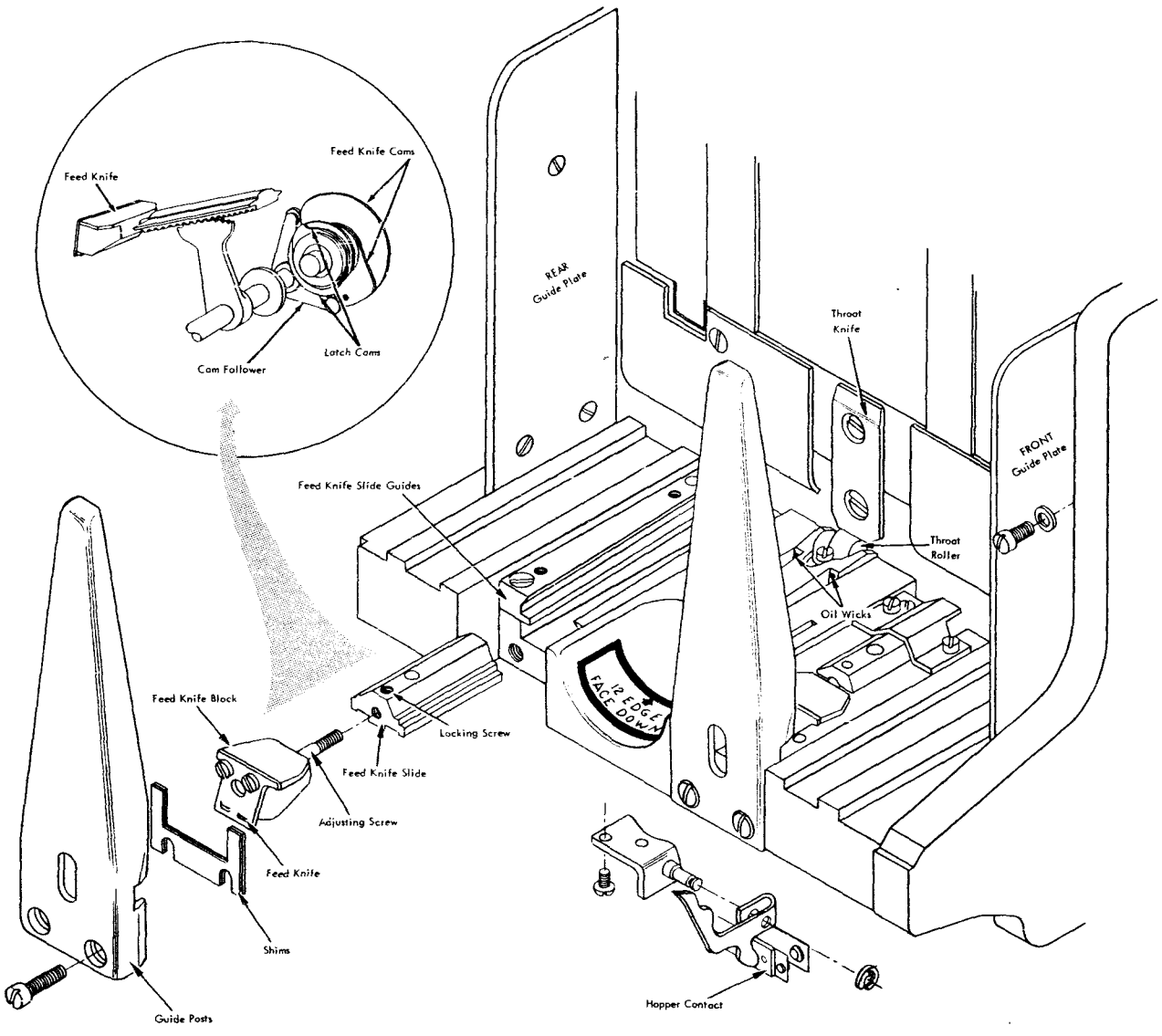


Figure 134. 323 Hopper

in one card represents one cycle point. The distance from the 12 punching position in one card to the 12 punching position in the following card is one cycle.

There are 12 punching positions in each column of the card. Since each punch position is ¼ inch from the next, the card moves ¼ inch on its path through the machine for each cycle point.

Since the card is 3¼ inches wide, 13 cycle points are required to advance a card past any given point. In this machine there is ¼ inch between cards; therefore the cycle consists of 14 cycle points. The teeth on the intermediate index gear and the marks on the dynamic timer scale are used for further subdivisions. A timing given as 11.1 indicates one tooth past the 11 index mark. Since the punch clutch latches at 14.5, this is the starting point of each machine cycle.

Geneva Mechanism

As indicated previously, the feed rolls must operate intermittently to allow punching of the card. The card must be standing still when punched, but it must be moved to a new punching position fourteen times each cycle. This intermittent motion is provided by the geneva mechanism.

The geneva drive gear is located just inside the gear housing and pinned to the pulley shaft. A stud and roller fastened to this gear operate in the slots of the

geneva (Figure 135). The hub of the geneva drive gear is a cam surface for approximately two-thirds of its periphery. The cam surface holds the feed rolls in a stationary position during punching time by locking the geneva in position.

The geneva disk has seven deep slots and seven shallow cuts. The roller of the drive gear operates in the deep slots and the cam surface rides in the shallow cuts. As the drive roller leaves the deep slot of the geneva disk, the cam surface turns into the shallow cut, thus stopping the geneva disk from turning and holding it until the drive gear has rotated to a point where the drive roller enters the next deep slot. Then the cam surface has turned to a point where it releases the disk and allows it to turn freely.

The geneva disk and disengaging cam turn continuously as long as the drive motor runs; however, no motion is transmitted to the feed rolls until the geneva pawl is engaged with its 7-tooth ratchet. The geneva ratchet is pinned to the same shaft as the geneva disk. This shaft runs through the geneva pawl arm and gear (Figure 137). The pawl is free on the shaft and does not turn unless the pawl is engaged with the ratchet.

When the punch clutch is not engaged, the geneva pawl is cammed away from each tooth of the 7-tooth ratchet by the disengaging cam roller. The disengaging cam makes one revolution each cycle point. Before the 7-tooth ratchet starts to turn counter-clockwise, the disengaging cam roller moves against the tail of the pawl, raising it out of the ratchet tooth. The geneva and the 7-tooth ratchet start to turn. After the pawl is clear of the ratchet tooth, the disengaging cam roller moves to the left, allowing the pawl to ride down into the next tooth.

Because the disengaging cam makes one revolution for each index point, it will operate the disengaging roller and raise the pawl to clear each tooth on the 7-tooth ratchet. By hand-cranking the machine, it can be noted that the disengaging roller prevents the geneva pawl from engaging.

The operation of the geneva pawl is controlled by the pawl disengaging roller. As shown in Figure 137, the pawl disengaging roller is mounted on an L-shaped lever which pivots on the latch cam arm. When the punch clutch is engaged, the latch cam turns, causing the latch cam arm to rotate in a counter-clockwise

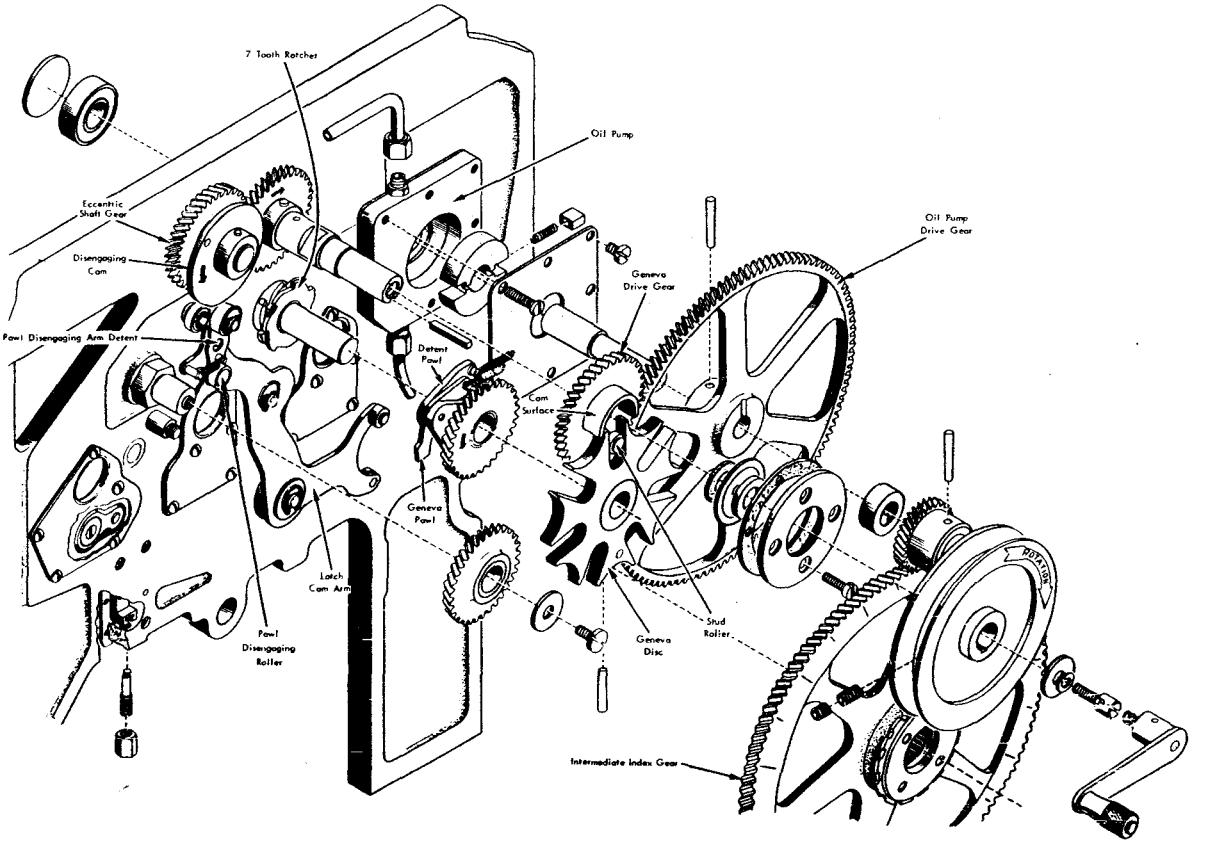


Figure 135. Geneva Mechanism

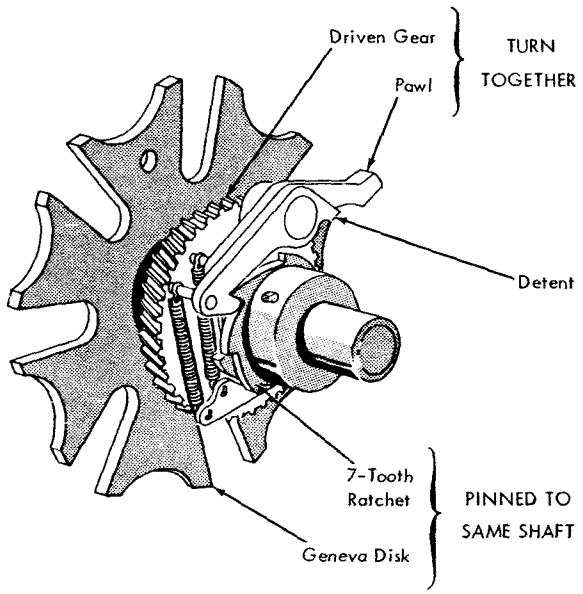


Figure 136. Geneva Assembly

direction. As the latch cam arm rotates, the upper end moves to the left and down, allowing the pawl disengaging roller to move away from the pawl, permitting the pawl to engage the next tooth of the geneva ratchet.

As the punch cycle is completed and the punch clutch latches, the latch cam causes the latch cam arm to rotate in a clockwise direction, carrying the pawl disengaging roller to the right. This allows the disengaging cam to raise the pawl out of the geneva ratchet tooth.

The geneva ratchet makes two revolutions each punch cycle. The geneva pawl is not disengaged after the first revolution of the geneva ratchet because the latch cam arm is moved back into the disengaging position only at the end of each punch cycle.

Principles of Punching

The mechanism for punching holes consists of the following:

1. 80 individual punches, each controlled by an interposer.
2. 80 punch magnets together with armature and pull wires to control the 80 interposers.
3. A punch bail to drive the punches through the card.
4. An eccentric drive shaft and links to operate the punch bail.

For each card column there is one punch which may punch a hole in any of the 12 punching positions. The card feeds 12-edge first, and every 12 hole to be punched is punched at 12 time. The card then moves to the 11 position and every 11 hole to be punched is punched. The process is repeated for each of the twelve digit positions.

As previously mentioned, the eccentric shaft operates continuously, as long as the drive motor is in operation. The purpose of the eccentric shaft, with its links to the punch bail, is to convert the rotary motion of the shaft to the reciprocating motion necessary to operate the punch bail; this is illustrated in Figure 138. Only one of the 80 punches with its associated punch magnet is shown.

When the punch magnet is not energized, the punch bail may move up and down without contacting the interposer; therefore, no punching takes place. When the punch magnet is energized, its armature is attracted, and through the pull wire the corresponding interposer is pulled under the punch bail tongue. As the punch bail tongue moves down, it carries the punch interposer and the punch connected to it down through the card. On the return stroke, the punch is positively withdrawn from the card by the action of the punch bail. As the interposer is returned to its normal position, the upper rounded edge strikes the knockoff bar and the interposer is cammed away from the punch bail tongue. The interposer spring then holds the interposer in normal position.

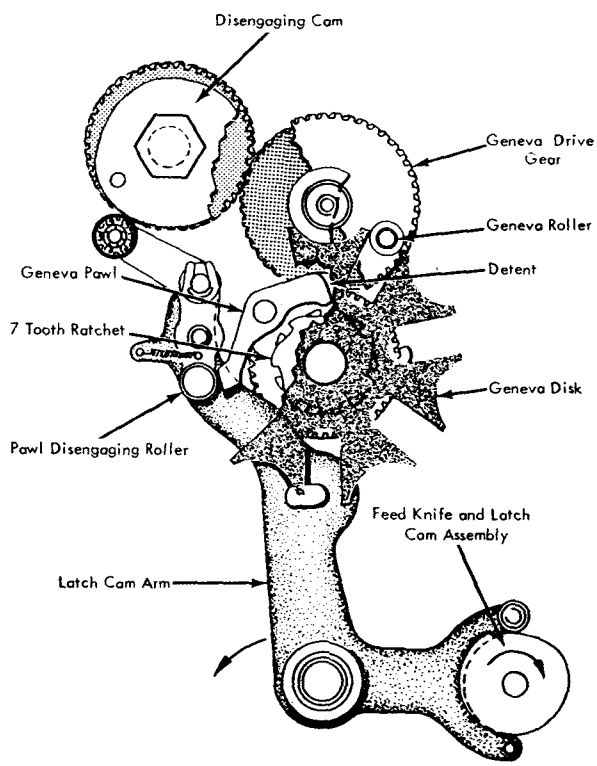


Figure 137. Geneva Assembly and Drive

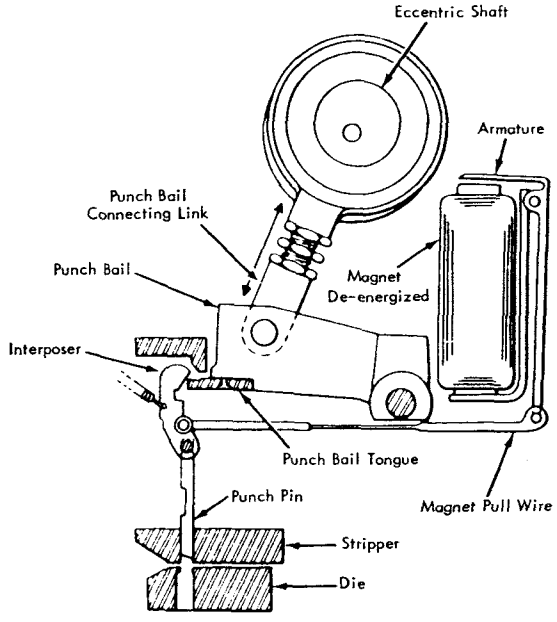


Figure 138. Principle of Punching

Magnet Unit

The punch magnet unit consists of 80 punch magnets along with their armatures and pull wires, 80 interposers and punches, the die and stripper assembly, and the punch bail assembly.

There are three types of interposer and punch assemblies. One type is used in the first column, a second type in the 80th column, and a third type is used in all columns from 2 to 79 inclusive. The interposer used in the 80th column is provided with a long stud for the eye of the magnet pull wire to prevent slipping off the stud. The interposer used in column 1 is attached to the punch to prevent the interposer from slipping off. The space between the interposers prevents the interposers from sticking together and causing extra holes to be punched.

The magnet unit is held in place by four mounting screws and is located by two aligning screws. The magnet unit aligning screws are located approximately midway right and left on the front and back of the magnet assembly. These aligning screws determine the vertical punching registration. The left front and back mounting screws hold the punch magnet assembly through wide slots. Thus, horizontal registration can be adjusted. The right front and back mounting screws pass through elongated holes to permit vertical registration adjustment by the aligning screws.

Oil Pump

The oil pump is a simple rotary-vane pump. It is located inside the gear housing on the shaft of the small gear which drives the index. It pumps the oil from the bottom of the gear housing to the top, where it is free to run down over the geneva mechanism and gears.

The rotor is pivoted off-center in the housing. The expansion chamber at the inlet provides a vacuum and causes the oil to enter the pump from the well below. The compression chamber at the outlet causes oil to be forced out at the top. See Figure 139.

Card Feed Control

The fundamental purpose of the 323 is to serve as an output device for the RAMAC. It may also be used as a gangpunch when it is not required in the RAMAC program. When used exclusively for gangpunching the gangpunch hubs on 7.44.21 must be jackplugged. When used as an output device in the RAMAC system, the run interlock hubs must be jackplugged. In this condition the 323 may gangpunch and punch from the output track. The following discussions cover the 323 when used as a RAMAC output device.

Punch Ready

It is necessary to place the 323 in a ready status before it can operate as an on line output device. This is accomplished by depressing the start key after placing cards in the hopper. This causes two feed cycles, and

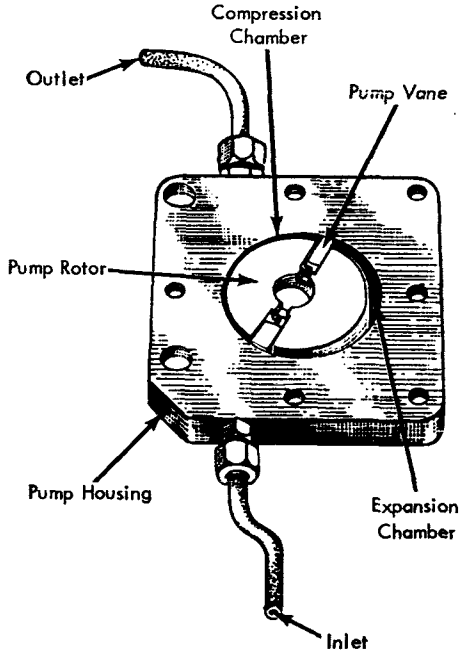


Figure 139. Oil Pump

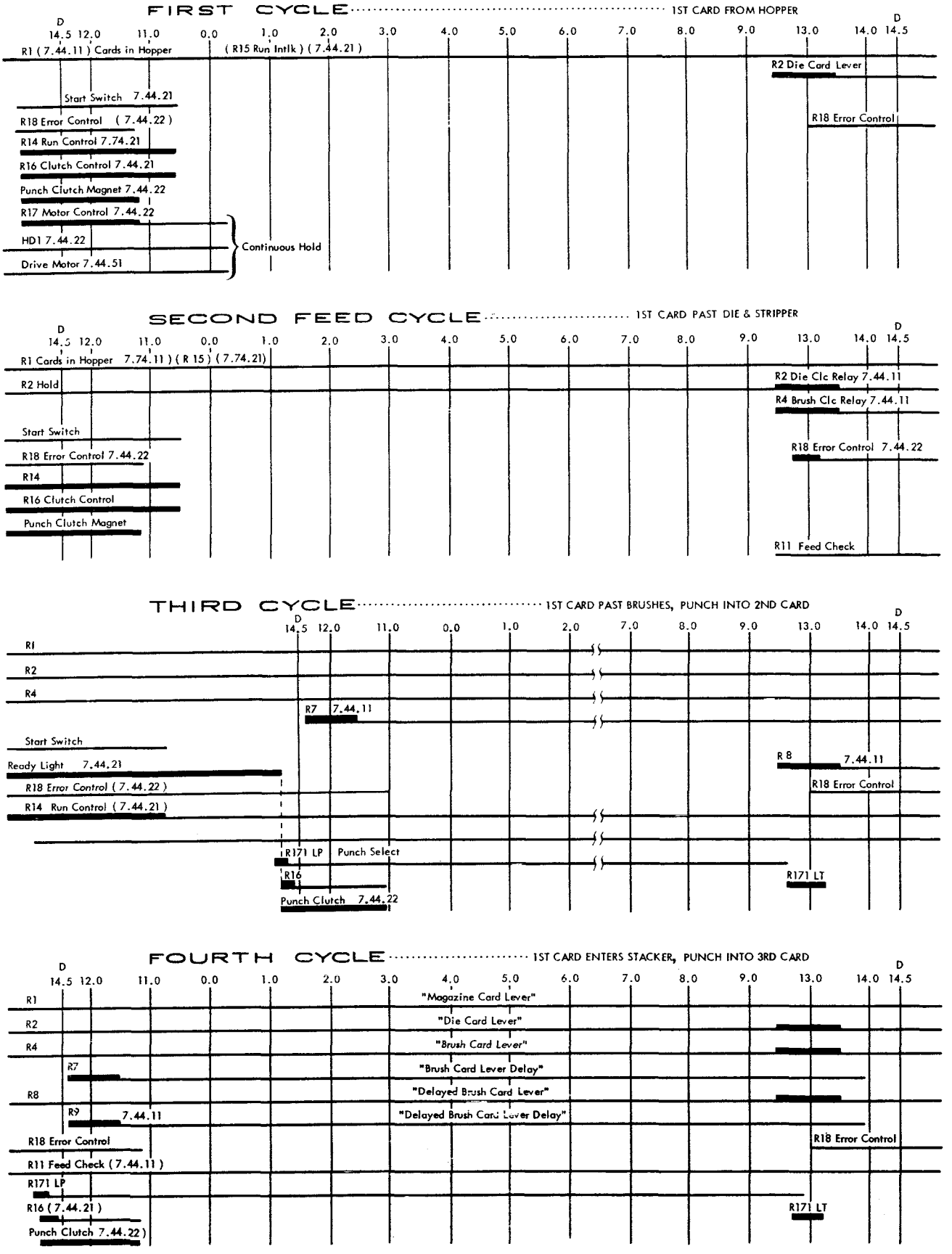


Figure 140. Punch Feed Cycles

then turns on the ready light. The second card into the 323 will be the first card punched by the RAMAC.

Once the punch is ready, feeding of cards is controlled by the process unit. Each PROGRAM EXIT impulse received at the punch hubs causes one punch feed cycle until the hopper runs out of cards. In this case, punch ready is obtained by placing cards in the hopper, then depressing the start key.

When a job is complete, cards may be run out of the feed by removing the cards from the hopper, then depressing the start key.

OBJECTIVES:

1. Energize the drive motor (7.44.51).
2. First card feed cycle (7.44.22).
3. Second card feed cycle (7.44.22).
4. Punch ready (7.44.21).

The drive motor operates when HD1 is up. HD1 picks on 7.44.22 when R17 picks parallel to the punch clutch magnet. Once the motor starts, it runs continuously until machine DC power is removed.

The first card feed cycle is obtained by impulsing the punch clutch magnet through P11 on 7.44.22. R16 picks through the start key and R15-1 N/O on 7.44.21.

The second card feed cycle is accomplished in the same way that the first is. Figure 140 is a sequence chart of card feed relay operation.

The punch ready light glows when R18 on 7.44.22 picks with R16 down. R16 does not pick because R4-6 N/C is transferred. The circuit for the light passes through R11-1 N/O on 7.44.21. R11 picked late in the second card feed cycle.

Punch Select Feed Cycle

Each program exit impulse into the punch hubs on the 305 control panel causes one punch feed cycle. When this happens R16 on 7.44.21 is picked through R171-3 N/O on 7.44.22, providing the punch is ready. The CR cam in this circuit is timed to close one index division after each tooth of the punch clutch ratchet passes the latch position. R16 energizes the punch clutch so that the clutch pawl will engage the next ratchet tooth. During this cycle, data will be selected by control panel wiring from the output track, and will be punched into the card passing the die and stripper. The punching circuits will be covered later. In Figure 140 the third and fourth cycles are examples of relay operation during a punch select cycle.

Punch Not Ready

Whenever data is being punched the transfer of new data to S track is prevented by the punch not ready line on 3.02.08. This input keeps the not W cycle gate line high. The punch not ready line is high whenever the punch select relay, R171 on 2.07.03, is up. R171 is latch tripped just after 9 time punching. On the third feed cycle this impulse passes through R9-2 N/C on 7.44.31. On the fourth and successive cycles it must pass through the DPBC relay points. DPBC checks are made only from the fourth feed cycle on. R171 is latch tripped if there has been a successful DPBC check or if the DPBC stop hubs are not wired. The R171 LT impulse also passes through R22-1 N/C on 7.44.22. This insures that a successful parity check of S track has been made. Parity check and DPBC are discussed later.

If the punch takes only one punch cycle, punch ready is obtained when R18 picks. It picks through its hold coil and R171-3 N/C on 7.44.22.

Punching Circuits

Control panel flexibility allows data from any S track character to be punched in any column of a card. The bit data on S track must be translated to Hollerith code impulses at the appropriate output track hub to do this. Then a wire from the output track hub to a punch magnet hub causes punching. The logic of this translation is shown in Figure 141.

Whenever the digit impulse CB's make, all characters of S track must be analyzed to determine if their associated thyratrons should fire. This is possible because each CB impulse is 23 milliseconds long, which is equivalent to 2⅓ drum revolutions. A thyratron fires if, at a given impulse and character time, the gated data and decoder output compare equally. At BR of the character analyzed, a punch gate is developed if there is an equal comparison. Do not be misled by the words "punch gate." The signals on the punch gate line are actually BR pulses. The character timing of the punch gate determines which thyratron fires.

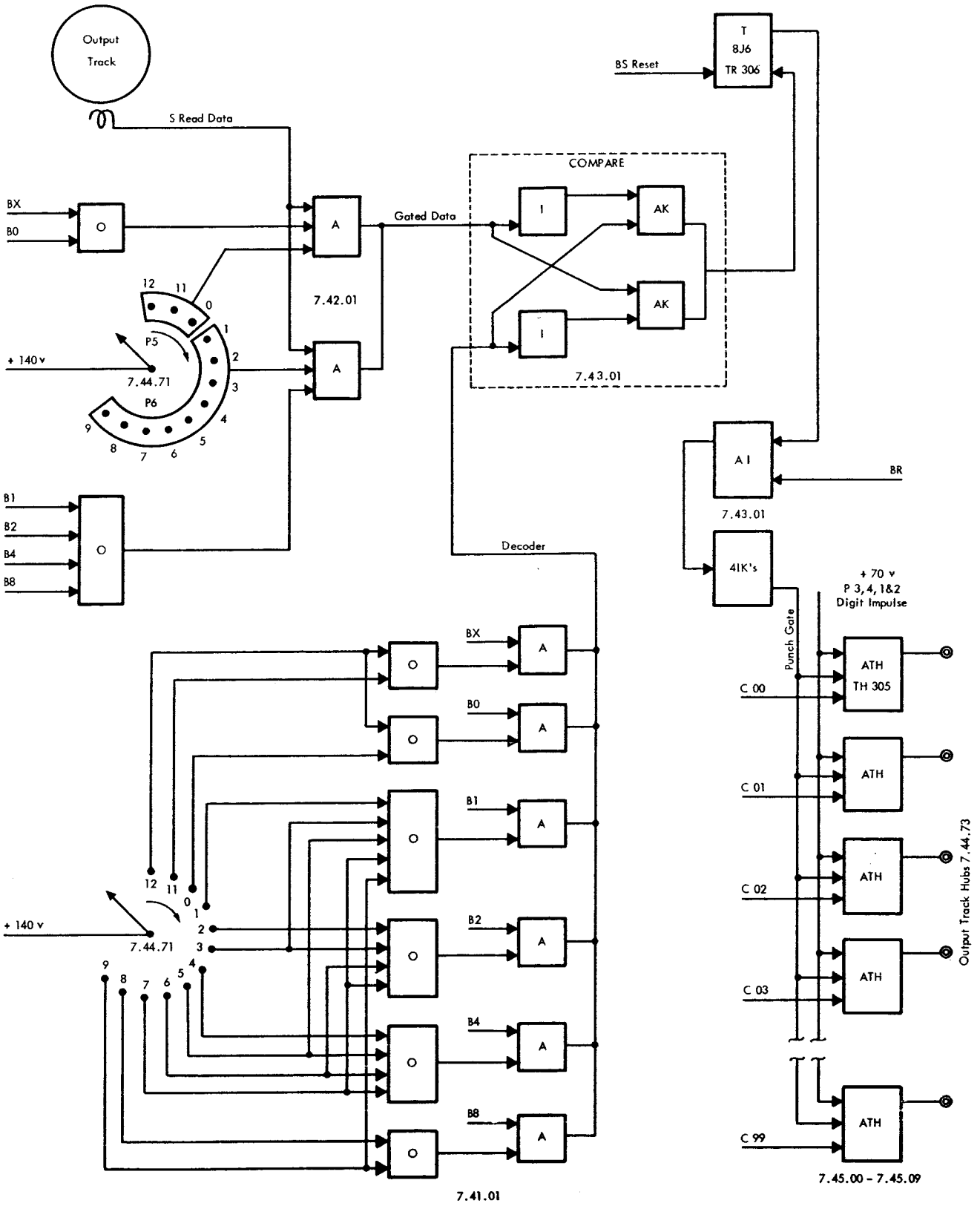
OBJECTIVES:

1. Gated data (7.42.01).
2. Decoder output (7.41.01).
3. Equal compare (7.43.01).
4. Punch gate (7.43.01).
5. Fire thyratron (7.45.00 - 7.45.09).

The following describes the development of the above objectives when a Bx and B0 are sensed in C01 at 12 impulse time. Refer to Figures 141 and 142 when developing these objectives.

Gated data is developed whenever there are 3 coinciding inputs to either of the "and" switches on 7.42.01. In this example 8F6b conducts during Bx and B0 time.

The decoder output consists of Bx's and B0's as long as the punch emitter is made for 12.



NOTE : Additional Circuitry is Required to Accomplish the Translation of Special Characters Having 3 -8 or 4 -8 Combination .

Figure 141. Punch Translation Logic

An equal comparison occurs at C01 time because the inputs are equal.

A punch gate is developed at BR of any character whose inputs to the comparator are equal. The trigger at 8J6 is not flipped when this gate is developed. The trigger is flipped when a character is not to be punched. The trigger is reset after each character at Bx time.

A thyratron fires during digit impulse time when the punch gate coincides with the thyratron's character input, C00BR *in this example.*

Translation of 8-3 and 8-4 Combination

Most special characters have an 8-3 or 8-4 Hollerith code combination as seen in Figure 1. Because of this the punch translation logic of Figure 141 is modified on the machine. Analysis of Figure 1 shows that the modification of the translation circuitry must accomplish the following objectives. If the character contains:

B1 + B2 + B8	a 3 and 8 must punch.
B4 + B8	a 4 and 8 must punch.
B8	An 8 must punch.
B1 + B8	An 8 *must not* punch.

The above objectives are accomplished by controlling the trigger 8J6 to originate a punch gate when you need it.

OBJECTIVE:

Punch 3 or 4 with a B8 present (7.42.01).

When the 323 emitter is making on its #3 spot or its #4 spot, the decoder circuit supplies B1 and B2 pulses or B4 pulses, respectively. A character on the output track may include a B8 in combination with a B1 and B2 or a B8 in combination with a B4. In either of these cases the presence of the B8 in a character must be prevented from destroying the comparison between the gated data and the decoder pulses. For this reason, B8 pulses are excluded from the gated data when the 323 emitter is making on its #3 spot or its #4 spot. This is accomplished on 7.42.01 where the inversion of EM 4 or EM 3 prevents B8 pulses from being gated through 8C9b.

OBJECTIVE:

Punch 8 with B8 present (7.43.01).

At 8 emitter time to insure that an 8 is punched when a B8 is present, the lower half of the comparator is crippled. This is done through 8G6b on 7.43.01. With this unit operating a B8 must be in the gated data or the trigger 8J6 is flipped. With a B8 present 8J6-10 remains high at BR and a punch gate is developed.

OBJECTIVE:

Not punch 8 with B8 and B1 present (7.43.01).

The previous objective showed how an 8 is punched when a B8 is present. The objective is now to suppress B8 punch gate when a B1 is present. This is accom-

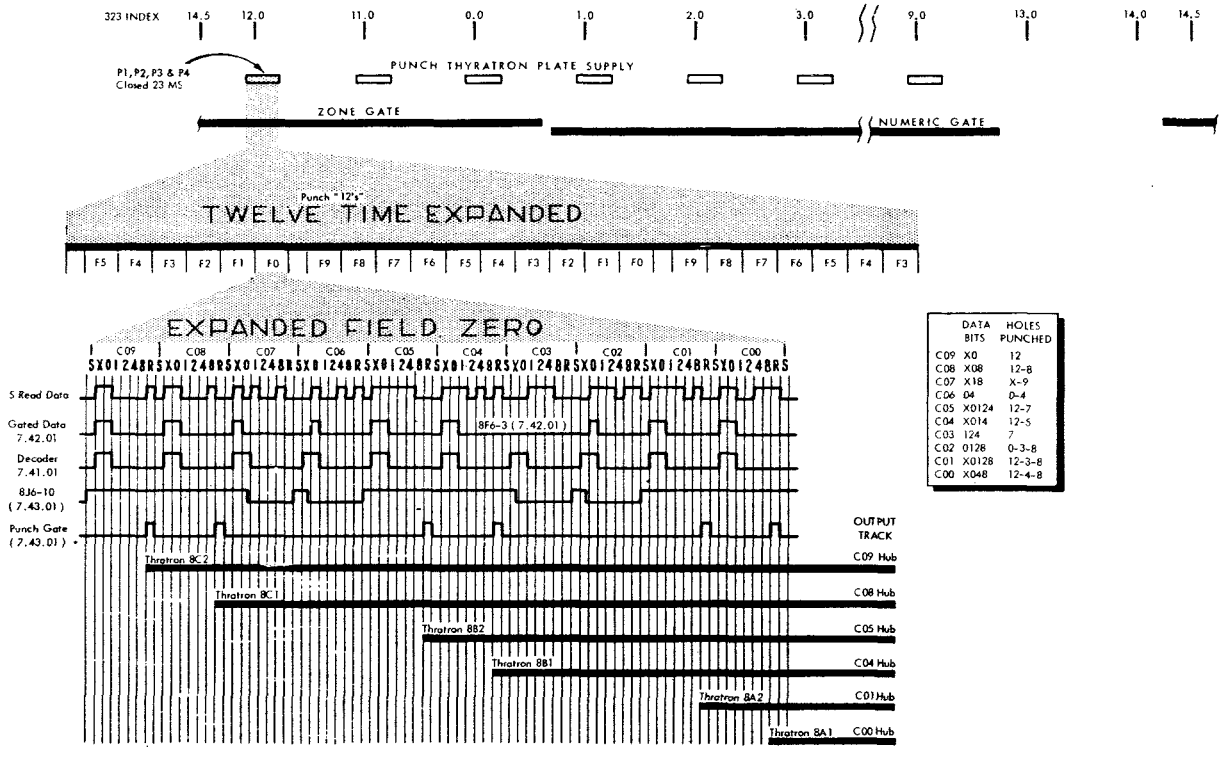


Figure 142. Punch Gate Development

plished by flipping 8J6 pin 10 low. 8H6-5 receives B1 ⌀C impulses from 8H7b when this condition exists. This impulse flips 8J6 pin 10 low to prevent punching.

Punch Parity Check

When data is being punched, a parity check is made of all data on the output track. If there is a parity error, the punch will stop at the end of the punch cycle. The punch not ready line remains high. The punch parity light glows. With the punch not ready line high, a $T_2 = S$ instruction may not be performed.

The card being punched when a parity error occurs, may or may not be in error. If the error character is not wired to punch, the card will be punched correctly. The operator may determine which character is in error by reading S track from the console. Parity error characters will be underlined by the typewriter.

Manual Correction of Parity Error Card

The procedure to manually correct the card follows:

1. Depress the console check reset key.
2. Read the output track. Error characters are underlined.
3. Depress the program start key.
4. Remove the cards from the punch stacker. Depress the 323 check reset and start keys. The second card to reach the stacker is the error card.

Repunching of Parity Error Card

Following is the procedure to eliminate the error card and to cause the controlled data to be punched into a new card:

1. Depress check reset key at console.
2. Read the output track. Error characters are underlined.
3. Correct the output track data and transfer corrected data back to output track.
4. Depress the program start key.
5. Remove the cards from the 323 hopper.
6. Depress the 323 start key to run the cards out of the punch feed.
7. Depress the 323 check reset key.
8. The last three cards must be removed from the stacker. The next to last card is the error card; replace it with a new card. Place these three cards at the front of the deck removed from hopper, and return the deck to the hopper.
9. Depress start key to cause run-in and to re-establish automatic operation.

The new card will be punched with the corrected output track data and processing will continue from that point.

OBJECTIVES:

1. Detect parity error (7.44.51).
2. Punch not ready (7.44.22).
3. Correct S track data.
4. Run cards from feed.
5. Remove parity error interlock.
6. Run cards into feed.
7. Punch second card into feed.

Parity error checks are made on the output track whenever the punch select relay is up. When the parity error relay (R22 on 7.44.51) is up, a parity error has been detected. The parity control trigger on 7.75.01 counts the bits in each character on S track. If the bit count is even, the thyratron 8C10 fires through R171-4 N/O to pick R22.

Punch not ready is maintained when a parity error occurs by not latch tripping the punch select relay, R171 on 2.07.03. R22-1 N/C on 7.44.22 opens the latch trip circuits.

S track data is corrected by a console read, alter, write operation. The details of this operation are discussed in the Console section of this manual. The console check reset key should be depressed before the read, alter, write operation. The program start key should be depressed after.

To remove the cards from the feed it is necessary to empty the hopper, then depress the 323 start key. When the hopper card lever relay drops, R1-3 N/C on 7.44.21 allows the start key to pick the clutch control relay, R16. Reference to Figure 143 shows that the next to last card into the stacker is the error card.

The parity error interlock is maintained by R22. Depressing the punch check reset key drops R22 on 7.44.51. However, this does not latch trip the punch select relay. This cannot be accomplished until after the delayed brush card lever relay, R8, picks. R8-5 N/O on 7.44.22 prevents tripping the punch select relay. When R8 picks the corrected S track data has been punched into the second card into the feed.

Cards are run into the feed by depressing the start key. This causes two feed cycles just as a normal run-in operation does. A third feed cycle occurs because R171 is up. R16 on 7.44.21 picks through R4-6 N/O and R171-3 N/O on 7.44.22. This third cycle is the cycle when the corrected data is punched.

Punching the second card into the feed is accomplished because R171 starts the feed cycle. Just before this cycle the brush card lever relay, R4, picks. This relay must be made, for any punching to take place. When it is down it prevents the first card into the feed from being punched. The R4-11 N/O point on 7.44.71 allows emitter impulses to the decoder. Decoder output is necessary for punching from the S track.

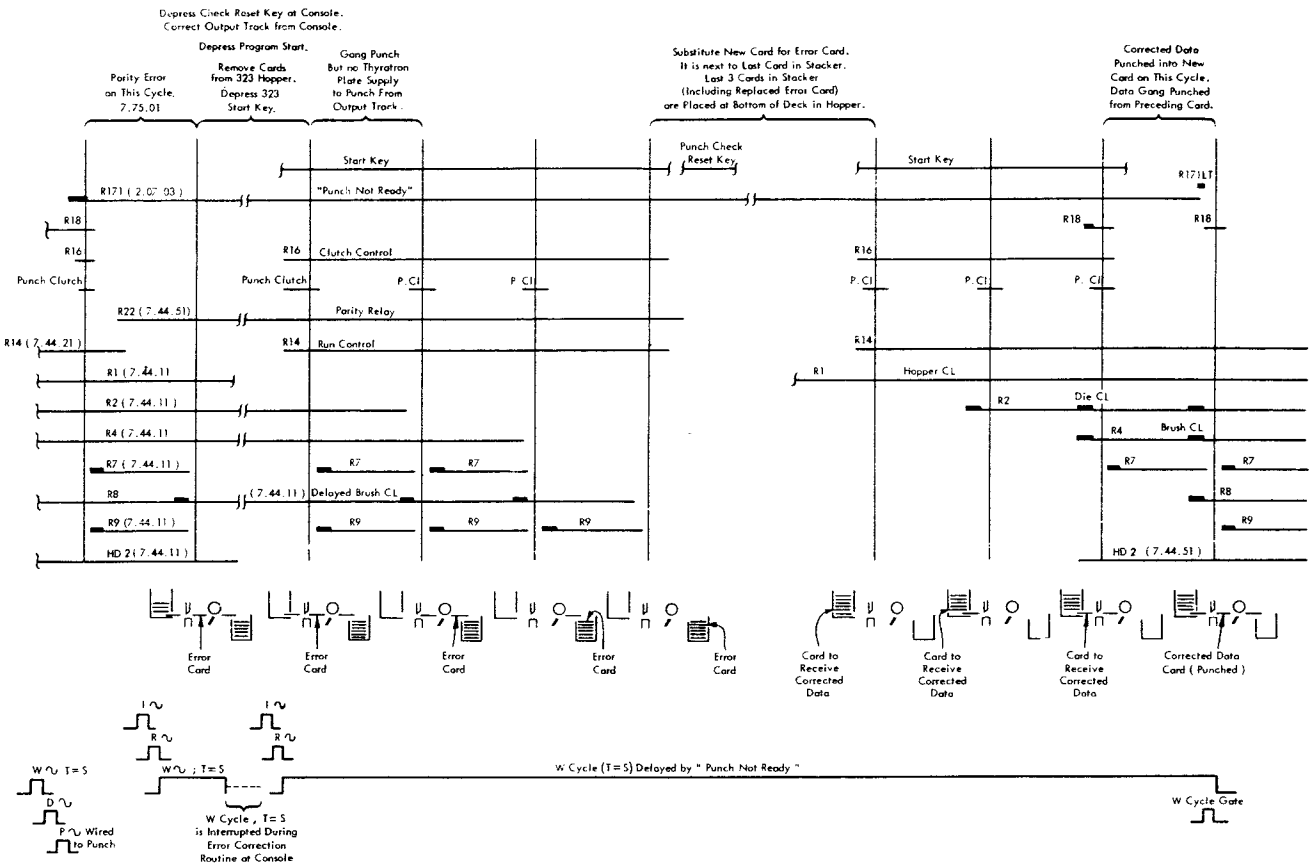


Figure 143. Correction of Parity Error Card

Punch Repeat

Punch repeat allows a 323 to take two punch cycles for each PROGRAM EXIT calling for a punch out operation. The format of the second card may be changed by using co-selectors. The co-selectors would be picked by the PUNCH REPEAT OUT impulse. This impulse is available only at the beginning of the second punch cycle.

Punch repeat may be initiated by the same PROGRAM EXIT that impulses punch select. This impulse must be wired to the punch repeat P hub via a communication hub. Punch repeat may also be initiated by impulsing the punch repeat D hub. The D hub should be wired from an output track hub via a digit selector. A sequence chart showing a punch repeat operation is shown in Figure 144.

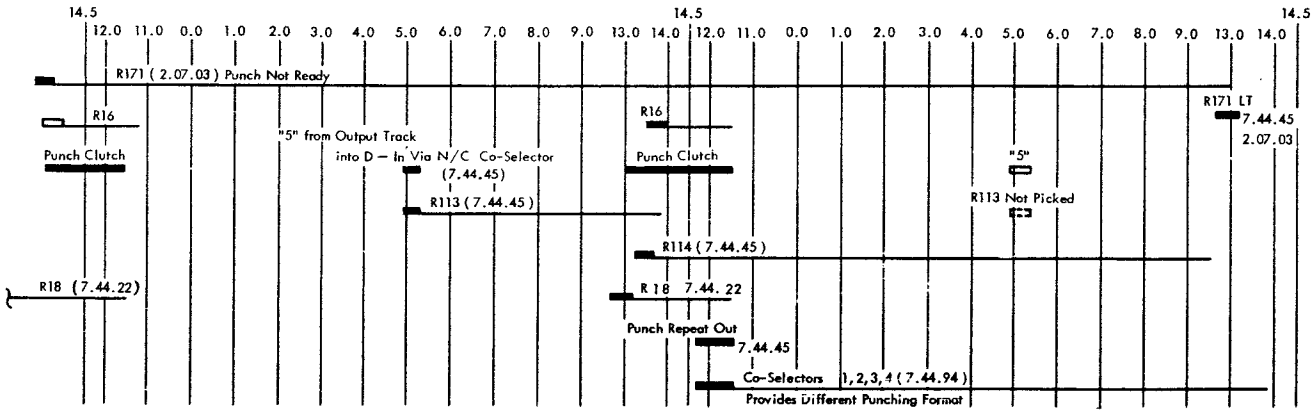


Figure 144. Punch Repeat

OBJECTIVES:

1. Start punch repeat (7.44.45).
2. Keep S track interlocked (3.02.08).
3. Energize punch clutch second time.
4. Punch repeat out impulse (7.44.45).

Punch Repeat is started by picking R113 on 7.44.45.

S track remains interlocked for the second cycle because R113-3 N/C prevents tripping the punch select relay. This does cause error control relay, R18, to pick though.

The punch clutch is picked a second time by R16-2 on 7.44.22. R16 is picked through R18-2 N/O since R171 is still up.

The punch repeat out impulse on 7.44.45 passes through R1-5 N/O on 7.44.45 and P12. Circuits are provided to remember the punch repeat status when correcting a parity error card. Figure 145 describes this operation.

Sign Conversion

A Bx in the units position of a number indicates that the number is negative. If the units position digit of a negative number is zero, the bit structure of the character is Bx, B0 and BR. Punch translation decodes the Bx and B0 into a 12 time impulse. However the units position should be punched with an 11 and a 0 punch, not a 12 punch. The sign conversion circuits convert a 12 time impulse into 11 time and 0 time impulses.

The circuits are on 7.44.41. The units position output track hub should be wired to one of the sign conversion in hubs. The corresponding sign conversion out hub should be wired to a punch magnet hub. The only impulse that is changed when it enters an in hub is a 12. All other impulses travel through the two normally closed points to the out hub. R55 picks during 12 time. If a 12 impulse is received at an in hub, R55 N/O points allow picking of an impulse relay, for example, R81. The impulse relay -2 point then allows 11 time and 0 time impulses to reach the out hub.

Column Split

It is often desired to provide a different assignment for a 12 or 11 impulse than is afforded the numeric impulse emitter from the same output track hub. In

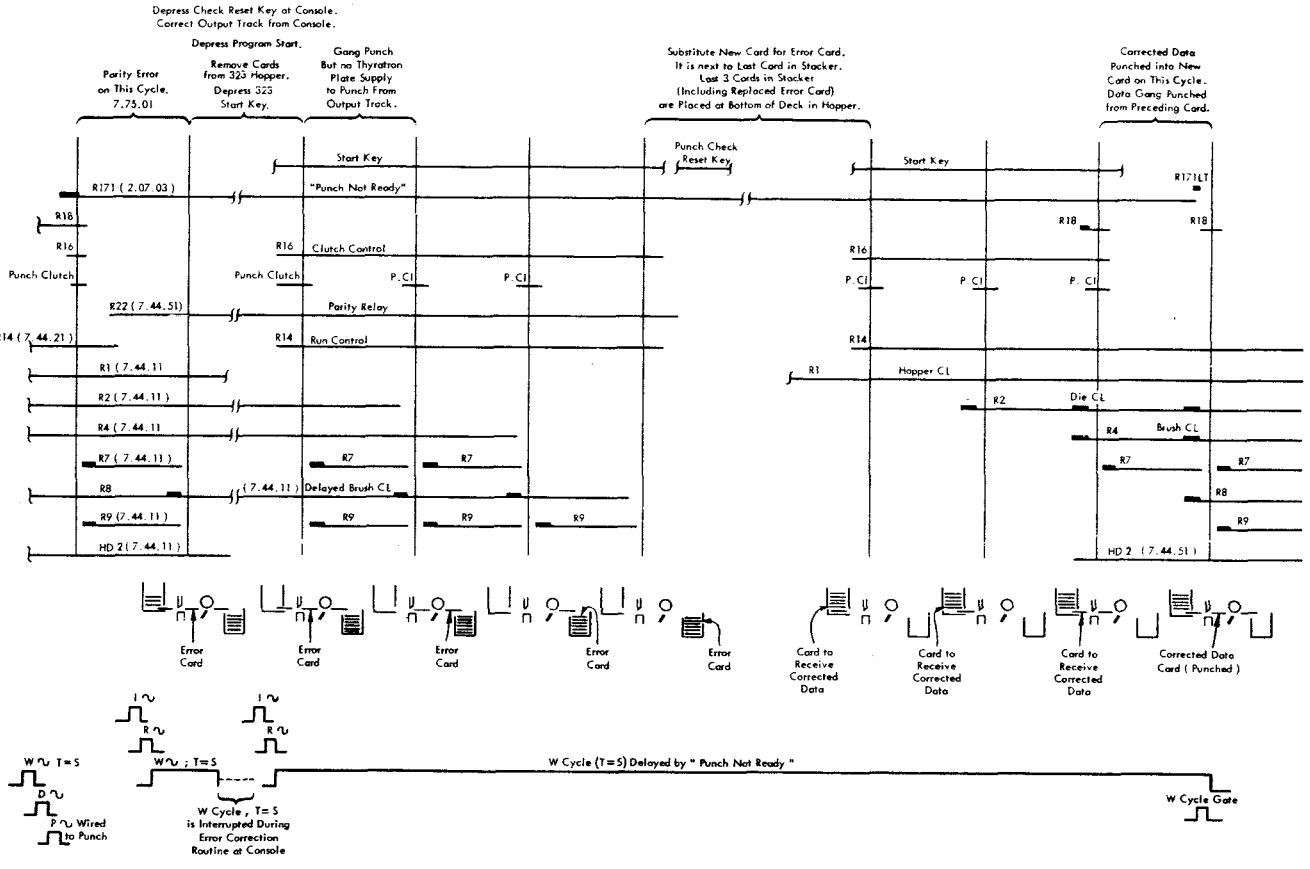


Figure 145. Delay of Punch Repeat During Error Correction

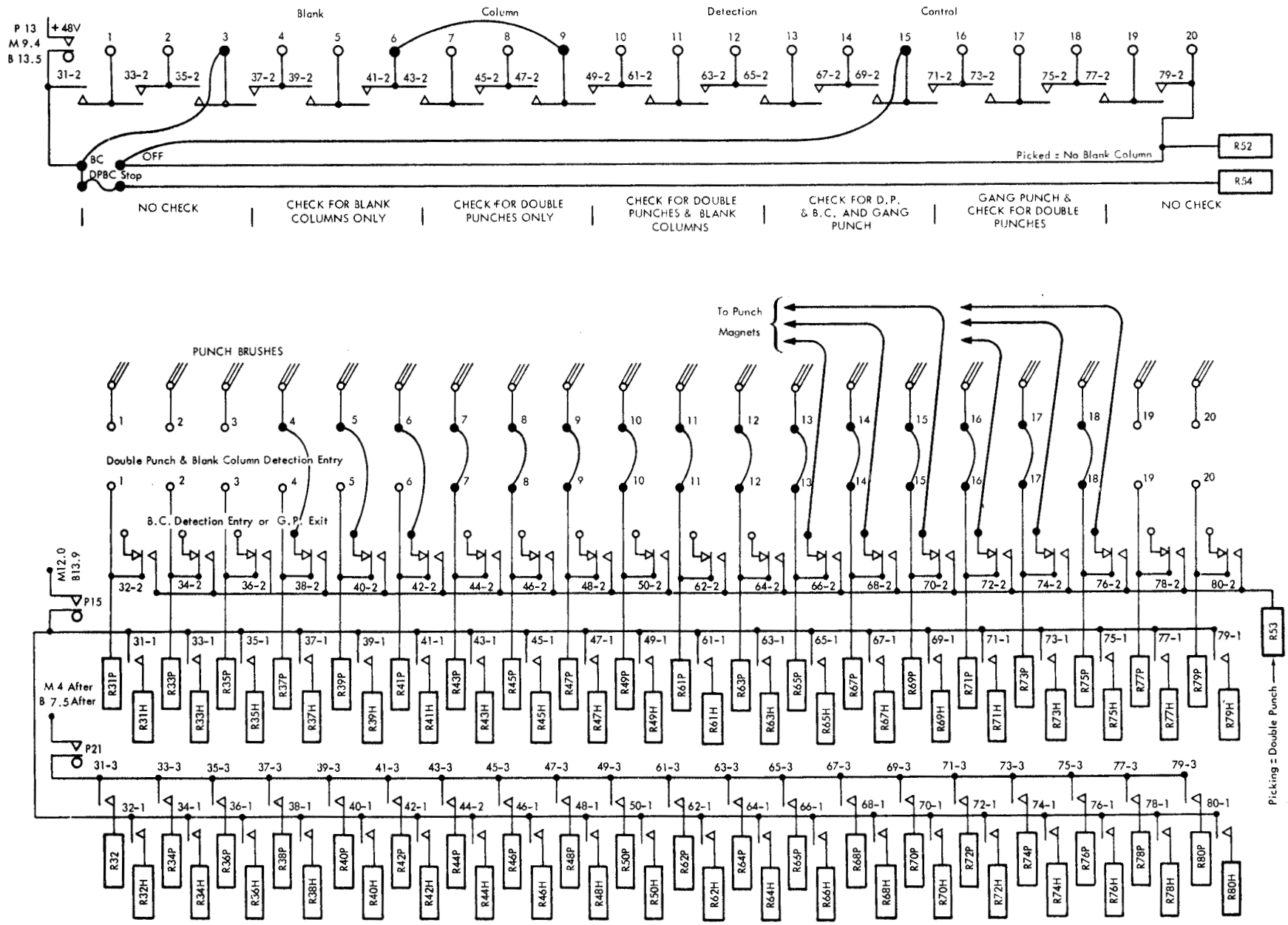


Figure 146. Double Punch and Blank Column Detection (7.44.31 - 7.44.33)

such a case, the output track hub may be wired through a COLUMN SPLIT. 12 or 11 time impulses received at the column split common hub will be emitted from the 11 – 12 hub (7.44.61). Numeric impulses received at the common hub are emitted from the 0 – 9 hub.

Ten positions of column split are included on the 323 control panel. Each position is controlled by a point of R27, which is energized during the time that P16 is closed, 14.6 to 11.6.

Double Punch and Blank Column Detection

The 323 is provided with 20 standard and 60 optional positions of double punch and blank column detection. This feature permits any column of the card to be checked for either double punches, blank column, or both. The 323 may be wired to stop or offset stack the error card, or both, if a double punch or blank column is detected. Figure 146 shows the flexibility of this feature.

DPBC detection is accomplished as the card passes the punch brushes. The data from which the card was punched has already been replaced on S track when the DPBC check is made. For this reason error cards must be corrected manually. If DPBC STOP is wired, the first card to reach the stacker on a restart is the error card.

If inspection reveals that the error is in a gang punch field, all cards must be removed from the feed and a punch restart made.

OBJECTIVES:

1. Detect blank column (7.44.31).
2. Detect double punch (7.44.31).
3. Stop punch feed (7.44.22).
4. Interlock S track (3.02.08).
5. Restart punch.

A blank column is detected just after 9 time if the blank column control relay, R52 on 7.44.31, is not picked. Each punch brush wired for blank column detection must pick its DPBC detection relay. This will complete the test circuit to pick R52.

A double punch is detected when the double punch control relay, R53 on 7.44.32, is picked. R53 is picked when the second hole of a column wired for double punch detection is sensed. It picks because the first punch sensed transfers the dash two point of the position wired.

The punch feed stops because the circuit to pick the clutch control relay, R16, is open at R18-2 N/O on 7.44.22. R18 is down because it cannot pick through R171-3 N/C. R171 is not latch tripped because all the relay points between P14 and P23 on 7.44.31 are transferred. R51, the DPBC stop relay, is picked instead.

S track interlock is accomplished when the punch select relay, R171 is up. The reasons for this are explained above. R171 up develops the punch not ready line on 3.02.08.

Punch restart is accomplished by depressing the 323 check reset key, then the start key. The check reset key trips the punch select relay through R51-3 N/O on 7.44.22 and drops R51 on 7.44.31. The start key repicks the run control relay, R14 on 7.44.21.

Optional Features

Offset Stacker

The offset stacker provides an alternate method of indicating DPBC errors. If the offset stacker hubs are jackplugged (7.44.99), any card containing a DPBC error will be stacked in an offset position from the other cards in the stacker. The DPBC stop hubs (7.44.31) may be left unwired so that a DPBC error will not destroy continuous operation.

The offset stacker device consists of a split stacker roll and a cam assembly, a pair of cam fingers, and a magnet that controls the operation of the cam fingers (Figure 147).

The two cam fingers are so arranged (mechanically) that they operate simultaneously, and one controls the operation of the other. One cam finger latches on the magnet armature. It carries a stud, which operates the other cam finger. This assures that the two cam fingers operate at the same time and permits them both to be controlled by a single latch. When the cam fingers are

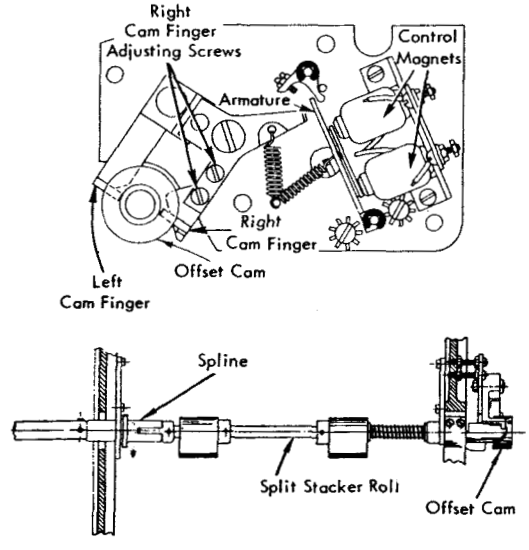


Figure 147. Offset Stacker

latched in an open position, they clear the cam surface and are inoperative. When the magnet coil is energized, the armature is attracted, and the cam fingers are released and allowed to close about the cam shaft. As the stacker roll revolves, the cam surface causes the stacker roll to be carried toward the front of the machine. The stacker roll has a split shaft, splined so that it may be driven in either a normal or extended position. At the end of the cycle the restoring cam carries the cam fingers beyond the latching point and knocks the armature away from the cores. With the cam fingers relatched, the stacker roll is free to be returned to its normal position by spring tension.

Since the unpunched or double punched column is sensed by the punch brushes one cycle before the card reaches the stacker, the operation of the offset stacker magnet is delayed for one cycle until the card containing the blank or double punched column is being stacked.

On 7.44.99 R111 must be energized in order to provide a P18 impulse to the offset stacker magnet. When the offset stacker hubs are jackplugged, a circuit is provided to R111 by the energization of R53 or the failure to energize R52. This is a P14 impulse supplied from 7.44.31 at 9.7 to 13.2 of the cycle during which the error is detected. Once picked, R111 holds through P17 until 9.5 of the following cycle, thereby providing a circuit to the offset stacker magnet from 0.5 to 2.5.

Pilot Selectors

Ten pilot selectors are available on the 323. Each of these has a P exit or immediate pick up hub and a delay pick up hub.

An impulse into the P exit pick up hub for pilot selector 1 latch picks R231 and transfers the selector points immediately (7.44.92). This hub is designed primarily to receive 305 PROGRAM EXIT impulses wired through a COMMUNICATION channel.

An impulse into the delay pick up hub selector 1 picks R232, which then holds until 13.9. R232-2 provides a P20 impulse to the pick of R231 at 13.2 to 13.7. Thus, the selector points will be transferred during the following cycle. This hub is intended primarily to receive digit impulses from an output track hub.

All selectors are tripped by the same impulse that trips the punch select relay in the 305 (2.07.03, 7.44.22). This impulse is provided at 9.7 to 13.2 after punching is complete.

Co-Selectors

Twenty co-selectors are available on the 323. Each selector has five sets of points. An impulse into the pickup hub for co-selector 1 picks R118, which then holds until 13.9 through P19. The points of R118 immediately alter the circuit through the selector positions so that the circuit is from C to T rather than from C to N. The circuits are on 7.44.94.

407 Accounting Machine

The 407 Accounting Machine--Models R1 and R2--is an optional RAMAC output unit. When selected by the 305, it performs a list cycle reading S track instead of a card in its feed. When on line, its card feed is inoperative. When selected by the 305, any standard 407 function may be accomplished; for example comparing, MLR, carriage controls, selection, programming, storage, counters, and summary punching. The 407 may be used off line as a standard 407.

Mechanical Principles

The mechanical principles are the same as a standard 407 Accounting Machine. The 407 Customer Engineering Manual of Instruction, Form 22-8090-4, contains descriptions of all 407 mechanical principles.

407 Circuits

Standard 407 circuits are altered so that it can perform on-line operation. The additional circuits are shown on wiring diagram 210950. All relays and CB's on this diagram are prefixed by "RA." This diagram supplements 407 diagram 123165B. The following discusses only the circuits peculiar to a Model R1 or R2.

Standard 407 circuits are explained in the 407 Customer Engineering Manual of Instruction, form 22-8090-4. **All wiring diagram references in this writeup refer to the 407 supplemental diagram unless otherwise designated.**

On Line 407 Ready

To place the 407 in a ready condition, wire its interlock hubs then depress its start key. This causes the 407 CR mechanism to run continuously, and the 407 ready light to glow. The card feed will not feed cards.

OBJECTIVES:

1. Cause CR mechanism to run continuously.
2. Prevent card feeding.
3. Pick power interlock relay (7.44.51).

The CR mechanism runs continuously whenever the drive clutch is energized. The hold circuit for the drive clutch is through the run relay point, R1638 AU N/O in section 4A of the 407 diagram. The run relay is held through a second read card control relay point, R1632 BL in 1A. The run relay picks through standard 407 circuits. R1632 is picked in 2B through RA112-6 N/O and RA112-4 N/O to the line. RA112 picks through the interlock hubs in 3A.

Card feeding is prevented by opening the circuits to the gripper clutch and picker clutch magnets. The gripper clutch circuit is opened by RA111-7 N/C in 1A. The picker clutch circuit is opened by RA111-6 in 1A. Card reading is prevented by RA131-A and B N/C points in 2A. RA131 picks in 3A when the run interlock hubs are wired.

The power interlock relay on 7.44.51 picks through RA112-10 in 3A, and CR108 in 3A of the 407 diagram. It picks on the first 407 cycle after depressing the start key. The power interlock relay points on 7.44.51 allow 340 regulated voltages to the 407.

Off Line 407

To take a 407 off line it is necessary to drop all the function interlock relays. They are relays RA112, RA111, and RA131 in section 3A. To drop RA112 and RA131, open the INTERLOCK connection. (The INTERLOCK may be wired through an alteration switch.) Then, depressing the start key will cause RA111 to drop.

407 Print Select

A PROGRAM EXIT impulse to the 407 print (select) hub on the process control panel, causes the 407 to perform a list cycle. R134 is latch picked (2.07.03) when the

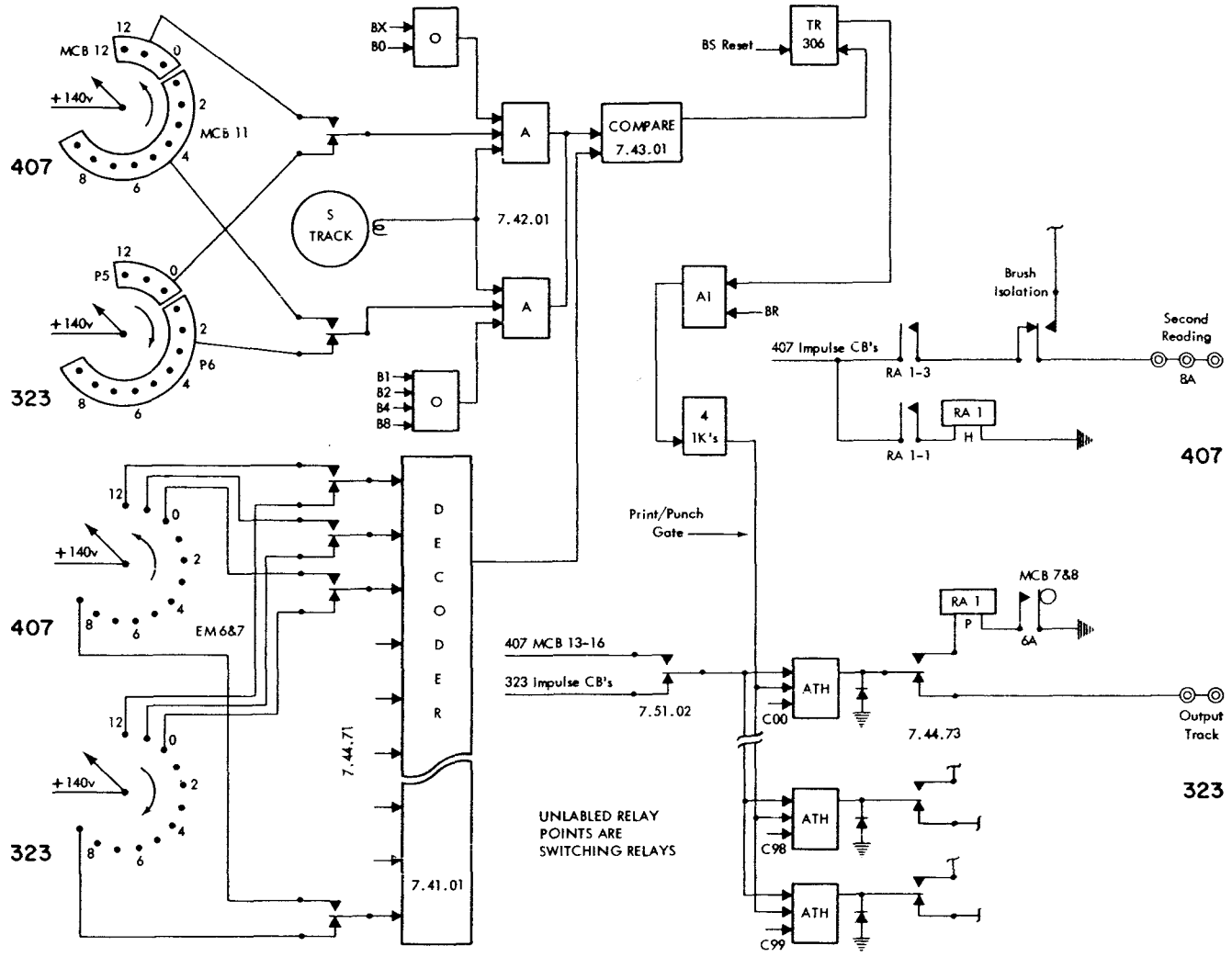


Figure 148. 407 - 323 Switching

407 is selected. This causes the next 407 cycle to be a list cycle if the impulse is received before 230° of the 407 index (see Figure 149). Printing during this cycle will be discussed later. Data on S track cannot be altered until the 407 has finished reading it. This interlock is accomplished by 407 not ready on 3.02.08. At 180° of the 407 print cycle, the 407 has finished reading S track data. R134 LT is energized (2.07.03) through SCL-40 to 1A of the Supplement through CRRA 9, RA111-7 N/O, to CR30 in 7A of the 407 diagram. This allows 50° (about 55 milliseconds) for writing new data on S track and selecting the 407. Therefore, it is possible to have successive list cycles.

407-323 Select

Whenever the same PROGRAM EXIT is wired to the 407 print (select) and the punch (select) hubs on the 305 control panel, 407 printing will precede 323 punching. This sequence is controlled by relays 133, 134, and 135 in the 305. Relays 134 and 171 on 2.07.03 are latch picked simultaneously when this happens. R134-2 N/O allows a 407 list cycle on 2.07.03. The 323 punch cycle is held up because R135-6 N/C prevents a pick of R16 on 7.44.22. R134 is latch tripped at 180° of the 407 list cycle through CRRA 9 in section 1A. R16 picks through R135-1 N/O. R135 was picked through R171-3 on 7.44.22. R16 then allows a punch cycle. At the end of the punch cycle, R171 and R133 are latch tripped.

On Line Printing

When the 407 prints, switching relays in the 323 connect it to the punch translation logic circuits shown in Figure 141. Figure 148 shows how this is accomplished. The thyratrons, instead of developing an impulse at the 323 output track hubs, pick high speed permissive make relays in the 407. These relay points

allow 407 master CB impulses to the second reading hubs. Each permissive relay pick then is similar to reading a hole in a card at the second read station.

Printing circuits are best described by using an example. The following assumes the 407 to be performing an on-line 407 list cycle. It can be applied to the printing of a 5 from C00 of S track. Figure 149 shows relay operation for printing a 5 from C00.

OBJECTIVES:

1. Pick switching relays (7.51.02).
2. Pick read relay (3B).
3. Develop print/punch gate (7.43.01).
4. Fire thyratron (7.45.00 - 7.45.09).
5. Pick print relay (6A).
6. Hold print relay through impulse time (6A).

The switching relays pick to synchronize the punch translation logic to the 407. They pick on 7.51.02 through RA130 B N/O in section 2A. Their hold is through CR82 in 2A until 180°. When they drop, punch translation logic is synchronized to the 323 so punching can begin.

The read relay, RA109, picks in 3B through the R1422-1 N/O point (feed control relay). It is up during

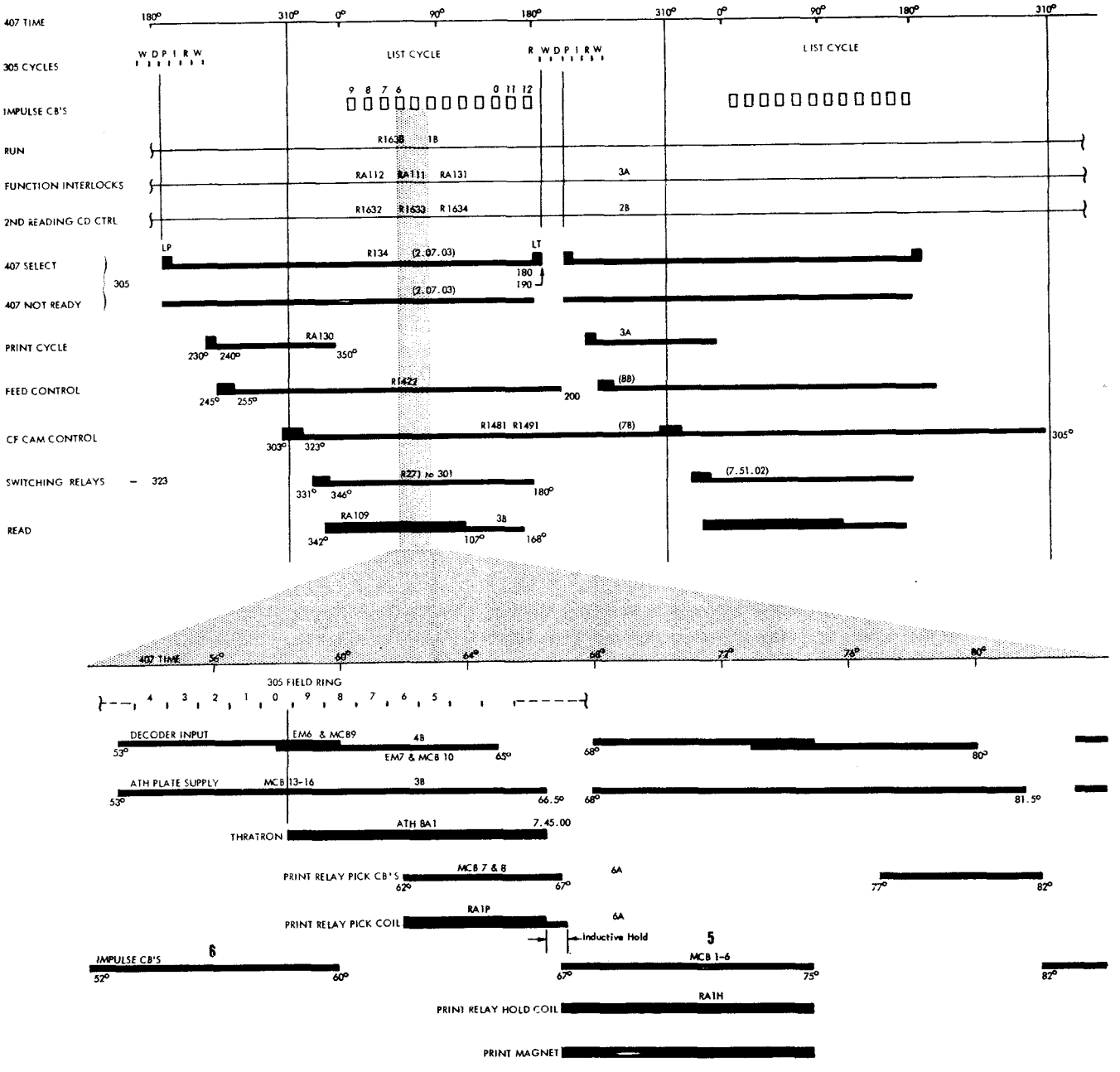


Figure 149. Printing a "5" from C00

read time only. R1422 picks in 8B of the 407 diagram. The pick circuit is modified by RA130 AL and RA112-7 in 1B. RA130 is picked in 3A through CRRA 2, and a 407 select relay point, R134-2 N/O on 2.07.03.

The print/punch gate develops the same way the punch gate develops. A description of this development is in the 323 section. However, there is a modification to the circuits which prevents development of a print gate until a full character has been analyzed. This modification is necessary because the thyratron plate supply and the decoder input occur at the same time. Since these two signals are not synchronized with the 305, they may begin at the middle of a character. If this happens, the first character can be incorrectly compared and a print gate developed in error.

The pluggable units 8J7 and 8K6a are added to prevent this false print gate. 8J7-3 rises slowly and falls rapidly. This prevents development of a false print gate for the first and last character.

Figure 150 shows how this is accomplished. The emitter gate is high, searching for "5's" on S track. C07 data is a 4. If 8J7-3 rose immediately a false print gate would have developed since the decoder could not emit a B1 before the emitter gate went high. Similarly a B1 in C84 was prevented from firing a thyratron when 8J7-3 fell quickly.

The thyratron fires as soon as it has coinciding print gate and character inputs through the plate supply CB's.

The print relay picks through the thyratron when or after MCB's 7 and 8 make. The circuit for picking a print relay runs from ground through MCB8 and the relay coil in section 6A; to 7.44.73 through a N/O switching relay point; to the thyratron.

Print relays hold through the impulse CB's. If the impulse CB's are at their extreme low tolerance, the print relay pick coil is held by its inductive kick back circuit after the thyratron stops firing. This circuit runs from ground through MCB's 7 and 8 and through the diode attached to pin 10 of the thyratron to ground. The print relays hold circuit starts in 6A and runs through RA131-A and B N/O points in 2A, and the impulse CB's in 26A of the 407 diagram.

Parity Check

A parity check of all S track data is made each time the 407 is selected by the 305. If a parity error is detected, the 407 parity error light glows and the 407 parity error hub emits an impulse. This impulse may be wired to MACHINE STOP to cause the 407 to stop at the end of the list cycle. When this happens, S track is interlocked. To remove the interlock, depress the 407 parity reset switch, then the start key.

OBJECTIVES:

1. Parity check S track (7.75.01).
2. Indicate parity error (7.75.01).
3. Stop 407 (30A - 407 diagram).

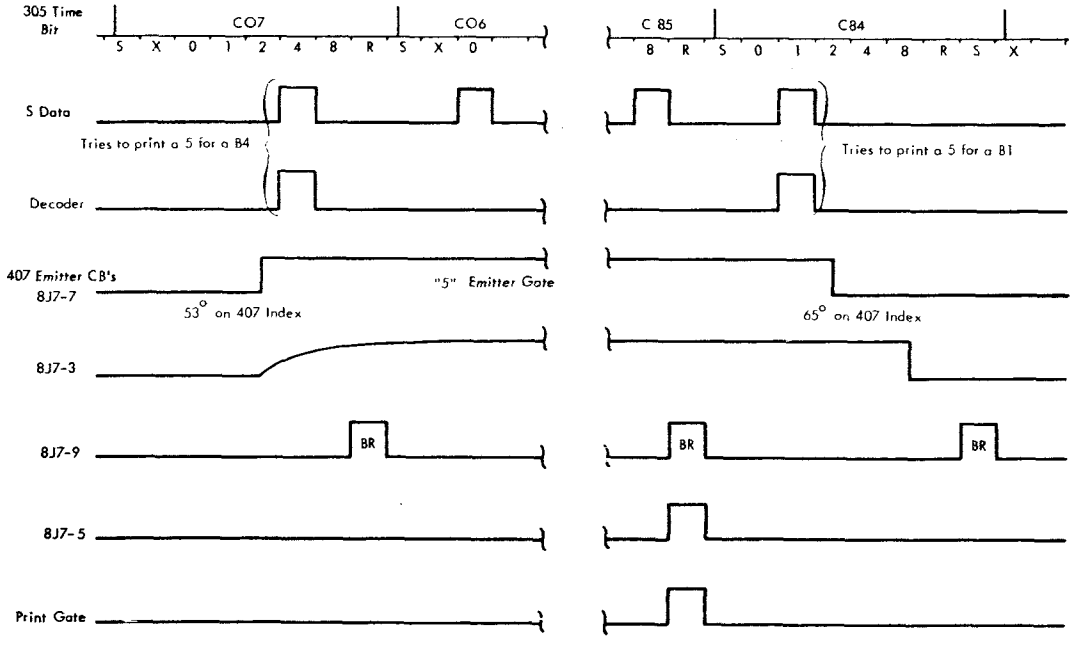


Figure 150. 407 Print Gate Control (7.43.01)

4. Interlock S track (3.02.08).
5. Clear interlock.

S track parity check occurs on 7.75.01.

Parity errors are indicated when the thyratron 8C11 on 7.75.01 fires. It fires at Bs∅B following a character, when 8D9-10 is left high, if 8C11-7 and 8 are high. 407 not ready is high when the 407 is selected. 8C11-6 is high when CR41 in 3A is made. RA109-2 N/O allows the error 1 relay, RA113, to pick during S track read time only.

The 407 stops when the parity error impulse is received at the stop hub. R1464 in section 30A of the 407 diagram picks to cause a normal 407 stop manual start.

S track interlocks when the 407 select relay, R134, is up. The trip circuit to R134 is open at RA113-5 N/C. 407 not ready on 3.02.08 prevents a W cycle gate when T = S.

The interlock is cleared by depressing the parity reset switch, then the start switch. RA108 in section 3B picks after the error 1 relay picks. While up, it nullifies the 407 start key with its - 3 N/C points in section 1A. RA108 drops when the parity reset switch is depressed (3B). 407 ready is obtained by depressing the start key. This also allows CRRA 9 in 1A to trip the 407 select relay, thus releasing S track interlock and developing 407 ready.

Error Print

An asterisk prints to indicate a parity error when the 407 error print hub is wired to a lower zero print hub. This will not stop the 407; however, the stop hub could be wired also. The parity error light remains on after an error, until the parity reset switch is depressed. RA113-6 N/O, and error 1 relay point in section 3B, allows the asterisk entry CB impulse to reach the error print hub.

Program Exit Translator

The program exit translator in hubs accept program exit impulses from the 305 control panel via communications hubs. Translators may be used only when picking pilot selectors and impulsing the last record hub. The PROGRAM EXIT used must be the same as that used for 407 PRINT (select). The translator converts the program exit impulse into a 407 timed 10° impulse, occurring at 318° of the first list cycle following reception of the impulse. The translators are in 4A of the 407 supplement.

Multiple Line Read

The MLR hubs in 2A of the supplement may be wired from a 305 PROGRAM EXIT via communication hubs to start a MLR operation. The PROGRAM EXIT used must also be wired to 407 PRINT. The MLR hubs may not be wired from a PROGRAM EXIT TRANSLATOR. All standard MLR controls remain the same.

Record Ahead Control

When 407 counters are used to accumulate, they may be controlled for programming the same as an off-line 407 by simulating cards feeding through the 407. This is accomplished by carrying two complete input records in the 305 program. The data to be printed and the control data for the next item to be printed can be assembled and transferred to S track. In this way, control data for the next item is available one list cycle ahead, just as it would be if wired from first reading in an off-line operation. The comparing unit can then be used to compare control data and initiate program cycles. An example of wiring to accomplish this is shown in Figure 151. Counters controlled by this wiring may be "run-in-reset" by wiring the RI - ON hubs (2B-supplement). The reset occurs the first time the 407 is selected. This run-in-reset will function the same as a standard 407 run-in total cycle. Print suppression will occur. The counters wired will clear. Relay sequence is shown in Figure 152.

RUN IN RESET OBJECTIVES:

1. First 407 select.
2. 407 program start.
3. Suppress printing (1A).
4. Reset counters.
5. Fail to read S track.
6. 407 ready.

The first 407 select impulse causes the 407 to perform an S track read cycle.

407 program start occurs as a result of the control panel wiring shown in Figure 151. There is no data in the "data to be printed this cycle" fields (Figure 151). This causes an unequal comparison with the "next card data."

Printing is suppressed on this first list cycle and the following total cycles. Picking the non-print relay, R1656 in 1A, does this. R1656 PL picks through R1633 AU N/C, CRRA 5 in 3B, and 1422-1 N/O in 8B of the 407 diagram.

The non-print relay holds through the "run-in control change" cycle and the counter reset total cycles. On the counter reset total cycles the non-print relay, R1656 PL, picks through R1633 AU N/O in 1A of the 407 diagram.

The non-print relay picked through a second read card control relay N/C point, R1633 AU N/C in 1A. This relay does not pick until 225° of the first list

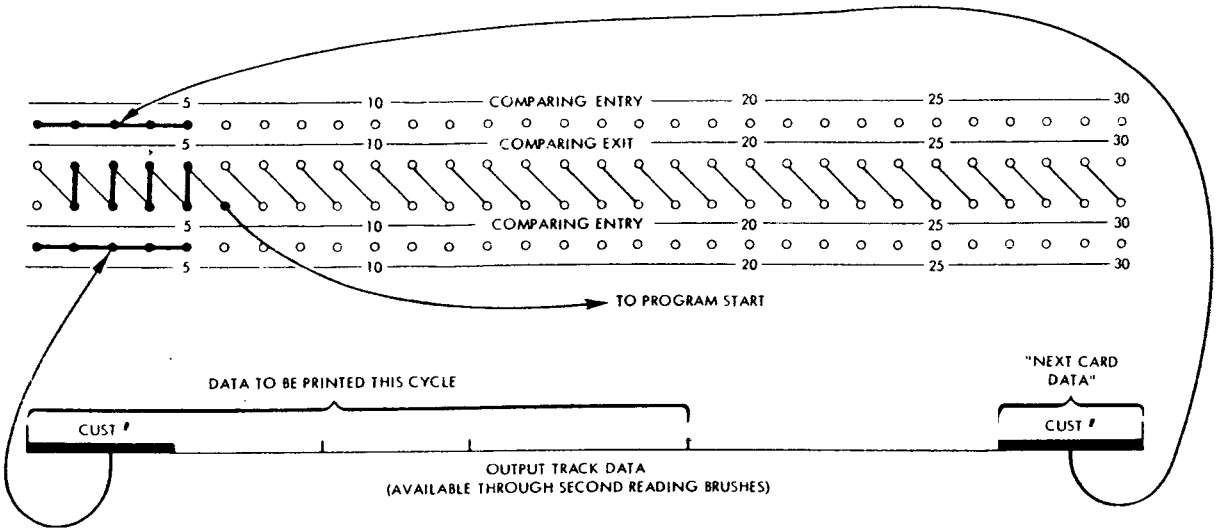


Figure 151. On Line Comparing

cycle when RUN-IN—ON is wired. RA117-3 N/C in 2B prevents picking R1632 until the first list cycle after R1481-12 makes.

All counters reset that are wired to reset. The reset occurs during the total cycles started by the unequal comparison. This is a standard 407 function accomplished with standard 407 circuitry.

S track cannot be read during total cycles because R1422, the feed control relay, cannot pick. This prevents the read relay, R109, in 3B from picking.

407 ready occurs after the last total cycle when the minor 2 relay drops. R1413-5 N/C in 1B lights the ready light. This same point prevents starting 407 on-line list cycles, while the 407 is still in a total cycle.

Last Record Operation

The last record hub in 2B of the 407 Supplement may be wired from a PROGRAM EXIT via a PROGRAM EXIT TRANSLATOR, or a 407 control panel impulse. The PROGRAM EXIT used should be the same one that is wired to 407 print (select). The wire to the LR hub may test the 305 last card selector. The run-in—on hubs must be wired to make the LR hub active. Wiring the LR hub causes the 407 CR mechanism to stop, after printing the last output of a job. RA118 in 2B picks during the last on-line list cycle. This causes the second read card control relays in 2B to drop at 228°. This opens the permanent hold to the run relay, R1638, at R1632-BL N/O in 1B. R1638 drops and picks R1464 in 30A through R1638-AU N/C in 4A. R1464-4 N/C transferring in 4A opens the permanent hold to the drive magnet.

If a program start occurs during the last list cycle, the 407 stops after the programs are over. The drive clutch is kept energized by delaying the pick of R1464 in 30A until after the program cycles have finished. The minor 2 relay, R1413-11 N/C in 30A, opens the pick of R1464.

Wiring the LR hub activates the LCT hub in section 1B of the 407 supplement.

407 Final Total

At the completion of a job it is possible to take a 407 final total. One of the two following procedures must be followed:

1. When the LR hub is wired, depress the final total key after the 407 stops at the end of a job. A final total will print.
2. When the LR hub is not wired, do the following:
   a. After the job is finished open the INTERLOCK connection. (Wire the INTERLOCK through an alteration switch.) This causes the CR mechanism to stop.
   b. Depress the 407 start key. This insures that all function interlock relays drop.
   c. Depress the final total key.

The first card in relay, R1688, must be down to allow a final total. R1688 AL N/C in 8A of the 407 diagram must be made. R1688 remains up as long as the second reading card control relay, R1632 in 2B of the 407 supplement, is up. R1632 is dropped by opening RA118-2 N/C in the first procedure. RA112-5 N/O drops R1632 in the second procedure.

Reset Check

Circuits added to the 407 allow clearing a reset check while the 407 remains on-line. To clear a reset check, depress the 407 stop key. This turns off the reset check

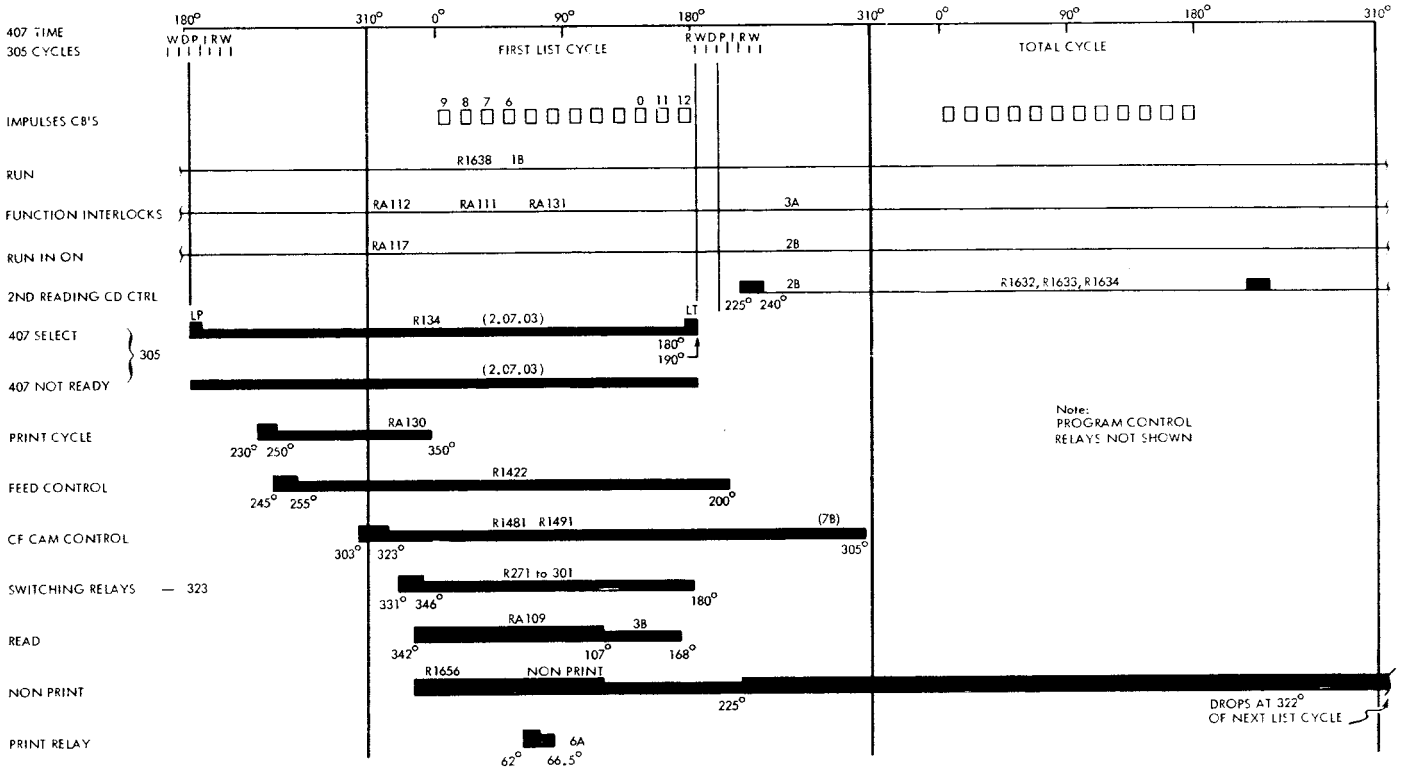


Figure 152. Run-in Reset Operation

light. Then advance the form to prevent over printing. Depress the 407 start key, followed immediately by the stop key for each total cycle. If the reset check light remains off, the counters are clear. Resume processing by advancing the form, then depressing the 407 start key.

When a reset check occurs, R1444 - 2 N/C transferred in 1A, opens the circuit to the start key. Depressing the stop key picks the reset check release relay, R1669 in 8B of the 407 diagram. Section 5A shows a RA112-2 N/C modification of the 407 circuits. This allows R1669-A N/C to drop out R1444, the reset check relays, and the reset check light.

382 Paper Tape Reader

Functions and Operations

The IBM 382 Paper Tape Reader is an optional input unit for the 305 system. The tape reader is designed to read 5-channel telegraphic tape and 8-channel tape, using the IBM 858-884 coding as standard input to the system. In addition, an all-channel decoding principle has been incorporated so that virtually all types of paper tape can be used for input to the RAMAC.

Tape is read at the rate of 20 characters per second and is written on the tape input track (\$) in the same sequence in which it is read. Writing on the input track can be turned ON or OFF at the 382 control panel to eliminate the entry of unnecessary data from the tape.

The entry of data from the tape reader to the process unit is controlled by a program exit impulse wired to the feed tape hub on the process unit control panel. The impulse to the feed tape hub initiates a tape feed operation, and the 382 will continue to feed and read tape until the end of the tape record is signalled by the presence of an identifying special character. A control panel exit corresponding to the special character will emit an impulse when that character is read from the tape. Wiring the exit impulse to the record end hub will suspend tape feeding until another tape feed operation is initiated at the process unit.

Tape Reader

The paper tape reader is mounted in a desk type cabinet which can be located either to the right of the

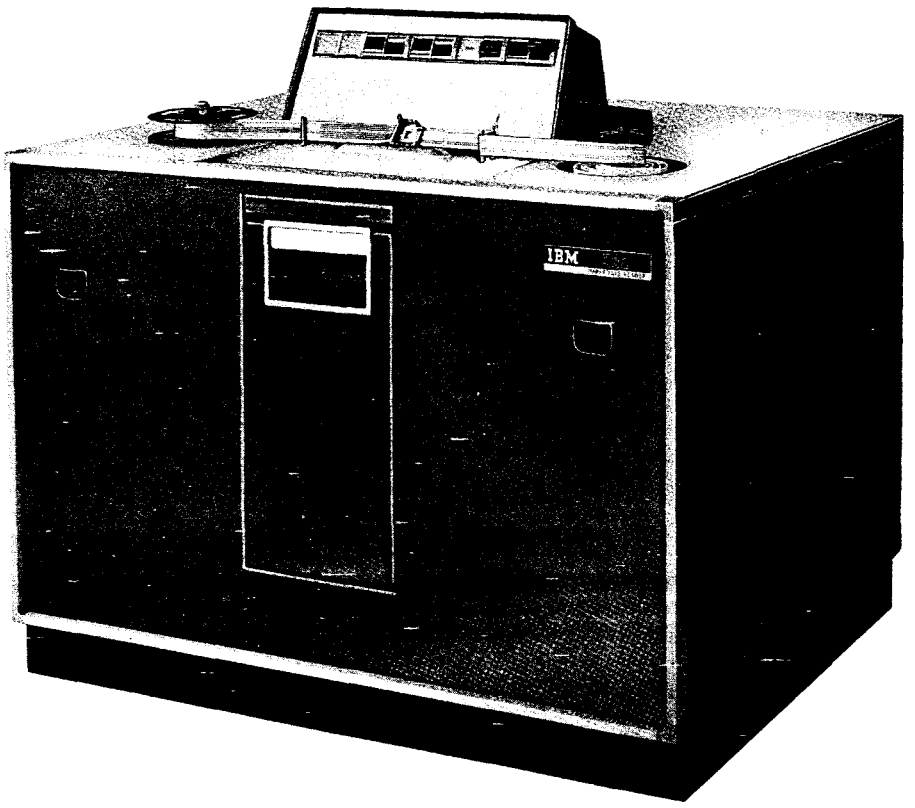


Figure 153. IBM 382 Paper Tape Reader

console or to the left of the printer. The reading mechanism is the same as that used in the 46-47 Tape-to-Card Punch. The reading mechanism accepts tape up to one inch in width. All punched holes must have a spacing of one-tenth of an inch center to center both vertically and horizontally. The tape feed sprocket can be adjusted to allow tape with offset feed holes to be read.

Tape Input Track

As tape is read into the system, it is written on the $ track. Each time the tape reader is impulsed to read a new record, the tape input track is automatically erased. The information from the tape is then entered serially, starting at track position 00 and progressing in ascending sequence.

Writing on the input track is controlled by a track position counter. Each time a character is written, the track position counter advances to condition the next track position on the following read cycle. If the tape record contains more than 100 characters, the track position counter will advance from position 99 to 00 and begin writing again at track position 00. When writing is turned off, counter advancing stops, even though tape continues to pass through the tape reader.

The tape input track is interlocked to prevent transferring data from the input track until tape reading is complete, and to prevent entering data from a process drum track during the time that tape is being read.

8-Channel Operation

8-channel tape is used by the IBM CARDATYPE 858 and the 884 Typewriter Tape Punch. The code structure is the same binary coded decimal system that is used in the RAMAC.

An 8-channel tape contains two types of data:

1. Alphabetic and numerical information.
2. Functional codes which are needed to identify or control the operation of the reader in assembling and selecting data to be written on the input track. This includes such items as skip codes, error codes, and end-of-line codes.

Eight punching positions across the tape provide for coding alphabetic, numerical, and functional codes. Combinations of six of these channels are used for the letters, numbers, and special characters. The remaining two channels are used for checking and end-of-line codes.

The eight channels are labeled, from bottom to top, 1, 2, 4, 8, check, 0, X, and end-of-line. Each character is represented by a single hole or combination of holes as illustrated in Figure 154.

When the tape is punched correctly, each vertical column contains an odd number of holes. When the tape is read by the 382 each column is checked to see that an odd number of punched holes are sensed. If an even number of holes is sensed, the tape reader stops and the tape check light turns on to indicate the reason for the stop.

Control panel functions are controlled by placing special character codes in the tape. For example, selectors may be picked up or dropped out by character codes in the tape. The last character in every record must be unique so that when it is recognized tape reading can be suspended. This final character or special function code must be wired from its exit to the record end hub.

5-Channel Operation

The tape reader will accept standard 5-channel 11/16 inch telegraphic tape. When reading 5-channel tape, the lower five reading pins are used for sensing and the upper three perform no function. The 5 CHA STD switch on the 382 control panel must be wired in order to interpret telegraphic codes.

The 5-channel tape system includes 31 valid code combinations which are divided into 5 functional codes and 26 character codes. The functional codes correspond to printing telegraphic equipment functions. Space, carriage return, line feed, letters shift, and figures shift are the five functional codes. The 26 character codes are dual purpose codes. In one shift (letters shift) they represent the 26 letters of the alphabet and in the other shift (figures shift) they represent numerical digits and special characters. After

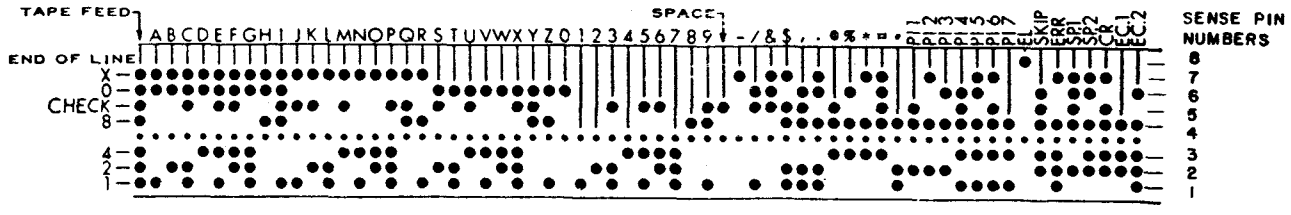


Figure 154. 8-Channel Code

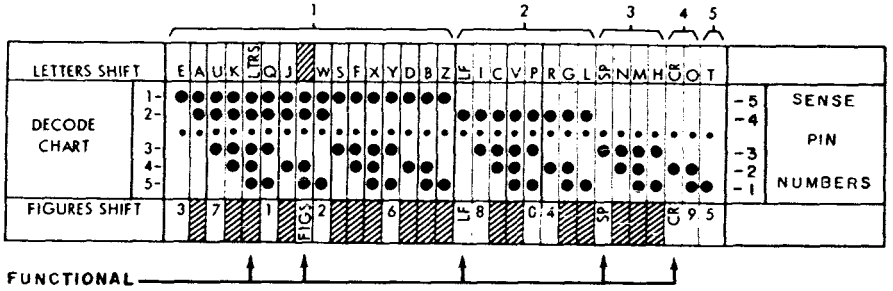


Figure 155. 5-Channel Code

a shift code has been sensed by the 382, the decoding circuits remain in that shift until the next shift code is read from the tape.

The special characters are represented by the normally unassigned figures shift codes. Any of these characters not assigned to digits or special characters may be used for functional codes.

All Channel Exits

The ALL-CHANNEL EXITS are provided so that tape codes other than 8-channel or 5-channel telegraphic may be decoded and processed. The concept of decoding with the all-channel exit hubs is based on assigning a binary value to each of the seven punching positions, numbering from the bottom of the tape and progressing to the top. To determine which of the 128 all-channel exit hubs will emit for a particular punched code, the binary value of the holes are added and the total determines the number of the exit hub for that code. By wiring the ALL-CHANNEL EXITS to the character entry hubs any tape code of up to seven channels can be decoded. Figure 156 illustrates the process of selecting an appropriate ALL-CHANNEL EXIT for a given combination of tape punches.

Mechanics

The 382 contains the following major mechanical units:

1. A clutch controlled circuit breaker unit.
2. A cam operated, latch controlled tape reading unit.
3. A continuously operating tape rewind unit.

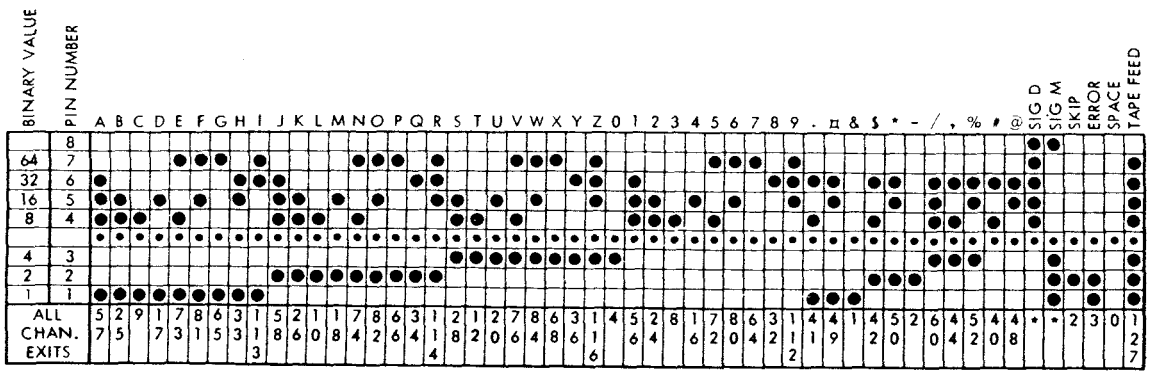
CB Unit

A clutch controlled circuit breaker shaft, operating eight circuit breakers, provides for electrical control of the tape reading process. The tape reading unit is gear driven from the circuit breaker shaft; therefore, the circuit breaker clutch must be energized in order to furnish mechanical power to the tape reading unit.

Tape Reading Mechanism

The tape reading mechanism performs two functions:

1. Mechanical sensing of the tape.
2. Advancing the tape one character position during each tape read cycle.



* Use SIG D and SIG M hubs (L-M, 21-22) provided for these codes instead of exits 120 and 7.

Figure 156. All-Channel Exits

Figures 157, 158, and 159 illustrate the operation of the tape sensing mechanism. With the tape reading mechanism latched, the reader pins are held in a retracted position by the individual reader pin interposers. The group of eight reader pin interposers are held in a retracted position by the latched interposer bail.

A reader cycle is initiated by energizing the reader control magnet and transferring the control arm. With the control arm in the fully operated position the interposer bail assembly is free to follow the pin operating cam. As the interposer bail follows the pin operating cam, the reader pin interposers drive the reader pins against the tape under spring tension. The same interposer bail motion releases the pin contact lever bail assemblies by removing the stud that separates the two bails when the reading mechanism is latched. The motion of the pin contact lever bails allows the eight pin contact levers to pivot toward the reader pin interposers. If the reader pin is stopped by the tape, the position of the interposer will prevent the pin contact lever from transferring. If the reader pin passes through a hole in the tape, the position of the interposer will allow the pin contact lever to transfer and close the pin contact.

As the pin operating cam restores the interposer bail to the latched position, the reader pin interposers retract the reader pins. The stud on the interposer bail forces the pin contact lever bails apart and restores the pin contact levers to their normal position. Positive relatching of the interposer bail assembly is provided by the control magnet armature knockoff cam.

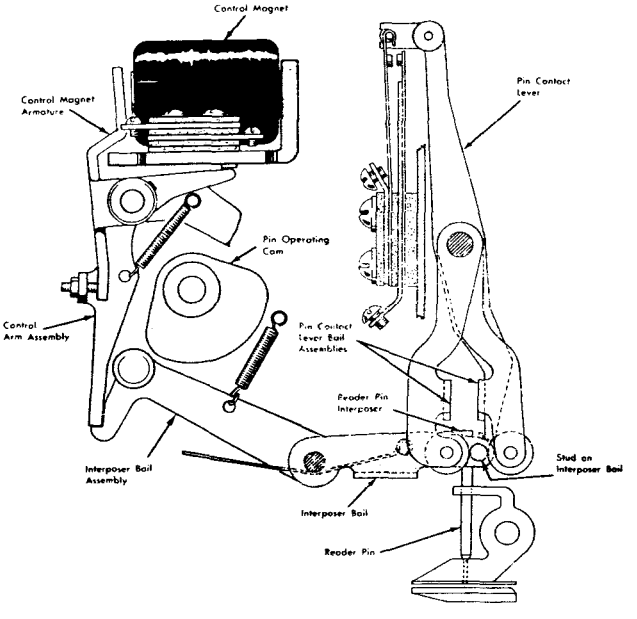


Figure 157. Sensing Mechanism, Latched Position

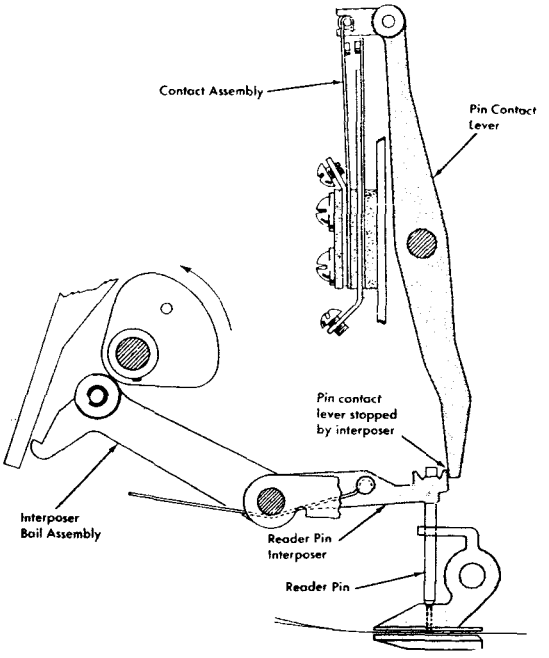


Figure 158. Reader Pin Stopped by Tape

Tape feeding occurs between 225° and 227° on the clutch drive index during each tape sensing cycle. Tape feeding is mechanically interlocked by the tape sensing mechanism. Therefore, tape feeding can only take place during a tape sensing cycle.

Figure 160 illustrates the operation of the tape feed mechanism. The driving power for the tape feeding mechanism is furnished by the tape feed cam, which is mounted on the same shaft as the pin operating cam. In the latched position the feed pawl operating arm is held away from the feed ratchet wheel by the feed pawl latch. As the feed pawl operating arm reaches the high dwell of the tape feed cam, the feed pawl latch is free to pivot away from the feed pawl operating arm under spring tension. As the feed pawl operating arm approaches the low dwell of the tape feed cam, the feed pawl engages with the feed ratchet wheel and advances the pin wheel one position.

The auxiliary latch is used to restore the feed pawl latch and to interlock the operation of the sensing mechanism and the tape feed mechanism. The tail of the auxiliary latch normally rests against the contact lever bail of the sensing mechanism. If the sensing mechanism is in the latched position the auxiliary latch resting against the contact lever bail prevents the feed pawl latch from releasing the feed pawl operating arm. During a sensing cycle, the pin contact lever bails move toward the sensing pins and allow the feed pawl latch and the auxiliary latch to pivot and release the feed pawl operating arm. As the pin contact lever bails are returned to the latched position, the left bail

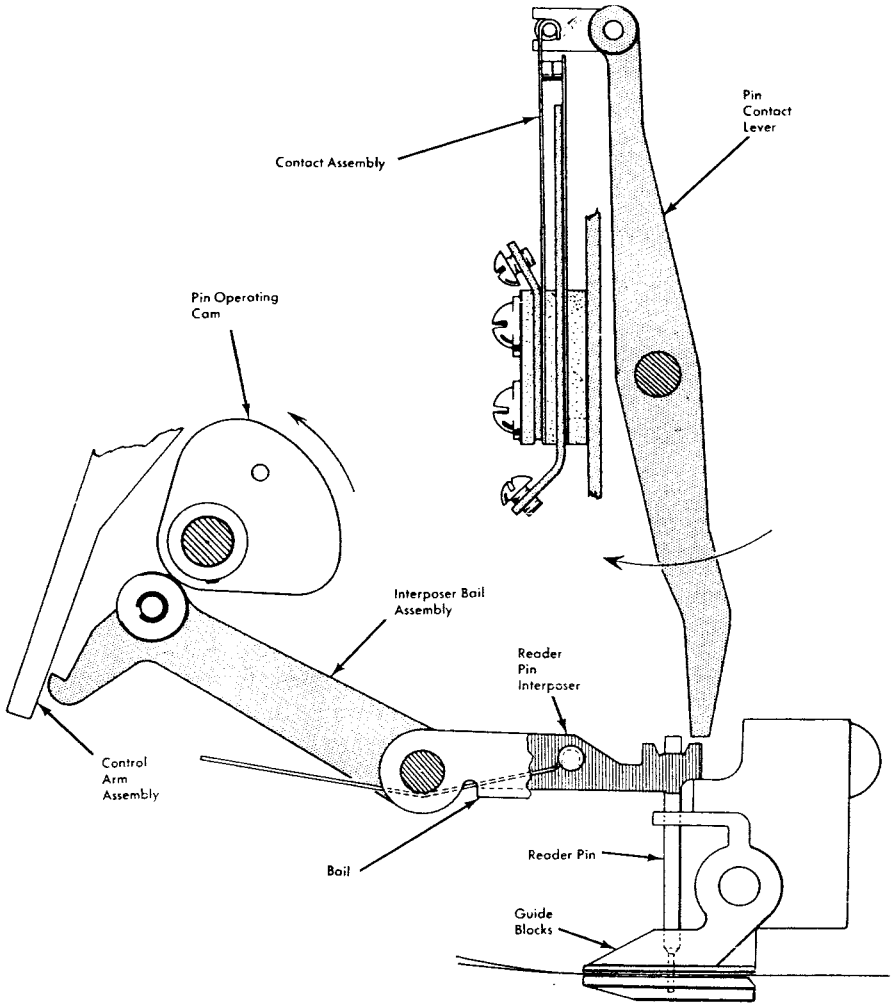


Figure 159. Reader Pin Sensing Hole in Tape

operates against the tail of the auxiliary latch and restores the feed pawl latch on the feed pawl operating arm.

Tape Rewind

Two tape reels are furnished with each machine—one for supplying tape to the machine and one for storing tape which has been processed. The rewind assembly is driven from a small motor located under the rewind spool. A friction disk is driven directly from the motor. The rewind reel is impelled by friction between the bronze shoes of the spider assembly and the surface of the friction disk. The reel mounts above the spider assembly and its weight increases the force with which the shoes on the spider assembly rest against the surface of the friction disk. As the spool receives tape, the weight of the reel and tape increases and the torque exerted on the reel gradually increases to compensate for the added load.

Circuit Description

Tape Feeding

To set up the RAMAC to read tape, the operator must first depress the RAMAC reset key and then depress the 382 start key. The 382 will go through one circuit breaker shaft cycle as the reset key is depressed. This cycle is called a reset cycle and establishes circuits to activate the 382 start key. As the start key is depressed the 382 goes through a second circuit breaker shaft cycle to set up the $ track for the entry of tape data. During the setup cycle, $ track is erased and the 100 character counter is reset to position 00. The 382 will begin to feed and read tape automatically after the setup cycle is complete. Tape feeding will continue until the first record end code is read from the tape. A CHANNEL EXIT wired to the record end hub suspends tape feeding and places the 382 in a ready condition. Feeding of the next tape record must be initiated by

a PROGRAM EXIT impulse to the feed tape hub on the 305 control panel. Whenever tape is being fed, the tape not ready signal interlocks the $ track. Figure 162 is a tape feeding sequence chart.

Service aid. The read control magnet is impulsed every other circuit breaker shaft cycle when the 382 start and stop keys are held depressed. Depressing the console reset key allows you to use this technique. It is possible to connect the 305 remote cycling box to the 382 (see 10.12.11) and have the 3 keys mentioned above at your finger tips. (Depressing the check reset key on this box latch picks the tape select relay on 2.07.04.)

OBJECTIVES:

1. Initiate a reset cycle when the console reset key is depressed by energizing the CB clutch (10.02.00).
2. Initiate a setup cycle when the 382 start key is depressed by energizing the CB clutch (10.02.00).
3. Write R bits on $ track during the setup cycle (10.06.01).
   a. $ Erase gate (10.06.00).
   b. $ Erase data (10.06.00).
4. Reset the 100 character counter during the setup cycle (10.05.01-.02).
5. Feed the tape until a record end code is read.
   a. Energize the CB clutch each cycle until record end (10.02.00).
   b. Energize the reader control magnet each cycle until record end (READY) (10.02.01).
   c. Interlock $ Track (2.07.04 Optional).
6. Transfer control of the 382 start circuits to the 305 (10.02.00).

Tape Reading

Figure 161 illustrates the process of entering tape data on the process drum input track. As the reader pins sense punched holes in the tape, the reader pin contacts close and complete circuits to pick corresponding analyzer relays. The points of the analyzer relays form a decoding network to activate the channel exit hub that corresponds to the character that was read from the tape. The channel exit is normally wired to the associated character entry hub.

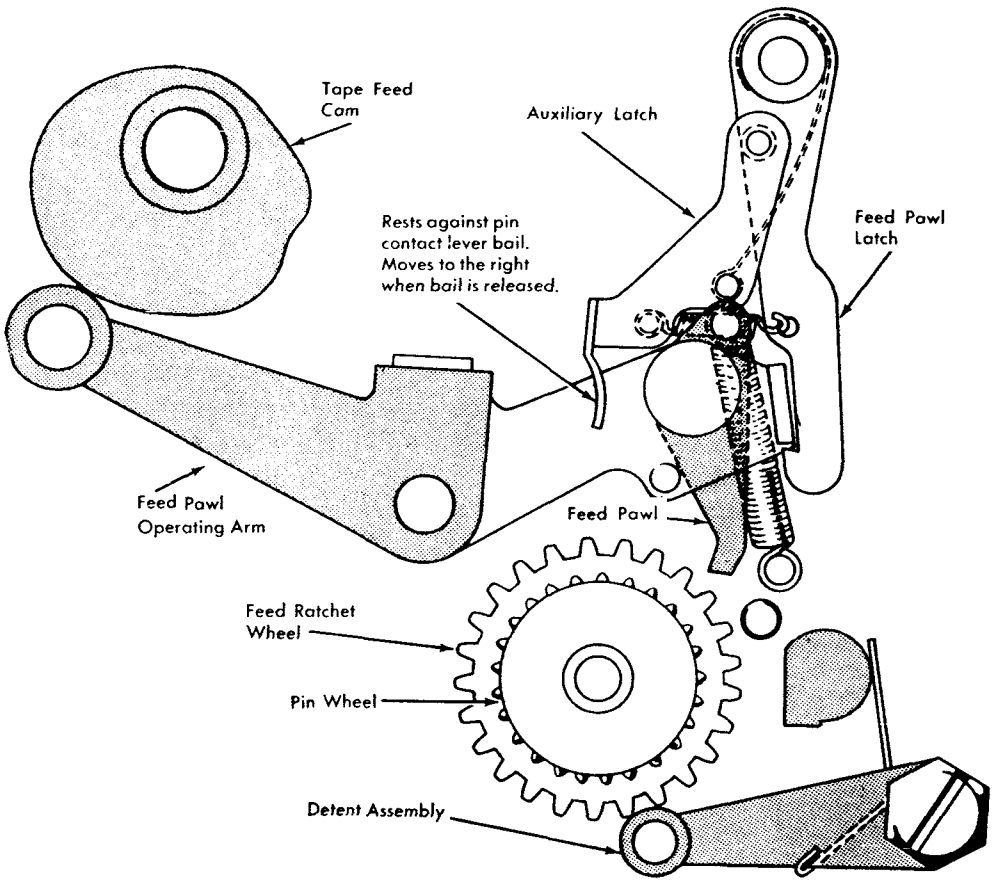


Figure 160. Tape Feed in Latched Position

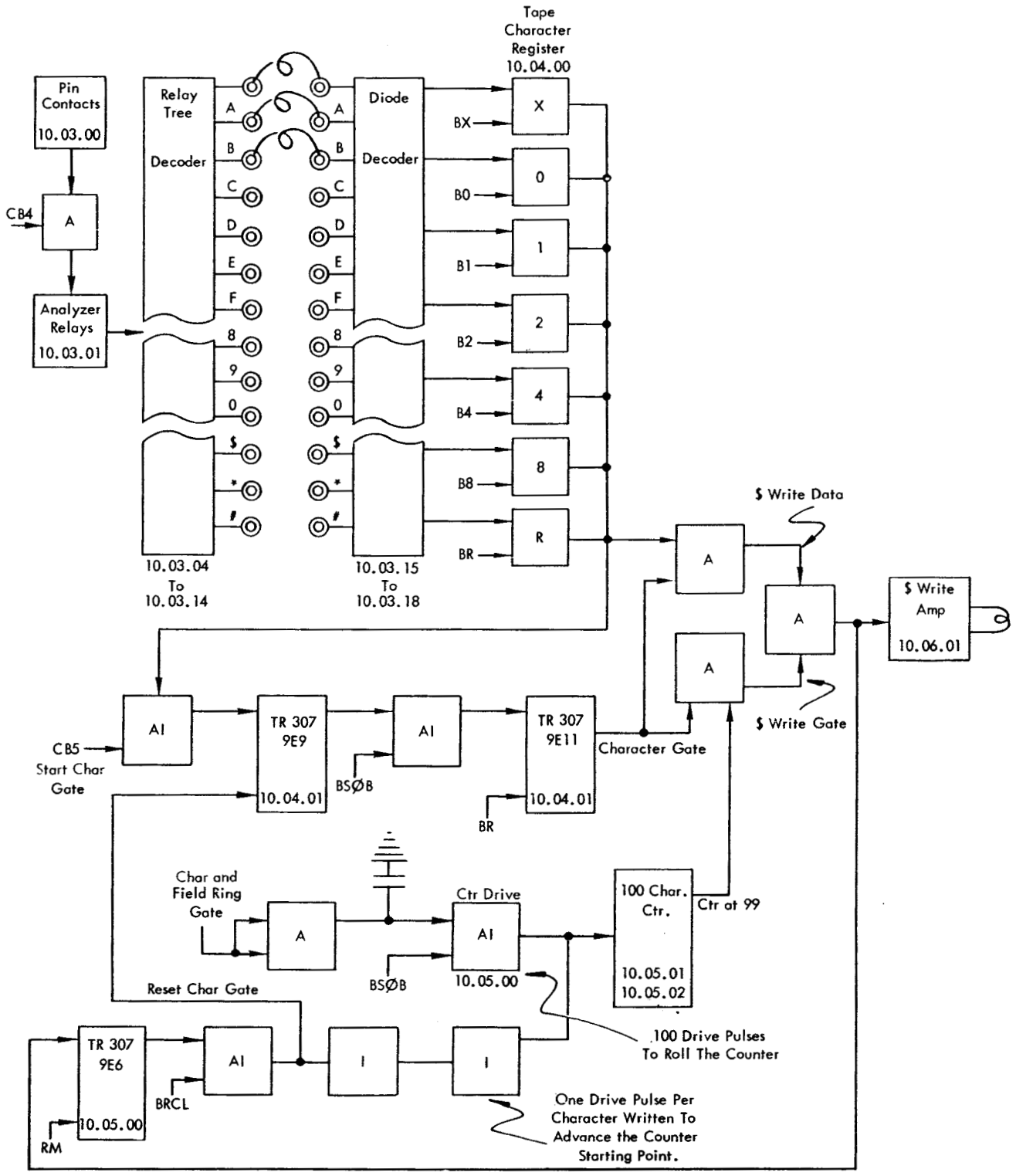


Figure 161. Paper Tape Data Input

The impulse to the character entry hub is translated to standard RAMAC code by the diode decoding network. The diode decoding network conditions units within the tape character register to produce an output in serial bit form that corresponds to the decoded character. The output of the tape character register is available during each character time of the drum revolution.

The character gate indicates that the tape character register has a new character to write. After CB 5 makes the first output pulse from the tape character register flips the character gate control trigger (9E9). The character gate trigger (8E11) produces an output from Bs ∅ B through BR during each character time.

The 100 character counter determines the character position in which the tape character will be written on $ track by combining the output of the counter with the character gate to produce the $ write gate. The output of the counter is available only when the counter is standing at a value of 99. The 100 character counter is reset to a value of 00 during the setup cycle. The counter receives an additional advance after writing each character. This causes the counter to allow writing one character sooner than the last character was written. Figure 162 shows the $ track writing sequence.

If the write off hub is impulsed, writing on the $ track will stop at the next character sensed. The paper tape continues to feed, however. Impulsing the write on hub re-establishes the ability to write on the $ track. The N/C write off relay points on 10.03.15 prevent decoder output when WRITE OFF is impulsed.

OBJECTIVES:

1. Channel exit impulse (10.03.04) (10.03.14).
2. Tape data (bit structure) (10.04.00).
3. Character gate (10.04.01).
4. Advance 100 character counter (100 pulses) (10.05.00).
5. Write on $ track (counter at 79) (10.06.01).
6. BRCL advance 100 character counter after writing a character (10.05.00).

8-Channel Redundancy Check

When an 8-channel tape is read, an automatic redundancy check is made of each character as it is read. If an even number of holes is sensed a read check error is indicated. This error stops tape feeding and keeps the $ track interlocked. To clear this error the operator must reread the tape record. This is accomplished by repositioning the tape to read the preceding record end hole, then depressing the rerun key. If the tape record reads correctly processing resumes. If not the read check re-occurs.

Figure 163 shows the operational sequence when the rerun key is depressed after a read check.

Optional Features

Telegraphic Checkable Code

This feature checks the accuracy of standard 5-channel tapes, if the tapes have been punched with a checkable code character at the end of each record. It counts the number of holes punched in each tape record and compares the units position of the total with the tape check code number punched at the end of the record. If the two numbers are equal, no tape punches have been dropped or misread.

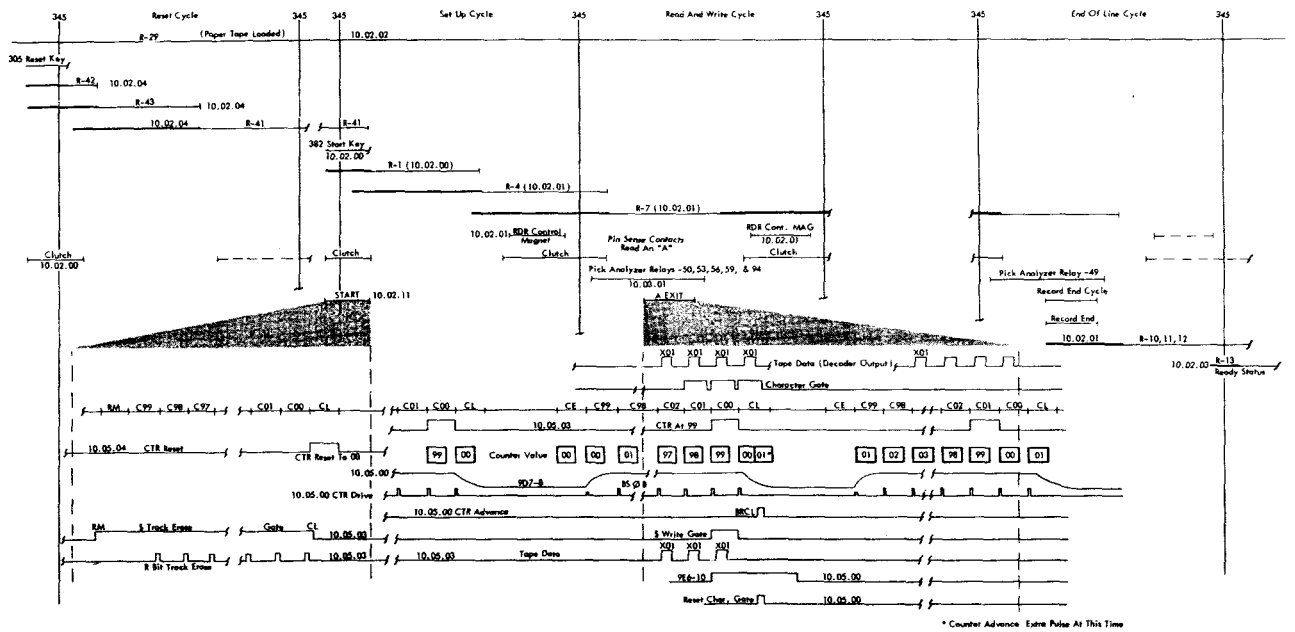


Figure 162. Tape Feed, Read and Write Sequence

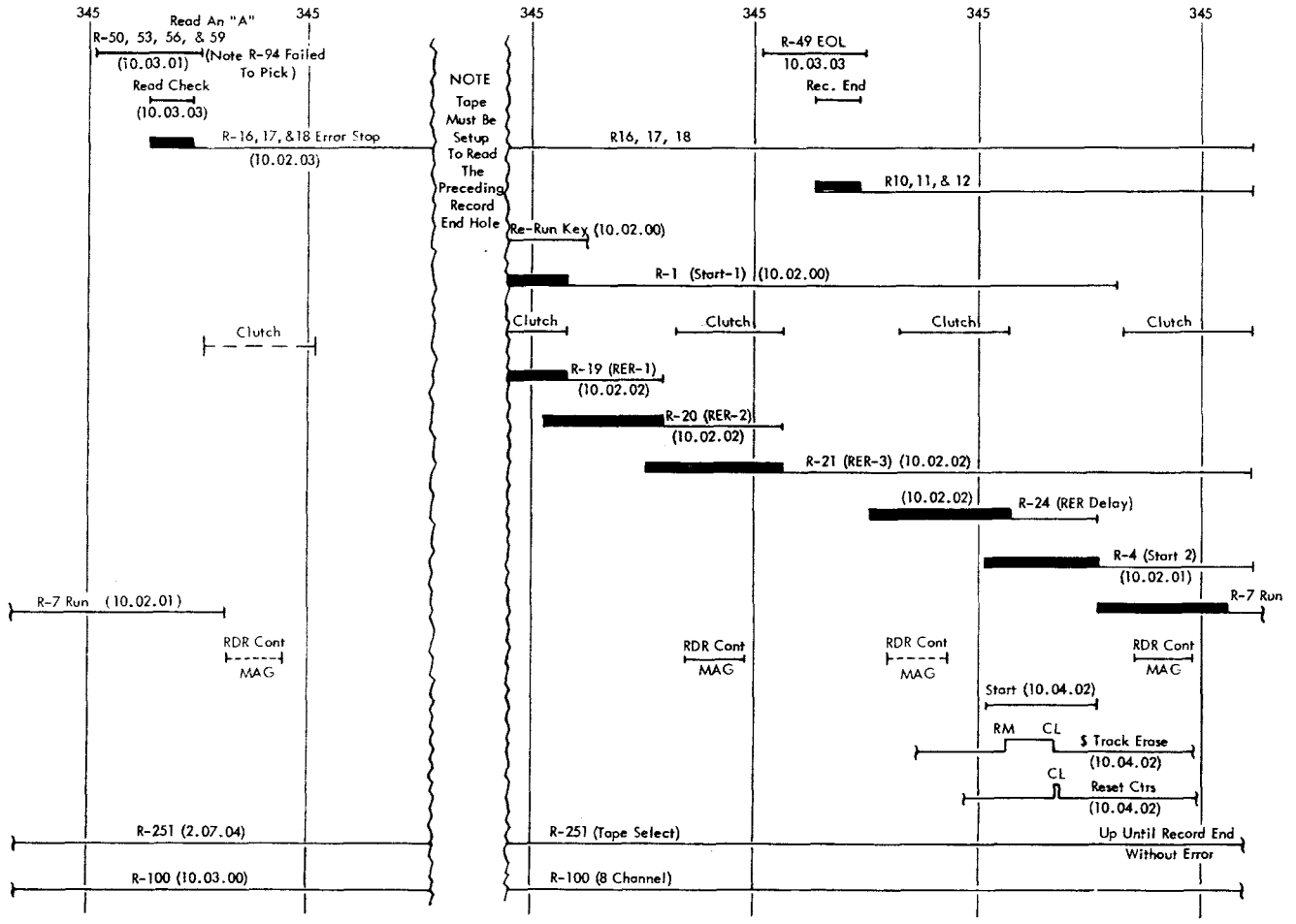


Figure 163. Read Check Rerun Operation

The beginning of each tape record is defined by a Figure (Figs) shift code. The end of each tape record is identified by the following four codes in order: carriage return, figures shift, line feed, and the tape check code. Figure 164 shows tape record codes.

Two sets of hubs are added to the 382 control panel for this feature. They are TCCC RECORD END (TRE) and the TCCC switch (TCCC). They are at NP 18 and 19. Jackplug the TCCC switch when a tape is to be read and checked. The TRE hub emits the record end impulse when TCCC is jackplugged and the compare to the check digit is equal.

Figure 165 shows a sequence chart of a TCCC operation. In this operation the TCCC tape data and the counter data compare equally. If the comparison were unequal, a read check stop would occur. Restarting the 382 when a read check occurs is described under "Redundancy Check."

Track Skip Control

Track skip control allows skipping over portions of the $ track while writing the tape record. Writing on the skipped over area of the track is suspended during skipping. Writing resumes at the position skipped to. The effect of a skip is to set the track write control counter to the position indicated by the skip wiring.

The control panel hubs used for skip control are shown in Figure 166. This figure also shows an example of skipping caused by the wiring in the figure.

The following explains the sequence chart in Figure 166. The control panel wire from the skip control 1 hub develops the skip gate. The skip gate occurs at the character at which the first skip will stop, C30. When the skip control in hub receives its first impulse, the skip starts. This causes the counter to reset when the skip reset counter line goes high. After the reset

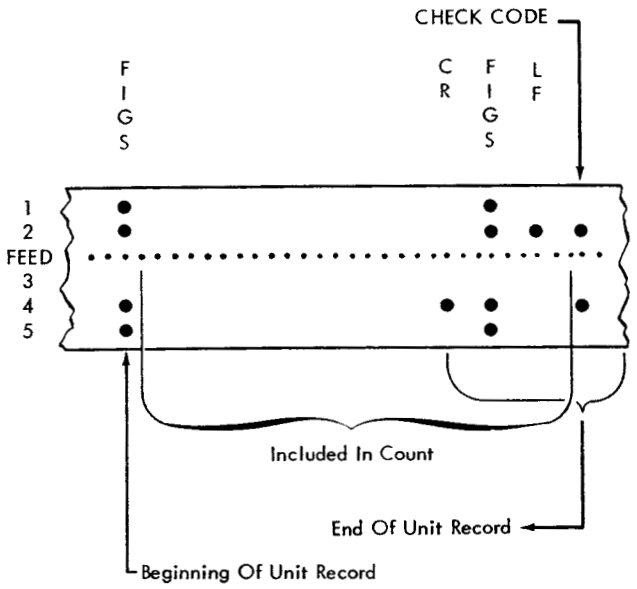


Figure 164. TCCC Tape Codes

the counter drive line advances the counter at each character time. This causes the counter to reach 99 at C30 time. The next character read then writes in C30. The skip start character doesn't print, because it is not wired to print. The next skip control hub (2) becomes hot at the RM following the reset of the counter. This is controlled by R162. R162 picks when the thyratron 9R10 on 10.51.15 fires. With the skip control 2 hub hot, the skip gate developed occurs at C50, the stop character for the next skip.

If the skip code is not punched in the tape because the field is completely filled with data (making the skip unnecessary), passing the SKIP TO TRACK POSITION (position wired from a skip exit) advances skip control to the next exit. For example, if SKIP 1 is wired to SKIP TO TRACK POSITION 30, passing position 29 without a skip, advances skip control from SKIP 1 to SKIP 2. This is accomplished by 9K10b on 10.51.04. At B4 as C29 is being written the skip counter advance sets up the ATH 9R10 on 10.51.15 to fire at the next RM.

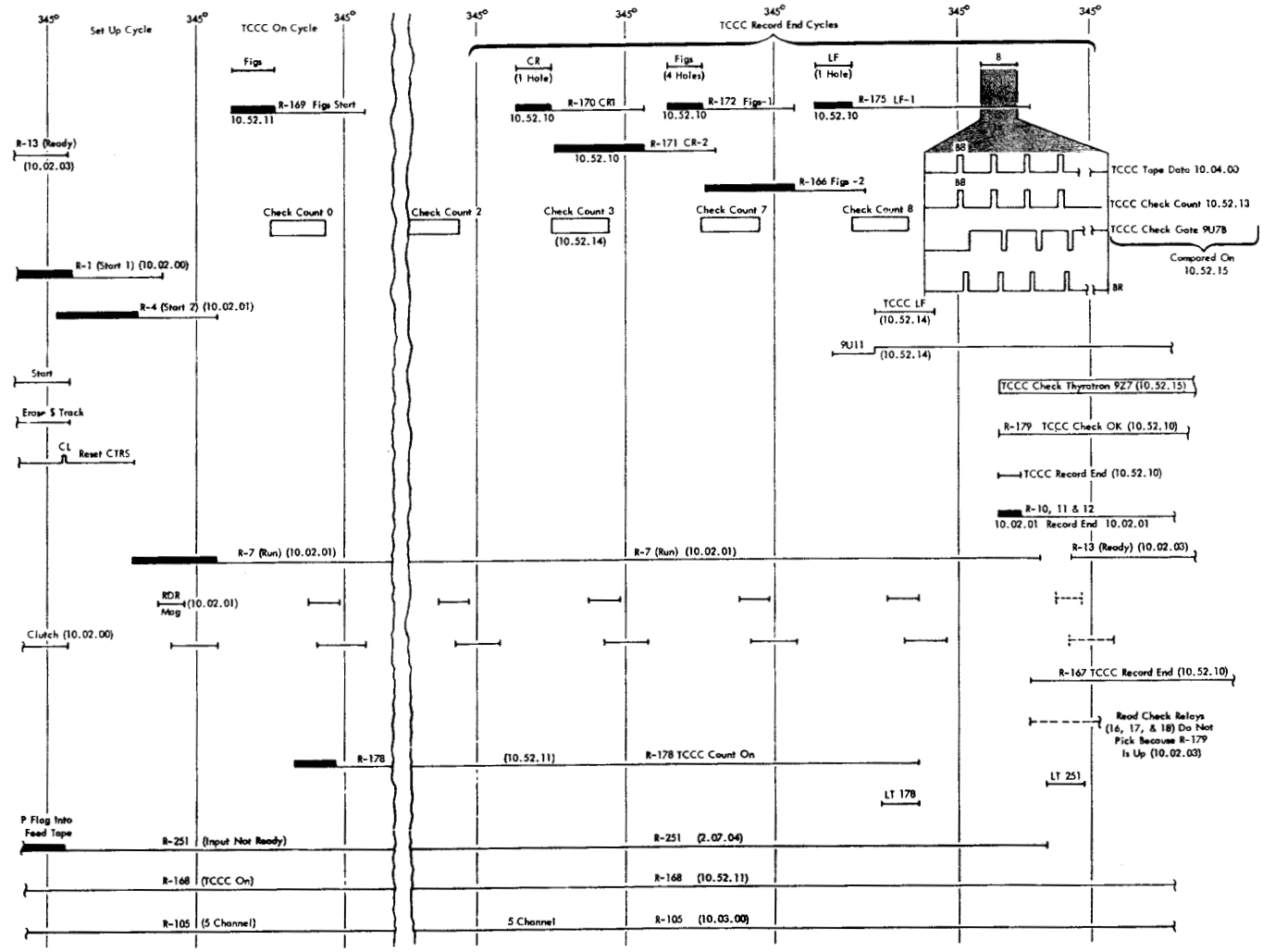


Figure 165. TCCC Operation Sequence

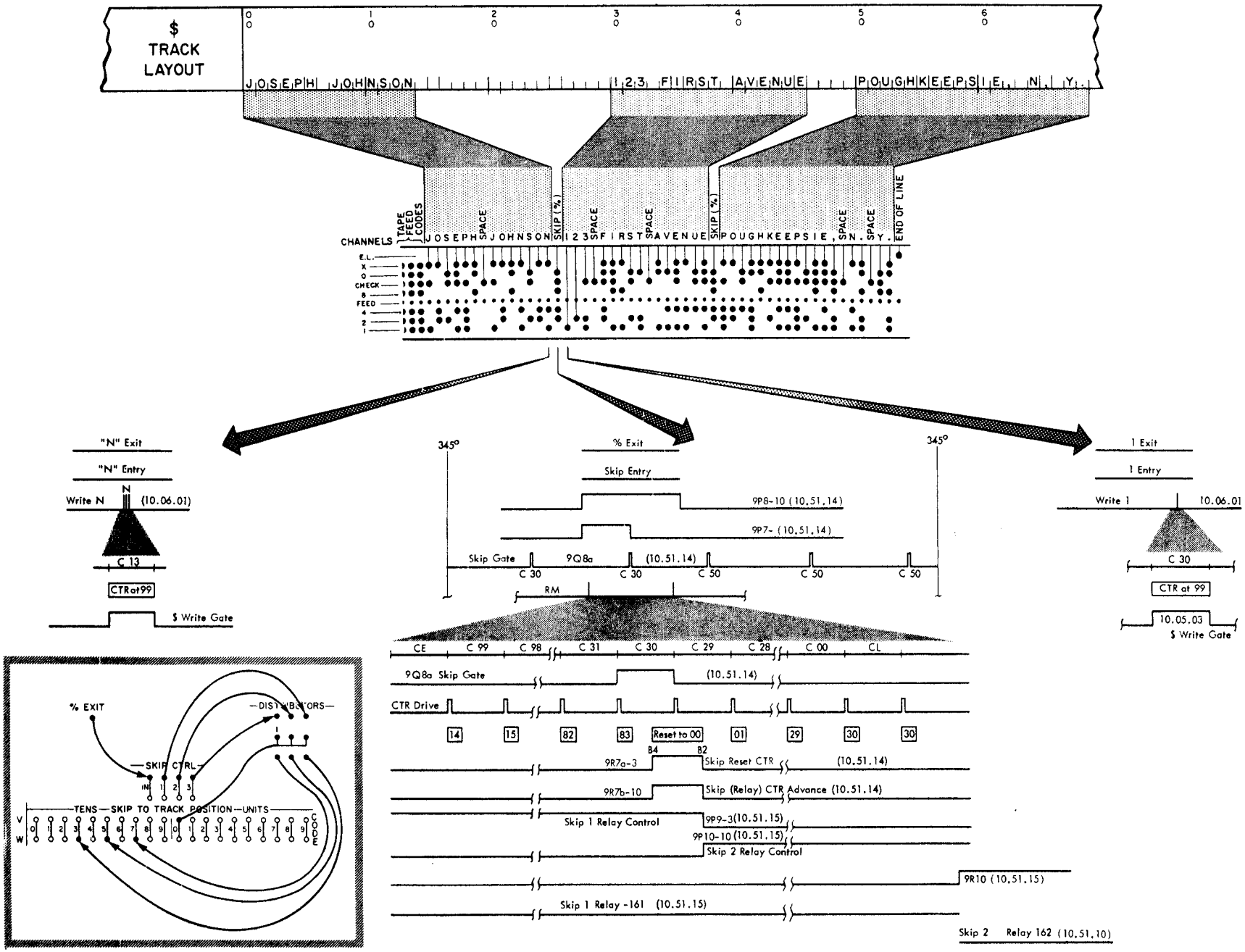


Figure 166. Skipping Characters on $ Track

Arithmetic

General Principles

The RAMAC is capable of performing addition, subtraction and multiplication. Division is also available as an optional feature. However, the basic arithmetic function of RAMAC is addition, since subtraction is performed by complement addition, multiplication by repetitive addition, and division by repetitive complement addition.

Accumulator Track

The accumulator track and associated circuits are provided to accomplish the basic arithmetic functions. Like other processing tracks, the accumulator track is divided into ten fields with ten character positions per field. Each field of the accumulator track is also called an accumulator. Thus, RAMAC has 10 accumulators, each of which can store 10 digits. Within each accumulator, the C9 position stores the lowest order digit, and the C0 position stores the highest order digit.

Unlike the normal process drum track, which has a single head for reading and writing, the accumulator track employs two heads, one for reading and one for writing. The read head is positioned to read one character earlier than its corresponding machine character time, and the write head is positioned to write one character later (Figure 167).

The reason for this read head and write head displacement is that the accumulator must be capable of reading a digit contained in any character position, adding to that digit, and writing the sum back in the same character position.

Programming, For Add, Subtract, and Read Out

A positive number may be added into an accumulator by employing the character L in the T_2 section of the instruction. For example, to add the six digit number located in position 54-99 of track W into accumulator 2, the instruction is W59L2906.

A positive number may be subtracted into an accumulator by employing M as the T_2 character. For example, to subtract the three digit number located in positions 13-15 of track X into accumulator 1, the instruction is X15M1903.

It is not possible to couple two accumulators in the manner that accounting machine counter groups are coupled. If an accumulated amount exceeds the 10 positions of an accumulator, this condition is indicated by the transfer of a selector on the control panel. This overflow selector may be tested after each addition, and when found to be transferred, a special program step may be executed to add 1 into the low order position of another accumulator. Thus, even though two accumulators may not couple automatically, effective coupling may be accomplished by programming, but an extra program step is required.

If it is desired to read a number out of an accumulator, the T_1 character must be either L or M. If $T_1 = L$, the number will remain on the accumulator track after read out. This is the same as a normal process drum transfer. If $T_1 = M$, the affected accumulator, or accumulators, will be reset to zero during read out. If the instruction requires any portion of an accumulator to be reset, the complete accumulator will be reset.

True Add, Complement Add

Since RAMAC adds algebraically, a true add operation is performed under the following two conditions:

1. $T_2 = L$ and the number coming from core buffer into the adder circuits is positive.
2. $T_2 = M$ and the number coming from core buffer into the adder circuits is negative.

A complement add operation is performed under the following two conditions:

1. $T_2 = L$ and the number coming from core buffer into the adder circuits is negative.
2. $T_2 = M$ and the number coming from core buffer into the adder circuits is positive.

Logic of RAMAC True Add Operation

During the execution of an example instruction, X75L4903, the R cycle operation is the same as with any ordinary process drum transfer. During W cycle

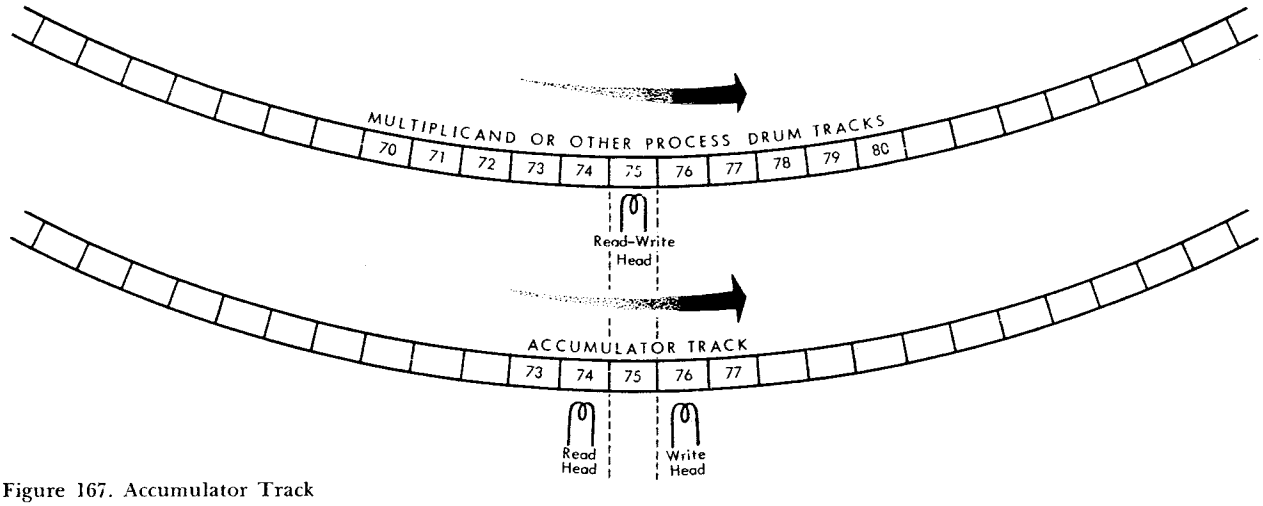


Figure 167. Accumulator Track

the three characters which were transferred from track X are scanned out of the core buffer during C49, C48, and C47 time. These three numerical digits are entered into the adder circuits simultaneously with the three digits already stored in C49, C48, and C47 positions of the accumulator track.

Since the accumulator read head reads one character early, the digit in the C49 position of accumulator 4 will be read during C50 time. However, the entry of the accumulator digit into the adder circuits must be simultaneous with the digit coming from the core buffer during C49 time. Therefore, the accumulator digit is delayed one character time in a delay register before entry into the adder circuits.

If the sum of the units position digits is 10 or greater, there must be a decimal carry into the tens position. This is accomplished by entering a numeric 1 into the adder along with the digit coming from the core buffer and the digit coming from the delay register during C48 time.

Three separate input lines to the adder are required to fulfill the needs shown above. These inputs are designated as inputs A, B, and C. A input is from the core buffer, B input is from the delay register and C input is the carry input.

Binary Addition, Modified

Since the numeric data on all tracks is stored serially in binary bit form, addition within the adder circuits takes place one bit at a time in binary form. The adder circuits will accept only the numeric bits, B1, B2, B4, and B8, from any character.

In order to accomplish addition a bit at a time, the following four rules are necessary:

Rule 1. If no bit pulses are received at any of the three inputs to the adder, the bit sum is zero.

Rule 2. If a bit pulse is received at only one input, the bit sum is 1.

Rule 3. If a bit pulse is received at each of two inputs, the bit sum is 0, and there is a bit carry into the next bit.

Rule 4. If a bit pulse is received at each of the three inputs, the bit sum is 1, and there is also a bit carry.

Let us apply these rules to adding pulses at B1 and B2 time into adder input B, and pulses at B1 and B2 time into input A. In decimal form this problem is $3 + 3 = 6$.

	B8 time	B4 time	B2 time	B1 time
Input B	0	0	1	1
Input A	0	0	1	1
Input C	0	1	1	0
Bit Sum	0	1	1	0

The binary sum of this addition is B4 and B2, which translates to decimal 6, the correct answer.

Since four binary bit positions are used to represent each numeric digit, sums having a value 0 through 15 could be accumulated within a particular character position. However, a numeric bit value greater than 9 cannot be allowed to remain in one character position.

	B8	B4	B2	B1	
Input B	0	1	1	0	= 6
Input A	0	1	1	1	= + 7
Input C	1	1	0	0	
Bit Sum		1	0	1	= + 13

The bit sum in the problem above must be modified to leave B1 and B2 in the character position shown, and a decimal carry initiated to carry 1 into the next character position. In order to modify the

bit sum, ten must be subtracted. Since direct subtraction is not possible, complement addition is used. However, we are dealing with a 16 base counter, so the 16's complement of ten, 6, must be added. Figure 168 shows the correction necessary for the problem cited above.

The necessity of + 6 correction adds two simple rules to the four already given for RAMAC addition:

Rule 5. Whenever the bit sum exceeds 9, + 6 correction and decimal carry are initiated.

Rule 6. A bit 8 carry is thrown away whenever it occurs, since this carry situation is taken care of by the decimal carry set up as a result of rule 5.

Add Cycle and Correction Cycle

Since the adder receives inputs from the core buffer and from the delay register only during bits 1, 2, 4 and 8 time, the remaining four bit times may be used for correction. These two intervals of time are called add cycle and correction cycle. The correction cycle covers bit times, R, S, X, and 0, which have a value of 1, 2, 4, and 8, respectively, for correction purposes.

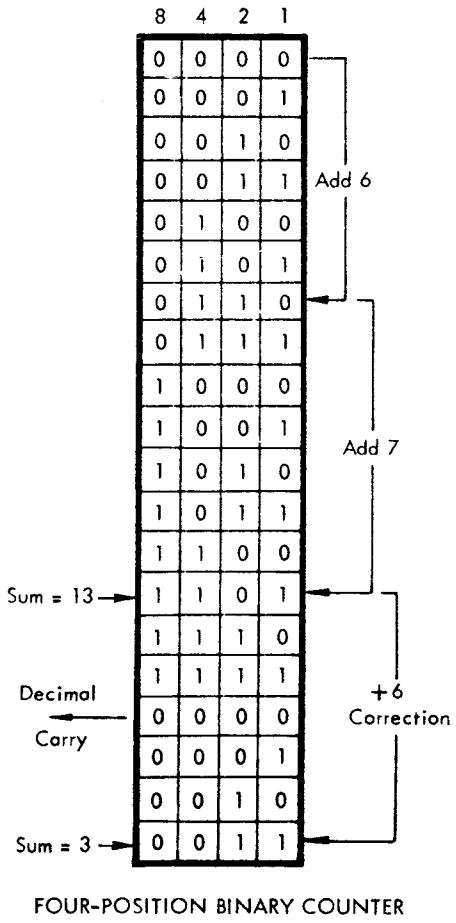


Figure 168. + 6 Correction

Use of Practice Problem Chart

The use of the practice problem chart (Figure 169) will aid in understanding the RAMAC arithmetic process during a true add operation. The numbered blocks across the top of the practice problem chart represent machine character time. Bit times are indicated for the add and correction cycles in relation to each character time. The three adder inputs are indicated along the right side. The input of a bit is indicated by a "1" in the proper square, no input is indicated by "0". The B1 square at input C is reserved for decimal carry. The adder register triggers which store the sum until it can be written on the accumulator track (one character later than machine time) are indicated below the adder inputs. A horizontal line is used to indicate that the trigger is storing the appropriate bit; the absence of a line indicates the trigger is not storing a bit.

Assume that the instruction being executed is X75L-4903 with 463 stored in C73, C74, and C75 positions on track X and 873 in accumulator 4 at the C47, C48, and C49 positions. Using Figures 169 and 170 together, trace the flow of data and the entry of data on the practice problem chart.

During R cycle a normal transfer was executed, transferring 463 from track X to the 00, 01, 02 positions of the core buffer. The actual arithmetic data flow, which we shall trace, takes place during W cycle as follows:

1. At C50 time the 3 in the C49 position of accumulator 4 is read into the delay register a bit at a time. At each following character time, the next character is read into the delay register, a bit at a time. Each character is stored in the delay register for one character time.
2. At C49 B1 time the add cycle is initiated. A pulse is received into adder input B from the delay register and into adder input A from the core buffer. This results in no sum, and a carry, which sets up the feeding of a bit carry into adder input C during B2 time.
3. At C49 B2 time a pulse is received into all three adder inputs. This results in a B2 sum, and a carry, which causes storage in the adder register B2 trigger at B4 time, and a bit carry into input C at B4 time.
4. At C49 B4 time a pulse is received into input C only. This results in a B4 sum which causes storage in the adder register B4 trigger at B8 time, and no carry.
5. At C49, B8 time no adder inputs are received. The add cycle is complete at the end of B8 time.
6. At C49 BR time the correction cycle is initiated. Since nothing is stored in the adder register B1 trigger, there is no entry into any input during BR.

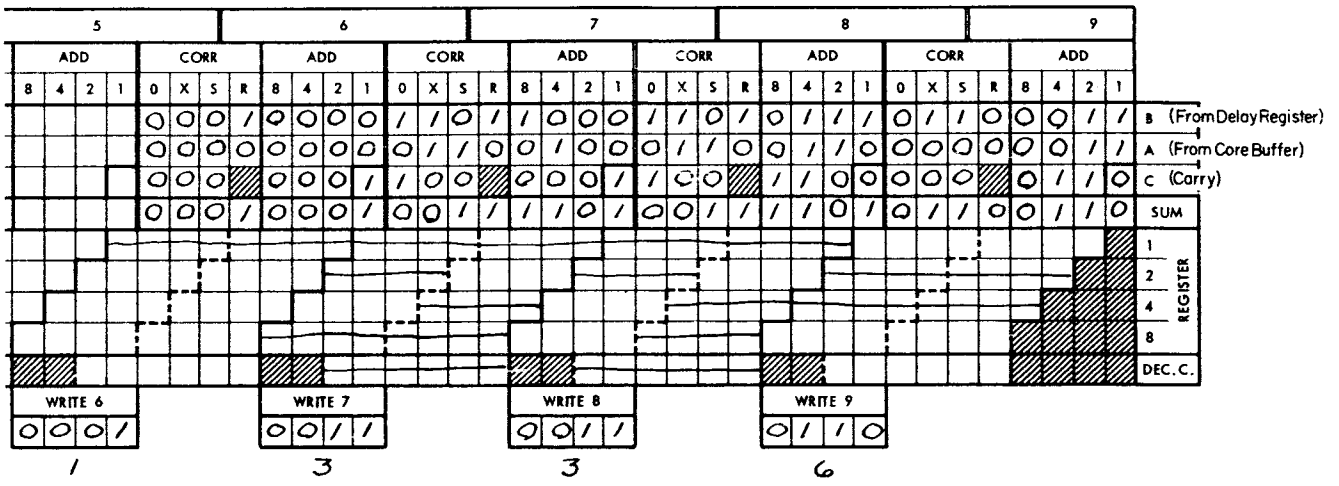


Figure 169. Development of 873 + 463

7. At C49 Bs time the adder register B2 trigger causes a pulse to be entered into adder input B. Since no correction is necessary, there is no pulse into input A. This results in a correction B2 sum, which causes storage in the adder B2 trigger at Bx time, and no carry.
8. At C48 Bx time the adder register B4 trigger causes a pulse to be entered into adder input B. There is no pulse into input A. This results in a correction B4 sum, which causes storage in the adder register B4 trigger at B0 time and no carry.
9. At C48 B0 time there is no entry into the adder, resulting in no sum and no carry. The correction cycle is complete at the end of B0 time.
10. At C48 B1 time another add cycle is initiated. A pulse is received into adder input B from the delay register. No pulses are received into inputs A or C. This results in a sum, which causes storage in the adder register B1 trigger during B2 time. Since the adder register B1 trigger had nothing stored in it at C48 B1 time, 0 is written in the B1 position of C49 on the accumulator track. (Remember: the accumulator write head is offset one character later.)
11. At C48 B2 time a pulse is received at both the A and B inputs, resulting in no sum and a carry. The adder register B2 trigger is in the "storage" state during C48 B2 (due to the addition that took place during C49 time), a 1 is written in the B2 position of C49 on the accumulator track.
12. At C48 B8 time a pulse is received into input C due to bit carry during B4. A sum and no carry results. Storage takes place in adder register B8 trigger at BR time. Since the B8 trigger had nothing stored during C48 B8, 0 is written in the B8 position of C49 of the accumulator track.
13. The correction cycle proceeds much as it did before, except that a + 6 correction occurs because the adder register B4 trigger is in the "storage" state when the B8 trigger is flipped to the "storage" state at BR time. A Bs pulse and a Bx pulse (correction B2 and B4) are fed into input A while input B pulses are controlled by the adder register triggers.
14. Since + 6 correction and decimal carry go hand in hand during true add, a B1 pulse is fed into adder input C at C47 time. Writing will occur on the accumulator track in the C48 position during C47 time, using the same principles used during C48 time.

Tracing the data flow and entry of data on the practice problem chart for the C47, C46, and C45 positions should cause no difficulty, if the principles and rules already presented are followed.

Adder

Logic and Data Flow

The adder (5.01.01), the result register (5.01.02) and the adder register (5.01.03, 5.01.04) will be treated as a unit with no consideration of the type of operation being performed (See Figure 170). Three inputs to the adder, A, B, and C, will be examined to raise two of the four following output lines: sum or no sum, carry or no carry.

This information is stored in 2 triggers, sum and carry, at ØC time for each bit. The sum triggers will be sampled to turn on the appropriate bit sum triggers in the adder register. These are scanned twice during a character time, once in the add cycle, B1 through B8 and once during the correction cycle, BR

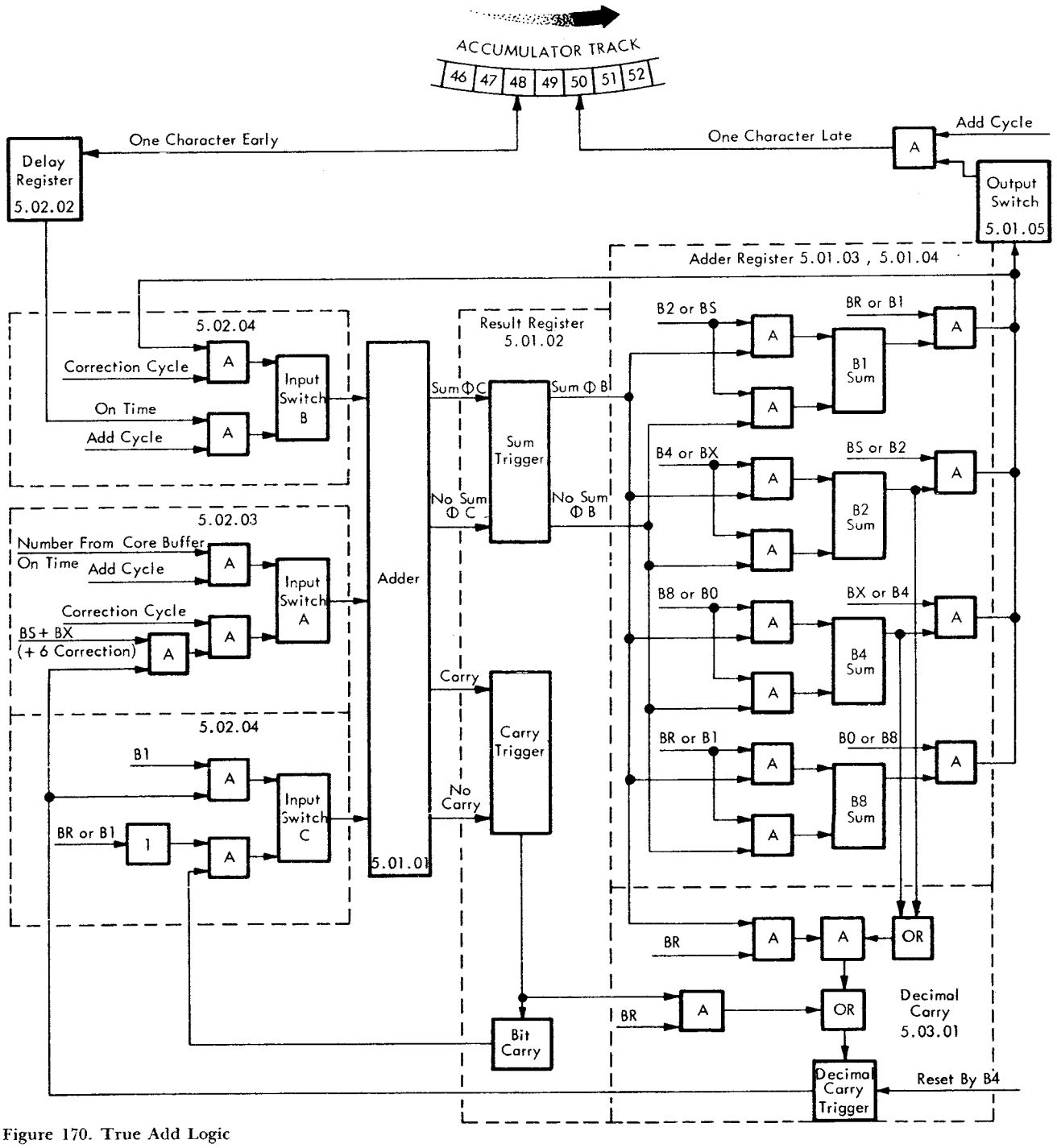


Figure 170. True Add Logic

through B0. The serial data from the adder register goes two places. During the correction cycle, it returns to adder input A for possible correction. During the add cycle, it is the output of the adder, delayed one character time from the inputs.

The carry trigger output is used to turn on the bit carry trigger. The latter provides an input to the adder, one bit later than it was developed. Also if a carry is sensed at BR time, indicating an attempt to accumulate 16 or higher, the decimal carry trigger is turned ON. This trigger is also turned ON when a bit 8 sum is sensed (BR time) and the 2 or 4 bit sum trigger is ON, indicating a sum over 9. This decimal carry trigger remains ON until B4 of the next character, and is used to enter the + 6 correction factor during the correction cycle, and to provide a carry at B1 time of the next add cycle.

The following circuit explanation covers only the adder and adder register circuits. For the various functions, the input switching may vary but the adder itself will still develop a serial sum out, one character time later than the inputs, and also sense the need for a decimal carry.

Figure 171 shows a sequence chart of adder operation.

Circuit Description

OBJECTIVES:

1. Establish add cycle (B1, B2, B4, B8) and correction cycle (BR, Bs, Bx, B0).
2. Combine input bits to produce output of sum or no sum, carry or no carry.
3. Develop serial data out, one character after input.
4. Determine need for decimal carry.

Add Cycle—Correction Cycle: The correction cycle trigger (6G10 - 5.01.05) is in continuous operation, being flipped 10 pin high at every BR for a correction cycle gate. It is flipped 3 pin high every B1 for an add cycle gate.

Add Operation: On 5.01.01 the three inputs to the adder, A, B, and C, are compared bit by bit to develop two outputs. At each bit time, the sum or no sum line will be high and the carry or no carry line will be high. At ∅C time, the sum and carry triggers on 5.01.02 are set. One bit later, these triggers are sampled with ∅B's.

The bit carry trigger 6N11 on 5.01.02 is turned 3 pin high one bit later than the carry trigger. This bit carry is returned to the adder through input C or 5.02.04 to be mixed with the other inputs. The sums or no sums are stored in the adder register on 5.01.03 and 5.01.04. Since the ∅B sums are arriving one bit late, the four bit sum triggers will set one bit later than their value indicates. Notice that the bit 1 sum trigger (6J10 - 5.01.03) is pulled 3 pin high at B2∅B time if the sum line is high. Once the sum trigger is pulled 3 pin high it will remain so until a no sum result for that bit arrives from the adder. For example,

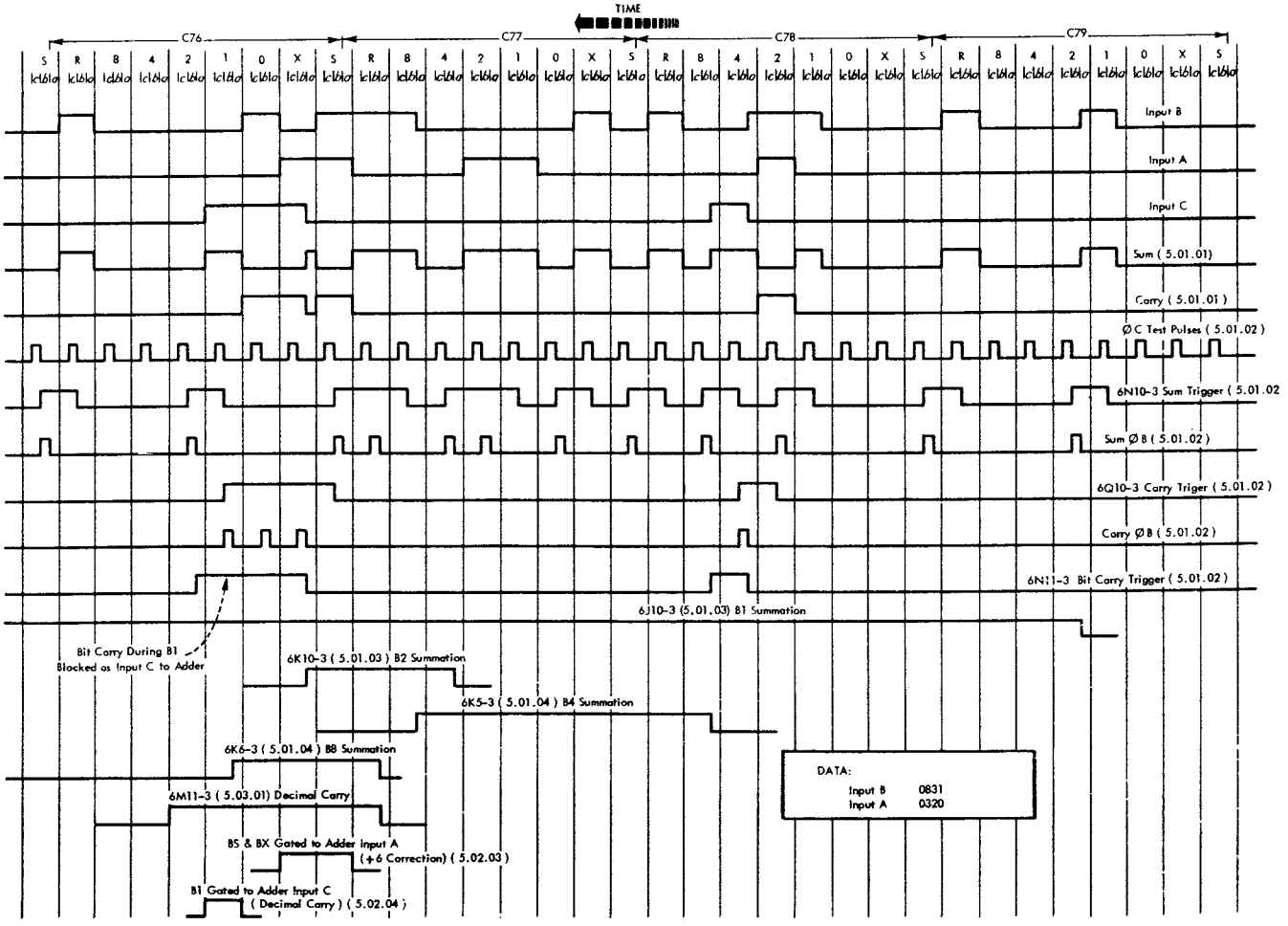


Figure 171. Adder Operation

the bit one sum trigger can only be pulled 10 pin high at B2 or Bs time with no sum ∅B.

Serial Data Out: The four sum triggers are scanned with B1, B2, B4 and B8 to produce ∅A to ∅A serial data out. The triggers are also scanned at BR, Bs, Bx and B0 to develop serial data for the correction cycle. All serial data appears on the register out line on 5.01.03.

Correction Cycle and Decimal Carry: The output of the four sum triggers is always returned to the adder during the correction cycle (BR, Bs, Bx B0) through input B (Q7b—5.02.04). If the sum counter accumulated more than 9 during the add cycle, a correction factor of + 6 is entered into the adder through input A (6Q9 — 5.02.03). During a true add operation, this becomes an input at Bs and Bx. The decimal carry trigger (5.03.01) is turned 3 pin high at the and switch 6L10a if the 8 sum trigger is turned ON (sum ∅B at BR time) and the 2 or 4 sum trigger is ON. Also, a sum greater than 15 (carry ∅B at BR time) will result in a decimal carry. This trigger will remain ON until B4 of the next add cycle.

True Add Operation

The instruction W95L7802bb will add characters 95 and 94 from W track to characters 78 and 77 of the accumulator track (L). During R cycle a normal transfer of data from W track to cores will take place. During W cycle, the add operation will occur and it is shown in the flow chart of Figure 172.

Data is being read one character early from the accumulator track and then delayed one character in the delay register. If a Q of 5, calling for a reset of the accumulator, were present, the on time accumulator data would never reach the adder. At adder input B the add subtract fields gate selects the desired accumulator track data for adder entry during add cycle time. This same gate is allowing the data from cores to enter adder input A. One character later the sum of the two inputs will appear from the adder register. During the add cycle the bit carries are returned to adder input C. If a + 6 correction is needed as determined by the decimal carry trigger, it is entered into adder input A during the correction cycle with the adder result going to input B. The adder result has BR inserted and is gated to the accumulator

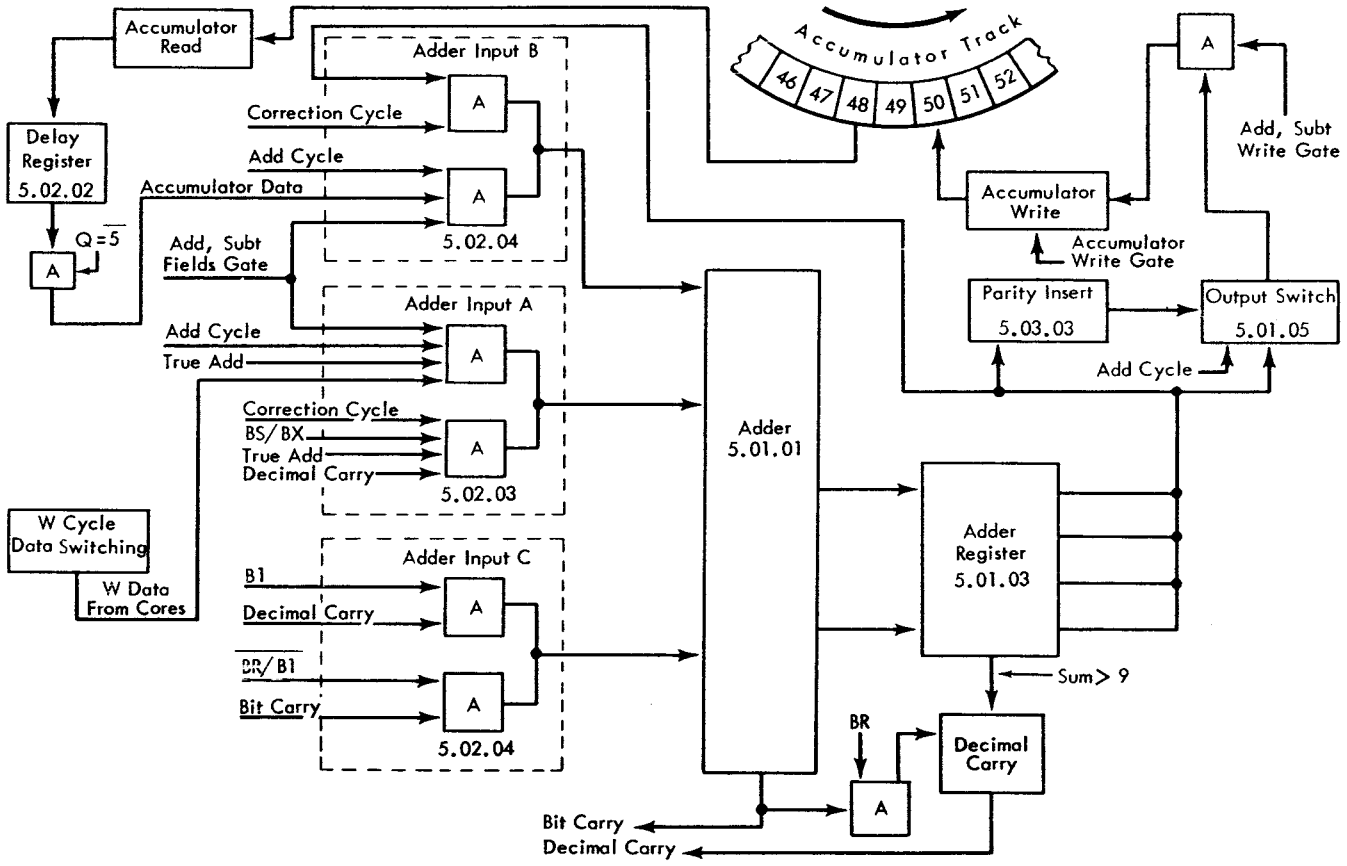


Figure 172. True Add Data Flow and Controls

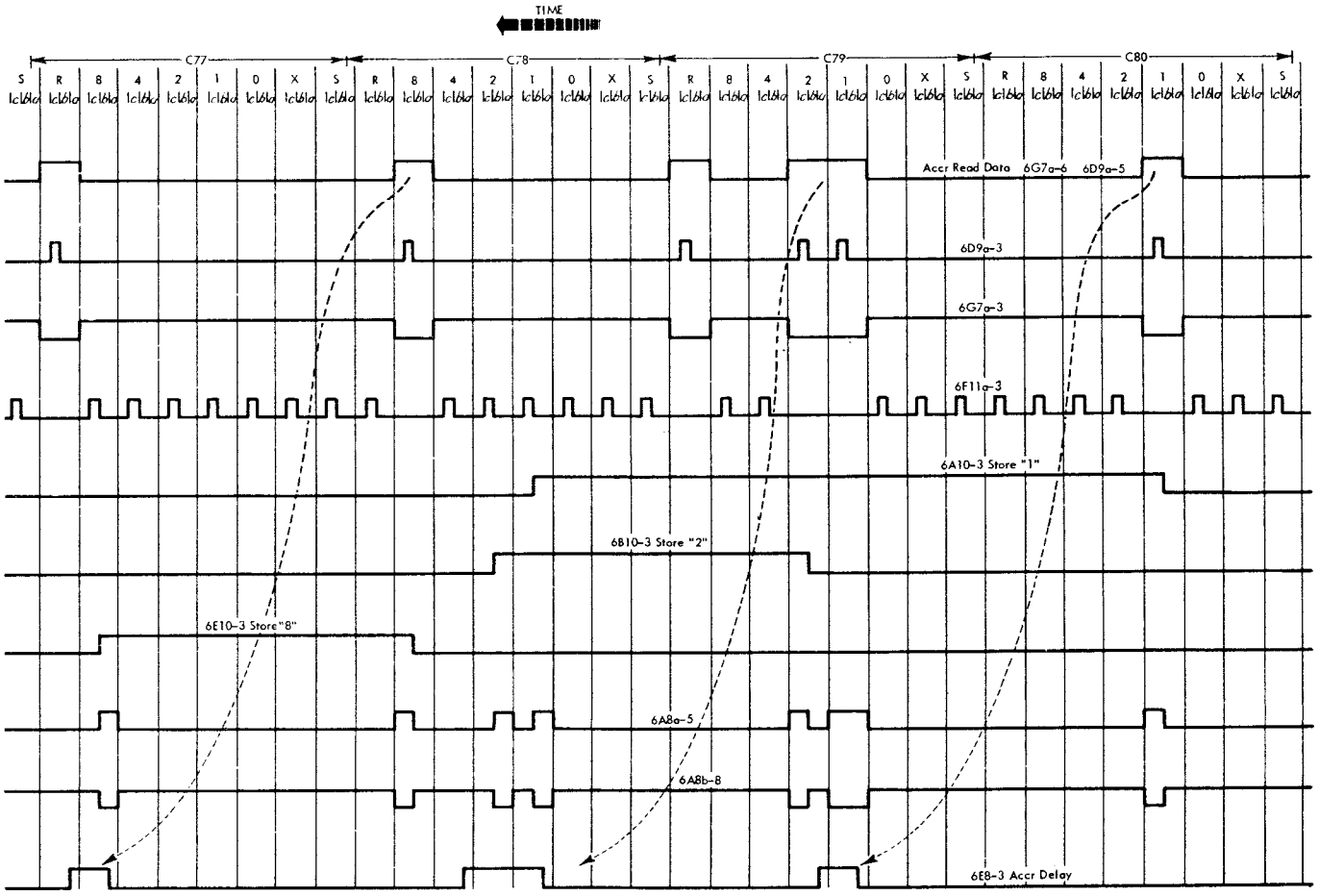


Figure 173. Delay Register Operation

write head one character late by the add subtract write gate. Since the write head is physically located one character late, the result is returned to the same character position from which the accumulator factor was read.

OBJECTIVES:

1. Develop true add gate.
2. Read and delay the accumulator track data one character time.
3. Select desired accumulator track data with the add subtract fields gate.
4. Enter adder with core data, accumulator data and carries.
5. Insert BR's after bit count.
6. Select adder output with add subtract write gate.
7. Write result on accumulator track.

True Add Gate: The inputs to adder input A will be controlled by the type of operation being performed. To establish a true add operation both the instruction and the sign of the factor coming from cores must be analyzed. For the present discussion we will assume true add is high for the entire operation. The detailed development of the true and complement add gates will be covered later under "Sign Analysis and Sign Control."

Accumulator Read Data and Delay Register: On 3.10.42 all data on the accumulator track appears as full bit pulses on the read data line. The read head is positioned to produce approximately ∅A to ∅A data one character early. At the delay register (5.02.02), this data is scanned with ∅C pulses to produce ∅C bits at 6D9a and ∅C no bits at 6F11a. This is shown in Figure 173. The ∅C bit pulses are scanned by the bit ring to turn their respective delay triggers 3 pin high. The ∅C no bit pulses are scanned to turn the triggers 10 pin high. Therefore, the four delay triggers will be set from ∅C to ∅C for at least a full character.

One character after one of the delay triggers has been turned 3 pin high, its 3 pin is mixed with a bit ring pulse. These ∅A to ∅A pulses are all sent to the AI-6A8a where they mix with a ∅B to pull the accumulator delay trigger, 6A7, 3 pin high. This same line of delayed bit pulses is inverted at AI-6A9a and mixed with ∅B's to pull the accumulator delay trigger

10 pin high. The result is on time ØB to ØB accumulator delay data. This data is gated at 6E8a with Q = not 5, Test R/W + W Cycle. Q = 5 is a reset command. The other conditions allow the changing of the accumulator track data from the console.

Add Subtract Fields Gate: We must now select the data specified by the instruction for entry into the adder with the add subtract fields gate. Since the accumulator track is really 10 separate accumulators we must always enter the entire field (s) into the adder. This is necessary because of the possibility that quantities added to low order positions of an accumulator (field) may require carries into several high order positions. In complement addition another reason for entering the complete accumulator will be discussed. In our sample instruction, W95L7802bb, all of field seven of the accumulator track must enter the adder.

The Add Subtract Fields Gate gates the on time accumulator data at 6P5 on 5.02.04. This gate is developed on 5.06.02 at trigger 6U7. 6U7 is pulled 3 pin high at A compare of W cycle. This can be seen in the sequence chart in Figure 174. A compare, developed on 2.04.14, always occurs at the beginning of the field (C0B8) in which the AB counters roll from 99 to 00. The add subtract fields gate trigger is pulled 3 pin low at C9Bx at the end of the add operation with the cycle complete gate high. Note that the add subtract fields gate actually comes up during bit 8 of the high order of the previous accumulator. If a bit 8 does enter the adder at this time it will not be written since the add subtract write gate comes up at BR, one character later.

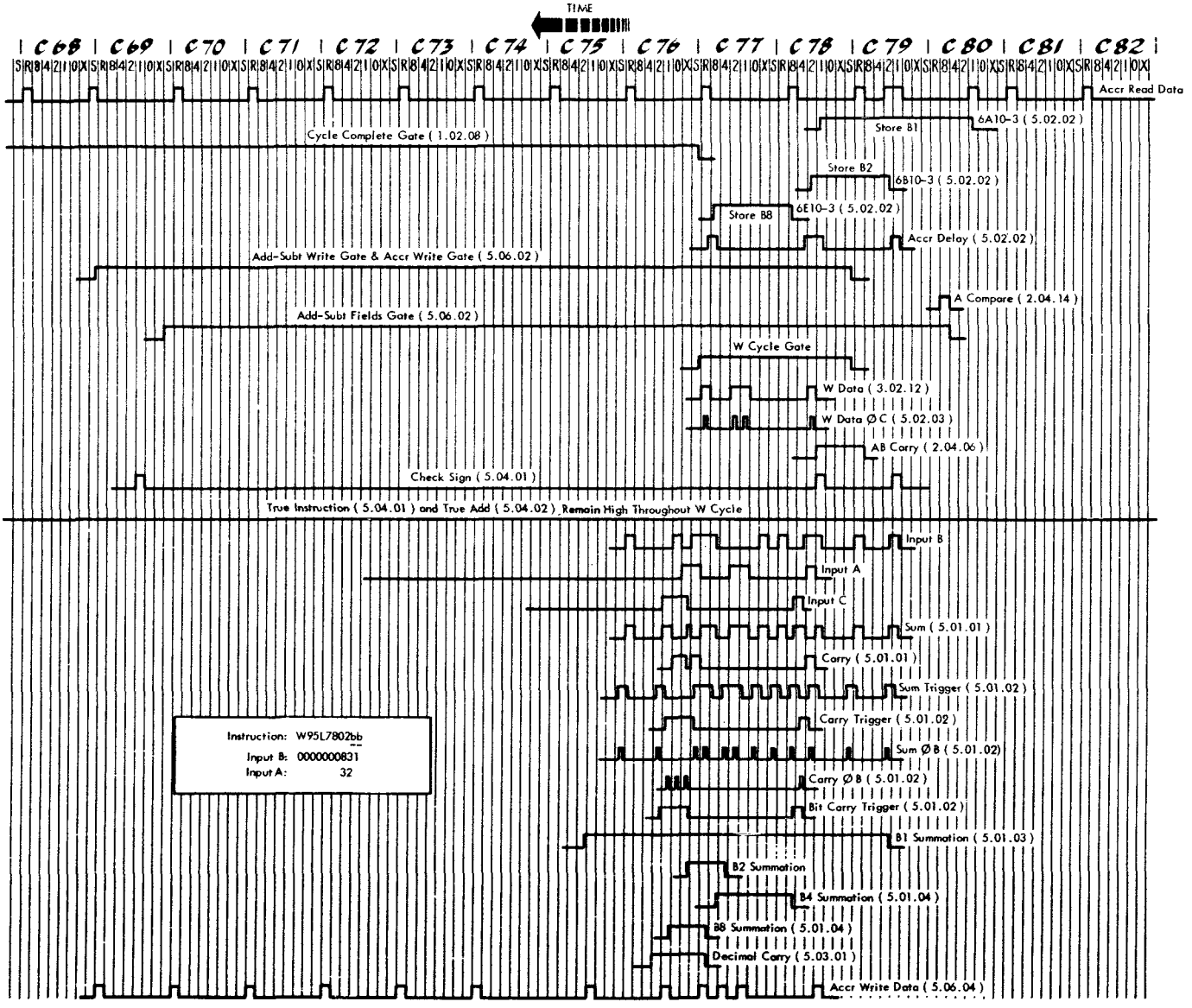


Figure 174. Example True Add Operation (W95L7802bb)

Adder Inputs: During the add subtract fields gate, adder input B has a complete field or fields of ∅B to ∅B on time data on it, as discussed above. W data enters adder input A from the core buffer during the add subtract fields gate. This data is further conditioned on 3.02.12 by W cycle gate which is established by the instruction. It is also conditioned on 5.02.03 by true add and add cycle gate. The bit carries and the decimal carry will function as outlined under "Adder" operation.

Parity Insert: The adder register out data appears on 5.01.05 in serial form, one character time after the inputs. At "and" switch 6H10, the add cycle data is allowed to pass through. These data bits are sent to 5.03.03 as parity insert control data. The trigger at 6J7 on 5.03.03 counts the bits within each character. If left 10 pin high at BR time, a BR is inserted in the data from adder line at 6G5a on 5.01.05.

Add Subtract Write Gate and Write Head: The data from the adder goes to 5.06.04 where it is gated with the add subtract write gate before going to the accumulator write circuits. Although the entire accumulator contents are sent to the adder from C9 through C0, the desired output will be from C8 through C9 of the next field. The add subtract write gate is developed on 5.06.02 at trigger 6V7. This trigger is pulled 3 pin high at C8 after the add subtract fields gate trigger is turned 3 pin high. It is pulled 3 pin low at C8 after the add subtract fields gate trigger is turned 3 pin low.

The full ten characters (or multiple of ten) of accumulator write data is sent to the write circuits on 3.10.42. Accumulator write trigger 5Q6 is flipped 3 pin high with each ∅C data bit from 5R5 pin 9. This trigger is flipped 3 pin low at each ∅C no data bit from 5R5 pin 6. The two complementary outputs of this trigger are gated to either side of the accumulator write head with an accumulator write gate. This latter is a conditioned add subtract write gate.

The sequence chart in Figure 174 illustrates the operation W95L7802bb with 0000000831 in accumulator 7 and 32 in characters 94 and 95 of W track.

Complement Add

Principles of RAMAC Complement Add

TENS COMPLEMENT

Complement addition within RAMAC is based on the tens complement principle. Using this principle, a number may be subtracted from another number by adding its tens complement. The tens complement of a number is the result of subtracting its units digit from 10 and all other digits from 9. For example, 473218 may be reduced by 51684 by two different methods to obtain the same answer.

Direct Subtraction	Complement Addition
0473218	0473218
− 51684	+9948316
0421534	0421534

Note that the carry from the high order position is dropped when doing tens complement addition.

Since this method of subtraction is used in RAMAC, a negative figure will appear on the accumulator track as its tens complement. When it is necessary to transfer such a number out of the accumulator with $T_1 = L$ or M, it is converted to a true number by complement addition to zero. A bit X is added to the units position digit to identify the number as being negative.

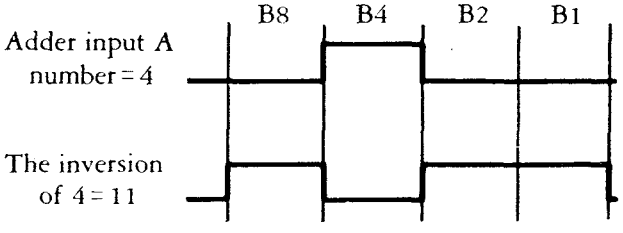
SIXTEENS COMPLEMENT

Since RAMAC stores and processes each digit as a four position binary number, the complement addition of individual bits within each digit must be done to a base of 16. This sixteens base binary number must then be modified to a decimal (tens base) number just as it was during true add.

In order to accomplish sixteens complement addition the following method is used:

1. The number coming from the core buffer is inverted into adder input A, giving the fifteens complement of that number.

Example:



2. A B1 pulse is automatically added to the units digit of the input A number to give the 16's complement of that number.

Example:	B8	B4	B2	B1
15's complement of 4 = 11	1	0	1	1
Add B1	0	0	0	1
16's complement, 12 results	1	1	0	0

The first digit from the core buffer into input A will always have a B1 added, as will all digits going into the C9 position of an accumulator. This B1 pulse,

automatically added into input C, is called "sixteens carry."

Modification from 16's Complement to 10's Complement

The sixteens base number that is in the adder register at the end of the add cycle must be modified to a decimal number during the correction cycle. This is accomplished during a complement add operation by either initiating a decimal carry or adding a +10 correction according to the following rules:

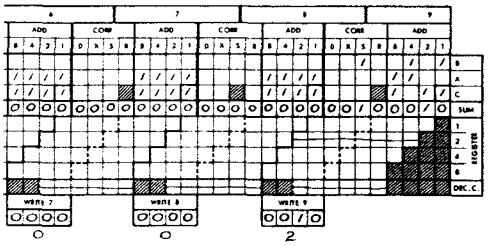
1. The need for a decimal carry is indicated by a bit 8 carry from the adder.
2. The need for a +10 correction is indicated by the absence of a bit 8 carry.

Complement Add Example Problems

1. True number resulting from a subtraction:

W75M2902
B = 00005
A = 03

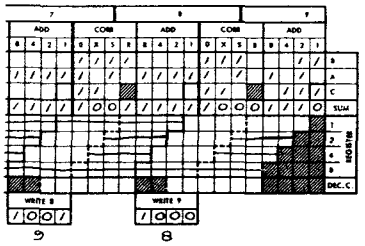
Result = 00002



2. Complement number resulting from a subtraction:

W75M2902
B = 00003
A = 05

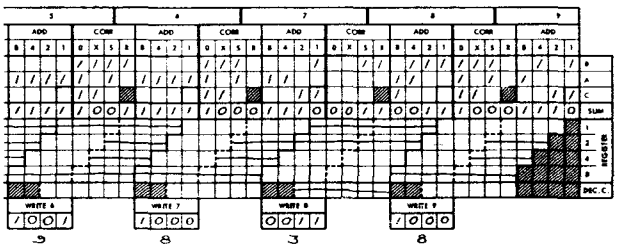
Result = 99998



3. Complement number resulting from the addition if a negative number:

W75L2903
B = 00175
A = 337 (negative)

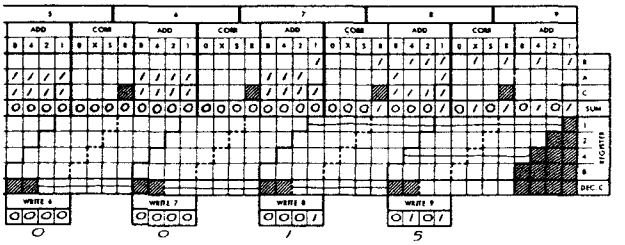
Result = 99838



4. True number resulting from the subtraction of a number that is entered one place to the left:

W75M2802
B = 00175
A = 16

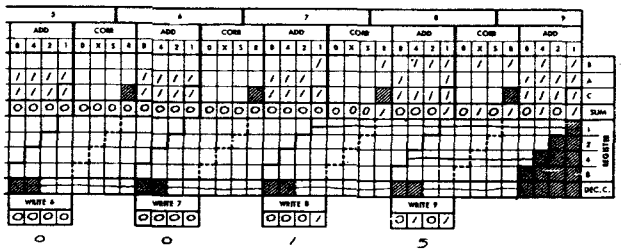
Result = 00015



5. True number resulting from adding a negative number that is entered one place to the left:

W75L2802
B = 00175
A = 16 (negative)

Result = 00015

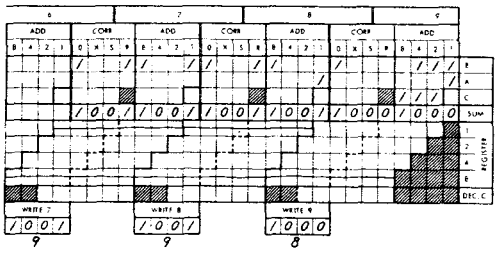


In example #5, note that true add, rather than complement add was performed during C9 time. The need for complement add was not recognized until Bx of C8. The sixteens carry was thus entered at B1 of C8. Compare with example #4.

6. There is a method of arriving at a complement result without complement adding the figure at input A. The addition of a positive figure to a negative number on the accumulator track is performed as a normal true add operation, since the negative number is already in the tens complement form.

W75L2903
B = 987 (complement)
A = 011

Result = 998



Complement Add Data Flow

During the add cycle, the data from cores is inverted to the fifteens complement form at adder input A by the complement add gate. At this time, the units position of the data from cores must be converted to the sixteens complement by the entry of a bit one into adder entry C. This occurs at AB carry time. In the event more than one accumulator is used during the complement add operation, there will also be a bit one added at every character 9 (units position of each accumulator).

A decimal carry is developed only if the result accumulated exceeds 15. This is indicated by a bit carry at BR time. The decimal carry signifies that the result in the adder register is already back to the tens complement form so no correction is necessary. A carry into the B1 position of the next character is needed, however, and is entered at input C.

No decimal carry signifies that the result is in the sixteens complement form, and must be corrected by adding 10 (Bs and B0) through input A during the correction cycle.

OBJECTIVES:

1. Develop complement add gate.
2. Read and delay accumulator track data (see true add).
3. Select desired accumulator track data (see true add).
4. Enter adder
   a. Complement core data.
   b. Insert units position sixteens carry.
   c. Correct result with +10 if no decimal carry.
5. Insert BR (see true add).
6. Select adder output (see true add).
7. Write result on accumulator track (see true add).

Complement Add Gate: This gate is developed at the same trigger that provides the true add gate (6M2-5.04.02). It will be pulled 3 pin high after an analysis of the T_2 character (L or M) and the sign of the factor coming from cores. This will be covered later in "Sign Analysis and Sign Control."

Adder Entry: The W data from cores is inverted at 6R10b on 5.02.03 to develop the fifteens complement input to the adder. The bit one carry to the units position is entered through input C (5.02.04) by the line labeled sixteens carry. This line is developed on 5.04.02, as a result of complement instruction and a check sign pulse. The check sign impulse (5.04.01) is a B1 at C9 or AB carry of W cycle. The AB carry occurs at BR to B2 of the first character coming from cores (see Figure 174). Character 9 allows a sixteens carry insert at the units position of each accumulator if more than one enters the adder. The number of accumulators (fields of the accumulator track) is determined by the M of the instruction.

A correction factor of +10 will be entered through input A only if there has been no decimal carry (6R8-5.02.03).

Sign Analysis and Sign Control

Sign Analysis

Sign analysis refers to the examination of the operation called for and the sign of the factor in cores to determine whether this factor will be true added or complement added to the factor in the accumulator. This is shown in the table below:

	+ Sign	− Sign
T_2 = L, Add	True add	Comp. add
T_2 = M, Subtract	Comp. add	True add

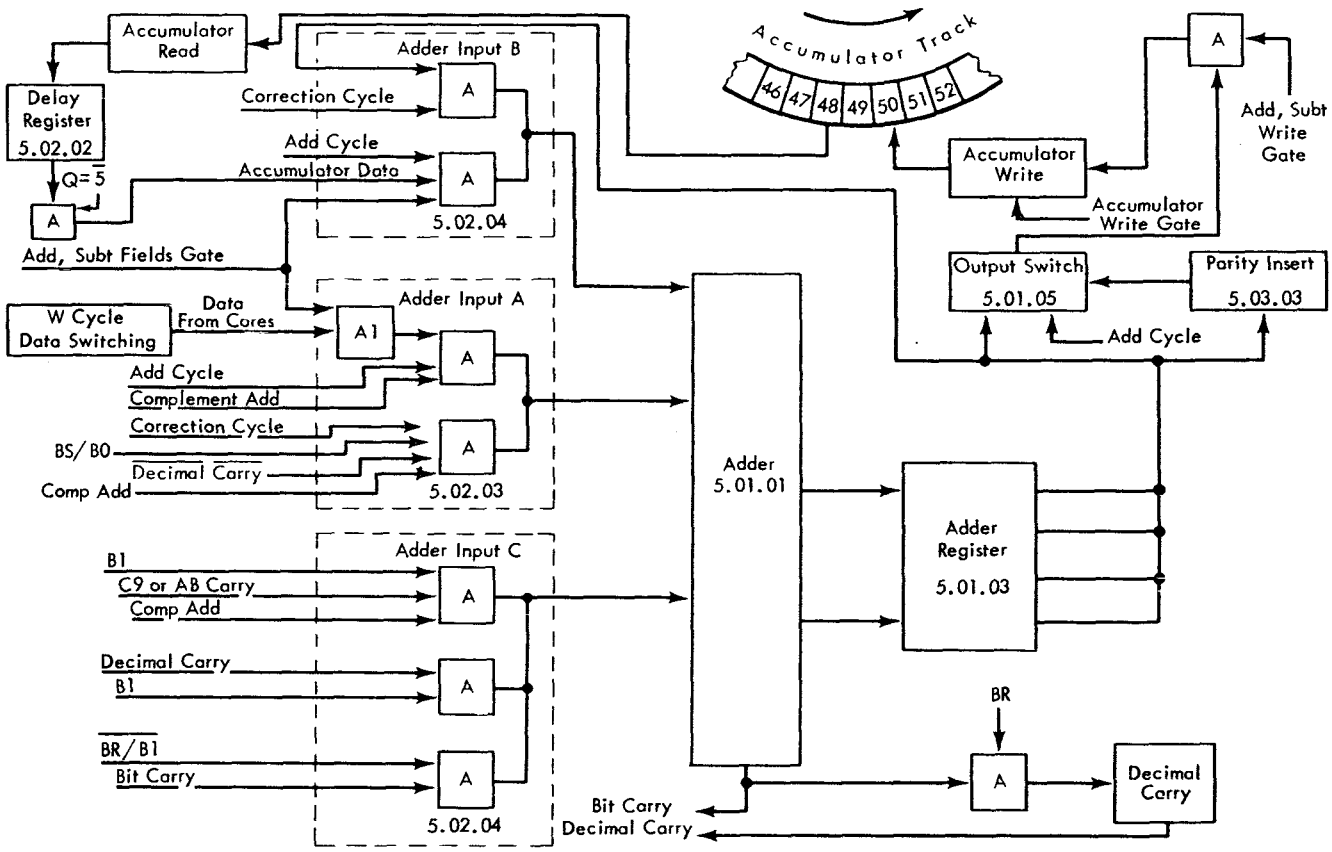


Figure 175. Complement Add Data Flow and Controls

The accumulator track consists of ten separate 10 position accumulators which cannot be coupled. However, the RAMAC is designed to permit more than one accumulator to be added to or subtracted from during one program step. For example, an instruction W95 L7743bb will add 43 characters from W track to the accumulator track. Characters 95 through 88 will enter accumulator 7 beginning with character 77. Characters 87 through 78 will enter accumulator 6, characters 77 through 68 will enter accumulator 5, etc. The first character from W track will be analyzed for a sign; after that each character entering the C9 position of the accumulator will be analyzed. Some factors from W track may true add and some may complement add to the accumulator depending on the sign stored in the units position of the factor. A bit X written in the units position indicates a negative number on the process drum (excluding the accumulator track) or file.

Circuit Development

Each character coming from cores during W cycle is checked for the presence of a Bx. Any Bx flips the sign trigger 6R4 on 5.04.01 3 pin high (or minus). Every Bs then returns the trigger to 10 pin high (or plus). The two instruction, T=L and T=M, are switched with the outputs of this trigger to raise either complement instruction or true instruction each character. This switching results in the sign analysis pattern shown above. Since the only positions which contain a sign are the first one or those arriving at the adder at C9 time, this is when a check sign impulse, developed at 6Q4, on 5.04.01, tests the true or complement instruction line. This B1 check sign impulse controls the condition of the true-complement trigger on 5.04.02 and also develops a sixteens carry for complement add.

Sign Control

For purposes of console display and control panel decisions, the sign of each accumulator is stored in a relay. The condition of zero or non-zero for each accumulator is also stored in relays. The points of these relays used for control panel decision elements and console lights are shown on 5.05.09. The pick and drop-out of the sign relays (5.05.02, 5.05.03) is thyratron controlled. A pulse on the fire minus (thy) line picks the desired relay, indicating a negative quantity in that accumulator. A fire plus pulse causes the blow-out thyratron to conduct, dropping the relay.

Immediately following any operation on an accumulator the following items must be analyzed to determine what the new sign is to be:

1. The operation performed, determined by the instruction and the sign of the factor in cores.
2. The original sign of the accumulator.
3. Was there a decimal carry from the high order (character 0) of the accumulator?

The table in Figure 176 covers all the possible conditions with numeric examples.

This table can be covered by a standard rule. During a true add operation there should be no decimal carry and during a complement add operation there should be a decimal carry if the sign is to remain unchanged. Any violation of this rule indicates a sign change of the accumulator or an overflow of the accumulator.

Control Logic

Figure 177 shows the flow of information required to change the accumulator sign. The ten sign relays are scanned each machine cycle by the field ring. The plus and minus trigger indicates the sign condition for each accumulator during its field. This in turn raises the write minus or write plus line during each accumulator field. During an arithmetic operation, all the items required for sign control are compared. The C9/Bx pulse checks the decimal carry trigger for the high order (C0) of the previous field. Q = 5 tells the machine to ignore the accumulator factor and its sign.

Following the operation on any accumulator the fire minus or fire plus line will send a pulse to the sign relay storage unit, except in the two conditions of no sign change shown on the chart.

Circuit Development

On 5.04.03 the normally closed points of each sign relay are scanned one field early. On 5.04.04 the plus-minus trigger is set at C0B1 and will indicate the accumulator sign during the correct field. On 5.04.05 the write accumulator sign trigger is set at C9B0 to C9B0 of the next field. At C9Bx on 5.05.01 (6F5a)

Result	Operation	Accr. Sign	CO Decimal Carry	Controling Unit 5.05.01	Examples Actual	Examples Adder
FIRE MINUS	True Add	–	No	6L2	-012 +009 -003	988 009 997
	Comp Add	–	Yes	6L3	-012 -009 -021	988 991 DC 979
	Comp Add	+	No	6E5	+012 -015 -003	012 985 997
	Comp Add Q = 5	+ or –	No	6D5	000 -007 -007	000 993 993
FIRE PLUS	True Add	–	Yes	6D6	-012 +022 +010	988 022 DC 010
	True Add Q = 5	+ or –	No	6D7	000 +031 +031	000 031 031
	FIRE ZERO			6F6a	+022 -022 000	022 978 DC 000
	T_2 = N (Multiply) Fire Plus For Accr 0 & 1			6L9b	Accr 0 & 1 Used For Product	
No Sign Change	True Add	+	No		+023 +040 +063	023 040 063
	Comp Add	+	Yes		-015 -021 -036	985 979 DC 954
FIRE OVERFLOW	True Add	+	Yes	6B6 5.05.07	+939 +200 X 139	939 200 DC 139
	Comp Add	–	No	6C7 5.05.07	-939 -200 X 139	071 800 871
	Comp Add	–	Yes	6B7 5.05.07	-939 -061 X 000	861 939 DC 000
		FIRE ZERO				

Figure 176. Accumulator Sign Analysis

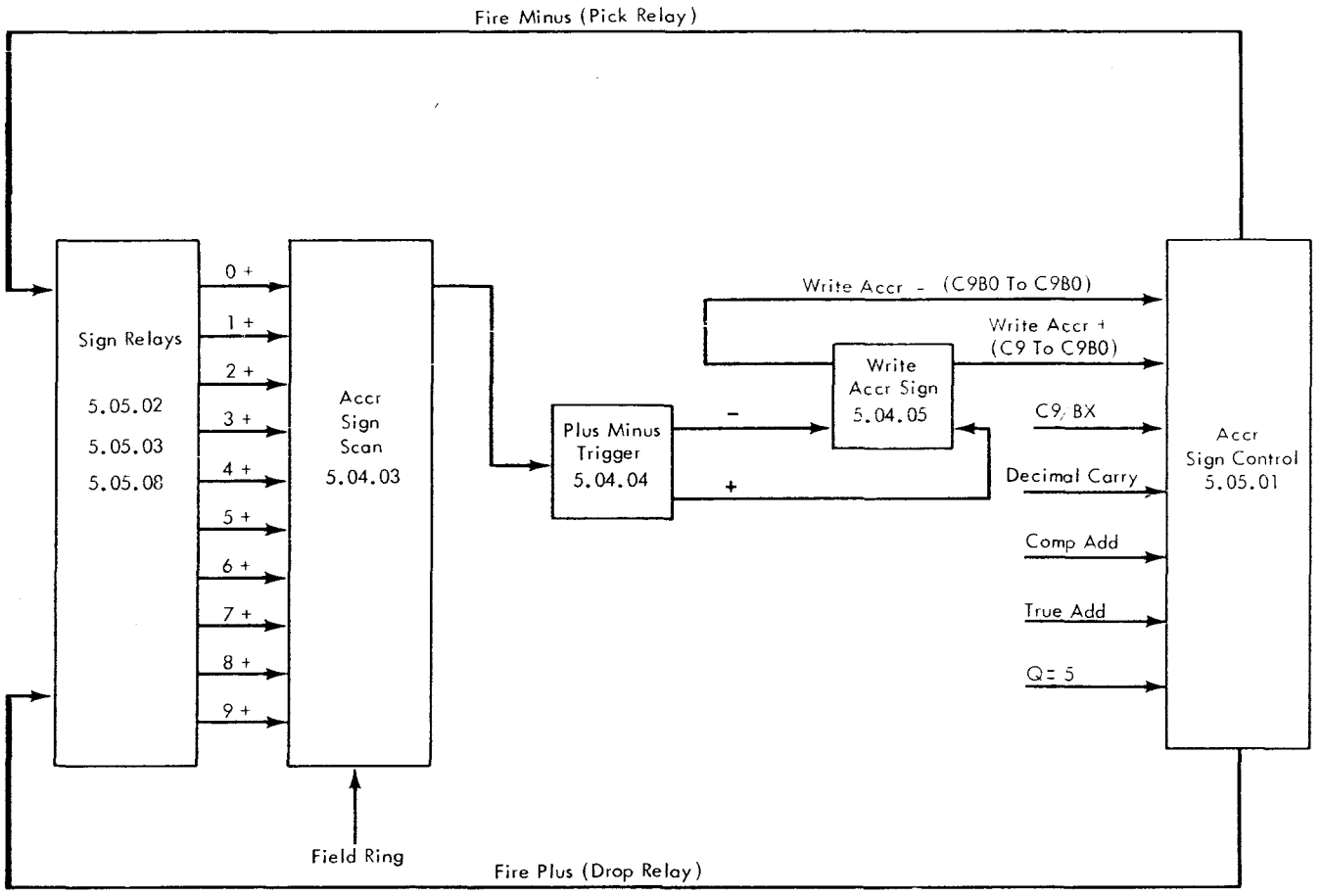


Figure 177. Accumulator Sign Control Logic

we will mix all the required items together at one of the units indicated on the chart to provide a fire plus or minus. This occurs during the units position of the next accumulator. The fire minus line will flip trigger 6Y2 10 pin high. At character 7 time pin 10 is scanned to develop a fire minus (thy) line. This occurs 3 characters after the accumulator operation was completed. Fire plus is simply the C9/Bx pulse from 1K 6M1b.

All units on 5.05.01 used for sign control during add or subtract operations are gated with the add subtract write gate. Fire Plus when the accumulator is zero is developed at 6F6a with only the fire zero line high. Sign control during multiply and divide will be covered later in the appropriate sections.

Zero Control

If any operation should cause an accumulator to go to zero, the zero relay for that accumulator must be energized. Each of the zero relays (5.05.05, 5.05.06) is controlled by two thyratrons: one thyratron to energize the relay, and the second thyratron to drop the relay by extinguishing the first.

The method of controlling the zero and non-zero thyratrons is to examine the data scanned out of the adder on add cycle during each field that the add-subtract write gate is high. If any bit is included in this data, the accumulator is not at zero and a fire non-zero pulse is supplied. If the data is completely blank, a fire zero pulse is provided. Note that each thyratron is gated by the field gate following the accumulator field, to allow the correct thyratron to be fired after the data has been examined for that accumulator.

The fire zero and fire non-zero pulses are developed at 6E8b and 6M10a (5.05.04). The test pulse, BrC9 or BrCl is developed at 6E9. These test pulses are controlled by 6E7 so that they are available only during accumulator write gate or reset cycle. Each test pulse will cause either a fire zero or a fire non-zero output, depending on the state of the zero field trigger, 6F7.

6F7 is plate pulled pin 3 high by each B0C8 pulse through 6F8a. If any numeric data bit is scanned out of the adder during the add-subtract write gate, 6F7 will be plate pulled pin 10 high from 6F8b.

Reset zero field search (5.01.05) is developed at 6H10 by the "anding" of add cycle and register out. At this point neither X nor R bits have been added to the data from the adder register.

In multiplication and division operations, fire non-zero is forced for accumulator 1 and 0. This is accomplished by clamping the left grid of 6F7 (5.05.04) at its high level by multiply/divide: zero thyratron control, which is developed at 6W9 (5.06.02) for multiplication and at 6W8 for division.

Accumulator Overflow

RAMAC has only one overflow relay, R27 (5.05.08). It is a latch type, and will be picked if any one of the ten accumulators should overflow. After an overflow, the overflow hubs will remain transferred until an impulse is wired into the overflow drop out hub. This will latch trip R27.

It is not possible for an accumulator to overflow on an operation having Q = 5. For this reason Q = not 5 is supplied as one input of the thyratron 6A5. Note that 6A5 is fired by fire overflow and extinguished by firing of 6A6 during P cycle.

Fire overflow is developed on 5.05.07 as a result of any one of the three sets of conditions listed in Figure 176. The overflow trigger is only used to indicate a decimal carry during a complement add and a negative accumulator, a normal occurence. Its output, however, is "anded" with fire zero to indicate the special overflow condition resulting in a zero accumulator.

Reset Cycle

Since the sign data and the zero, non-zero data are stored in thyratron controlled relays, removing DC from the RAMAC will destroy this data. The first I cycle following an X reset becomes a reset cycle (1L1-1.01.02) during which time the data on the accumulator track will be scanned to repick the appropriate zero relays. Any accumulator which contains a negative number will have a Bx in character 0, therefore, C0 of each accumulator must be scanned during a reset cycle to repick the sign relays. The writing of the Bx must be done when the accumulator goes minus. The sequence chart in figure 178 illustrates this operation.

OBJECTIVES:

1. Write Bx in C0 when accumulator goes minus.
2. Develop reset cycle gate after reset.
3. Scan accumulator data for zero.
4. Scan C0Bx to fire minus.

Write Bit X: The bit X is inserted into data from the adder at 6H11b on 5.01.05. The fire minus line is a C9/Bx from 5.05.01 indicating a minus result. Remember that data from the adder is one character late so the bit X is written in character 0 of the accumulator track.

Reset Cycle: The reset cycle trigger (1L1-1.01.02) is reset 3 pin high by X reset, and mixes with I or P cycle. It is pulled 3 pin low at the end of I cycle by the reset cycle reset line.

Repick Zero Relays: The reset cycle line allows C0/CL BR's to test the zero field trigger (6F7-5.05.04) and fire zero or non-zero. The data from the accumulator must pass through the adder to become reset zero field search data on 5.05.04. The add subtract write gate must be up at 6F8b on 5.05.04. The add subtract fields gate must also be up to allow all ten fields of the accumulator track to pass through the adder.

On 5.06.02, the reset cycle line flips the add subtract fields gate trigger 3 pin high. This in turn flips the add subtract write gate trigger 3 pin high at C8 time. The reset cycle line also blocks the accumulator write gate to prevent writing on the accumulator track.

Repick Sign Relays: On 5.05.01, the restore sign trigger, 6E6, will be flipped 10 pin high by a Bx at C1 of the accumulator read data during a reset cycle. At C9/Bx of the next accumulator field, we flip trigger 6Y2 10 pin high from the restore sign trigger, if a C0Bx was sensed. This results in a fire minus (thy) at C7. At C8 and RM the restore sign trigger is restored to 3 pin high.

Accumulator Read Out

When an instruction with a T_1 = L or M is executed, the numeric data must be transferred from the accumulator into the core buffer during R cycle. This data is passed through the adder for several reasons. First, the early accumulator data must be delayed one character time to enter cores on time. Secondly, a negative number in the accumulator must be converted from complement to true form.

The data flow chart for this operation is Figure 179. On every R cycle, accumulator data enters adder input A directly, one character early. Each accumulator sign relay is scanned to develop a true or complement add gate for that accumulator. This is the only entry to the adder during add cycle. The serial data from the adder goes to the output switch where BR's are inserted. Also, an absence of bits from the adder represents a zero so B0's must be inserted. Any negative accumulator must have a Bx in the units position to identify it on the process drum, since it is now in true form. The units position will be the first character to enter the adder after AB carry. If more than one

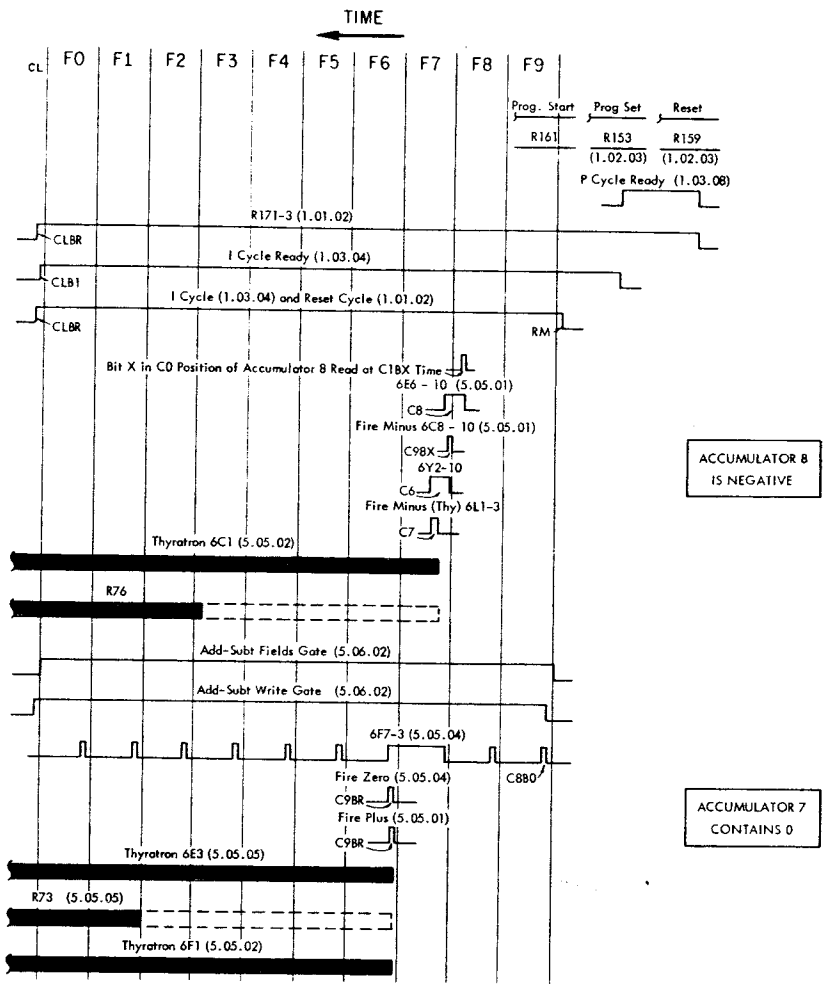


Figure 178. Reset Cycle Operation

accumulator is read out, all those following the first will have their units position in C9. Remember, the Bx on the accumulator track was only used to pick the minus relays on a reset cycle and was located in C0.

The zero insert requires more discussion. Since the B0 insert must occur during a correction cycle, the analysis of the adder register for this condition must occur before correction. Using an unmodified binary counter, the zero condition may appear in several forms. During a true add operation it will always occur as no 8, 4, 2 or 1 bits since adder inputs B and C will never receive any data. During complement add several conditions may arise as shown below:

Accr Track	9	9	9	0	3	9	9	0	0	0
Input A	6	6	6	15	12	6	6	15	15	15
Input B	0	0	0	0	0	0	0	0	0	0
Input C							1	1	1	1
Result	6	6	6	15	12	6	7	0	0	0
Correction	10	10	10	10	10	10	10			
Sum	0	0	0	9	6	0	1	0	0	0

The fifteens complement of the complementary number appearing on the accumulator track is shown at adder input A. A sixteens carry is inserted into the units position at input C. This results in decimal carries to the next position since our counter rolls from 15 to 0. The result before correction must be tested for zero inserts. A digit 6 and a digit 0 always require a zero insert when complement adding. Notice that when using the tens complement form on the accumulator track, any zeros to the right of the lowest order significant digit are in 10's complement form, as well as the low order significant digit.

OBJECTIVES:

1. Scan sign relays to develop a true or complement add gate.
2. Enter adder input A during R cycle.
3. Insert Bx at C9 of negative accumulators.
4. Insert B0's.
5. Insert BR's (see "True Add Operation").
6. Gate adder output to cores.

True or Complement Add: Since the accumulator read data is obtained one character early, the data from accumulator 9 enters the adder during the interval from CE through C91; the data from accumulator 8 enters the adder during the interval from C90 through C81, etc. Because of this timing, the true-complement trigger, 6M2 (5.04.02), must be forced into the desired state at CE or C0. During read out, 6M2 is controlled from 6N2 and 6P3 by not accumulator sign scan and accumulator sign scan, respectively. These two units are gated with R cycle and a B1CE or B1C0 test pulse. These gates (5.04.04, 5.04.03) represent the positive or negative condition of accumulator 9 during CE time, accumulator 8 during F9 time, etc.

Adder Input A: On 5.02.03, the accumulator read data, one character early, is permitted to enter the adder when the accumulator to adder gate is high (6S10b). This gate is actually R cycle, developed on 5.06.04. Within adder input A, the data is mixed with the true or complement add gate.

Bx Insert: During complement add on an R cycle, a bit X is inserted in the units position of the accumulator data at 6G6 on 5.01.05. The units position will occur at AB carry for the first accumulator read out or at C9 of all following accumulators read out.

B0 Insert: The bit 0 is inserted at 6G5b on 5.01.05 when the zero insert trigger on 5.03.02 is 3 pin high. This trigger is set 3 pin low at B1. Then either of two conditions existing in the adder register at BRØC will pull it 3 pin high. These conditions are explained above.

Adder to Cores: The on time data from adder goes to 3.02.06 where it is gated with T = L/M to become read data. This in turn is gated by R cycle and ØC (3P2) to become data to cores.

Read Out Example

Figure 180 shows an example of a read out operation for the instruction L84Y5912 with accumulator 8 negative and accumulator 7 positive. The number in accumulator 8 is 9248900426. The number in accumulator 7 is 0000000019.

Read Out and Reset

In a $T_1 = M$ operation the accumulator track is the origin of a data transfer as in the case with $T_1 = L$. In addition to data transfer, however, the particular

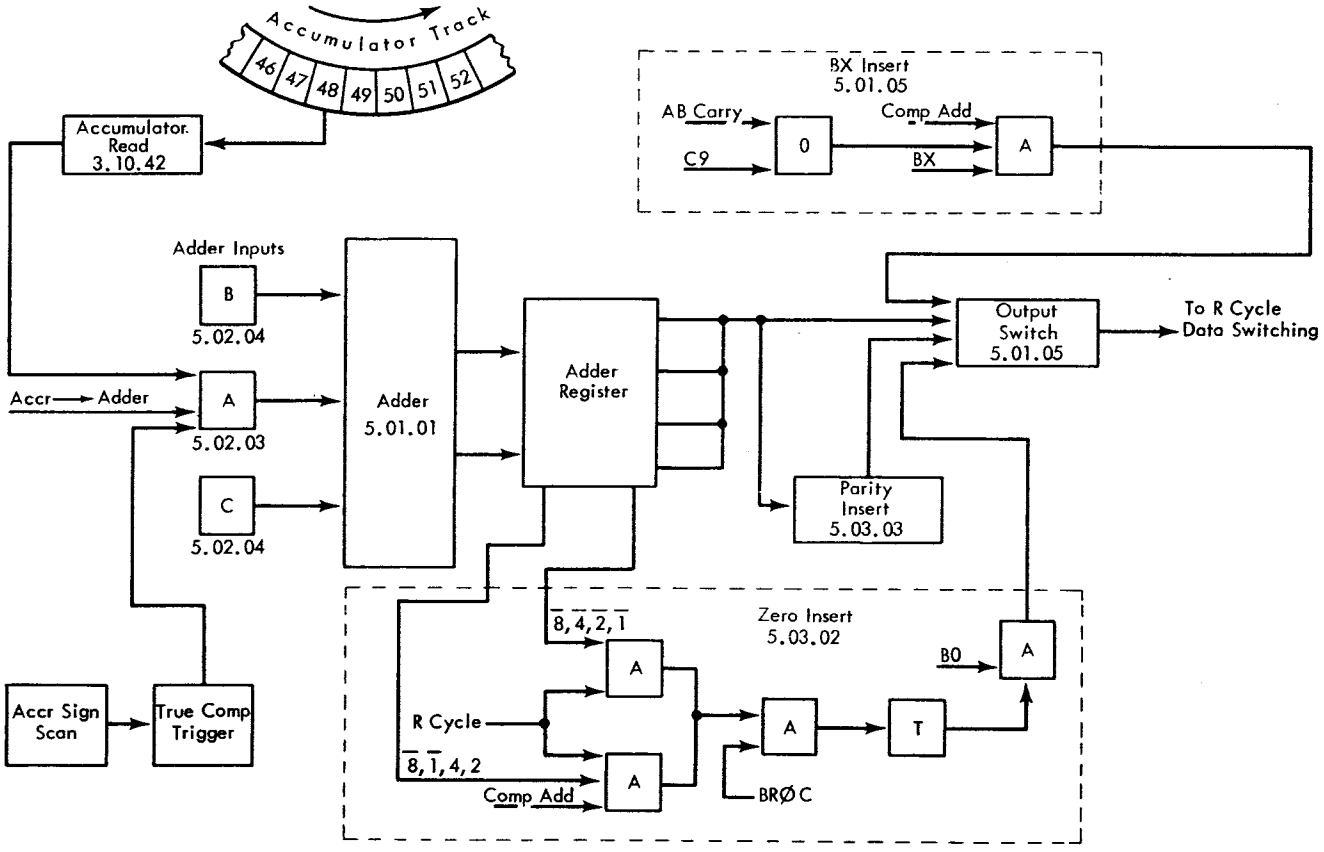


Figure 179. Accumulator Read Out Data Flow and Controls

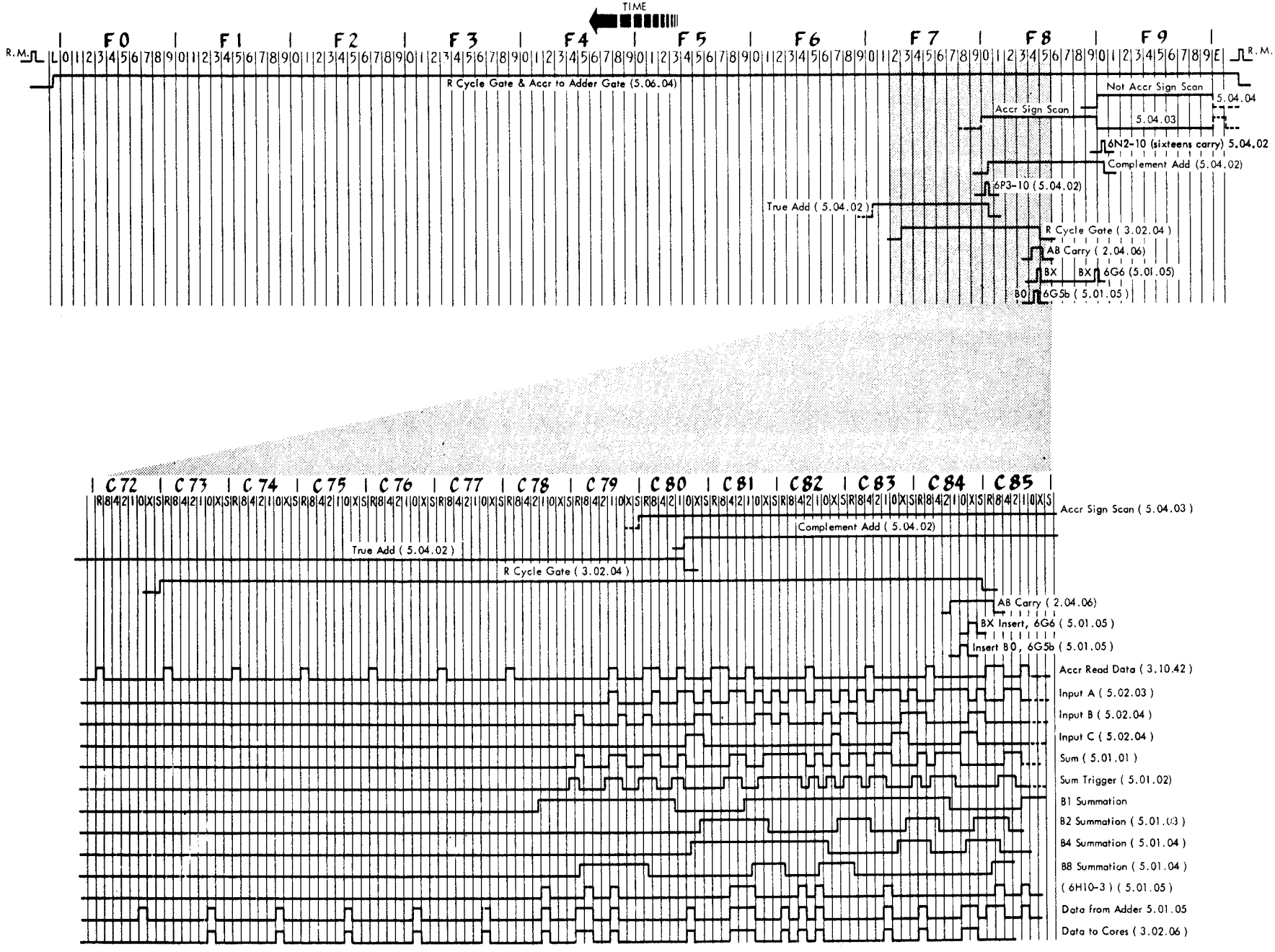


Figure 180. Read Out Operation (L84Y5912bb)

accumulator from which the data is taken must be reset to zero. It is important to note that a read out and reset operation requires that the complete accumulator be reset if any part of it is reset.

To accomplish read out and reset we need only to modify read out by bringing up the accumulator write gate but provide no write data, i.e., write blanks in the accumulator. Accumulator write gate is brought up on 5.06.02 by read out and reset coming from 5.06.01. The read out and reset trigger will be pulled 3 pin high at C8 of a T = M operation when the set up trigger is 3 pin high. This will occur at A compare, which is a C0B8 pulse occurring prior to the field in which the AB counters develop a carry, i.e., develop R/W cycle gate. This assures us that the entire accumulator will be reset. At C9 after the cycle complete gate is raised (6X8b - 5.06.01) the reset trigger will be pulled 3 pin low dropping the accumulator write gate.

During this time no data should be present on the accumulator write data line on 5.06.04.

Multiplication

Multiplication is performed by RAMAC as a series of repetitive additions, involving three process drum tracks: the multiplicand track, the partial product track, and the accumulator track. The multiplicand track is addressed by a T_1 or T_2 of V, and may serve either as the track of origin or destination in a transfer of data. The partial product track may not be addressed, but is utilized automatically in the process of multiplication. The accumulator track was discussed in the development of addition.

The multiplicand is limited to 9 digits. A larger multiplicand might develop an 11 digit partial product and the high order digit would be lost. The product can be as large as 20 digits; therefore, an 11 digit multiplier may be used with the 9 digit multiplicand to develop a 20 digit product. A larger multiplier may be used; however, all lower order digits beyond the 20 high order digits of the product are lost.

Programming of Multiplication

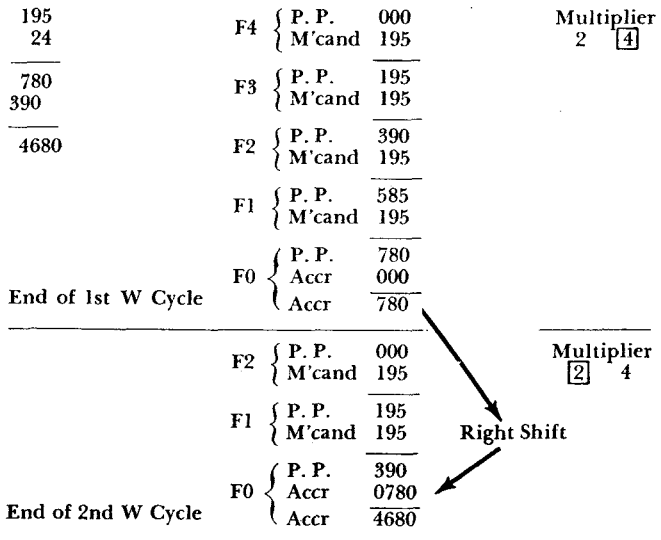
In order to accomplish multiplication, the following two program steps are necessary:

1. The first, containing a T_2 of V, writes the multiplicand once in each field on the multiplicand track. The A_2B_2 is normally 99 to cause the units digit to be written in the C9 position of each field.
2. The second instruction contains a T_2 of N, an A_2B_2 of 99, and an MN of the number of digits in the multiplier. The $T_1A_1B_1$ part of the instruction is the address of the multiplier. This program step requires an I cycle, an R cycle and a long W cycle composed of as many machine cycles as there are digits in the multiplier. Thus with an MN of 06, there will be six machine cycles. We shall call each machine cycle occurring during this long W cycle a "multiply W cycle."

Theory of Multiplication

Multiplication by the RAMAC is a series of repetitive additions combined with the right shifting of the partial products stored in the accumulator. The number of additions of the multiplicand to itself is controlled by the digits of the multiplier. Each digit of the multiplier, beginning with the low order, requires a complete machine cycle to perform its adding requirements. Each of these cycles are W cycles, therefore a multiply operation requires as many continuous multiply W cycles as there are digits in the multiplier. The multiplicand is added to itself by adding each field of the multiplicand track to each field of the partial product track and writing the sum on the next field of the partial product track.

Since the largest possible multiplier digit is 9, requiring 9 additions, one field is left in the machine cycle to add the partial product to the previous partial product from the accumulator track. At the same time the accumulator data must be shifted right one character, so that the tens position adds to the units position of the partial product. This sum is then rewritten on the accumulator track in accumulator 0. This is shown in the example below:



Notice that the developing product is being shifted out of accumulator 0 into accumulator 1 during the

right shift. These two accumulators (20 digits) are reserved for the product. The units position of the product will always be found in character "n−2" of accumulator 1 where "n" is the number of digits in the multiplier.

Multiply Data Flow

Figure 181 shows the data flow and controls during a multiply W cycle. The multiplier has been previously placed in each of the 10 fields of the multiplicand track with a $T_2 = V$ instruction. On a $T_2 = N$ instruction, I cycle and R cycle occur normally, placing the multiplier in cores. For example, W49N9902bb would place C49 and C48 of W track in the cores.

At CE time of each multiply W cycle, the multiplier digit is transferred to the multiplier comparator, core position 00 reading out on the first W cycle, position 01 on the second cycle, etc. At the comparator, the digit is analyzed to raise the multiplicand to adder gate for the number of fields specified (See gate 1 on Figure 181). This gates on time data from the multiplicand track into adder input A. The fall of this gate is fixed at C9F0, therefore, the time it is brought up determines the number of additions performed.

The output of the adder is written on the partial product track one character late, due to the adder delay. Nine characters later this same information must be read from the partial product track, on time, to adder input B to add with the next multiplicand field. Therefore, the partial product write head is physically displaced 9 characters ahead of the read head. The partial product to adder gate (gate 2 on Figure 181) is raised one field after the multiplicand to adder gate, when the first partial product is read from this track.

By C8F0 the fully developed partial product has been written on the last field of its track. During field 0 this data will be added to the right shifted accumulator track. On the first W cycle accumulators 0 and 1 contain zeros; however, on following W cycles the previous partial product is located there. C8F1 through C9F0 of the accumulator track will be right shifted through the delay register. C9F1 is lost each shift cycle. C8F0 through C0F0 of the accumulator track will be shifted right by the one character delay of the adder. While C8F0 of the accumulator enters adder input A one character early, C9 of the partial product track is entering adder input B since the partial product to adder gate is still up. The accumulator to adder gate (gate 3 on Figure 181) is up from C9F0 to C0F0 to gate C8 through C0 to the adder. The shift gate (gate 4 on Figure 181) is up from C8F1 through C9F0 to right shift the rest of the product accumulators.

The accumulator write gate will be up for field 1 and field 0 to gate the data from the delay register and the adder to the accumulator write head.

To summarize, the major objectives of multiply are listed below. The detailed objectives will be covered later.

MAJOR OBJECTIVES:

1. Place multiplicand on track V with a $T_2 = V$ instruction.
2. Place multiplier in core buffer on R cycle of a multiply instruction, $T_2 = N$.
3. Analyze first multiplier digit on W cycle.
4. Repetitively add multiplicand to itself (partial product).
5. Shift accumulators 1 and 0 right one character.
6. Add partial product to accumulator 0 (during shift).
7. Analyze next multiplier digit and repeat steps 4, 5, and 6.
8. Continue for MN times.

Loading the Multiplicand Track, $T_2 = V$

When the instruction having a $T_2 = V$ is executed, the multiplicand is written into each field of the multiplicand track. In order to accomplish this special type of transfer, the W cycle gate is raised by the leading edge of each C9, and lowered by N compare. A special operation is also required of the core buffer.

If the instruction W75V9907 is executed, the data from C75 through C69 of track W will be transferred into the core buffer during R cycle. During W cycle, the W cycle gate will be raised at the leading edge of each C9 and will be lowered by N compare at the trailing edge of each C3. When the W cycle gate is lowered, the core units and tens rings will have advanced to 07. Since the same characters must be entered into each field of the multiplicand track, the core units and core tens rings must be reset prior to the beginning of each field.

An additional requirement of $T_2 = V$ is to erase and then insert R bits in any position on V track which does not receive data.

OBJECTIVES:

1. Develop 10 W cycle gates of 9 characters or less to load multiplicand track.
2. Erase V track and insert BR when W cycle gate is down.
3. Reset core units and tens rings to 00 at each C0.

W Cycle Gate: Pin 10 of the W cycle multiplicand trigger, 3W2 on 3.02.08, controls the W cycle gate through AI 3X3a. Each C9 pulls this trigger 10 pin

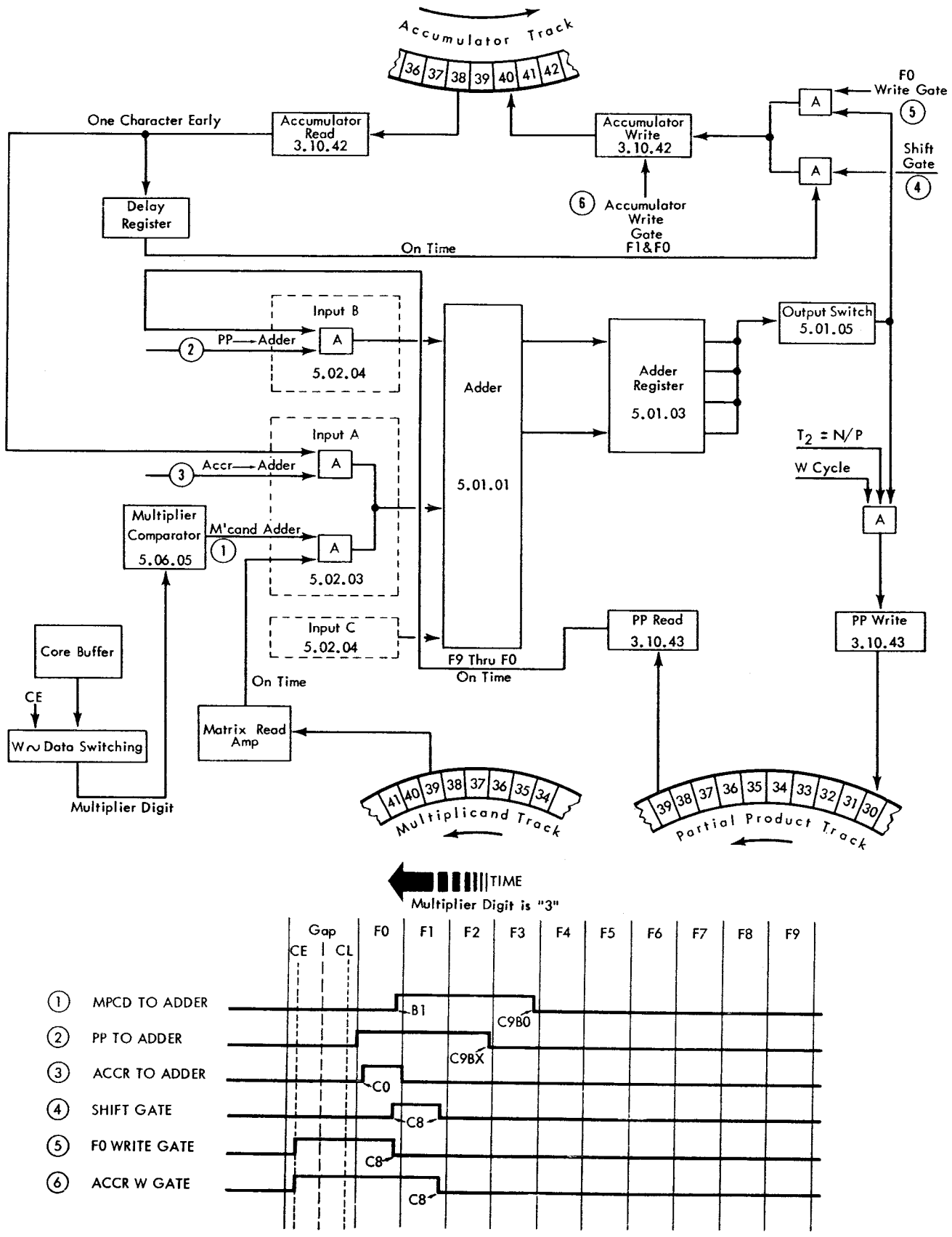


Figure 181. Multiply Data Flow and Controls

high. At N compare it is pulled 10 pin low. N compare (2.04.14) occurs 10 times during W cycle, when the digit value of the N register is the same as the quantity in the B_2 counter which began advancing at BR of CE time. In the example above (W75V9907) N compare will occur each C2 at Bs⌀B, seven characters after C9.

Erase and Insert BR: Erasing of V track when the W cycle gate is down, is accomplished by keeping the matrix write gate high throughout W cycle. T = V is "anded" with W cycle at 3V6a (3.02.09) to keep the matrix write gate high. Since the matrix write gate remains high during intervals of time when no data is coming from core buffer, R bits must be inserted into the matrix write data path to prevent subsequent parity errors. BR pulses are inserted into the matrix write data through 3U7 (3.02.12), where they are gated by not W cycle gate, T = V, and W cycle.

Reset Core Buffer: Buffer counter reset (3.02.10) is supplied from 3Q3 with the anding of C0, T = V, W cycle and the output of 3Q4 from every B0 to every Bs. Thus, buffer counter reset is high from B0 to Bs of every C0 during W cycle when T = V.

Multiply, T_2 = N

For this discussion, the major objectives listed above under "Data Flow" will be broken down into detailed objectives. Notice that there is no sign analysis of the multiply factors. A fire plus is developed at 6L9b on 5.05.01 for the product accumulators on all multiply operations. Figures 182 and 183 illustrate portions of a multiply instruction W49N9902bb, with factors of 746 × 43.

OBJECTIVES:

1. Transfer multiplier to core buffer during R cycle (see "Track to Track Transfer").
2. First multiplier digit to multiplier comparator.
3. Gate required number of fields from multiplicand track to the adder with the M'cand to adder gate.
4. Write adder output on partial product track.
5. Gate partial product track output to adder with PP to adder gate.
6. Right shift accumulators 0 and 1 one character.
7. Add partial product track to accumulator 0 during shift.
8. Write shifted accumulator 0 and 1 data.
9. Repeat W cycles for MN machine cycles.

Load Multiplier Comparator: The comparator on 5.06.05 is a modified binary counter capable of developing a carry when advanced from 9 to 0. The multiplier digit is entered as W data which is strobed by the bit ring to set each of the four triggers. This must occur prior to the multiply W cycle, at CE time. To develop W data from the data from cores at 3K4 on 3.02.12, the W cycle gate must be raised during CE time. On 3.02.08 at 3X3b the not W cycle gate is lowered by the "anding" of T_2 = N and multiplier read out gate. This gate is always raised at RM and lowered by the first Bs⌀B of a drum revolution (1P4 - 1.01.07). See Figure 183.

During this special W cycle gate, a core start is developed on 4.11.00 at Bx of CE at 4H5. The character register reset line will be high during this time while the core bit ring is still at Bs (4M6). The core buffer counters are reset (3.02.10) at CL of R cycle and then the reset is suspended for the duration of W cycle by T_2 = not N being low. This enables the multiplier digits to be read out progressively at each CE time, since the core units and tens rings are advancing.

Multiplicand to Adder Gate: The multiply comparator counter (5.06.05) is advanced each field time with C9. A carry pulls the multiplicand gate trigger on 5.06.03 3 pin high to raise the MPCD to adder gate at C9B0 time. This gate remains high until the beginning of F0. On 5.02.03 the matrix read data is gated into adder input A through 6R9. True add will be up throughout multiply, since there is no sign analysis. The matrix read data is from V track, which is selected by TN = 5 and TZ = 0. TN = 5 is high since T_2 = N. TZ = 0 is artificially developed on 3.10.14 at 5S6a.

Partial Product Write: Data from the adder is gated to the partial product write circuits by T_2 = N/P on 3.10.43. The trigger at 5T3 is flipped 10 pin high by a bit from the adder, to cause *write 1* current to flow at the fall of ⌀C. With no bits from the adder 5T3 is flipped 3 pin high for *write 0* current. Notice that the partial product track is constantly erased except when data from the adder is present.

Partial Product to Adder Gate: The adder output is written one character late and the PP Read Head (3.10.43) is physically positioned and adjusted to read the data 9 characters after it is written. Therefore, 10 characters after character 9 of the multiplicand track first enters the adder, it is returned from the partial product track to adder input B. At the same time C9 of the multiplicand track is again entering input A. The partial product to adder gate is developed on 5.06.03 (6T4) at BxC9, one field after the MPCD to adder gate came up. This gate will stay up until CL.

Right Shift: The product, which is being accumulated in accumulators 0 and 1, must be right shifted each W cycle, before the next partial product is added to it.

All accumulator data is appearing at the output of the delay register as on time accumulator delay data.

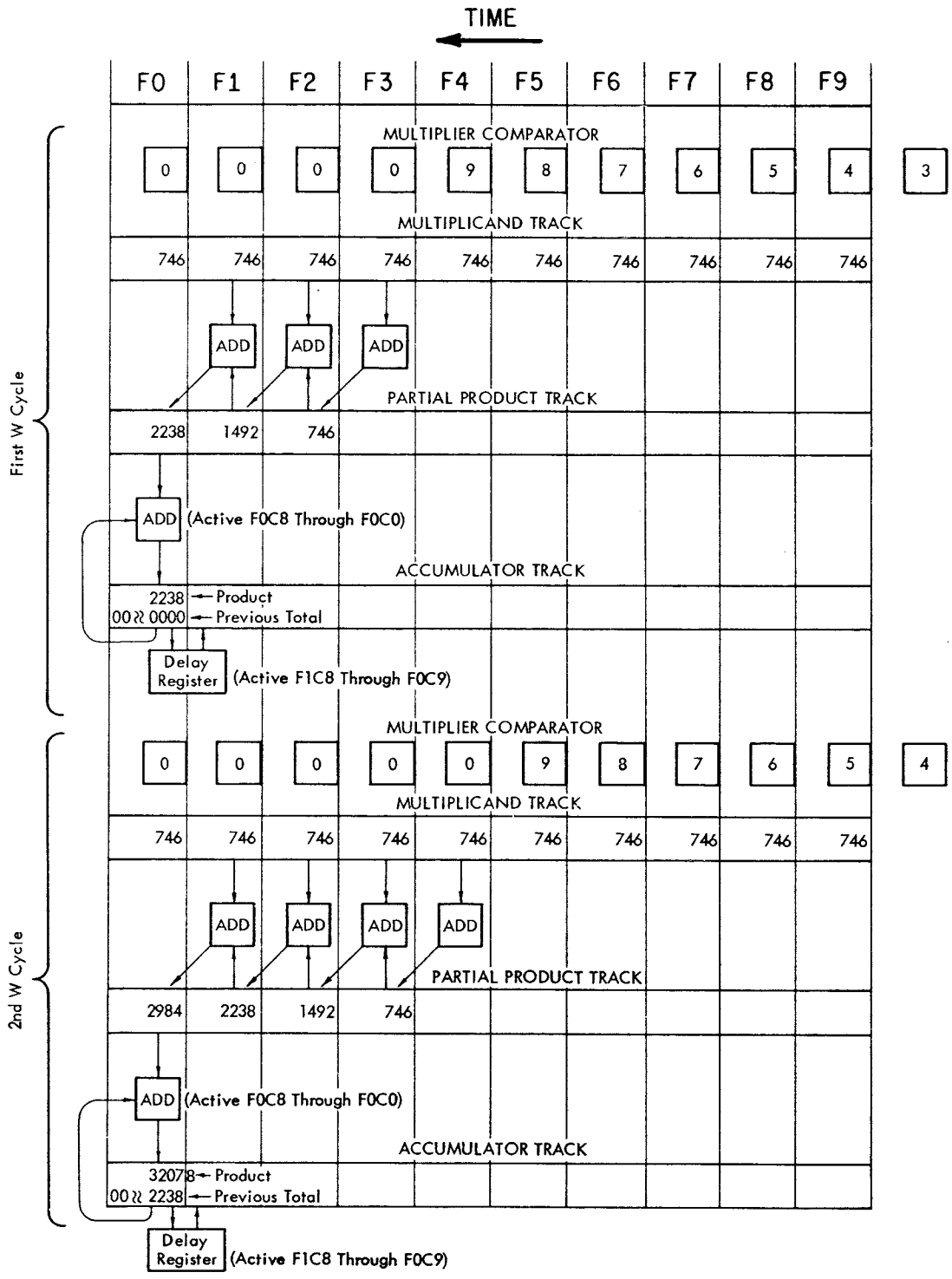


Figure 182. Multiplication During Instruction W49N9902bb

This is gated to the accumulator write data line at 6V10a on 5.06.04 when the shift gate trigger is 3 pin high. The shift gate goes high at F1C8 of a multiply W cycle when the product gate trigger is pulled 3 pin high. It remains 3 pin high until F0C8. The on time data is written one character late due to the physical position of the accumulator write head.

C8 through C0 of accumulator 0 will enter the adder to be right shifted (delayed one character) under control of accumulator to adder gate (6S10b - 5.02.03).

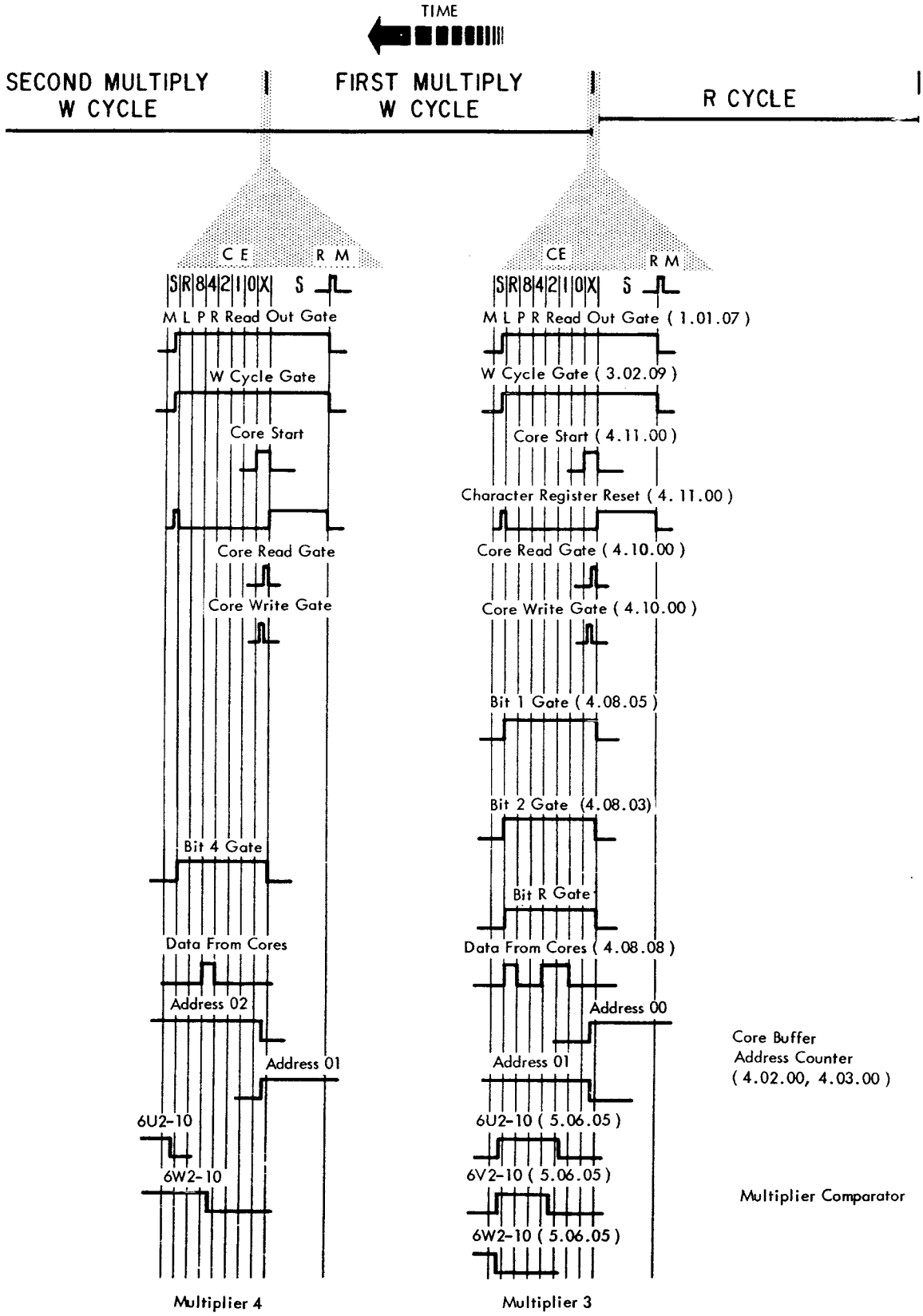


Figure 183. Storage in Multiplier Comparator

This gate is a result of the product trigger (6T8 on 5.06.04) being 3 pin high and F0.

Add PP to Accumulator 0: The accumulator read data enters input A while the partial product read data enters input B from F0C9 to CL. The PP to adder gate is up until CL (5.06.03). The accumulator to adder gate is up until F0C0.

Write In Accumulators 1 and 0: The accumulator write data on 5.06.04 consists of the accumulator delay data (6V10a) during F1 and then data from the adder beginning at F0C8 when the shift gate goes down. Data from the adder is gated at 6U11b when the partial product trigger is pulled 3 pin high to develop the F0 write gate.

Repeat W Cycle: The above steps are repeated for each multiplier digit. To accomplish this, W cycle end, on 1.03.06, is delayed by blocking cycle complete on 1.02.08. The cycle complete gate trigger at 1H9 will not be flipped 10 pin high until MN compare falls at 1K10b. MN compare is a Bs∅B pulse occurring when the MN register equals the A_2B_2 counters. These counters were set to 99 during I cycle. At R cycle end they advance to 00 (2K6a - 2.04.03) and normal B_2 counter advance is blocked by $T_2 = N$. At the end of each W cycle they advance one more unit (2K5b - 2.04.03). The MN compare will occur after MN W cycles, which is equal to the number of digits in the multiplier.

Reset Multiply

If accumulators 0 and 1 contain significant data at the start of the multiply W cycle this data will be added to the partial product. A Q of 5 in a multiply instruction will erase these two accumulators during the R cycle by raising accumulator write gate. Trigger 6V4 on 5.06.02 is flipped 10 pin high at this time and reset every CE. Since there is no accumulator write data, during R cycle, *write 0* current will be drawn through the write head.

Division (Optional Feature)

Automatic division is performed by RAMAC in much the same manner as multiplication. Multiplication is a series of repetitive additions using tracks L, V, and PP. Division is a series of repetitive subtractions also using tracks L, V, and PP.

The following is a definition of the terms used in division:

$$\text{divisor} \;\overline{)\;\text{dividend}}\;\text{quotient}$$

Programming of Division

In order to accomplish this process of division, three program steps are necessary as follows:

1. The first, containing a T_2 of L, loads the dividend into accumulators 0 and 1 according to the following rule for quotients of 11 digits or less: The number of digits in accumulator 0 must not exceed the number of digits in the smallest divisor used, providing the dividend does not exceed 11 digits. For dividends greater than 11 digits, at least 2 digits will be in accumulator 0. It may be necessary, therefore, to shift the divisor to the left on V track to obtain the correction quotient.

Note: A Q flag of 5 is usually used to clear accumulators 0 and 1 before the dividend is entered.

2. The second instruction contains a T_2 of V and is used for loading the divisor into each field of the multiplicand track. For quotients of 11 digits or less, the A_2B_2 will be 99 to load the divisor into the low order positions of each field. (For quotients greater than 11 digits, it will be necessary to position both the divisor and dividend further to the left by the number of places desired in the quotient minus 11.) The execution of this instruction causes the V track to be loaded exactly as it is during the multiplication process.
3. The third instruction must be L09P99 with an MN of twice the desired number of digits in the quotient. This instruction starts the actual division operation. The MN of this instruction determines the number of machine cycles that W cycle lasts during the development of the quotient. The machine cycles that occur during this long W cycle are divided into pairs, which occur repetitively. The first cycle of the pair is called "divide odd W cycle" and the second cycle of the pair is called "divide even W cycle."

Description of Division

During the division process, the development of the quotient involves counting the number of repetitive subtractions of the divisor from the dividend which are necessary to reduce the dividend to less than the divisor. The divisor is written in each field on track V (the multiplicand track) and the dividend is stored in accumulators 0 and 1. The quotient is developed in a single position quotient counter and transferred to C9 position of accumulator 1 (F1C9) the next drum cycle after it is developed. Since the quotient counter is a single position, the quotient must be developed a digit at a time. Therefore, the divisor must be subtracted from only the high order digits of the dividend to insure that the quotient digit will be nine or less. These high order digits of the dividend, which we shall call

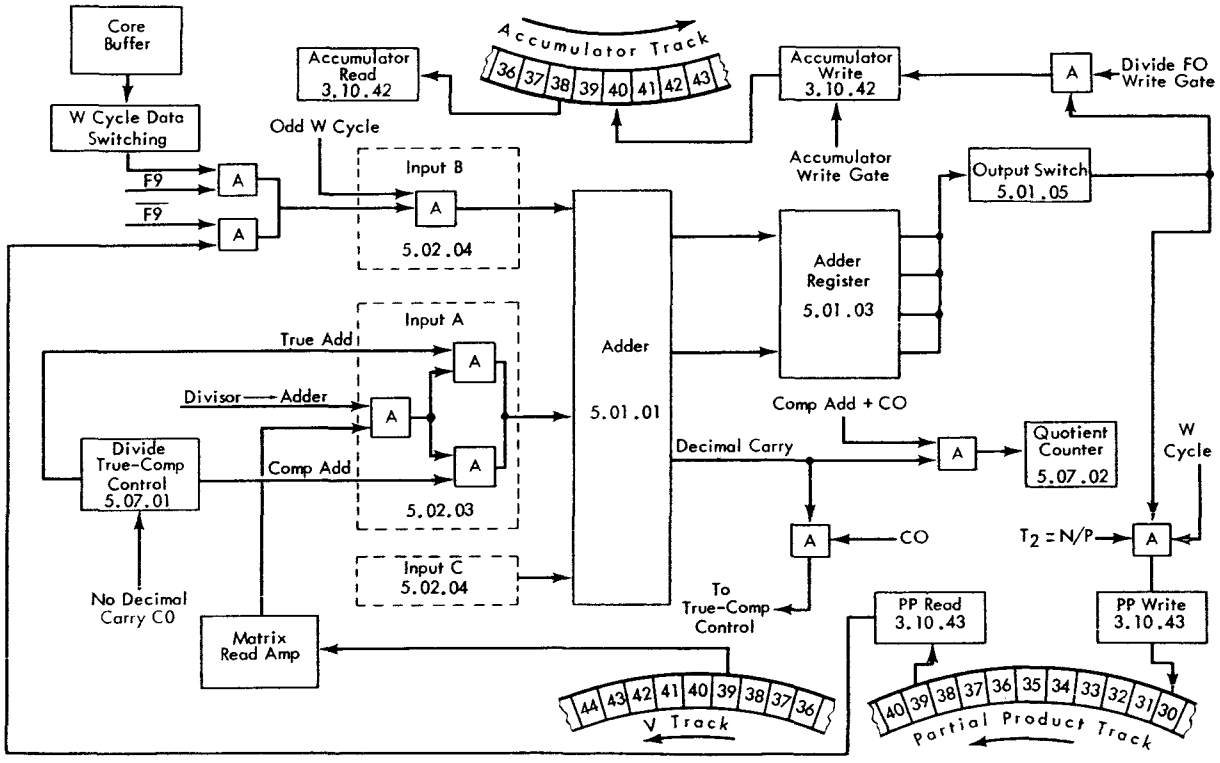


Figure 184. Divide Odd W Cycle — Data Flow and Controls

the "active dividend," are placed in accumulator 0, and the rest of the dividend, which we shall call the "inactive dividend," is placed in accumulator 1. The two data flow charts, Figures 184 and 185 show this operation.

MAJOR OBJECTIVES:

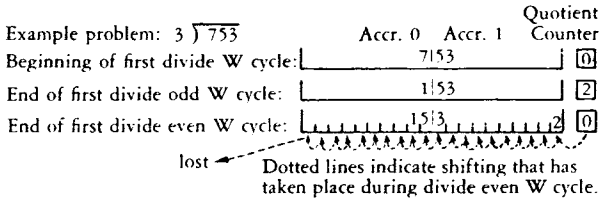
1. Analyze sign of accumulator 0 and 1.
2. Repetitively subtract divisor (V track) from active dividend (in cores during F9, then on PP track.)
3. Count successful subtractions to develop quotient digit.
4. Detect overdraw and true add divisor to remainder.
5. Enter quotient in C9 of accumulator 1.
6. Left shift accumulator 0 and accumulator 1.
7. Enter shifted accumulator 0 into core buffer.

During R cycle the dividend in accumulator 0 will be loaded into cores as the instruction demands. On the divide odd W cycle the divisor will be complement added to the dividend from core buffer during field 9. The result is written on the partial product track. During field 8 and later fields the divisor is complement added to the amount on the partial product track.

During these subtractions a decimal carry at each character 0 tells the machine that a successful reduction has been made. It adds one to the quotient counter and keeps complement add up. No decimal carry indicates the remainder has gone from plus to minus and initiates a true add of the divisor to the partial product. The remainder on the partial product track continues to pass through the adder and back to the partial product track on each field. The divisor is blocked from input A following the true add field. At F0 time the remainder is written in accumulator 0 as it leaves the adder.

At the beginning of the divide even W cycle the quotient digit is in the quotient counter and the remainder in accumulator 0 and 1. At F2C0 the quotient is passed through the adder and written at F1C9 of the accumulator track. All of accumulators 1 and 0 are left shifted one character. This is accomplished by delaying the early accumulator read data 3 character times. It is passed through the delay register, the adder and the divide left shift register, each stage providing one character delay. For example, C9 is read at C0 time, delayed three character times until C7 time and written in C8 of the accumulator track. At the same time the new active dividend is taken from the adder output to core buffer from F0C9 through F0C0. The odd and even W cycles are continued for the number of times specified by the MN of the instruction. At the end of the division process, the quotient will be in accumulator 1 beginning with the units position (C19), and any

remainder will be in accumulator 0 (and perhaps the high order positions of accumulator 1, depending on the size of the remainder).



The divisor and dividend are treated as plus factors resulting in a positive quotient. There is a possibility that the dividend in accumulator 0 or 1 may be in complement form, since it was loaded on a previous instruction. In this case it must be returned to true form before it is used in the divide operation. This situation will be covered later under "Divide Sign Control."

Divide Circuits

This discussion will treat only the divide instruction. It would have been preceded by two other instructions loading the dividend in accumulators 0 and 1, and the divisor on V track. The two data flow charts in Figures 184 and 185 and the diagram of the divide gates in Figure 186 will aid in tracing the circuits. Assume an instruction of L09P9906 for the problem 753 ÷ 3.

OBJECTIVES:

1. Transfer dividend in accumulator 0 to core buffer on R cycle.
2. On odd W cycle repetitively subtract to develop one digit of the quotient.
   a. Divisor to adder gate at F9 to enter core buffer contents into adder.
   b. Partial product read data to adder on all fields after F9.
   c. Complement add divisor from V track to adder.
   d. Write results on partial product track.
   e. Add "one" to quotient counter when decimal carry at C0 occurs.
   f. True add V track to correct overdraw when no decimal carry occurs at C0.
   g. Write remainder in accumulator 0.
3. On even W cycle left shift accumulator 1 and 0. Enter quotient digit in F1C9.
   a. Gate quotient counter to adder at F2C0.
   b. Delay accumulator read data 3 characters for left shift.
   c. Transfer remainder in accumulator 0 to core buffer.
4. Continue W cycle until MN compare.

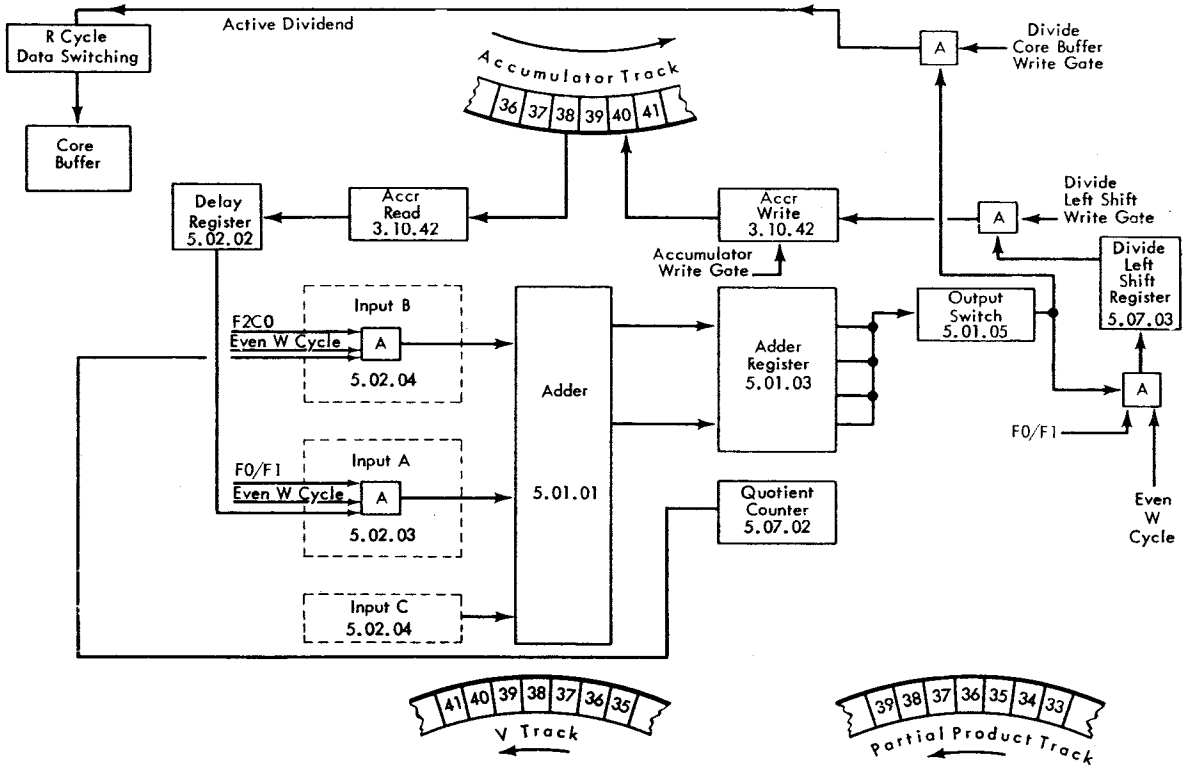


Figure 185. Divide Even W Cycle — Data Flow and Controls

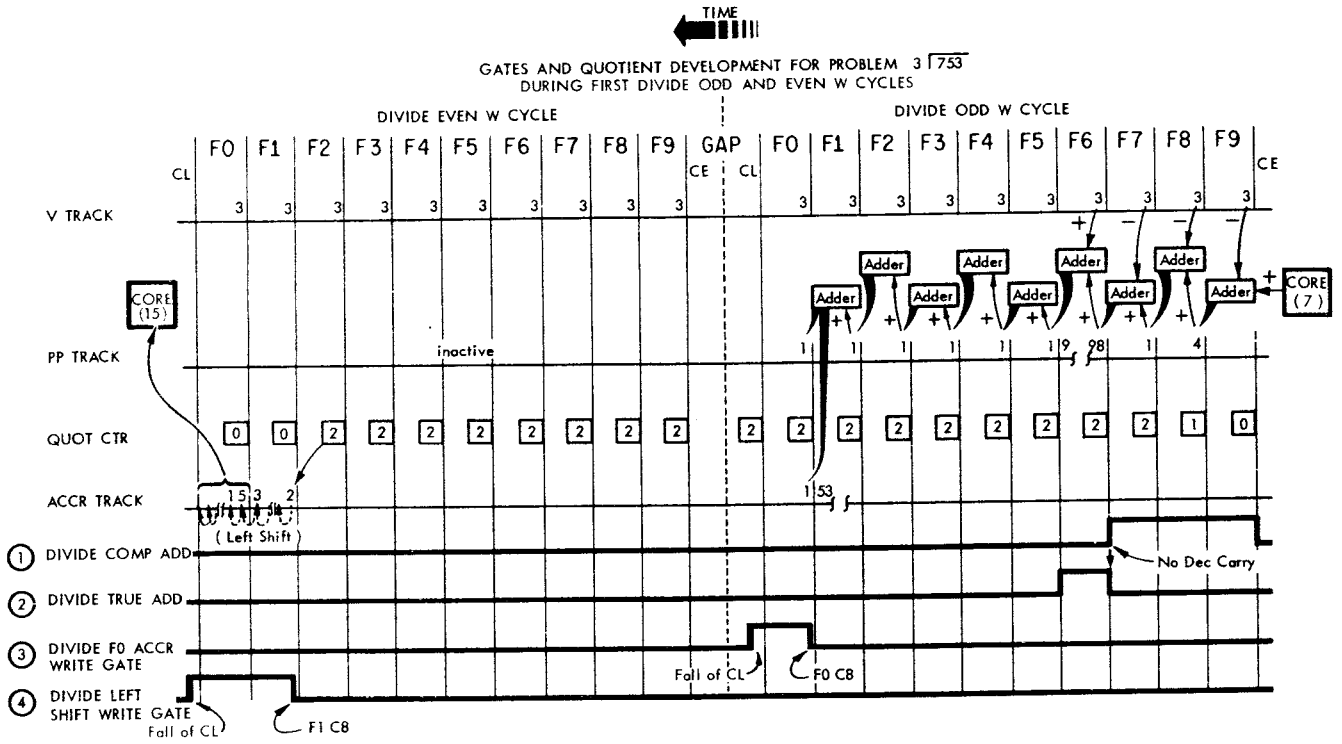


Figure 186. Division Gates

Dividend to Cores on R Cycle: The transfer of data from the accumulator track to cores is accomplished in the same manner as an accumulator read out, with one exception. The R/W cycle gate (3.02.03), raised by AB compare, is not lowered until CL. MN compare is blocked by the conduction of 2Z4a (2.04.14) on a divide operation. This must be done since the MN characters of the instruction now specify the number of W cycles to be taken.

Divide Odd W Cycle: The sequence of events during the long divide W cycle is controlled by the trigger 4U9 on 5.07.04. This trigger is reset 3 pin high with "C" reset. Each W cycle start pulse flips the trigger when $T_2 = P$. 10 pin high raises divide odd W cycle. An even number of W cycle start pulses will leave it at divide even W cycle, or 3 pin high.

Dividend from Cores to Adder: The data to adder input B during the odd W cycle (6N8 - 5.02.04) is labelled dividend to adder data. It comes from two sources on 5.07.01. During F9 it is W data from core positions 00 to 09. For all other fields it is partial product read data. All that is necessary to place core data on the W data line is to raise the W cycle gate during F9 (3.02.12). This is provided at 3E6a on 3.02.09.

Partial Product Track to Adder: Following F9 all fields of the partial product track will be gated to the adder on the dividend to adder line (5.07.01).

Complement Add V Track to Adder: V track is selected in the read matrix by TN = 5 and TZ = 0. The latter is forced at 5S6a on 3.10.14. The matrix read data enters adder input A (5.02.03) under control of the quotient digit not 9 gate and the divisor adder gate. The divisor adder gate (5.07.01) will remain up until the overdraw is corrected. It is a result of either divide complement add or divide true add being high. The divide complement add trigger is set 10 pin high at F9 of each odd W cycle, and will remain there until an overdraw (no decimal carry).

If a quotient digit greater than 9 is attempted due to incorrect placement of the dividend in accumulator 0, trigger 4V6 will be flipped 3 pin low, blocking adder input A. This condition is signaled by a decimal carry at F1C0 because the dividend was not reduced to a negative number after 9 subtractions.

Once the matrix read data (track V) is at input A it will be complement added until an overdraw. The true-complement trigger (5.04.02) is set to complement each field by divide complement add and check sign, a C9B1 pulse.

Partial Product Write: All data from the adder will be written on the partial product track by $T_2 = P$ and W cycle on 3.10.43.

Develop Quotient: Each successful reduction of the divisor during the odd W cycle results in a decimal carry at C0 time. "One" is added to the quotient counter on 5.07.02 at this time. Notice that this operation is

conditioned by complement add. Following the overdraw a true add operation takes place to return the remainder to a positive condition. This results in a decimal carry also, but it is not part of the quotient.

Correct the Overdraw: If the subtraction of the divisor from the dividend results in a negative remainder, no decimal carry occurs at C0. This signals a divide true add operation to correct the remainder. On 5.07.01 the divide complement add trigger is flipped 10 pin low by no decimal carry. This in turn flips the true add trigger, 4U6, to raise the divide true add gate. This trigger is pulled 10 pin low each C0 time so the gate is never up for more than one field. The divide true add gate will flip the true-complement trigger on 5.04.02 to true add. V track will enter the adder from input A without inversion.

Remainder to Accumulator 0: Following the true add of the divisor, the correct remainder is read from the partial product track, passed through the adder with no change and rewritten on the next PP field. This continues until F0 when the output of the adder will be directed to the accumulator write circuits (see Figure 184). The divide F0 write gate trigger (4U10-5.07.04) is flipped 10 pin high at F0C8. It remains high until CL. At the same time the accumulator write gate is raised on 5.06.02 through 6W8.

Divide Even W Cycle: On 5.07.04 trigger 4U9 is flipped 3 pin high at the start of the second W cycle.

Quotient Digit to Accumulator: The contents of the quotient counter are always present on the quotient digit line. It is gated into adder entry B (6T7 - 5.02.04) at F2C0. This means it will be written one character later at F1C9 on the accumulator track.

Left Shift Accumulators 0 and 1: The entire remainder in accumulators 0 and 1 must be left shifted one character in preparation for the next reduction operation. When adding and subtracting a delay of two character times between the accumulator read head and accumulator write head resulted in writing the data in the same position from which it was read. This is due to the physical location of the two heads. A delay of three characters will write the data in the character position immediately following the one from which it was read. The additional delay in the divide left shift register results in a left shift.

The accumulator delay data is entered into adder input A, on time, at 6N7 on 5.02.03. It leaves the adder one character late and is entered into the left shift circuits on 5.07.03. This circuit operates very similar to the delay register. The ⌀C bits from 4X6a flip the respective shift triggers 3 pin high while the ⌀C no bits from 4W7a flip them 3 pin low. The 3 pins are all sampled with ⌀B's at 4X11b resulting in one character delay.

The accumulator read data appears three characters later as divide left shift data. It is gated to the accumulator write data line by the left shift write gate from trigger 4U11 on 5.07.04. At the same time the accumulator write gate is raised through 6W8 on 5.06.02.

Remainder to Core Buffer: The new "active dividend," appearing at the adder output from F0C9 through F0C0 of the divide even W cycle is sent to core buffer by the divide core buffer write gate (4V11a-3.02.06). This gate also provides a character register reset and core start pulses through 4J8b on 4.11.00.

W Cycle Control: The odd and even W cycles continue until the correct number of digits in the quotient have been developed. The completion of W cycle is signalled by an MN compare since MN in a divide instruction must be two times as great as the number of quotient digits desired. The A_2B_2 counters are advanced "one" for each machine cycle during the long W cycle at 2K5b on 2.04.03. MN compare, a Bs⌀B pulse, occurs during F0C9 to raise the cycle complete gate (1H9 - 1.02.08) on the last divide even W cycle.

Divide Sign Control

The sign of the quotient is always set to plus. Fire plus for accumulator 1 occurs at 6K8b on 5.05.01 and for accumulator 0 at 6K8a.

The dividend and divisor must be sent to the adder inputs in true form. A negative figure is always written in true form on all process drum tracks except the accumulator track. Track V, the divisor, will always be in true form. A negative dividend, however, will be written in complement form on the accumulator track prior to the divide instruction. Either accumulator 0 or accumulator 1 or both, may be in complement form. The complement accumulator must be changed to true form by passing it through adder input A with the complement add gate up, prior to its use in the divide operation. Accumulator 0 will be recomplemented, if negative, when first sent to cores on the R cycle of the divide instruction. Accumulator 1, if negative, will be recomplemented on the first left shift cycle.

Recomplement Accumulator 0: When the accumulator delay data from accumulator 0 enters adder input A on R cycle, the true complement trigger on 5.04.02 will be set to complement add at 6N2. The sign relay for this accumulator is not set to plus until the first divide odd W cycle.

Recomplement Accumulator 1: On the first left shift operation at F1 of the even W cycle the sign of accumulator 1 is still negative. The true complement trigger is set to complement at 6P7 on 5.04.02. Then, at F0C8 of the divide even W cycle the sign relay for accumulator 1 is set to plus at 6K8b on 5.05.01.

380 Supervisory Operations

The 380 Console includes a card reader, typewriter, keyboard, indicator panel, control keys and control panel. The various operations of the RAMAC are controlled from this station. The operation of the card reader and the control exercised over other RAMAC units from the supervisory console during the processing of data are covered in other sections of this manual. This section deals with the special operations performed by the supervisory station which supplement the actual processing of data.

The special supervisory operations include the correction of invalid characters which are indicated by a parity error, alteration of data on a process drum track, typing a record from the file, and operation of the typewriter as an auxiliary document printer. All of these operations involve the transfer of data to and from the typewriter track (Q track) and the analysis of individual characters from Q track in order to energize the corresponding typewriter key magnet.

Supervisory Mechanical Components

The four major mechanical components that make up the 380 supervisory station are: a magnet operated electric typewriter, a console keyboard, a supervisory circuit breaker unit, and a group of spring driven rotary stepping switches.

The console typewriter provides a printed output for data that is transferred as a result of manual console operations and also serves as an auxiliary document printer under control of the program being performed by the process unit. A control panel is provided to allow flexible format control of the output data. The control panel permits rearrangement of the output data, variable line length, controlled spacing, zero suppression, and ribbon color control.

The console keyboard contains a complete set of alphabetic and numeric keys that are used to enter information on the process drum and correct error information from the process drum or file. In addition to the alphabetic and numeric keys a group of function keys are provided to control manual console operations.

The supervisory circuit breaker unit is clutch controlled and makes one revolution for each console key depression or each character that is transferred from Q track to the typewriter.

The rotary stepping switches control the selection of individual character positions on Q track. As each character is read from Q track and typed, the rotary switches advance one position and select the next character for typing.

Keyboard

The keyboard used with the type 380 Console contains two mechanically independent units. One of these units is similar in design and functional operation to the 024 type keyboard; this unit contains all of the alpha-numeric keys. A mechanically independent 7-key unit for the functional keys has been mounted upon the rear of the alpha-numeric keyboard.

Alpha-Numeric Keyboard

The operation of an individual key is illustrated in Figures 187 and 188. The depression of a key causes the key stem bell crank to move its latch pull bar forward, causing the latch assembly to drop off the latch bar.

Individual key stem springs restore the keys and pull bars to normal. A separate flat spring holds each pull bar against its latch assembly and insures its relatching in the notch of the latch.

In Figure 188, notice that the latch assembly is made up of three parts, which are free to rotate about a pivot point. Each part has its own function. The permutation bar supports the operating spring and causes the contact bails to pivot and close the bail contacts. The latch hooks over the latch bar and holds the latch assembly and its permutation bar inoperative until its key is depressed. The check lever slides over the notch in the latch to block a second operation before the latch assembly is fully restored.

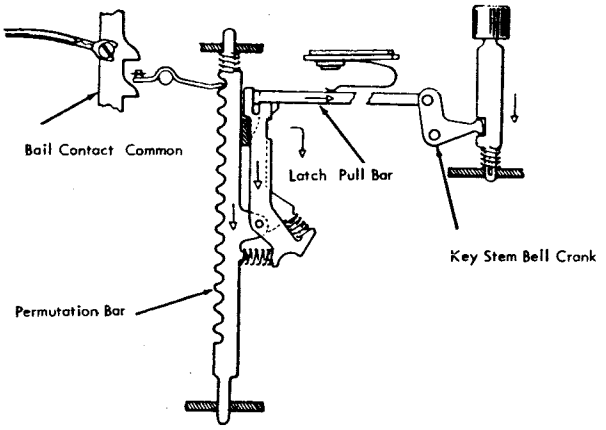


Figure 187. Keyboard Operation – Latch Normal

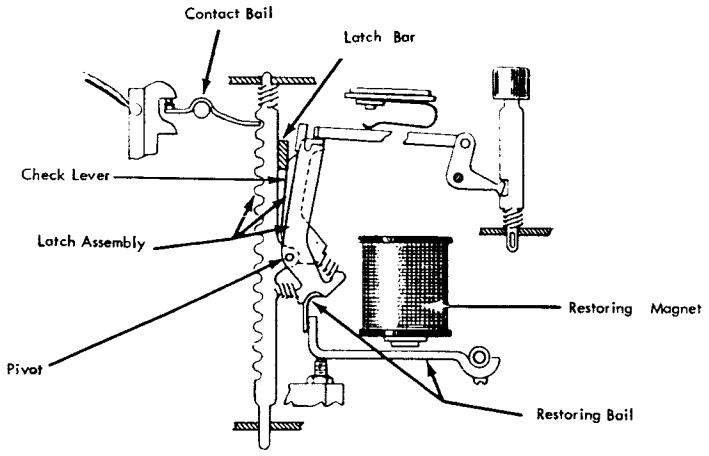


Figure 188. Keyboard Operation – Latch Tripped

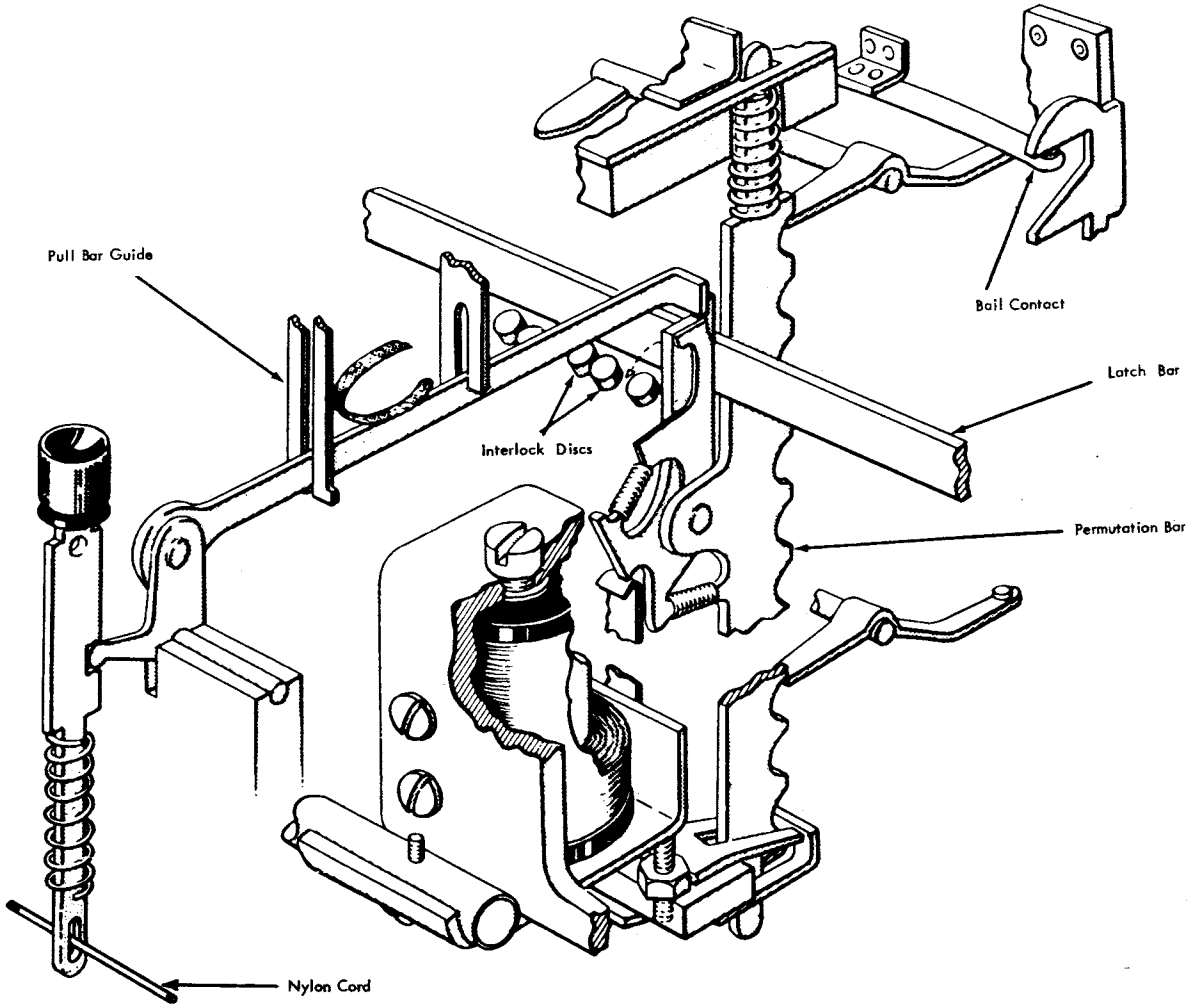


Figure 189. Keyboard Mechanics

In Figure 189, several keyboard mechanical features are shown. Disk interlocks, which are operated by the latches, prevent tripping more than one latch assembly at a time. The pull bar guide has L shaped separators which hook under the pull bars, to aid in disassembly of the keyboard. As each key stem is returned to its normal position, it comes to a stop against a nylon cord threaded through the slot in each key stem.

Notice the position of the restoring bail in Figure 188. The bail is operated by two restoring magnets, one at each end of the bail. When the restoring magnets are energized, the permutation bar and latch assembly are lifted to permit the latches to relatch on the latch bar.

Function Key Unit

The function key unit is illustrated in Figure 190. There are seven key positions identical to the one position shown.

When the key is depressed, the contact lever is moved downward until it is free of the latch bar. The upper spring pulls the contact lever to the right to close the contact. The contact lever remains in its operated position and the contact remains closed until the restoring magnets are energized. When the restoring magnets are energized, the armature pivots to move the contact lever clear of the latch bar. The contact lever return spring then moves the contact lever upward to its original position

Supervisory Clutch

The supervisory CB unit is controlled by a clutch similar to the type 24 punch clutch. Power is supplied to the unit from a continuously running V belt from the card feed drive mechanism. The drive pulley is formed with a sleeve which fits around the drive shaft and inside the clutch spring (Figure 191). With the

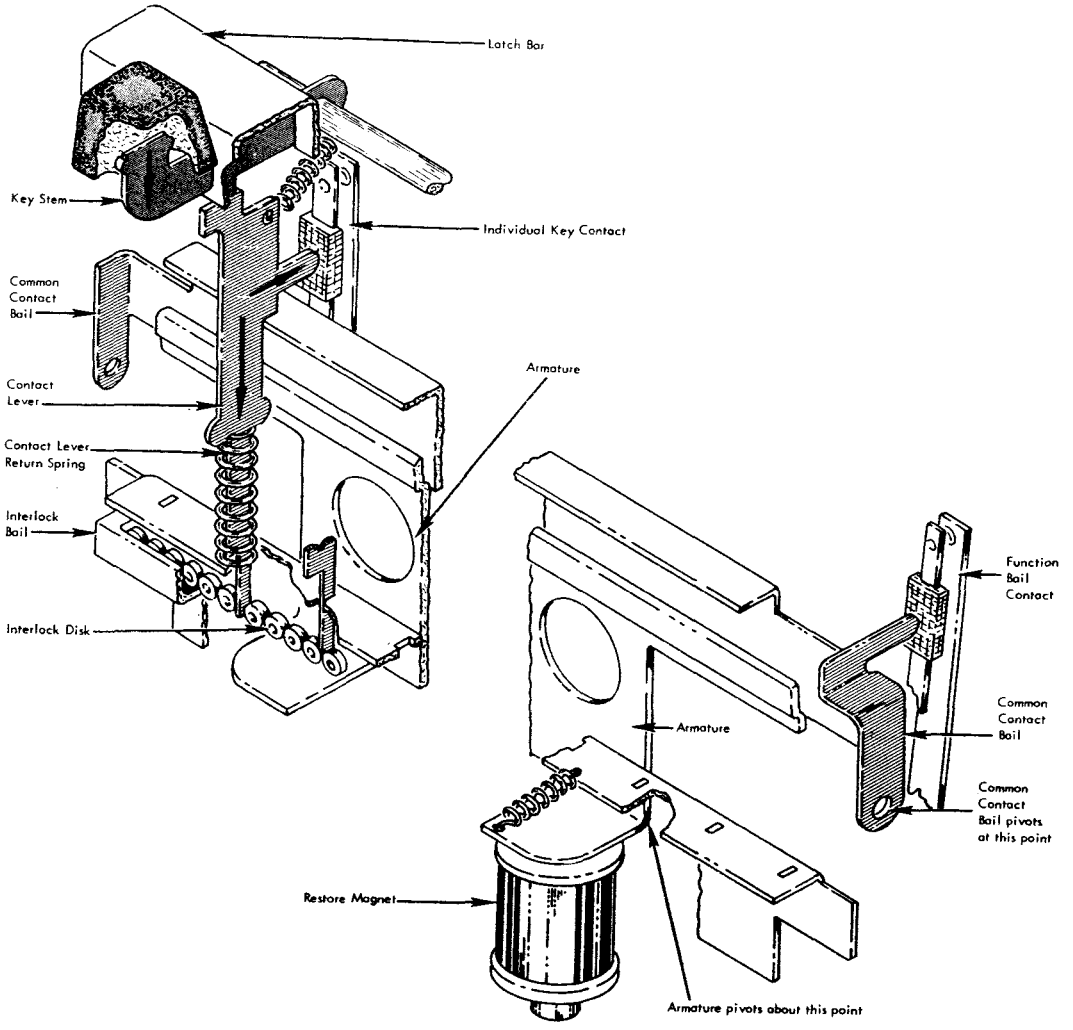


Figure 190. Function Key Unit

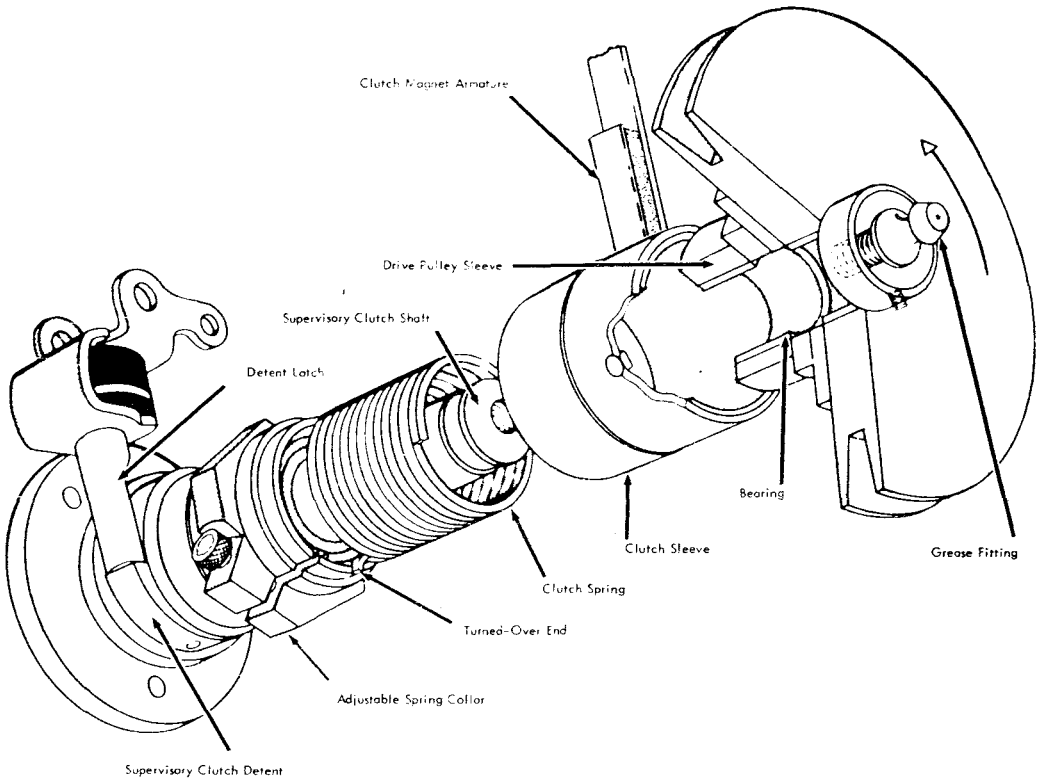


Figure 191. Supervisory Clutch Assembly

clutch sleeve latched on the clutch magnet armature, and with the detent latched, the clutch spring is uncoiled (expanded) tightly within the clutch sleeve. The position of rest for the clutch spring, circuit breaker shaft, and index is determined by positioning the clutch spring collar, which anchors the spring to the shaft.

When the clutch is unlatched, the tension of the clutch spring causes it to coil about the drive pulley sleeve, locking the pulley to the circuit breaker shaft.

As the drive shaft completes a revolution and approaches latch up position, a step on the clutch sleeve strikes the tip of the rubber-mounted clutch magnet armature. A step on the inner wall of the clutch sleeve engages the tip of the clutch spring. Momentum of the driven mechanism causes the clutch spring to unwind until a point is reached at which the clutch detent latch engages the detent. The spring being unwound frees the drive pulley from the circuit-breaker shaft. The index pointer should indicate 0° when the clutch is latched. One cycle of the supervisory CB shaft requires 100 milliseconds.

Rotary Switches

The 380 makes use of two types of spring driven rotary stepping switches. One has 11 operating contact positions, and the other has 20.

Eleven Position Rotary Switch

A drawing of an eleven position rotary switch is shown in Figure 192. The mechanism has 8 wafers of 12 contacts each. The wafers are numbered 1-8, front to rear. The uppermost contact on each wafer is the common position for the wiper. The contact immediately below the wiper common on each wafer is contact #1. These contacts are numbered consecutively in a downward and counter-clockwise direction so that the last contact is 11.

There is a wiper with three wiper arms for each wafer. The wipers make continuously against their respective wiper commons. With the rotary switch in any detented position, one of the three wiper arms will be making against one of the contacts 1 through 11 on each wafer. Contact 11 is the home position. If the rotary switch is advanced one step from home, the eight wiper arms making on contact 11 will be advanced to a position clear of all contacts; however, the next set of eight wiper arms will be advanced to contact 1. Successive pulses to the drive magnet would cause this set of wiper arms to step from contact 1 to contacts 2, 3, 4, etc.

The rotary switch is advanced one step by each de-energization of the drive magnet. When the drive magnet is energized, the drive spring is compressed and the drive pawl is moved to the right, where it engages

the next tooth of the ratchet. When the drive magnet is de-energized the drive spring advances the ratchet one tooth position. The detent holds the ratchet and wipers stationary when not being advanced by the drive pawl.

A cam with three lobes spaced 120° apart is mounted on the front end of the ratchet shaft. The lobes of this cam are used to operate a cam contact to give an electrical indication that the rotary switch is, or is not, at its home position. The reset cam contact is open at the home position and is closed at all other positions.

There are times when the rotary switch must search for a particular position. In order to permit searching to take place as rapidly as possible consistent with reliable operation, a set of interrupt contacts is included. This set consists of one normally closed and one normally open contact, both of which transfer when the drive magnet is energized.

Twenty Position Rotary Switch

The twenty position rotary switch is similar in construction and identical in operation to the eleven position rotary switch. There are twenty contacts, not including the wiper common, numbered 1 through 20 in the counter-clockwise direction.

Contact 20 is the home position. There are two wiper arms on each wiper and two lobes on the reset cam.

Rotary Switch Terminology Used In Systems Diagrams

Two eleven position rotary switches are used as the program counter for supervisory program control. One of these rotary switches maintains the program level and the other maintains the program step. PCLRS 4 designates the program control level rotary switch, wafer 4. PCLRS 4-2 designates the program control level rotary switch, wafer 4, contact 2. PCSRS is the designation for the program control step rotary switch.

One eleven position and one twenty position rotary switch are used as the character position, or column control counter when writing on, or typing from, the Q track. The tens counter is an eleven position rotary switch and is designated CCTRS. The units counter is a twenty position rotary switch and is designated CCURS.

Typewriter

The typewriter used in the supervisory station is similar to the model B cardatype typewriter. The motive power to operate the machine is supplied by a continuously rotating power roll, which is driven through cog belts by a 1/40th HP, 230 V, AC motor. The rubber composition power roll drives nylon cams to cause character printing, or metal cams to initiate such functional operations as spacing, carriage return, or tabulation. The cams are released magnetically. However, for

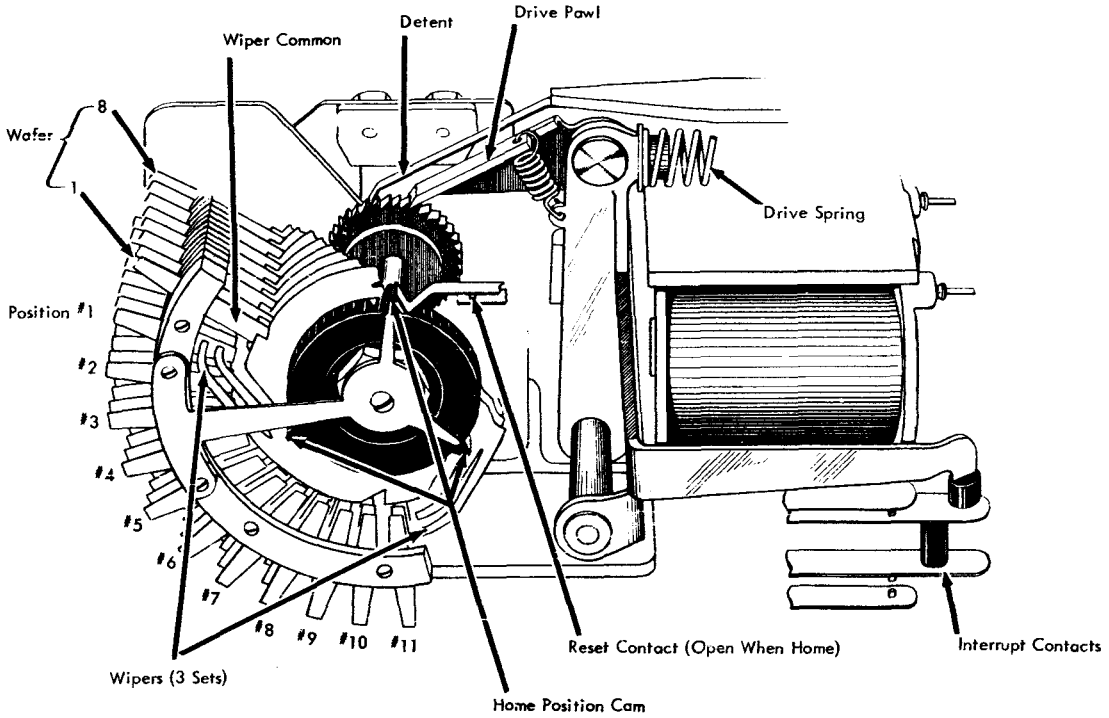


Figure 192. Spring Driven Rotary Step Switch

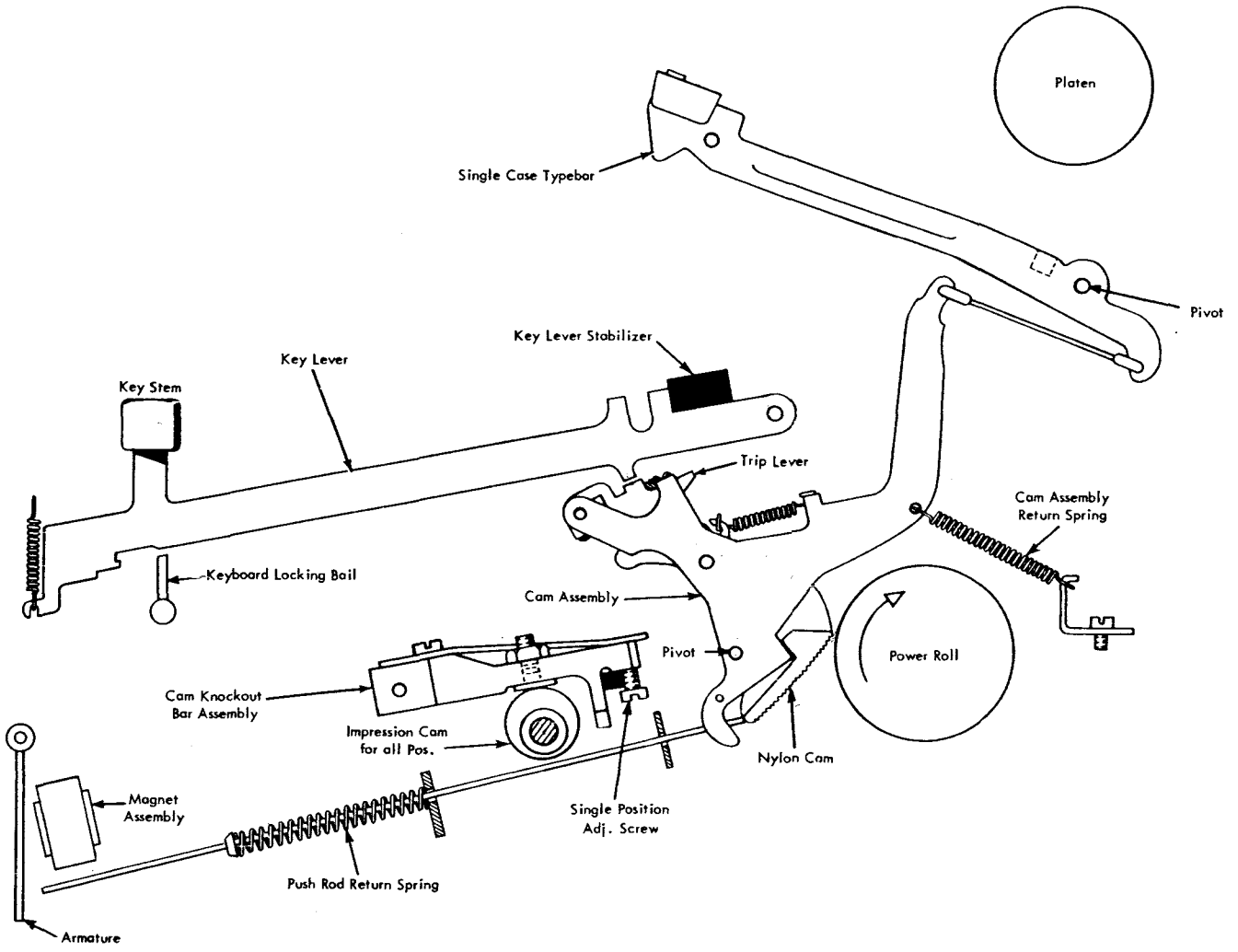


Figure 193. Typewriter Cam and Typebar — Rest Position

analysis or maintenance, manual depression of the keys may be made effective by pulling the keyboard locking bail toward the front of the machine.

Character Printing

Figures 193 and 194 illustrate the mechanical operation of typing a character. Energizing a character magnet attracts the armature, which forces a push rod against the lower part of a nylon cam. This causes the nylon cam to rotate against the periphery of the rubber power roll. As the cam follows the roll, it rotates the cam lever about its pivot, pulling the typebar forward at an accelerated rate. Momentum forces the upper half of the typebar toward the platen with a whipping action, until the center of the typebar strikes the ring or anvil. The resultant flexing of the typebar causes a short, clean impact of the type slug against the ribbon, which leaves an image of the type slug face on the paper. During the printing operation, the momentum of the cam lever pulls the cam away from the power roll as the tail of the cam strikes the knockout finger. The cam return spring pulls the cam back to its restored position, followed by the cam lever return spring pulling the cam lever back to its restored position.

Spacing

As a character is printed, the lower portion of the typebar pushes forward on a universal bar, or U-bar. The U-bar is a semicircular bail, located below the ring, and behind the typebar guide comb. It is common to all type bars. Forward travel of the U-bar is transmitted through linkage to lift the single escape pawl out of the rack for a one position escapement. Motion of the escape pawl can also be initiated by impulsing the space magnet, or by depressing the space bar manually, either of which releases a metal space cam. As this cam rotates, it operates linkage which lifts the escape pawl from the rack; thereby causing a space without printing.

Carriage Return

A supervisory station clear operation, or a manual depression of the carriage return key, causes the single lobe carriage return cam to be unlatched. This causes the carriage return friction clutch to be latched in its operated position. The clutch, located at the right end of the power roll, winds a carriage return tape onto a drum. As the tape is wound, it pulls the carriage to the right until the left hand margin control unlatches the clutch, allowing the carriage return mechanism to be restored. While the clutch is held engaged the escape pawl is held out of the rack, and an interlock contact is held in its transferred position. The interlock contact is located on the right side of the frame, toward the rear, near the off-on switch.

Tabulation

When the tabulation magnet is energized, it releases a single lobe metal cam. As this cam follows the power roll, motion is imparted to place the tab lever mechanism in its latched position, and at the same time the escape pawl is raised from the rack. The main spring pulls the carriage to the left, under control of a friction governor, until the tab lever is unlatched by striking a preset tab stop or the right-hand margin stop. Either of these will cause the tabulating mechanism to be restored and will permit the pawl to hold the rack. While the tabulating mechanism is in its latched condition, a tab interlock contact is held transferred. This contact is mounted in the left rear, above the motor.

Ribbon Feed

Each typebar, when operated, causes a common bail to move toward the operator. This movement is linked to cause both ribbon lift and ribbon feed. A ratchet drive rotates either the left or right hand ribbon spool to cause spacing of the ribbon. When a spool approaches the empty condition, increased ribbon tension initiates reversal of spool feeding and the ribbon moves in the opposite direction.

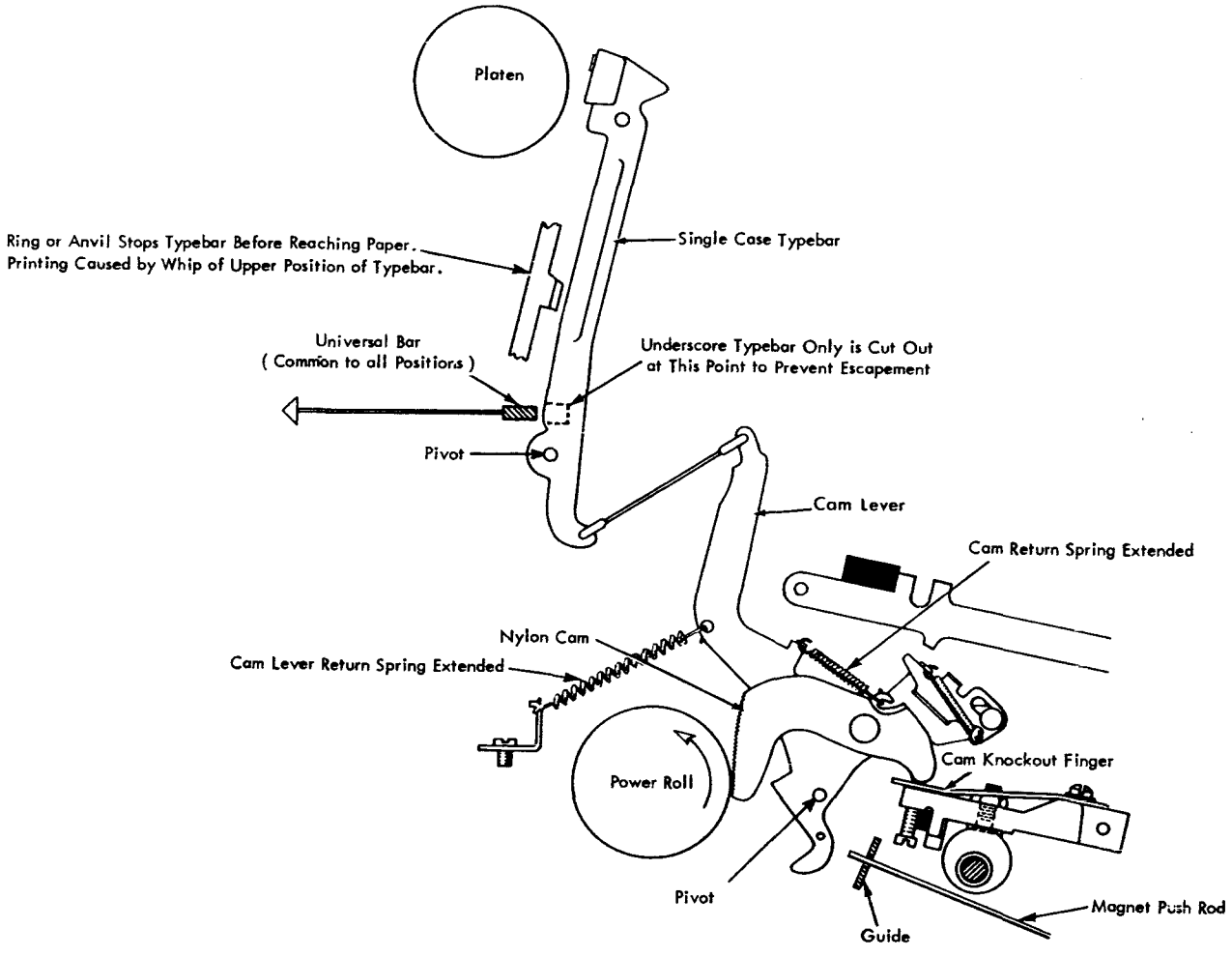


Figure 194. Typewriter Cam Knocking Out

UNDERSCORE

In RAMAC application, use of the underscore is restricted to error identification. The typewriter does not space when the underscore is printed; this permits the identification of an error character without backspacing. To prevent spacing when the underscore is typed, the underscore typebar is relieved at the point where it would contact the U-bar.

Supervisory Circuits

Typing a Character from the Console Keyboard

Typing a character from the console keyboard involves the selection of the typewriter key magnet that corresponds to the character to be typed. As an alphabetic or numeric key is depressed, one or more common channel relays are picked. There are common channel relays corresponding to each of the six bits that make up the RAMAC code and a network of common channel relay points directs an impulse to the proper typewriter key magnet. The logic drawing of console keyboard typing illustrates this operation (Figure 195). The timing of the SCB contacts is shown on System Diagram 0.89.21.

OBJECTIVES: Type a "5"

1. Energize the SCB clutch (6.01.05).
2. Pick the common channel relays (6.03.01).
3. Energize the 5 key magnet (6.14.05).
4. Restore the console keyboard (6.02.04).

SCB Clutch: The chart on 6.02.01 illustrates the keyboard bail contacts that will close as the result of any key depression. The 5 key will close the 8 and 9 contacts. The 8 bail contact serves as a common bail contact and is closed by every alphabetic and numeric key. The SCB clutch is energized by the 8 bail contact (6.02.04) and SCB-5 which is closed when the clutch is latched.

Common Channel Relays: The 1 and 4 common channel relays (R8081 and R8092) are energized by SCB 1 and the 9 keyboard bail contact through D1131 and D1138 (6.02.02).

Key Magnet: The 5 key magnet is energized by SCB 5 through a network of common channel relay points (6.14.03). The console switching relay point in series with the key magnet on 6.14.05 is used in conjunction with the 381 Remote Printing Station optional feature. It will be up for all normal console operation.

Keyboard Restoring Magnets: The keyboard restoring magnets (6.02.04) are energized by SCB 3 or SCB 9 through the points of R8042, late in the cycle after the common channel relays have been picked.

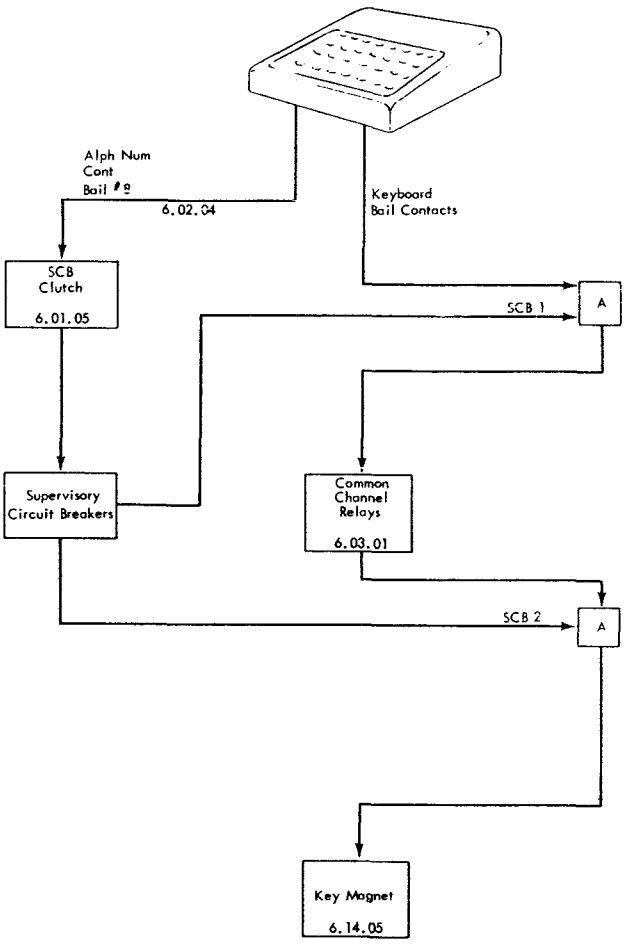


Figure 195. Console Keyboard Typing

Typing Data From Q Track

Most supervisory operations involve transferring data from Q track to the typewriter key magnets. The circuits for energizing the typewriter key magnets are very similar to those previously discussed under console keyboard typing. The key magnets are energized by the common channel relays, and a supervisory clutch cycle is required for each character that is to be typed. The circuit for energizing the SCB clutch and the method of picking the common channel relays are the major differences between Q track typing and keyboard typing. Controlling relays complete a circuit to the SCB clutch and the common channel relays are picked by analyzing one character of data from Q track for each SCB clutch cycle.

The actual selection of a character of data from Q track is performed by CCTRS #5 and CCURS #8 (Figure 196). If the CCTRS is in the 0 position, its output is anded with F0 to produce a controlling gate that is up only during F0. If the CCURS is in the 0 position, its output is anded with C0 to produce a gate that is high at C0 of each field. The two outputs are com-

bined to produce a gate that is high only at C00. The Q read/write gate at C00 is used to control the transfer of the first character of data from Q track. Each bit in the selected character of data fires a thyratron which picks a Q track data bit relay. The transferred points of the bit relays pick the corresponding common channel relays and the proper typewriter key magnet is selected by a network of common channel relay points. Late in the SCB clutch cycle the CCURS advances from the 0 position to the 1 position. On the following clutch cycle the Q read/write gate is high at C01 and the second character of data is selected and typed in a similar manner.

OBJECTIVES:

1. Energize the SCB clutch (6.01.05).
2. Select one character of data from Q track (6.08.02).
3. Pick Q track data bit relays (6.09.11).
4. Pick the common channel relays (6.03.01).
5. Energize a typewriter key magnet (6.14.05).
6. Advance the column control rotary switches (6.06.10).

SCB Clutch: The typing of data from Q track is normally the result of a programmed type operation, an inquiry, or a console read/alter/write operation. The circuit to the SCB clutch (6.01.05) is completed by the transferred points of the controlling relay for one of these operations. The circuit to the clutch is available until the line of typing is complete.

Selecting One Character of Data: The selected character of data appears on 6.08.02 labeled store data in bit relays. The desired character of Q track data is selected by combining Q read data with the Q read/write gate at 3C5. The Q read/write gate is developed at 3E5a and is high for one character time during each SCB cycle. The input to 3E5-6 is a gate that is high for one character time during each drum revolution. The input to 3E5-5 insures that the Q read/write gate will be developed only once for each SCB cycle. Early in

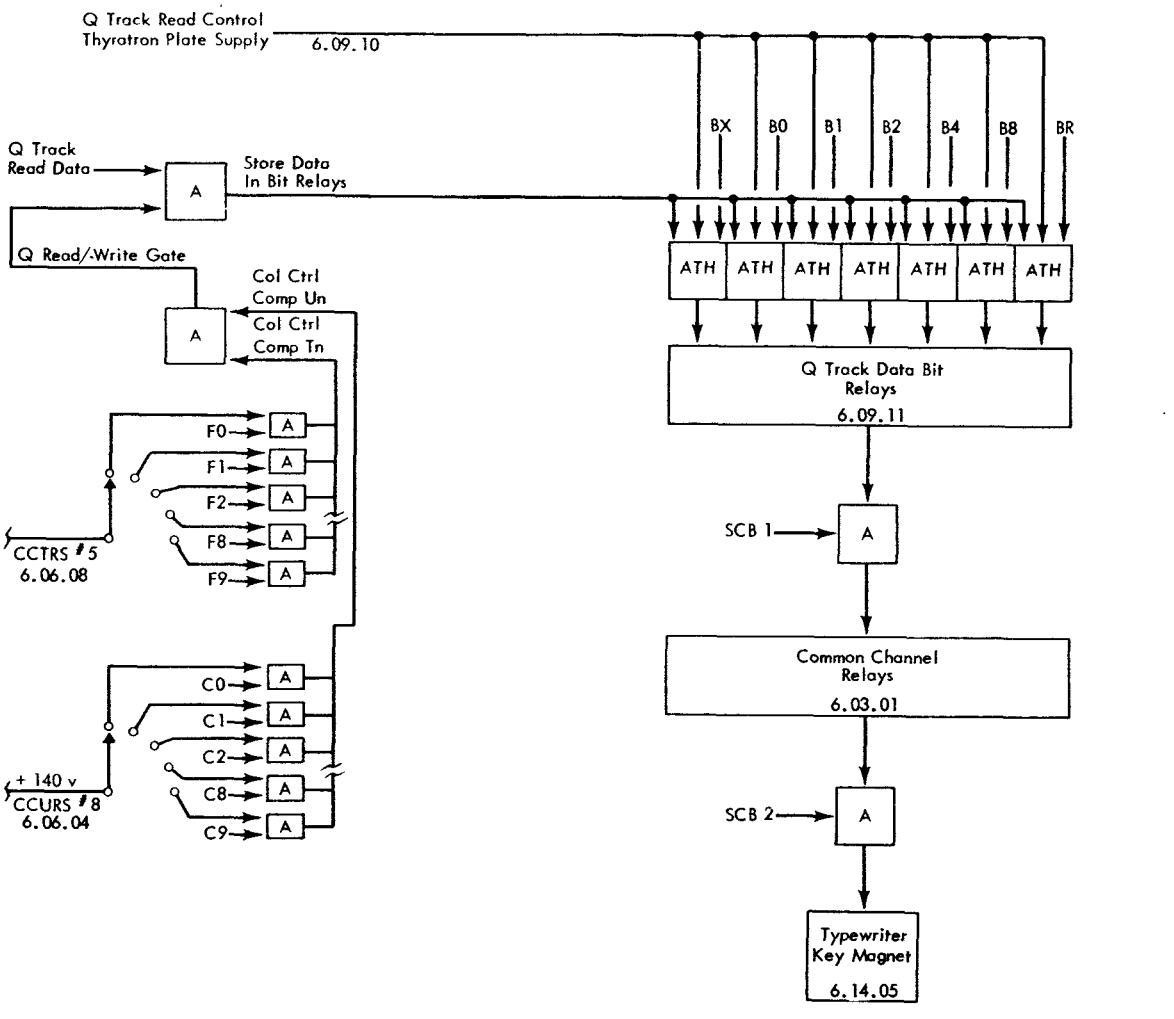


Figure 196. Selecting a Character of Q Track Data

the cycle, SCB-15 (Q track read) is applied to 3D1-5 and the leading edge of the SCB 15 impulse, inverted by 3D3a, flips the Q read/write gate control trigger at 3E4. The output of 3E4 allows the next RM to turn on the Q read/write gate trigger at 3D4. When 3E5-6 goes high for one character time the Q read/write gate is available to select one character of data from Q track. The Q read/write gate turns off the controlling triggers at BR to prevent the development of a second Q read/write gate during the same SCB cycle.

The specific character timing of the Q read/write gate is determined by the position of CCURS #8 (6.06.04) and CCTRS #5 (6.06.08). For example, with both rotary switches in the 0 position, plus 140 volts is applied to 1Q1-6 (6.08.06) to develop a F0 gate on the column control comparator tens output line. Contact 20 on CCURS #8 applies plus 140 volts to 1N1-6 (6.08.05) to develop a C0 gate on the column control comparator units output line. The outputs of the two comparators are combined at 1L3 (6.08.02) to produce a gate at C00. Before the next chararter is typed the units rotary switch will advance one position and the gate for the following cycle will appear at C01.

Q Track Data Bit Relays: Relays corresponding to the bits present in the selected character of Q track data (6.09.11) are picked by SCB-15 and the thyratrons on 6.08.03. SCB-15 (Q track read) and the selected character of Q track data are applied to each of the seven thyratrons. The coincidence of a bit impulse from the bit ring and a data bit from the selected character will fire a thyratron and pick the corresponding bit relay.

Common Channel Relays: The common channel relays (6.03.01) are picked by SCB 1 through the transferred points of the Q track data bit relays. For example, R8085 is picked through R8164-4 N/O and R8147-8 N/O to type a 2 during an inquiry operation.

Key Magnet: The key magnet (6.14.05) corresponding to the character of data from Q track is energized by SCB 2 through a network of common channel relay points (6.14.01, .02, and .03).

Column Control Rotary Switches: Near the end of each SCB cycle the CCURS advances one position. The rotary switch drive magnet (6.06.10) is energized during each cycle by SCB 10 through R8442-2 or R8212-8. The rotary switch is advanced by the spring returned magnet armature at the end of the SCB 10 impulse as the magnet is de-energized. The CCTRS (6.06.10) is advanced every tenth cycle by the contacts of the CCURS. When the CCURS #7 (6.06.04) is positioned on contact 09 or contact 19, an SCB-10 impulse is applied to the CCTRS drive magnet and as the units rotary switch advances from 9 to 0 the tens rotary switch advances one position.

Type Operation

A type operation is the process of using the console typewriter as an auxiliary document printer under control of the 305 program. Before the type operation can be performed the data to be typed must first be assembled on Q track. A program exit impulse wired to the type hub on the 305 control panel initiates the actual type operation by picking controlling relays in the 380 (Figure 197). An impulse emitted from the type hub on the 380 control panel is used to control the typing format. If the impulse is wired to COLUMN CONTROL ON, the COLUMN CONTROL EXITS (00-99) will emit impulses sequentially as each character is typed. These impulses can be wired to control spacing, tabulation, and other typewriter format functions. The typing of Q track data takes place in the manner previously described. When the desired number of characters have been typed, a COLUMN CONTROL EXIT impulse wired to the clear hub drops out the controlling relays and returns the typewriter carriage.

OBJECTIVES:

1. Initiate a type operation.
   a. Program exit wired to the 305 type hub (1.02.03).
   b. Pick the controlling relays (TYPE NO. 1, TYPE NO. 2, TYPE NO. 3 and INQ/TYPE) (6.04.05).
2. Establish format control.
   a. Emit an impulse from the 380 type hub (6.04.05).
   b. Emit impulses sequentially from the COLUMN CONTROL EXITS (6.06.03).
3. Type data from Q track.
   a. Energize the SCB clutch (6.01.05).
   b. Select one character of data from Q track (6.08.02).
   c. Pick Q track data bit relays (6.09.11).
   d. Pick the common channel relays (6.03.01).
   e. Energize a typewriter key magnet (6.14.05).
   f. Advance the column control rotary switches (6.06.10).
4. Clear and carriage return.
   a. Drop the controlling relays (6.04.05).
   b. Energize the carriage return magnet (6.14.04).
   c. Restore the rotary switches to the 00 position (6.06.10).
5. Prevent altering Q track until the type operation is complete.
   a. Interlock the W cycle gate (3.02.08).

Initiate a Type Operation: A program exit impulse wired to the 305 type hub (1.02.03) initiates the type operation by picking TYPE NO. 1 relays (R8151 and R8152) on 6.04.05. The SCB clutch (6.01.05) is ener-

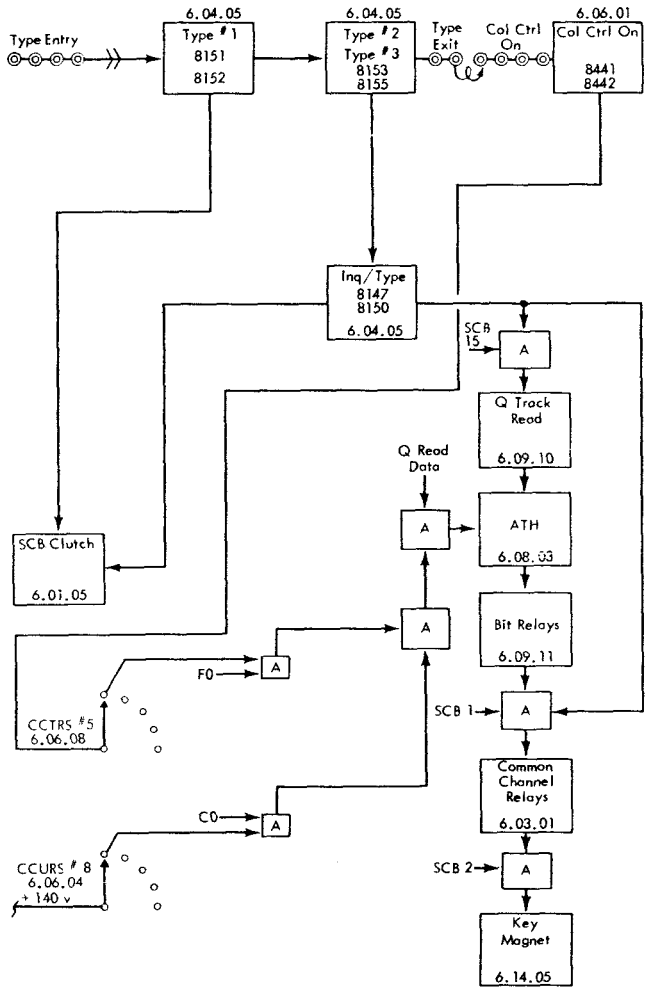


Figure 197. Programmed Type Operation

gized by a TYPE NO. 1 relay point and during the resulting clutch cycle TYPE NO. 2, TYPE NO. 3, and INQ/TYPE relays are picked by SCB-2, SCB 3, and the transferred points of a TYPE NO. 1 relay (6.04.05). TYPE NO. 1, 2, and 3 relays are used to control the initial set-up of the type operation and drop out during the first and second clutch cycles, but the INQ/TYPE relays must be up during the entire type operation. The INQ/TYPE relays are held up by overlapping SCB 2 and SCB 4 impulses until the end of the type operation.

Format Control: An SCB 1 impulse is emitted from the type hub (6.04.05) on the 380 control panel during the second SCB cycle of the type operation. The impulse is controlled by TYPE NO. 3 which is picked too late in the first cycle to make the SCB-1 impulse available. TYPE NO. 3 drops out late in the second clutch cycle to prevent emitting a second type impulse.

The type impulse wired to COLUMN CONTROL ON (6.06.01) picks COL CTRL ON #1 which picks COL CTRL ON #2 late in the same cycle. COL CTRL ON #2 remains transferred until it is latch tripped by the clear relay (CLR R8374) at the end of the type operation. COL CTRL ON #2 activates the COLUMN CONTROL EXITS on the 380 control panel (6.06.03). As each character of data is typed an SCB 1 impulse is emitted from the corresponding control panel exit. These impulses are used to control tabulation, carriage returning, and other format functions of the console typewriter.

Typing Data from Q Track: The details of selecting a character of Q track data and energizing a typewriter key magnet are discussed in a previous paragraph. For a type operation the necessary clutch cycles are provided by the transferred points of the INQ/TYPE relay (6.01.05). The selection of the characters to be typed is controlled by the COL CTRL ON # 2 relay activating CCTRS #5 (6.06.08). The pick of the common channel relays is controlled by the INQ/TYPE relay points (6.03.01).

Clear and Carriage Return: A column control exit wired to the clear hub (6.10.01) terminates the type operation by dropping out the controlling relays, returning the typewriter carriage, and restoring the rotary switches to the 00 position.

The column control exit impulse wired to the clear hub picks the clear setup relay (CLR SU R8189) (6.10.01). After the typing of the character selected for this clutch cycle is complete, the clear relays (CLR) are picked by SCB 5 and R8189-2 N/O (6.10.01). The CLR relays drop out the relays that have been controlling the type operation by latch tripping or interrupting overlapping pick and hold circuits. For example, the INQ/TYPE relay (6.04.05) drops out when the clear relays open the circuit from SCB 2 to the pick coils. The COL CTRL ON #2 relay is latch tripped by the clear relay points and SCB 9 (6.06.01).

The carriage return magnet (6.14.04) is energized by SCB 3 or SCB 9 through the points of the carriage return relay (CARR RET R8274). The CARR RET relay is picked by SCB 2 through D1196 (6.14.04) and the transferred points of the clear relay (6.11.04).

The CCURS and CCTRS are restored to the 0 positions by completing a circuit to the rotary switch drive magnets through the interrupt contacts and the search relays (COL CTRL UN SRCH) (6.06.10). The SCB 7 impulse through the interrupt contact advances the rotary switch one position at a time until the circuit is broken by dropping out the search relays. COL CTRL UN SRCH (6.06.02) is picked by CLEAR R8374-5 and the CCURS cam contact. This contact is open only when the rotary switch is resting in the 0 position. The rotary switch will continue to advance until COL CTRL UN SRCH is latch tripped. COL CTRL UN SRCH is latch tripped by SCB 7 through RS CLR (8450-2) when the rotary switch has advanced to the 0 position (CCURS #6 con-

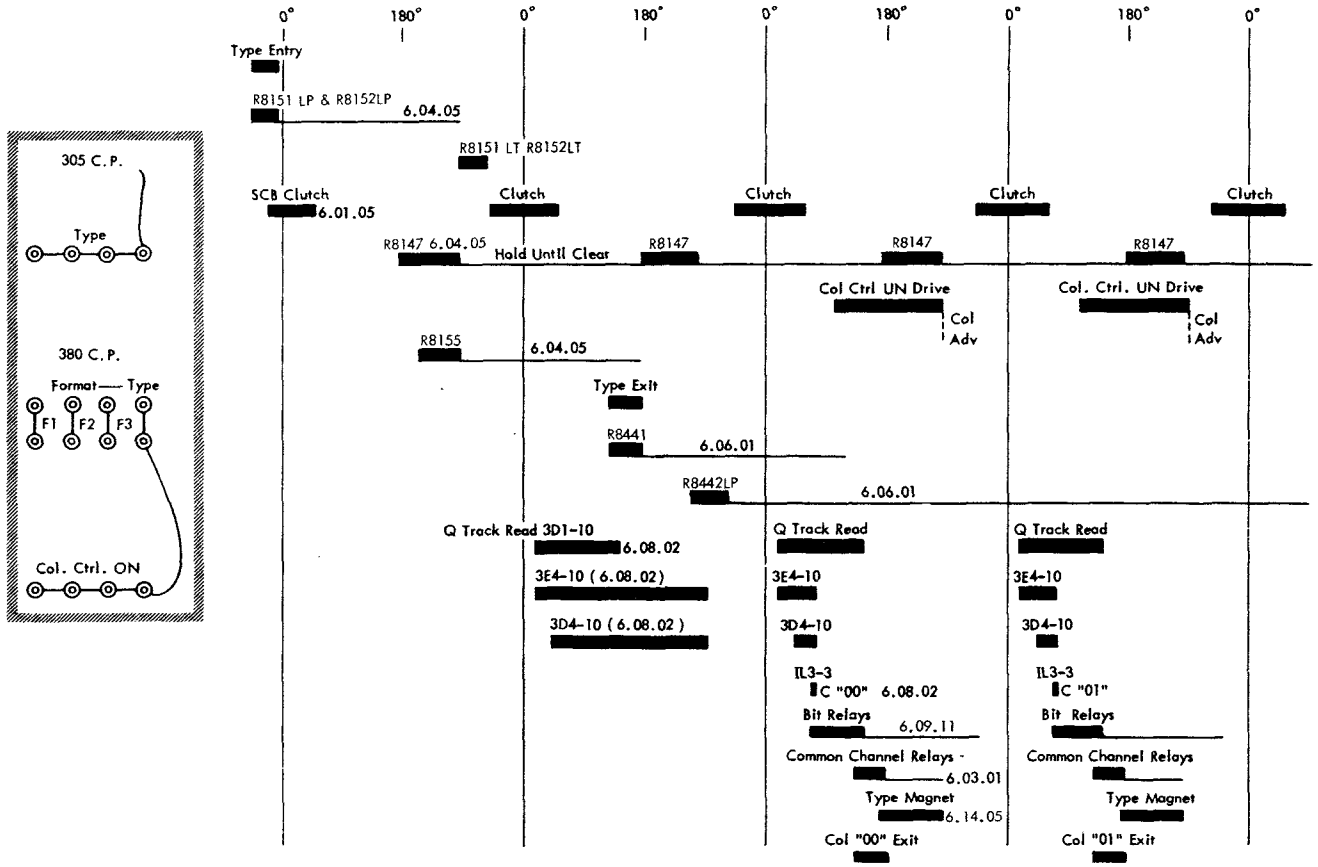


Figure 198. Type with Column Control ON

tact 19) (6.06.04). A similar circuit is provided to return the CCTRS to the 0 position during a clear operation.

Interlock Q Track: To prevent altering Q track while a type operation is in progress, the W cycle gate is interlocked by T = Q and typewriter not ready (3.02.08). The line labeled typewriter not ready is high until the INQ/TYPE relay is dropped out at the end of the type operation.

Format Control

The 380 supervisory control panel permits various arrangements of typewritten data. The sequence in which characters are selected from Q track for typing and all functional typewriter operations can be selected at the control panel. Two groups of hubs, column control exits and program exits, emit impulses which are used to control the typewriter format.

The column control exits are numbered 00 through 99 and correspond directly to the character positions on Q track. As character 00 of Q track is being typed, an impulse is emitted from the 00 column control exit. The column control exit impulses are controlled by the same rotary switches that perform the selection of characters from Q track. The rotary switches normally advance sequentially from position 00 through position 99 and are advanced one position for each SCB cycle.

The order in which the characters from Q track are typed can be altered by interrupting the normal step-by-step advancement of the rotary switches. If a column control exit impulse is wired to a COLUMN CONTROL ENTRY, the rotary switches will search to the new position before the next character is typed. In the example illustrated in Figure 200, after character 65 has been typed the rotary switches will advance to position 93. Character 93 will be typed immediately following character 65 and the rotary switches will continue to advance normally and select characters 94 through 99.

To perform a search operation a circuit is completed to the rotary switch drive magnet through the interrupt contact. As the magnet is energized, the interrupt contact opens and the rotary switch advances as the magnet is de-energized. The interrupt contact closes as the magnet is de-energized and the process is repeated until the circuit to the interrupt contact is broken when the rotary switch reaches the position that corresponds to the column control entries that were impulsed to initiate the search.

COLUMN CONTROL UNITS ROTARY SWITCH SEARCH OBJECTIVES:

1. Initiate a units search to position 3.
   a. COLUMN CONTROL EXIT wired to COLUMN CONTROL ENTRY UNITS #3 (6.06.01).
2. Energize the rotary switch drive magnet through the interrupt contact (6.06.10).
   a. Latch pick COL CTRL UN SRCH R8443 (6.06.02).
3. Open the circuit to the drive magnet when position 3 is reached.
   a. Latch trip COL CTRL UN SRCH (6.06.02).
4. Suspend SCB clutch cycles until the search is completed (6.01.05).

Initiating the Search: An SCB 1 impulse wired from a column control exit to COLUMN CONTROL ENTRY #3 picks R8405 (6.06.01). R8405 is held by SCB 8 and remains up until the next clutch cycle is initiated after the search is complete. If the search operation is initiated by an impulse other than a column control exit, column control will be turned on automatically when R8405-5 latch picks COL CTRL ON #2 (6.06.01).

Advancing the Rotary Switches: The units drive magnet is energized by SCB 7 through the interrupt contact and the transferred points of COL CTRL UN SRCH (6.06.10). COL CTRL UN SRCH is latch picked by SCB 9 through R8405-2 (6.06.02). The interrupt contact will continue to furnish a series of pulses to advance the drive magnet until the COL CTRL UN SRCH relay is latch tripped.

Search Stop: COL CTRL UN SRCH is latch tripped when the rotary switch reaches the new lecoation (6.06.02). The trip circuit is through ODD SECT R8442-2 N/O or N/C, R8405-4 or -3, CCURS #6 contact 2 or 12 and SCB 7 (6.06.04).

COL CTRL UN SRCH does not actually drop out until the rotary switch advances from the 2 contact to the 3 contact due to a parallel circuit to the trip and pick coils through R8463-2. As the rotary switch advances from contact 2 to contact 3 COL CTRL UN SRCH drops out and opens the circuit to the drive magnet.

Since the CCURS is a twenty position switch, the tens position of the new switch location must be analyzed to determine whether the CCURS should stop on the first half of the switch or the second. If the column control exit impulse that initiated the search was wired to any odd position of column control entry tens, the odd section relay (ODD SECT R8444) will be energized to transfer control of the stopping point to the second half of the rotary switch (6.06.02).

SCB Clutch: The circuit to the SCB clutch is suspended while a search operation is in progress by a normally closed COL CTRL UN SRCH point (6.01.05).

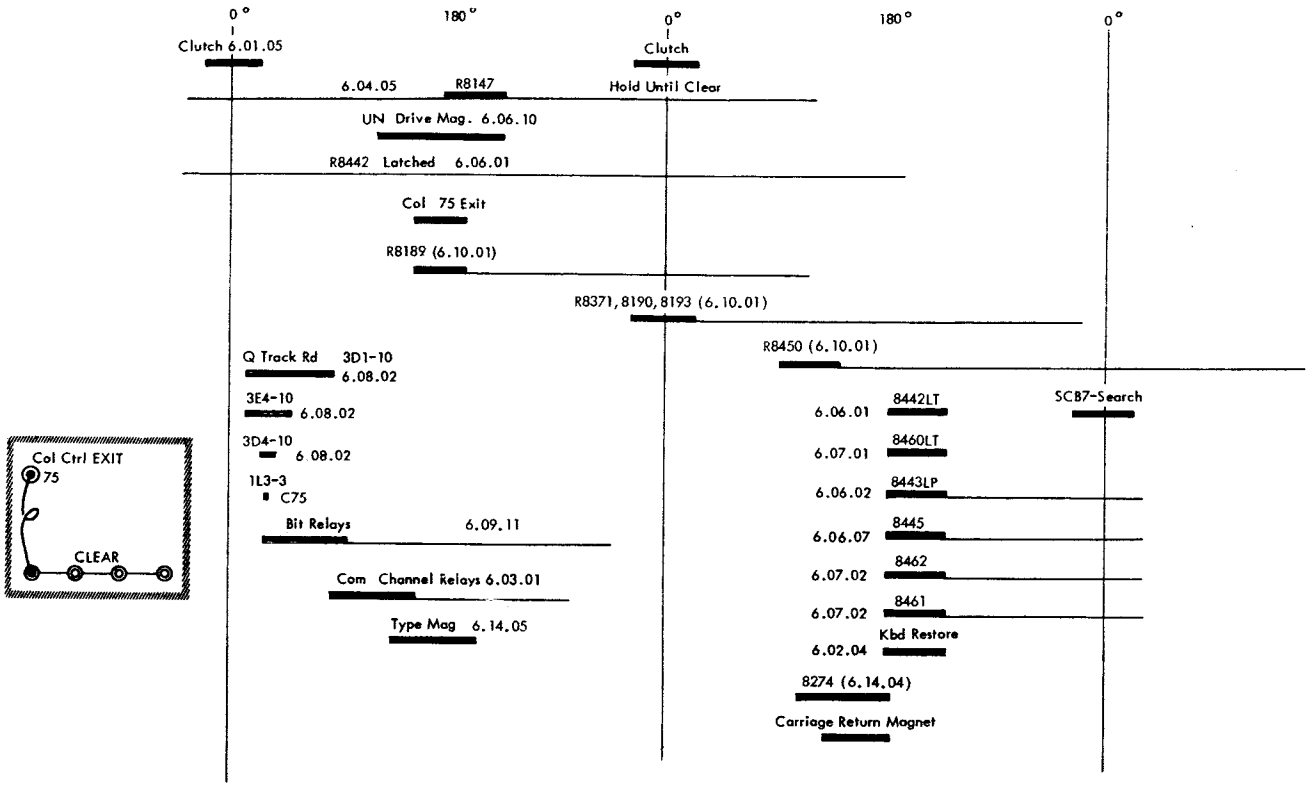


Figure 199. Clear

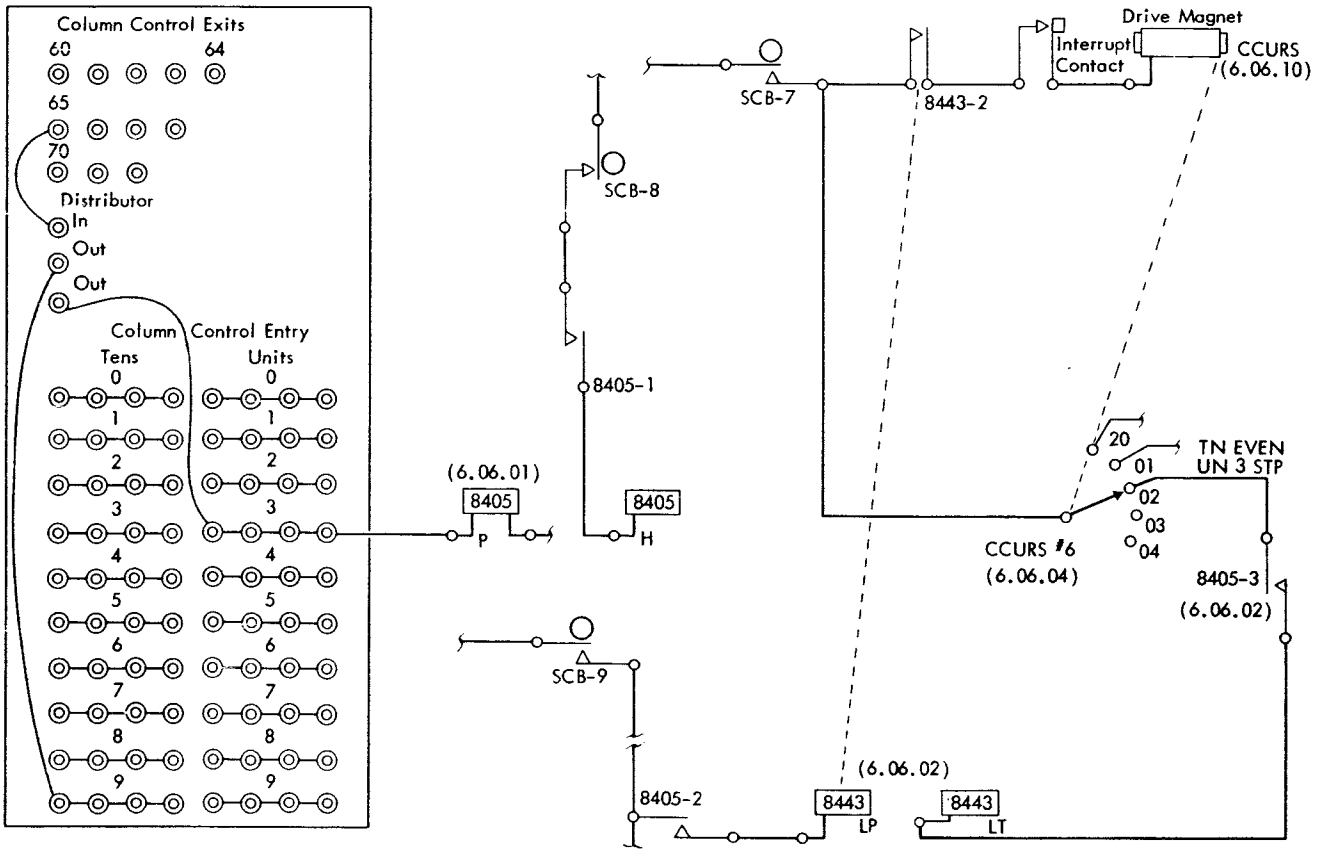


Figure 200. Column Control Search

COLUMN CONTROL TENS ROTARY SWITCH SEARCH

The tens search is initiated and controlled in the same manner as the units search. The circuits for a tens search can be developed by following the objectives that were listed for the units search. The tens drive magnet is located on 6.06.10 and the controlling relays are located on 6.06.06 and 6.06.07. CCTRS #2 (6.06.08) controls the stopping point of the tens search.

Program Control

The program exits provide an alternate source of impulses for controlling typewriter format. The column control exits are available only on cycles in which a character of data is being read from Q track and typed. In some cases it is necessary to type information that is not present on Q track or perform a series of functional operations that do not involve the typing of data from Q track. To perform this type of operation control of the typewriter format is transferred from the column control exits to the program exits by wiring a column control exit to PROGRAM CONTROL ON. After program control has been turned on, the program exits will emit sequentially starting with A0 and progressing through E4. Typing of data from Q track can be resumed at any point by wiring a program exit impulse to COLUMN CONTROL ON.

In the example illustrated by Figure 201, program control is turned on after C01 of Q track is typed. The A0 program exit causes a carriage return. The A1 exit shifts to the black ribbon and turns column control back on. Typing will be resumed on the next line starting with C02 from Q track.

The program control operation is performed by rotary switches (program control level and step rotary switches — PCLRS and PCSRS) in a manner very similar to column control operation.

OBJECTIVES:

1. Turn on program control.
   a. COLUMN CONTROL EXIT wired to PROGRAM CONTROL ON (6.07.01).
2. Turn off column control.
   a. Latch trip COL CTRL ON #2 (6.06.01).
3. Emit an SCB 2 impulse from level A step 0 (6.07.03).
   a. Energize the SCB clutch.
4. Advance the PCSRS.
   a. Energize the PCSRS drive magnet (6.07.07).
5. Advance the PCLRS after level A step 4.
   a. Energize the PCLRS drive magnet (6.07.07).

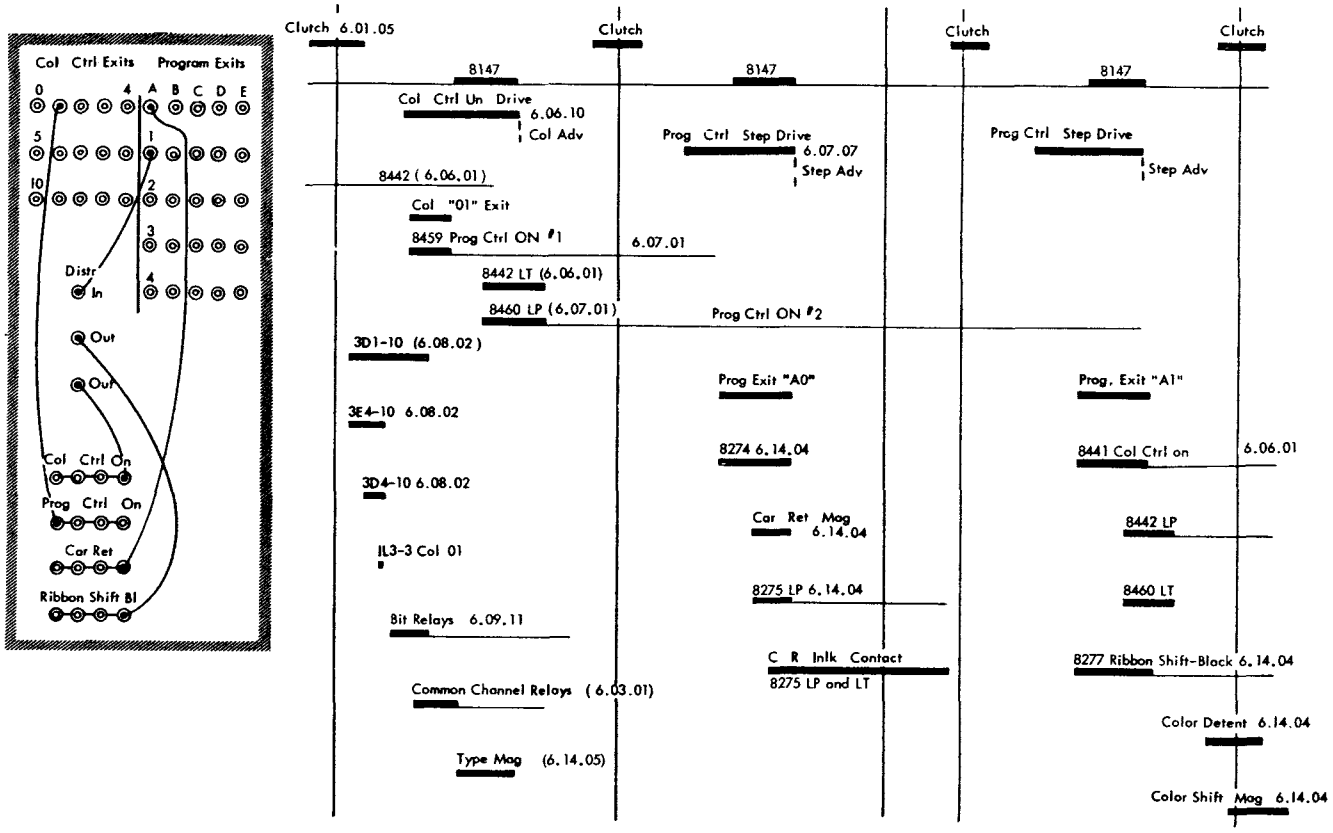


Figure 201. Program Control

6. Turn off program control.
   a. Program exit wired to COLUMN CONTROL ON (6.06.01).
   b. Latch trip PROG CTRL ON #2 (6.07.01).

Turn On Program Control: A column control exit wired to PROGRAM CONTROL ON picks PROG CTRL ON #1 (R8459) and a hold circuit is available through SCB 8 until early in the next clutch cycle (6.07.01). Late in the cycle SCB 9, through the transferred points of PRG CTRL ON #1, latch picks PRG CTRL ON #2 (R8460). The typewriter remains under program control until PRG CTRL ON #2 is latch tripped.

Turn Off Column Control: Column control is turned off by latch tripping COL CTRL ON #2 with the same impulse that latch picked PROG CTRL ON #2 (6.06.01).

Program Exit Impulse: If the rotary switches have been previously reset to level A step 0, an SCB 2 impulse will be emitted from the A0 program exit (6.07.03) through the 11 contact on PCSRS #1 and the 11 contact on PCLRS #1 (6.07.05). The circuit to the SCB clutch is still available through the transferred points of INQ/TYPE (6.01.05).

PCSRS Advance: The step rotary switch is advanced one position during each clutch cycle by SCB 10 and PRG CTRL ON #2 (6.07.07). The step rotary switch is an eleven position switch. As program control advances through steps 0 through 4 the step rotary switch advances through the first five contact positions. As program control advances through steps 0 through 4 of the next level the step rotary switch advances through the next five contact positions. Contacts 11 through 4, and 5 through 9 perform identical functions. When the rotary switches are reset by a clear operation, the step switch will stop on the #11 contact or the #5 contact (6.07.03). The #10 contact position is unused and as the step rotary switch advances from the #9 contact, the #10 contact must be skipped in order to return the switch to contact #11 and set-up step 0. This is accomplished by picking ADV STP 0 R8458 when the rotary switch is in the contact #9 position (6.07.01). ADV STP 0 initiates a search to contact #11 by latch picking PRG CTRL STEP SRCH R8461 (6.07.02). The theory of program control search operation is essentially the same as the column control search operation previously discussed.

PCLRS Advance: The level rotary switch is advanced by SCB 10 and the contacts of PCSRS #7 as the program step rotary switch advances from the contact 4 position or the contact 9 position (6.07.04).

Turn Off Program Control: Program control is turned off by wiring a program exit to COLUMN CON-

TROL ON (6.06.01). The same impulse that latch picks COL CTRL ON #2 latch trips PROG CTRL ON #2 and suspends the program operation (6.07.01).

Carriage Return

A column control exit or program exit wired to CARRIAGE RETURN will cause the typewriter carriage to return to the beginning of the next printing line before the next character of Q track data is typed.

OBJECTIVES:

1. Return the typewriter carriage.
   a. Energize the carriage return magnet (6.14.04).
2. Suspend typing until the carriage return is complete.
   a. Prevent energizing the SCB clutch (6.01.05).

The carriage return magnet is energized by SCB 3 or 9 and CAR RET R8274-2. (On systems not equipped with 381 the cathodes of D1171 and D1172 are jumpered). CAR RET is picked by the impulse to the carriage return hub (6.14.04).

Tabulation

An impulse wired to the tabulate hub will cause the typewriter carriage to escape to the next tab stop before the next character of data is typed. The impulse to the tabulate hub sets up an operation similar to the carriage return operation. The tab magnet is energized to release the carriage (6.14.05) and CLR DEL is picked to hold off the next clutch cycle until the tab operation is completed.

Zero Suppression

When typing fields of numeric data from Q track it is often desirable to suppress the typing of zeros to the left of the first significant digit. The suppression of zeros is accomplished by wiring the column control exit that corresponds to the high order digit to ZERO SUPPRESS ON. With zero suppression turned on, the impulses that would normally energize the zero magnet are rerouted to the zero transfer hub on the control panel. The zero transfer hub is normally wired to SPACE. Zero suppression is turned off by the first significant digit or by wiring a column control exit to ZERO SUPPRESS OFF.

OBJECTIVES:

1. Turn on zero suppression.
   a. Column control exit wired to ZERO SUP ON (6.15.01).
   b. Latch pick LFT ZR SUP #2 (6.15.01).
2. Reroute the zero type impulse to ZERO TRANSFER (6.14.01).
3. Turn off zero suppression with the first significant digit.
   a. Latch trip LFT ZR SUP #2 (6.15.01).

Column Control Delay

A column control delay operation suspends the typing of Q track data for one cycle and is initiated by wiring a column control exit impulse to the column control delay hub. In the example illustrated by Figure 202, the column control delay is initiated during the cycle in which C93 is typed. During that cycle the rotary switches do not advance, but on the following cycle the column control exits are suppressed to eliminate a second impulse from the same exit. During the delay cycle the impulse that would normally go to the key magnet is switched to the column control delay exit (CCD). The CCD impulse wired to the type only # hub will cause the "#" to be typed during the delay cycle. Late in the delay cycle the rotary switches advance and on the following cycle normal typing is resumed with C94.

OBJECTIVES:

1. Initiate a column control delay.
   a. Column control exit wired to COLUMN CONTROL DELAY (6.06.11).
2. Prevent the column control rotary switches from advancing.
   a. Hold the drive magnets in the energized position until the following clutch cycle (6.06.10).
3. Emit an impulse from CCD exit during the delay cycle (6.06.11).
4. Suppress the column control exit during the delay cycle (6.06.03).

Column Split

A column control exit wired to COLUMN SPLIT alters the key magnet circuits so that only the numeric portion of an alphabetic character will be typed. The column split operation initiates a column control delay and during the delay cycle the character is read from Q track a second time. The common channel relays are picked and analyzed for the presence of an X bit and the impulse that would normally energize a key magnet is transferred to the X or NX control panel exit (Figure 203).

OBJECTIVES:

1. Setup column split.
   a. Column control exit wired to COLUMN SPLIT (6.15.01).

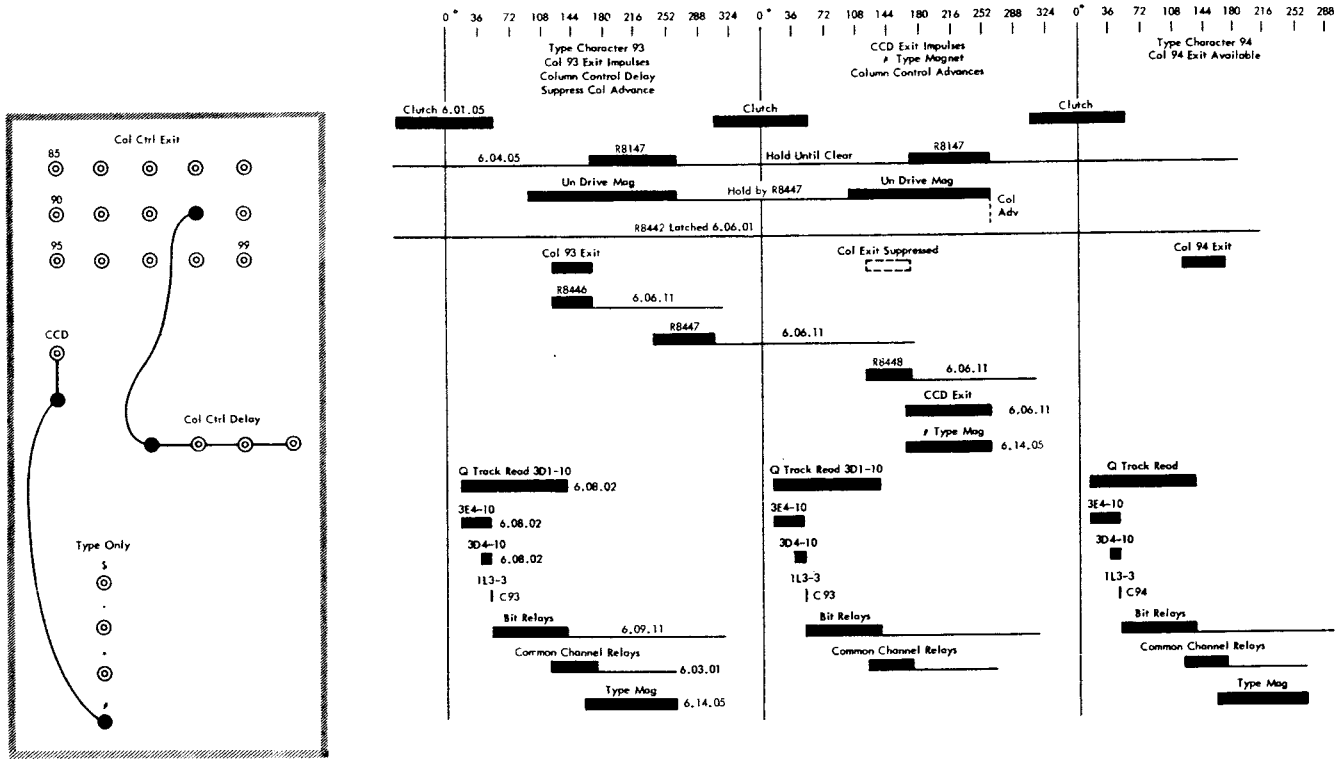


Figure 202. Column Control Delay

2. Type the numeric portion of the character (6.14.01).
3. Initiate a column control delay cycle.
   a. Pick COL CTRL DEL #2, R8447 (6.06.11).
4. Emit an impulse from X or NX hub (6.15.01).

Digit Selection

A column control exit wired to the digit selector PU hub will suspend typing of the corresponding character position. The character of data from Q track picks the bit relays and the common channel relays in the normal manner, but the impulse to energize the key magnet is transferred to a network of bit relay points that make up the character selector. Through the network of bit relay points the impulse is emitted from the digit selector exit hubs that correspond to the Hollerith code representation of the character.

OBJECTIVES:

1. Suppress the impulse to the type magnets (6.14.01).
2. Emit an impulse from the digit selector exit (6.15.02).

Ribbon Shift

The red or black portion of the typewriter ribbon can be selected by wiring a column control exit to RIBBON SHIFT—RED or RIBBON SHIFT—BLACK. Ribbon shifting is accomplished by the detent magnet, which removes the detent roller from the detent plate and allows it to be shifted, and the transfer magnet, which moves the detent plate to the black position. To shift from black to red the detent magnet only is energized and the detent plate moves to the red position under spring tension. To shift from red to black both magnets are energized (6.14.04).

Manual Console Operation

Read Operation

The operator may examine the data on any of the addressable tracks by depressing the read key and then the alphabetic or numeric key that corresponds to the track to be examined. The block diagram of read operation, Figure 204, illustrates the sequence of events and major units involved.

Depressing the read key resets the process unit to I cycle ready and sets up controlling circuits for a 100 column print operation (100 characters of Q track data typed consecutively with all format control panel wiring bypassed.) As the track key is depressed the corresponding character is typed to indicate which

track is being examined and the typewriter tabulates to the first tab stop. During the clutch cycle that results from the track key depression, the master stop trigger is turned OFF and the system advances through an IRWDP cycling sequence. During I cycle the common channel relays that were picked to type out the track indication, setup a corresponding T_1 value in the instruction register A T_2 value of Q is automatically set up during I cycle and a 100 character track to track transfer is performed during the R and W cycles to transfer the desired data to Q track. During P cycle a type operation is initiated by picking the read/write test write relays and 100 characters of Q track data are typed out under control of 100 column print. After C99 has been typed, a clear and carriage return is initiated automatically.

OBJECTIVES:

Read Key Cycle

1. Setup read operation control circuits.
   a. Energize the SCB clutch (6.01.05).
   b. Turn on I cycle ready (1.03.04).
   c. Pick 100 column print (6.11.04).

Track Key Cycle

1. Type the track indication.
   a. Energize the SCB clutch (6.01.05).
   b. Energize a key magnet (6.14.05).
2. Tabulate to the first tab stop.
   a. Energize the tab magnet (6.14.05).
3. Advance through an IRWDP cycling sequence.
   a. Turn OFF the master stop trigger (1.02.09).
4. Set up the instruction register during I cycle.
   a. Enter a T_1 value corresponding to the typed track indication (2.03.03).
   b. Enter a T_2 value of Q (2.03.05).
5. Perform a 100 character transfer to Q track.
   a. Develop a 100 character R cycle gate (3.02.04).
   b. Develop a 100 character W cycle gate (3.02.08).
6. Type 100 characters of Q track data.
   a. Condition the thyratron plates (Q track read) (6.08.03).
   b. Select Q track data (store data in bit relays) (6.08.02).
   c. Energize the key magnets (6.14.05).
7. Initiate a clear after C99 is typed (6.10.01).

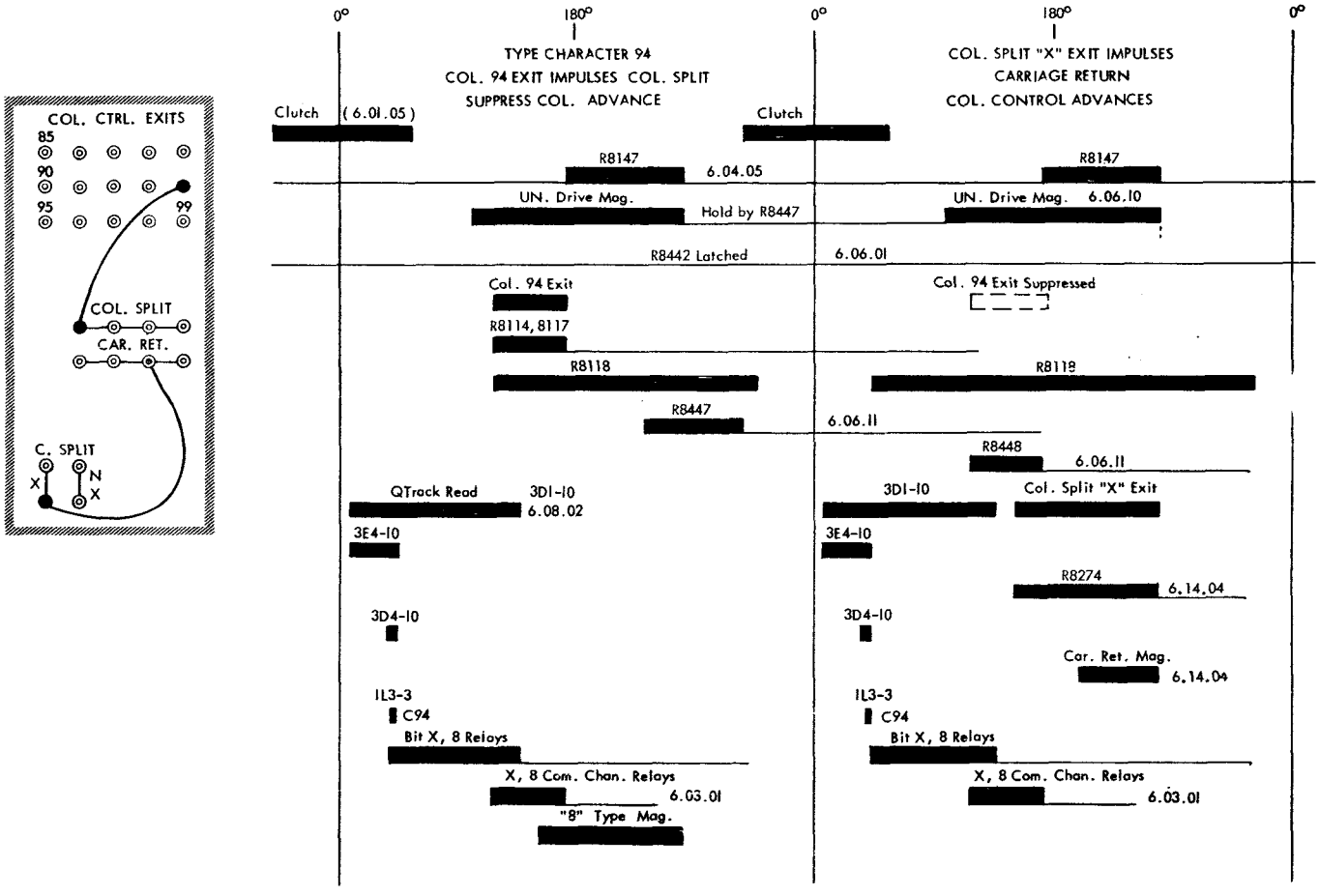


Figure 203. Column Split

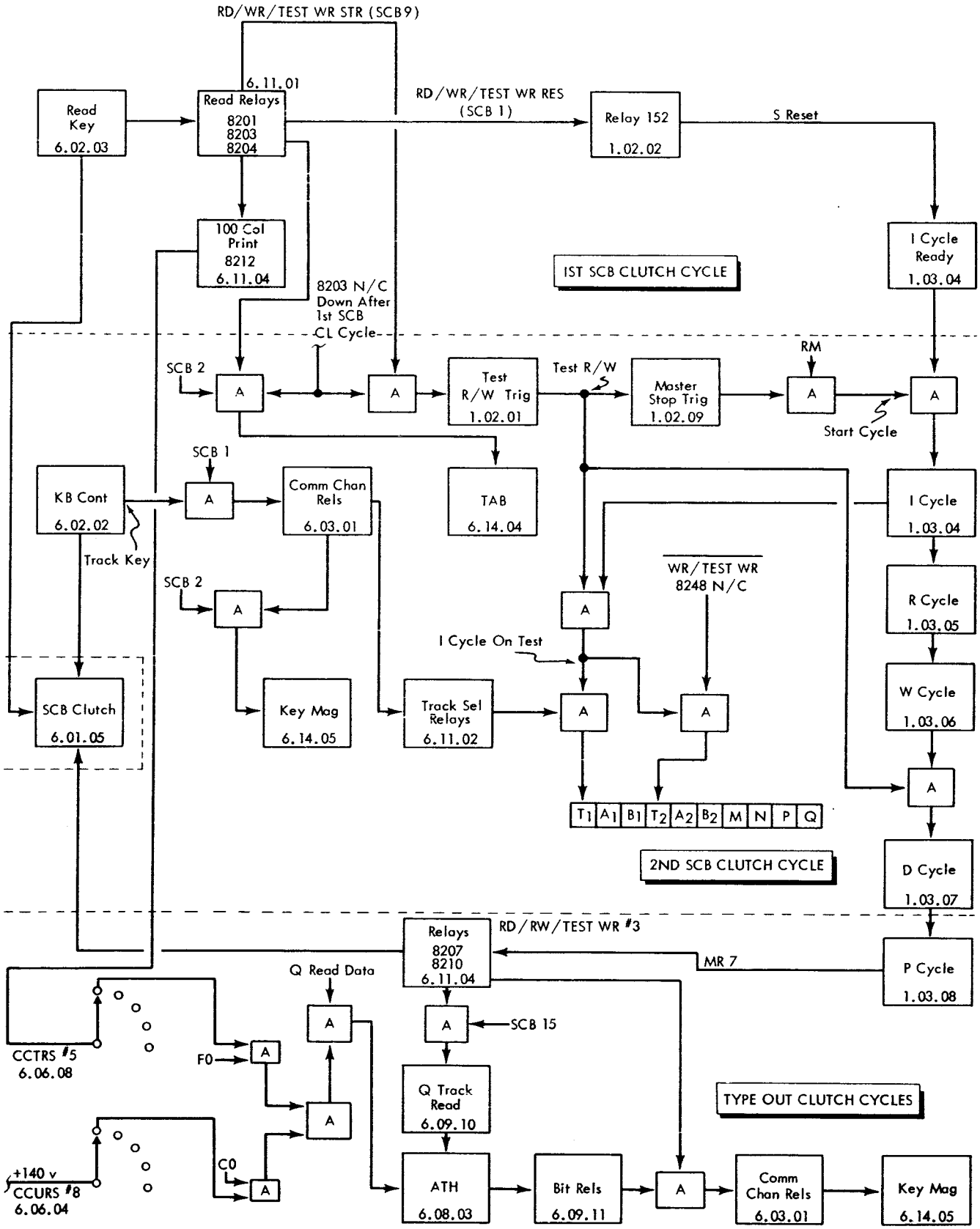


Figure 204. Read Operation

Typewriter Parity Checking

Each character of data that is selected for typing is parity checked before the typewriter key magnet is energized. At the same time that the common channel relays are being picked by the bit relays, a network of bit relay points are checked to determine if an even or an odd number of bit relays have been picked. If an even number of bit relays have been picked, the circuit to the key magnets is opened and the impulse that would normally energize a key magnet is switched to the underline magnet. The advance of the column control rotary switches is suspended on the cycle that the parity is detected and on the following cycle the same character of Q track data is selected a second time. On the second cycle the key magnet circuit is restored to normal and the error character is typed over the underline. At the end of the second cycle the rotary switches advance and normal typing continues until the end of the line is reached or another error character is detected.

OBJECTIVES:

1. Test for an even number of bit relays (6.09.01).
2. Open the normal key magnet circuit (6.14.01).
3. Energize the underline magnet (6.14.05).
4. Prevent the advance of the column control rotary switches.
   a. Hold the units drive magnet energized (6.06.10).
5. Suspend the parity test on the delay cycle (6.09.01).

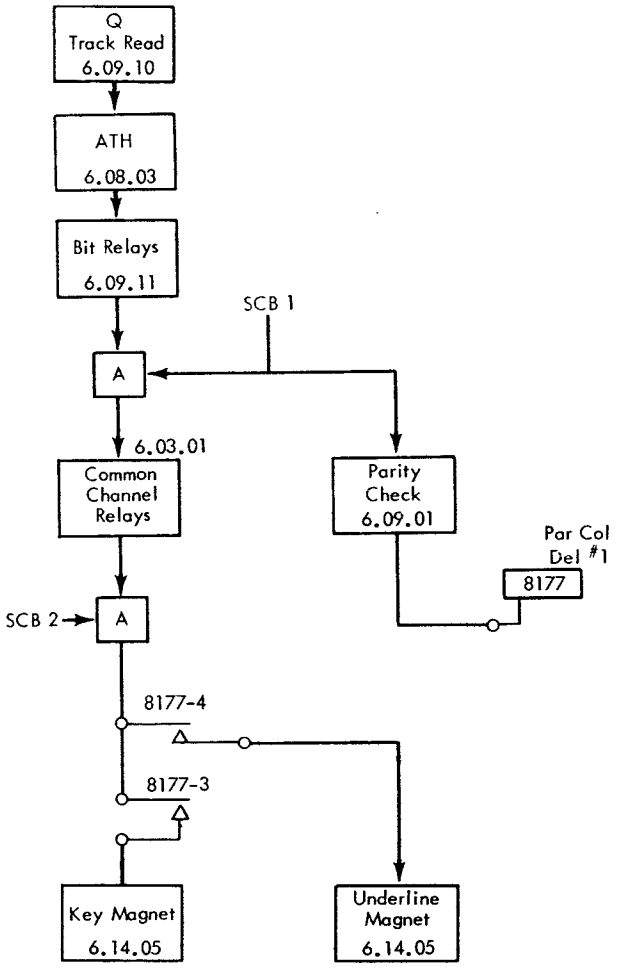


Figure 205. Typewriter Parity Checking

Alter Operation

An alter operation is the process of entering data on Q track directly from the console keyboard. The data on any addressable process drum track can be altered by first entering the new data on Q track and then transferring the data from Q track to the track to be altered.

An alter operation may be performed to enter new data on a process drum track or to correct an invalid character that has been indicated during a console read operation. The type of alter operation to be performed is determined by the test lock switch. If the test lock is ON, data can be written in any or all Q track positions during an alter operation and subsequently transferred to any process drum track. If the test lock is OFF, the only Q track character positions which can be changed are those positions which have been previously underlined to indicate an invalid character and after the error character is corrected the data can only be returned to the process drum track which was read initially.

Alter Parity Correction

An error character that is indicated while the machine is processing can be corrected by performing a simple three-step console error correction procedure.

1. Read the process drum track that contains the error.
2. The error character will be underlined as the track is typed. Depress the alter key with the test lock OFF. The typewriter will automatically space until the error character is reached. Depressing the alphabetic or numeric key to correct the error character will enter that character on Q track and the typewriter will resume spacing to the end of the line or until the next error character is reached.
3. Depress the write key. The corrected data will be typed out and automatically returned to the process drum track that was read initially.

Depression of the alter key initiates an operation that is very similar to a console read operation (Figure 206). The controlling relays that are picked by the

alter key energize the tab magnet and set up a 100 column print operation to control the advance of the rotary switches and the selection of data from Q track. As soon as the tab is complete the alter relays provide a continuous circuit to the SCB clutch and during each clutch cycle a character of data is read from Q track and set up in the bit relays. A normal parity test is performed on each character and if the character contains an odd number of bits, a circuit is completed to energize the space solenoid. If an invalid character is set up in the bit relays, the alter column delay relays will be picked and the space solenoid will not be energized. The alter column delay relays suspend the circuit to the SCB clutch and condition the Q track write circuits to accept one character of data from the console keyboard. Depressing the correct alphabetic or numeric key initiates one SCB clutch cycle. During the clutch cycle the corresponding common channel relays are picked and the corrected character is typed. The common channel relay points are analyzed and the corrected character is written on Q track. The character position in which the data is written is determined by the position of the column control rotary switches. During the manual clutch cycle the alter column delay relays drop out and spacing is resumed as the circuit to the SCB clutch and the space magnet is restored.

OBJECTIVES:

1. Set up alter operation control circuits.
   a. Pick 100 column print (6.11.04).
2. Tabulate to the first tab stop.
   a. Energize the tab magnet (6.14.05).
3. Set up one character of data in the bit relays.
   a. Condition the thyratron plates (Q track read) (6.08.03).
   b. Select one character of data (store data in bit relays) (6.08.02).
   c. Pick the bit relays (6.09.11).
4. Space past valid characters.
   a. Energize the space solenoid (6.14.05).
5. Detect an error character.
   a. Pick ALT COL DEL #1 (6.09.01).
   b. Open the circuit to the space solenoid (6.12.01).
   c. Open the circuit to the SCB clutch (6.01.05).
6. Type the corrected character.
   a. Energize the SCB clutch (6.01.05).
   b. Energize the key magnet (6.14.05).
7. Write one character on Q track.
   a. Q write gate (3.10.41).
   b. Q write data (3.10.41).
8. Resume spacing.

Writing on Q Track: Writing a character of data on Q track is controlled by the Q write gate (3.10.41). The Q write gate is an SCB 2 impulse controlled by ALT #2 and ALT COL DEL #3 (6.09.10).

During the time that the Q write gate is high, a one-character Q read/write gate is developed based on the setting of the column control rotary switches (6.08.02). A character corresponding to the alphabetic or numeric key that was depressed will appear on the bit data to be written line every character time until the common channel relays drop out near the end of the cycle. The Q read/write gate selects one character of data from the bit data to be written line and allows it to be transferred to the Q track write circuits as Q write data.

Alter Operation — Test Lock On

With the test lock switch turned ON, any character or group of characters of Q track data may be changed during an alter operation. Under normal operating procedures the track to be changed would first be typed out during a console read operation. By depressing the alter key and then holding down the dup key on the console keyboard, the existing data on Q track can be duplicated until the character to be changed is reached. Releasing the dup key suspends typing and allows data to be written on Q track one character at a time from the console keyboard. The alter operation is suspended automatically as C99 is duplicated or altered, or the operation may be suspended at any point by depressing the clear key.

Depressing the alter key with the test lock ON picks the test alter relays which energize the tab magnet and set up a 100 column print operation (Figure 207). After the typewriter reaches the first tab stop, no further clutch cycles are available until the operator depresses the dup key or a character key. Holding the dup key down provides a circuit to the SCB clutch and during each clutch cycle one character of Q track data is read from Q track and typed under the control of 100 column print. When the character to be changed is reached, releasing the dup key opens the circuit to the SCB clutch and completes a circuit to develop a Q track write gate on the following clutch cycle. The keyboard contacts provide the next clutch cycle as an alphabetic or numeric key is depressed. The altered character is typed through the normal common channel circuits and the character is written on Q track under control of the Q track write gate.

OBJECTIVES:

1. Set up test alter control circuits.
   a. Pick 100 column print (6.11.04).
2. Tabulate to the first tab stop.
   a. Energize the tab magnet (6.14.05).

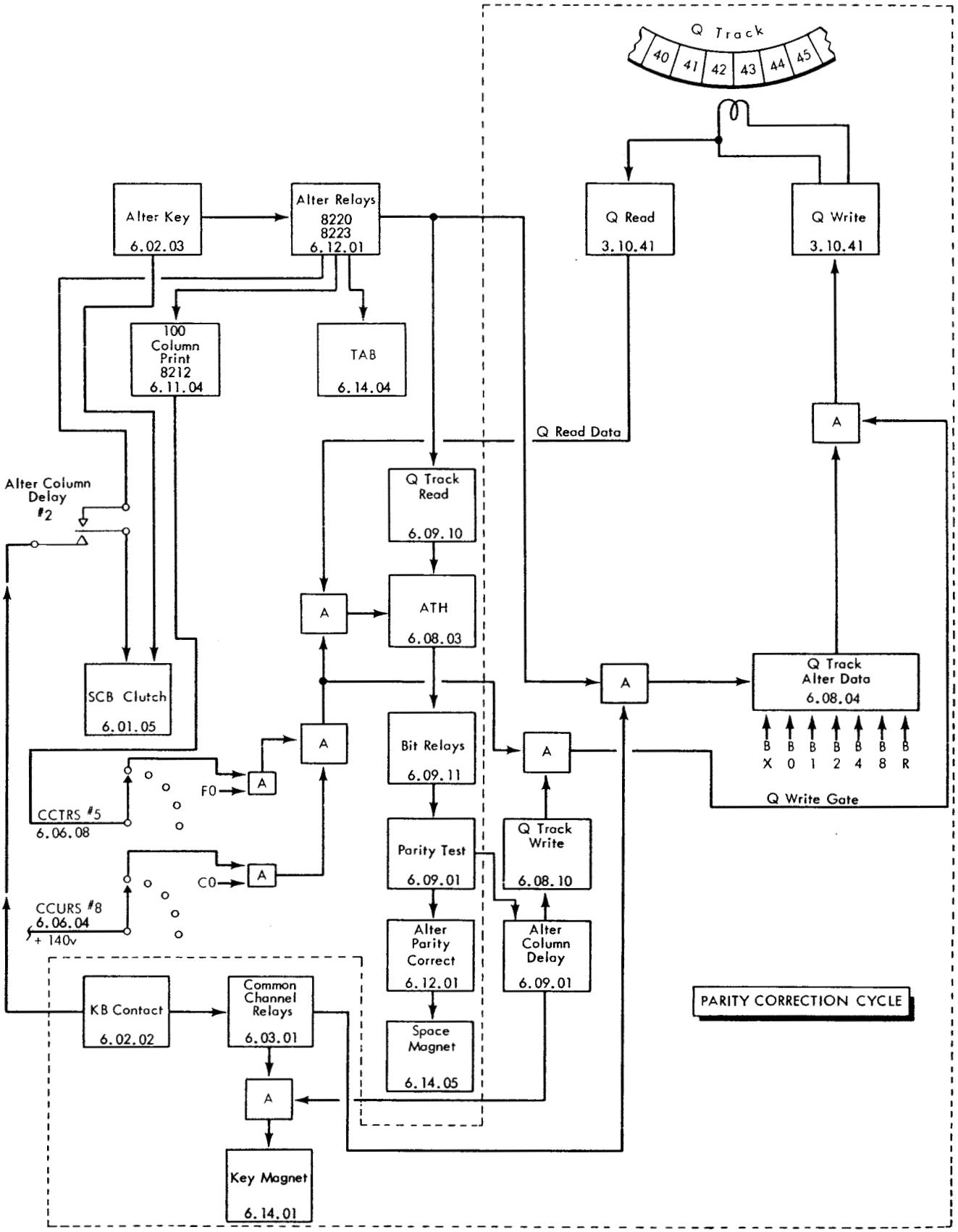


Figure 206. Alter Parity Correction

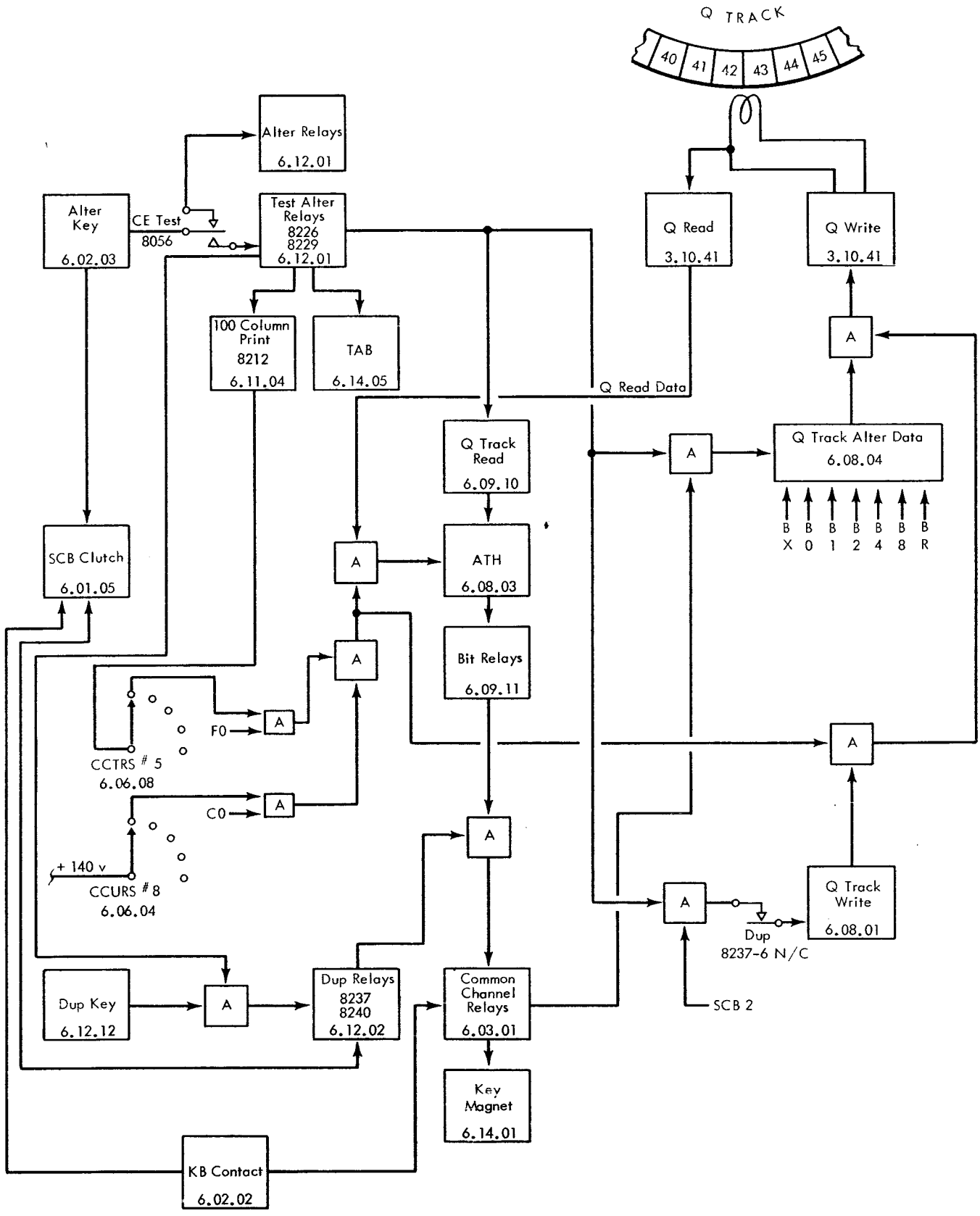


Figure 207. Alter Operation — Test Lock ON

3. Type Q track data under control of the dup key.
   a. Energize the SCB clutch (6.01.05)).
   b. Condition the thyratron plates (Q track read) (6.08.03) .
   c. Pick the bit relays (6.09.11) .
   d. Pick the common channel relays (6.03.01) .
   e. Energize the key magnets (6.14.05) .
4. Type the character to be altered.
   a. Energize the SCB clutch (6.01.05) .
   b. Pick the common channel relays (6.03.01) .
   c. Energize a key magnet (6.14.05) .
5. Write one character on Q track.
   a. Q write gate (3.10.41) .
   b. Q write data (3.10.41) .

Write Operation

In order to alter an addressable process drum track from the console, the data must first be entered on Q track and then transferred to the track to be altered. A console write operation is the process of manually transferring data from Q track to another process drum track.

The position of the test lock determines the type of operation that will be performed when the write key is depressed. If the test lock is OFF the only process drum character that can be altered is one that has been underlined as invalid during a console read operation, therefore, when the write key is depressed Q track is automatically transferred to the error track that was previously read. If the test lock is ON, any addressable process drum track can be altered. Depression of the write key must be followed by an alphabetic or numeric key depression to indicate the track on which the Q track data is to be written.

Write Operation — Test Lock Off

Depression of the write key initiates an SCB clutch cycle and during the cycle controlling circuits are established to allow the transfer of data from Q track to the error process drum track and the subsequent typing of the data that was transferred (Figure 208) . To prepare for the transfer of data the process unit is reset to I cycle ready. The 100 column print relays are picked to control the typing of Q track data.

When the error track was read initially, track selection relays were picked to set up the proper T_1 value in the instruction register. With the test lock OFF the track selection relays that are picked during the read operation do not drop out until a write operation is performed. During the first clutch cycle the track selection relays (SELD TRK MEM) pick the corresponding common channel relays to type out an indication of the track to which the data is being transferred. After the track indication has been typed the tab magnet is energized and the typewriter carriage escapes to the first tab stop.

Late in the first clutch cycle the master stop trigger is turned OFF and the process unit advances through a normal IRWDP cycling sequence. During I cycle the track selection relays (SELD TRK MEM) set up a T_2 value in the instruction register and the transfer of data from Q track to the error track is performed during the R and W cycles. During P cycle the typing of Q track data is initiated and a normal type operation is performed under control of 100 column print.

OBJECTIVES:

1. Set up write operation control circuits.
   a. Energize the SCB clutch (6.01.05) .
   b. Turn on I cycle ready (S reset) (1.03.04) .
   c. Pick 100 column print.
2. Type the track indication.
   a. Pick the common channel relays (6.03.01) .
   b. Energize a key magnet (6.14.05) .
3. Tabulate to the first tab stop.
   a. Energize the tab magnet (6.14.05) .
4. Advance through an IRWDP cycling sequence.
   a. Turn off the master stop trigger (1.02.09) .
5. Set up the instruction register during I cycle.
   a. Enter a T_1 value of Q (2.03.03) .
   b. Enter a T_2 value from selected track memory (2.03.05) .
6. Perform a 100 character transfer.
   a. Develop a 100 character R cycle gate (3.02.04) .
   b. Develop a 100 character W cycle gate (3.02.08) .
7. Type 100 characters of Q track data.

Write Operation — Test Lock On

Write operation with the test lock ON is essentially the same as write operation with the test lock OFF. The primary difference is that a second key depression is required to type the track indication and enter the proper T_2 value for the transfer of data (Figure 209) .

Inquiry Operation — RAMAC Reset

An inquiry operation is the process of reading and typing a selected 100 character record from the file. To perform an inquiry it is necessary to cause the access mechanism to servo to the selected record location, read the file record, transfer the data to Q track, and type out the data after the transfer is complete. If the RAMAC is not processing and is in a reset condition, an inquiry can be initiated by depressing one of the three format keys and then entering the proper five-digit address with the numeric keys.

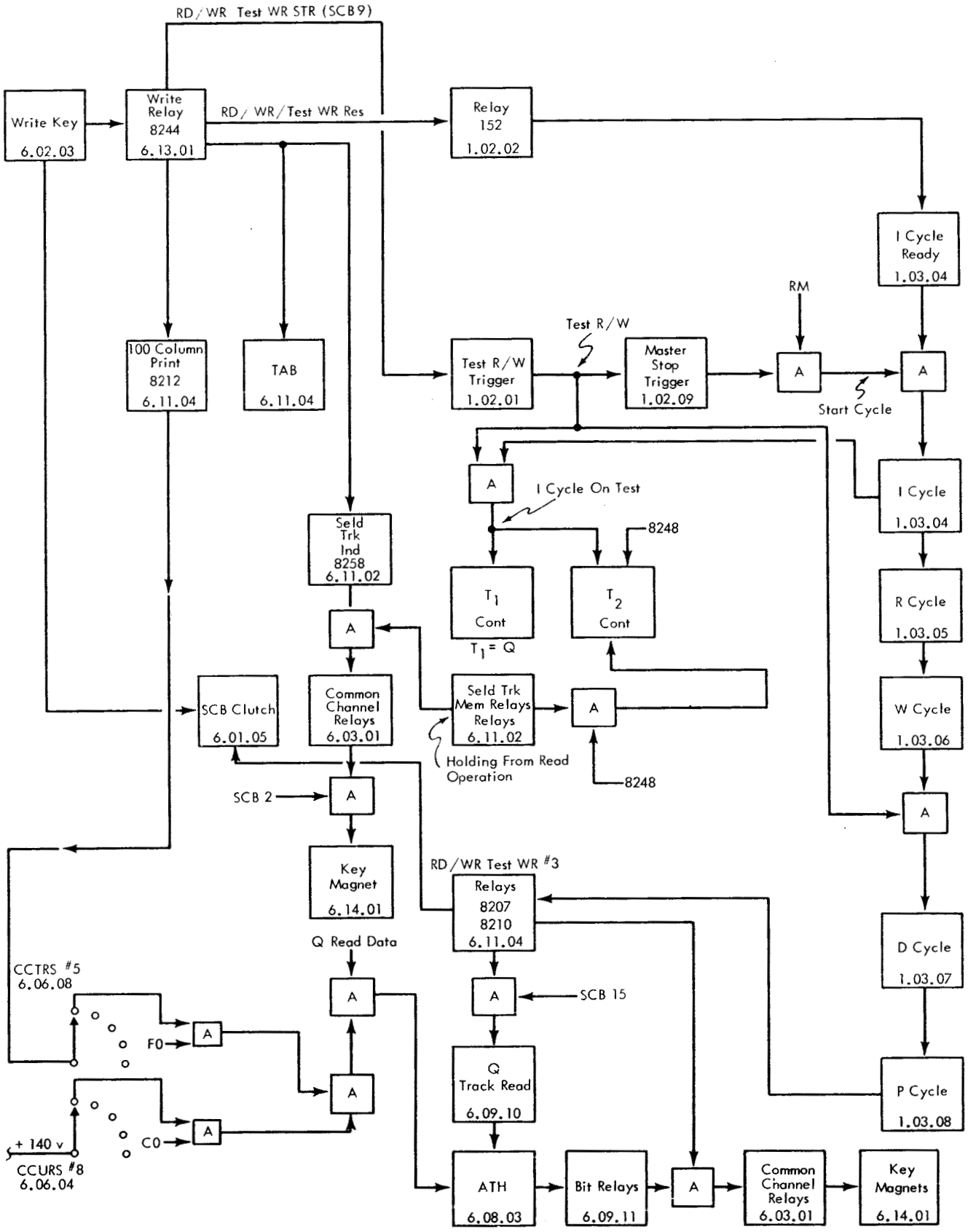


Figure 208. Write Operation – Test Lock OFF

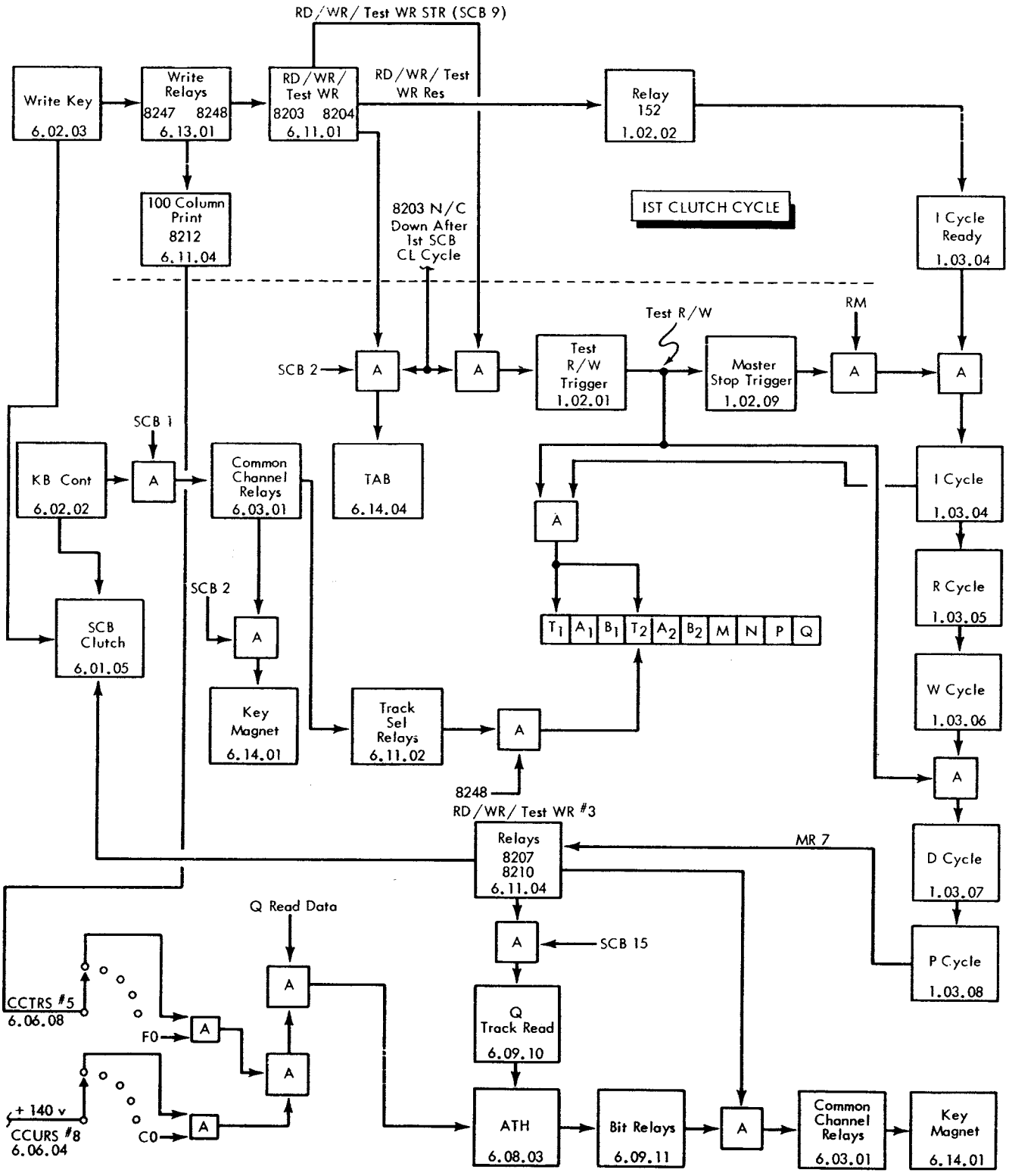


Figure 209. Write Operation — Test Lock ON

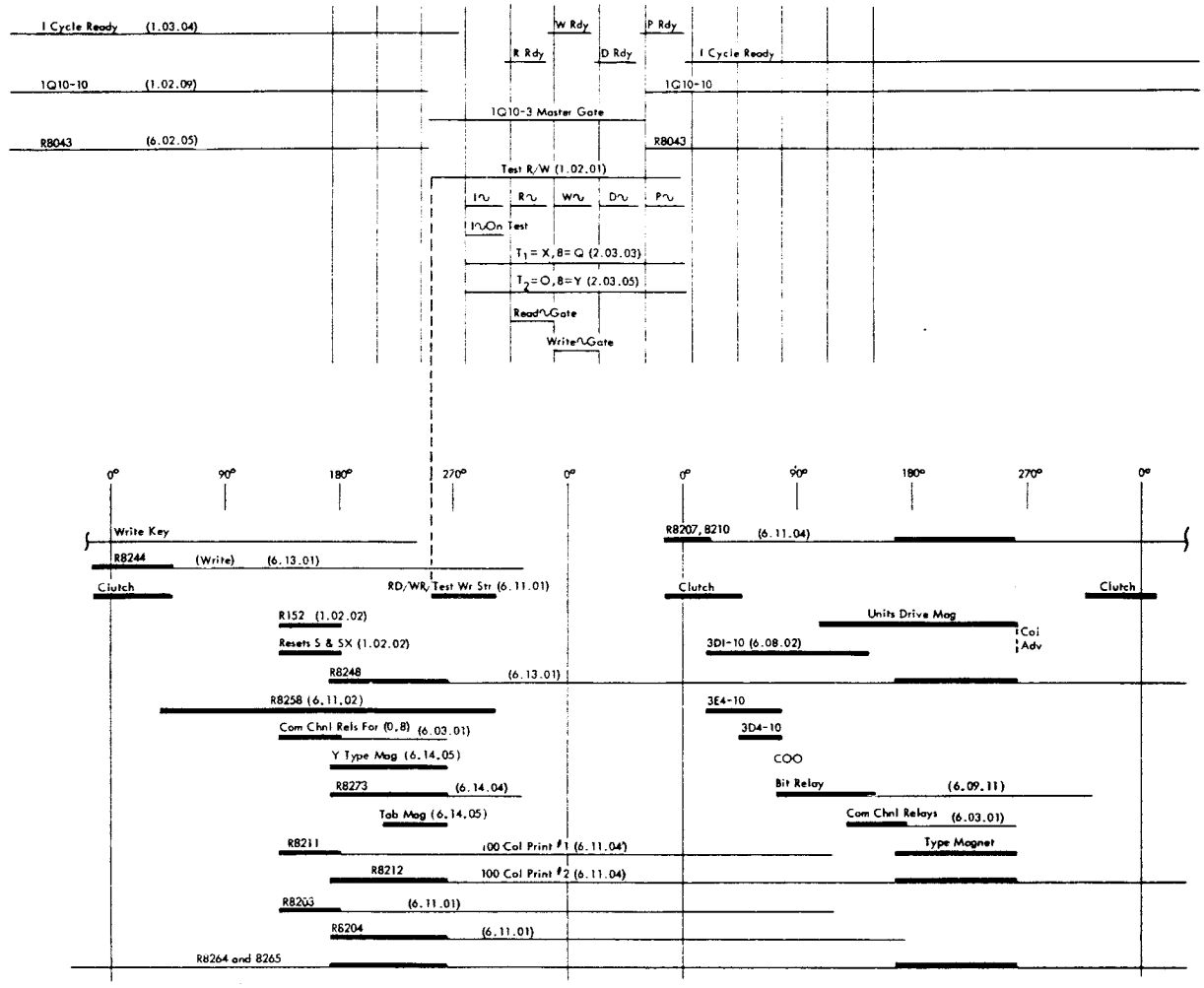


Figure 210. Write Operation — Test Lock OFF

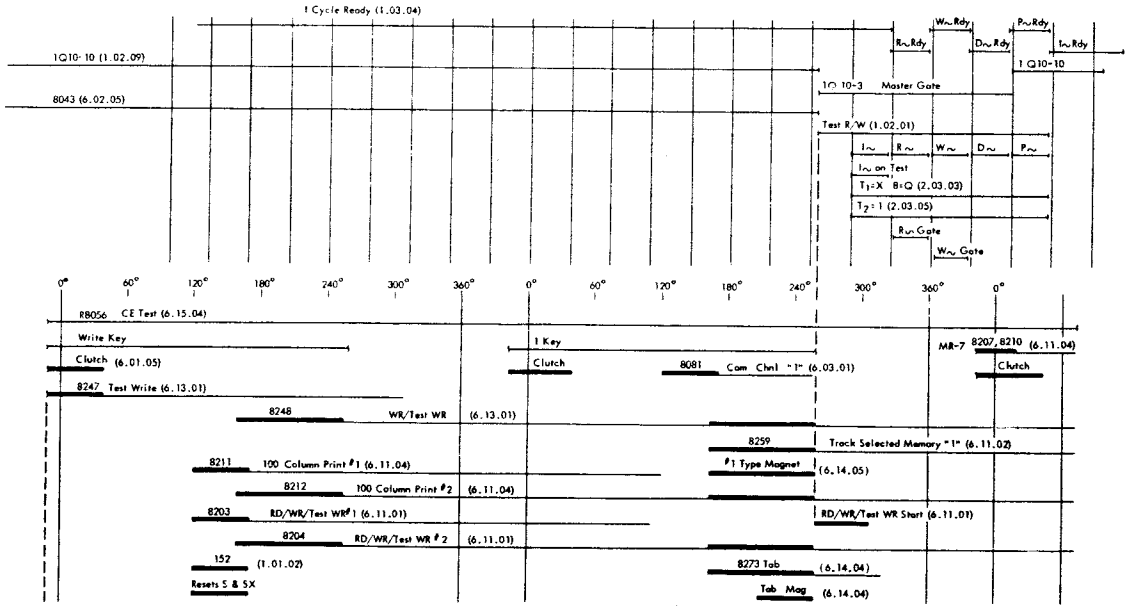


Figure 211. Write Operation — Test Lock ON

Depressing the format key conditions the console to accept a file address. Each of the three format keys perform the same controlling functions, but as the typing is initiated an impulse is emitted from a hub on the 380 control panel that corresponds to the format key that was depressed. The impulse from the format hub is used to establish the typing format for the file record.

The logic of inquiry operation is illustrated in Figure 212.

Depression of format key #1 picks the FMT 1 A and B relays. INQ SU and INQ ADDR relays. The FMT relays remain up until the typeout is initiated and they control the typing format. The INQ ADDR relays set up the entry of the five-digit file address.

Relay storage is provided in the console for each position of the file address. As each numeric key is depressed a circuit must be completed from the numeric keys to a different position of relay storage. The contacts of the PCLRS are used to switch the circuit successively from one position of storage to the next. As each key is depressed the rotary switches advance one position and set up the entry of the next digit. The rotary switch advancing from the fifth position to the sixth signals the completion of the file address and picks the INQ ADDR COMP relay.

Picking INQ TRANS SU, INQ TRANS START, and turning on the inquiry trigger, turns OFF the master stop trigger and allows the process unit to advance through a PDDPIRWDP cycling sequence. Late in the P cycle the address switching relays are energized to control the transfer of the file address from the supervisory buffer to the file address register. During the D cycles the MR 6 line picks up the file start relays and transfers the file address from the supervisory buffer relays to the file address relays. During I cycle a T_1 value of R and a T_2 value of Q are set up in the instruction register in a manner very similar to console read or write operation. Operation is suspended in the R cycle until the servo is complete and the selected record has been reached.

The transfer of data to Q track is completed during the W cycle and the completion of the transfer is signalled by an MR 8 impulse during the D cycle. The INQ TRANS COMP relays initiate the type operation by picking the INQ TYPE relays and conditioning Q track read. The INQ TRANS COMP relays also energize the SCB clutch for one cycle to control the impulse from the format hub. The type operation progresses normally as soon as COL CTRL ON is picked by the impulse from the format hub.

INQUIRY OBJECTIVES:

1. Set up the inquiry operation.
   a. Carriage return (6.14.04).
   b. Pick: FMT 1 A & B (6.04.01).
      INQ SU (6.04.01).
      INQ ADR (6.04.02).
2. Enter a five-digit address.
   a. Pick disk 10's relays (6.05.01).
   b. Advance the PCLRS (6.07.07).
   c. Pick disk units relays (6.05.01).
   d. Advance the PCLRS (6.07.07) etc.
3. Advance through a PDDPIRWDP cycling sequence.
   a. Turn OFF the master stop trigger (1.02.09).
4. Drop out the old address and start relays.
   a. MR 5 (2.09.10).
5. Servo to the inquiry address.
   a. Pick file address relays (8.01.01, 8.02.01, 8.03.01).
   b. Pick the file start relays (8.04.01).
6. Transfer data from file to Q track.
   a. Set up $T_1 = R$ in the instruction register (2.03.03).
   b. Set up $T_2 = Q$ in the instruction register (2.03.05).
   c. Develop a 100 character R cycle gate (3.02.04).
   d. Develop a 100 character W cycle gate (3.02.08).
7. Emit an impulse from the format hub (6.04.01).
8. Set up a type operation.
   a. Turn column control on (6.06.01).
   b. Develop Q track read (6.09.10).

Inquiry — RAMAC Processing

In order to perform an inquiry while the RAMAC is processing, the servo and file read operation must be executed at a time that does not interfere with programmed servo and file read operations. The inquiry on hubs must be wired before processing inquiries can be performed and the point in the program loop at which the inquiry servo can be initiated must be signalled by a program exit impulse wired to the inquiry in hub.

A processing inquiry is normal until the address has been entered and the INQ TRANS SU relay has been picked. At that point, the inquiry is suspended until a program exit impulse enters the inquiry in hub and initiates the inquiry servo and transfer by picking INQ TRF STR #1 (6.04.03). At the conclusion of the inquiry transfer an impulse is emitted from the inquiry out hub to return the process unit to the proper program step and resume operation.

Inquiry Type Interlock

If it is necessary to perform inquires while processing a program that uses the console typewriter as an out-

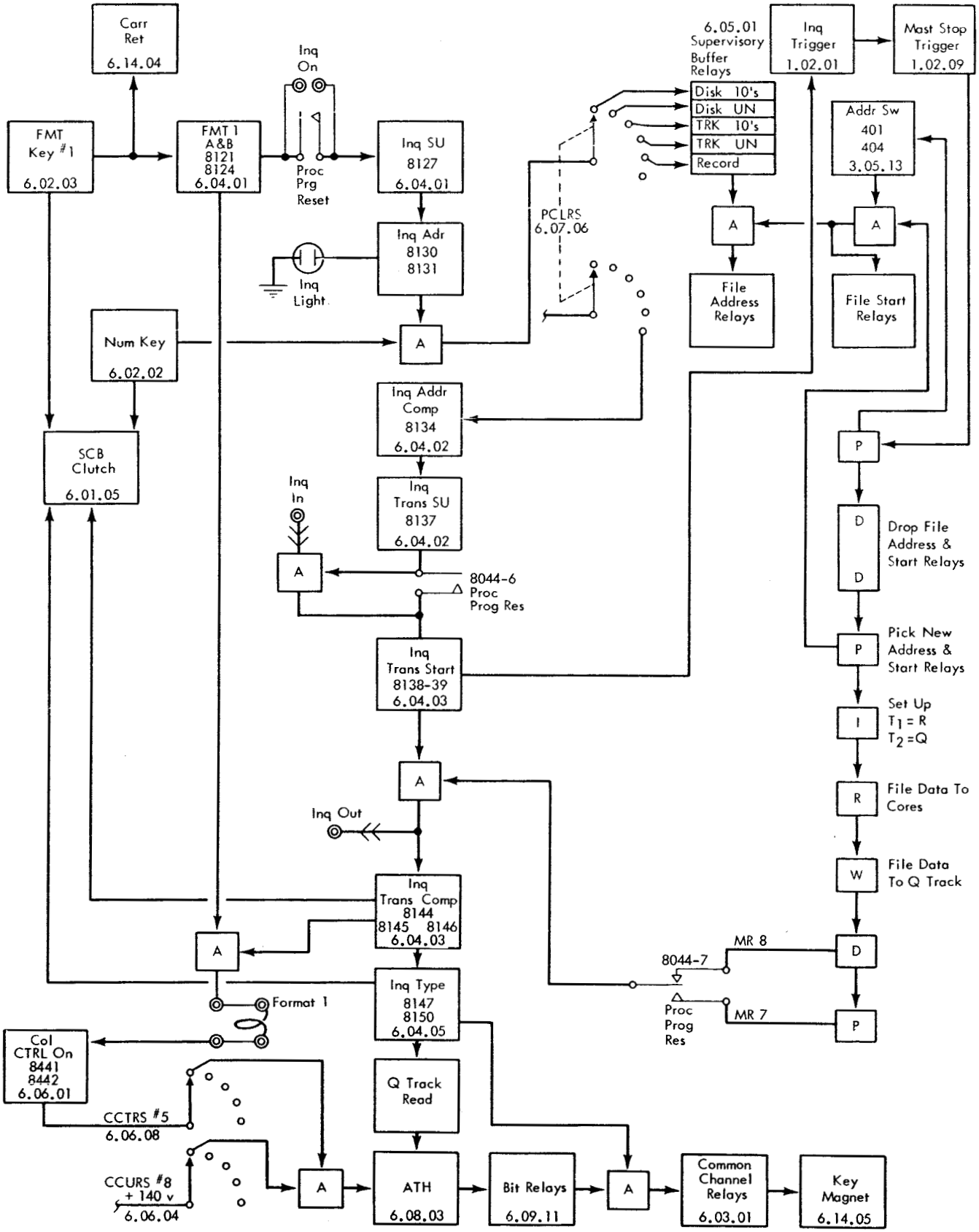


Figure 212. Inquiry

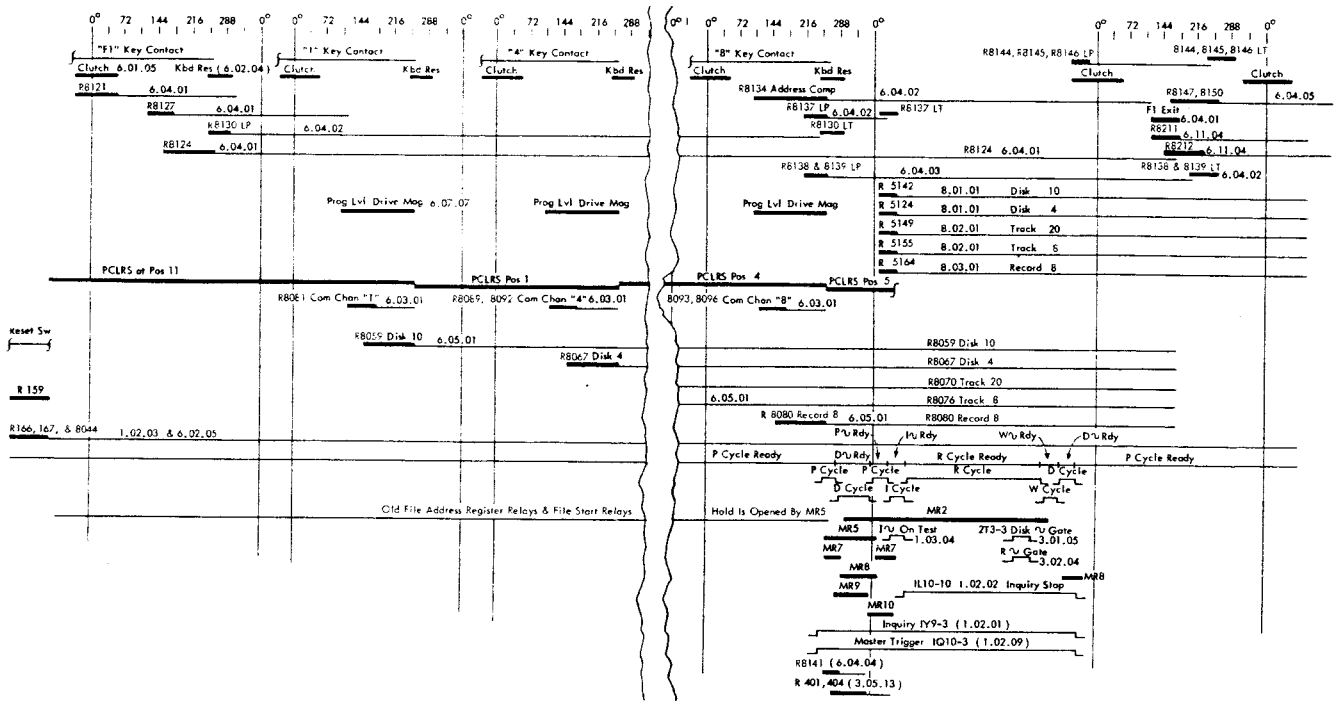


Figure 213. Inquiry with RAMAC Reset

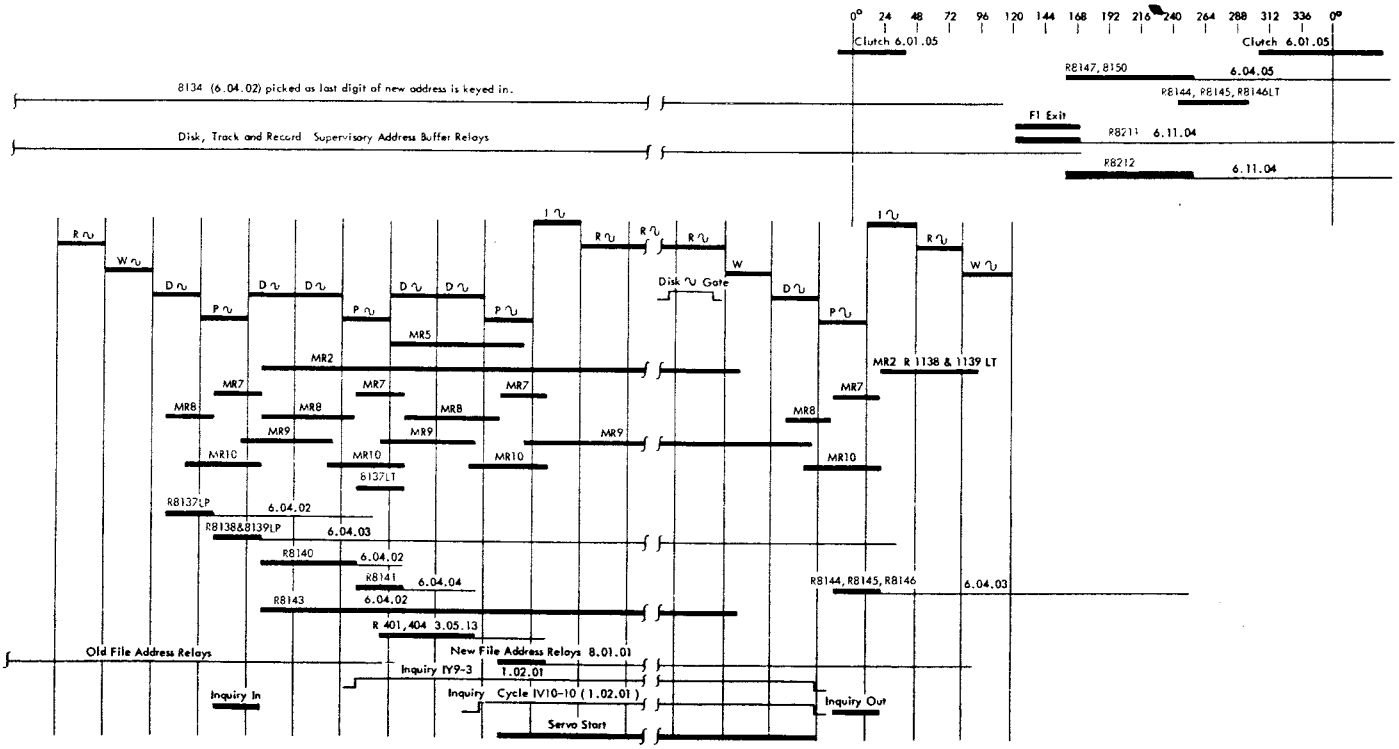


Figure 214. Inquiry with RAMAC Processing

put device, the inquiry operation must be modified to prevent the inquiry from interfering with the programmed typing. Wiring the inquiry type interlock hubs on the 305 control panel modifies the inquiry operation. After the format key has been depressed, the operator must wait until the inquiry light comes on before entering the file address. Once the format key has been depressed the INQ SU relay picks, but the INQ ADDR relays are not picked until a program exit impulse enters the inquiry in hub. When the INQ ADDR relays have been picked the file address can be entered and the inquiry proceeds in the normal manner.

The interlocking function is performed by latch picking INQ ADR INTLK (R8132). The INQ ADR INTLK relay places the pick of the INQ ADR relays under control of a program exit impulse wired to the inquiry in hub. If the operator attempts to enter the file address before the INQ ADR relays have been picked, a clear operation will be initiated by ALPH NUM BAIL CONT #8 (6.02.04).

Keyboard Interlocking While Processing

During processing all alpha/numeric keys and the read, write and alter keys are inoperative. Depressing any of these keys will result in an immediate clear operation, dropping all controlling relays and causing a carriage return. As long as the master stop trigger is OFF the PROC PRG STP relay (R8043) on 6.02.05 will be de-energized. Depressing the read key on 6.02.03, for example, will direct SCB-5 through R8043-4 N/C on 6.11.01 to pick the clear relays on 6.10.01.

Depressing any alpha/numeric key will close bail contact #8 on 6.02.04. This directs SCB-5 to the clear relays through R8043-3 N/C on 6.02.04.

Control Selector Switch

The operator may determine the mode of operation of the RAMAC by positioning the control selector dial switch on the supervisory panel. The switch has five positions, PROGRAM RUN, CONTROL STOP, SINGLE OPERATION, SINGLE CYCLE, and FORMAT TEST. Its wafers, designated 24A, 24B, 24C, and 24D, are located on 1.02.01, 1.02.02, 1.02.04, and 6.04.06, respectively.

Program Run

The control selector switch is placed in the PROGRAM RUN position for normal processing. When in this mode, the RAMAC executes the successive cycles and steps of its operations without any intervening idle periods, except for certain delays necessitated by interlocking conditions. All of the automatic processing operation discussed in previous sections of this manual have assumed the control selector switch to be in the PROGRAM RUN position. This does not include the manual supervisory operations.

Control Stop

Processing may be halted at a selected program step by first positioning the program selector switches to identify the program step and then turning control selector switch to CONTROL STOP.

Processing is halted by flipping the master stop trigger (1.02.09) to lower the master gate from 1Q10-3.

This prevents cycle start pulses from being gated through 1N10; hence, machine cycling is halted with the R cycle ready trigger ON. No cycle trigger will be ON.

If the program start button is depressed while in CONTROL STOP, the RAMAC will cycle through one complete program loop and stop at the same program step, presuming that the setting of the program selector switches has not been changed.

Single Operation

If the control selector switch is placed in the SINGLE OPERATION position, processing may be advanced one program step at a time by depressing the program start button. I cycle end will gate with single operate at 1S10a, and not inquiry and not test R/W at 1S11a (1.02.07), to cause the master gate to be lowered at 1Q10-3 (1.02.09). This will allow only one program step per depression of the program start button. Cycling will stop at R cycle ready on each occasion. No cycle trigger will be ON.

Single Cycle

If the control selector switch is placed in the SINGLE CYCLE position, processing will advance only one cycle with each depression of the program start button. The program start button raises the master gate at 1Q10-3 (1.02.09) in the same manner as in the examples above.

This gate is lowered by each cycle complete pulse gated with single cycle at 1S10b (1.02.07).

Format Test

The format test mode is designed to permit the testing of supervisory operations one cycle at a time. It is particularly helpful to the operator when programming a new typing format, but is also of aid to the Customer Engineer. When the control selector switch is in the FORMAT TEST position, each supervisory cycle must be a direct result of either the depression of a key at the supervisory keyboard or the depression of the program start button. If the supervisory operation being tested requires a transfer of data between tracks of

the process drum or file, each machine cycle (I, R, W, D, and P) will be taken individually, also under control of the program start button.

Any of the supervisory operations, read, alter, write, or inquiry, may be entered at the keyboard, and may be advanced, cycle by cycle, with the program start button. If the supervisory circuits are not already in some particular operational status, the depression of the program start button will initiate a type operation.

Format test does not result in any modification of supervisory operation other than to place supervisory and machine cycles under control of the program start button.

When in format test, if the program start button is depressed without first setting up a read, alter, write, or inquiry operation, a type operation will be initiated. The type operation will be executed just as though the type hub on the 305 control panel were impulsed, except that it will be executed cycle by cycle under control of the program start switch.

381 Remote Printing Station

The 381 Remote Printing Station provides for additional typewriter output at remote locations. One to four remote printing stations can be attached to the 305 System and installed at any distance up to 40 feet. A customer may install and maintain a cable to extend this distance to 2500 feet.

Three basic types of operation are possible with the remote printing station: 1) selected station type out, 2) inquiry transfer, and 3) remote inquiry.

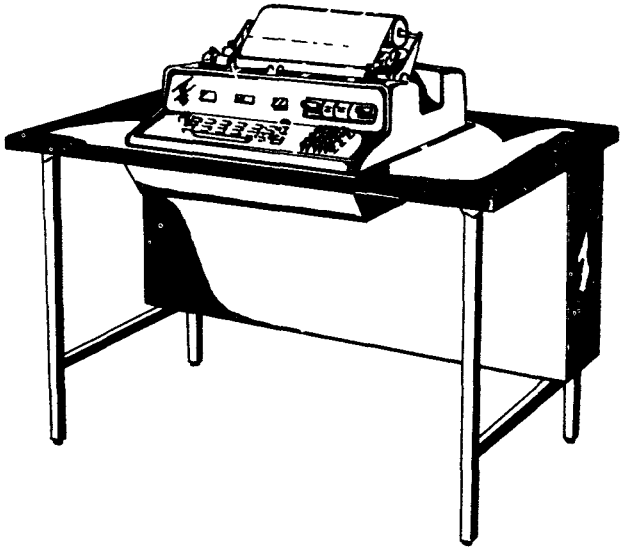


Figure 215. IBM Remote Printing Station

A selected station type out is a programmed type operation directed to one or more of the remote printing stations. A remote station type hub for each of the remote printing stations is provided on the 305 control panel. A program exit impulse wired to a remote station type hub will initiate a normal type operation and set up switching circuits to transfer the type impulses to the key magnets at the selected remote station.

An inquiry transfer operation is the process of typing out the results of a console initiated inquiry at one of the remote printing stations. The stations requesting file information are selected by positioning the station select switch at the console. Depressing the format key sets up a normal inquiry operation and depressing the station select set key establishes switching circuits to transfer the type impulses to the selected remote station at the same time that the information is typed out at the console.

Direct file inquiry from a remote location is possible with the installation of the remote inquiry optional feature. An additional keyboard containing five banks of address keys and five functional keys is added with the remote inquiry optional feature. The address keys select the five digit file address. The function keys control restoring of the keyboard (clear), selecting the desired format (format 1 - 2 - 3), and initiating the inquiry (inquire).

The 381 functional operations, use of switches, control panel wiring, and station description are covered in the IBM 381 Remote Printing Station, M Series Bulletin (Form G26-3503-1). An understanding of the material covered in the bulletin is a prerequisite to circuit and component description.

Additional Components

The following components are added to the 380 console:

1. Switching relays. One set of switching relays for the console and one set of switching relays for each remote station are added. The points of the switching relays are added between the network of common channel relay points and the typewriter key magnets.
2. Interlock relays. Wire contact relays are added to prevent normal console operations from interfering with a remote inquiry.
3. Intermachine shoe connectors. One shoe connector receptacle for each remote station is added to the 380 console.
4. Switches. An eleven position rotary stepping switch is installed on the console relay gate (optional inquiry only). The console control switch, station select wafer switch, station select

set switch and type release switch are installed on the console display panel.

5. Lights. The additional indicating lights are: type check, console control, and a station select light for each of the remote stations.

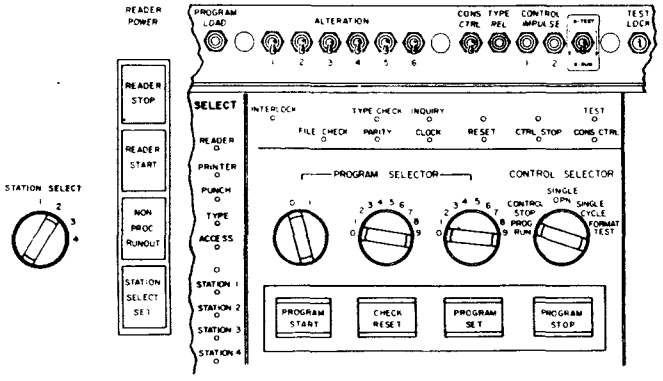


Figure 216. Console Keys and Lights

6. Control panel hubs. Four sets of remote station hubs are added to the 305 control panel for selecting a remote station with a program exit. Twelve format hubs (three per station), and four type exit hubs are added to the 380 console control panel.

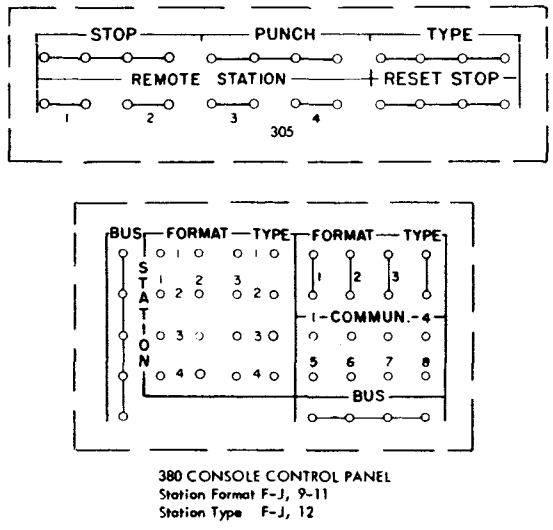


Figure 217. Control Panel Modifications

Each remote station contains the following components:

1. Typewriter. An IBM Electric Model B1 modified for DP equipment is provided and includes a 110v AC motor, paper sensing device, and a power switch controlled lockout bail solenoid.
2. Display panel. The ribbon control and tabulator clear-set levers extend through the display panel. The control switch, power switch, station ready light, RAMAC ready light, and form light are mounted on the panel.
3. Component gate. A component gate with two hinged covers opening toward the rear contains a cable reel for excess cable, 110v utility outlet, DC power supply, typewriter connectors and CE telephone connector.
4. Keyboard. When equipped with remote inquiry a special keyboard is added just to the right of the typewriter keyboard. The keyboard contains five banks of keys for file addressing and five functional keys for controlling the inquiry operation.

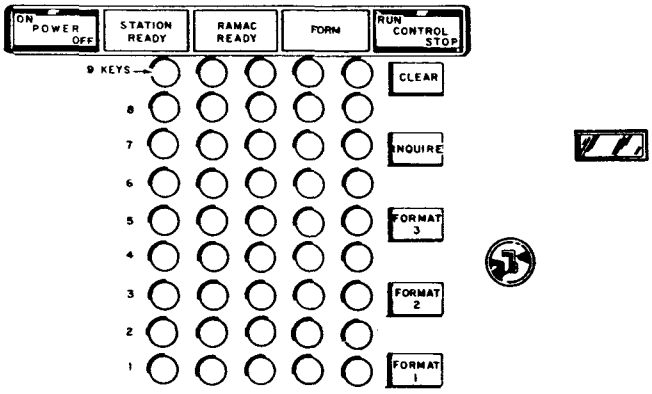


Figure 218. Inquiry Keyboard

Mechanical Principals

INQUIRY KEYBOARD

The keyboard consists of 5 removable key banks and a control key bank.

NUMERIC KEY BANK (FIGURE 219)

Each column of the inquiry keyboard is a separate key bank unit containing nine digit keys. When a digit key is depressed, the bottom of the key stem engages the cam bar and cams it to the rear. The travel of the cam bar is determined by the slant of the cam surface. The cam bar is designed so that two adjacent keys cannot be depressed simultaneously. The motion of the cam bar is imparted to the sector arm which is geared to the emitter finger assembly. The emitter fingers rotate to contact one of the emitter segments. If a key is not depressed, the emitter finger remains in contact with the zero emitter segment.

The digit keys are latched down by a spring-loaded latch bar that engages a formed ear on the front side of the key stem. The latch bar may be moved forward

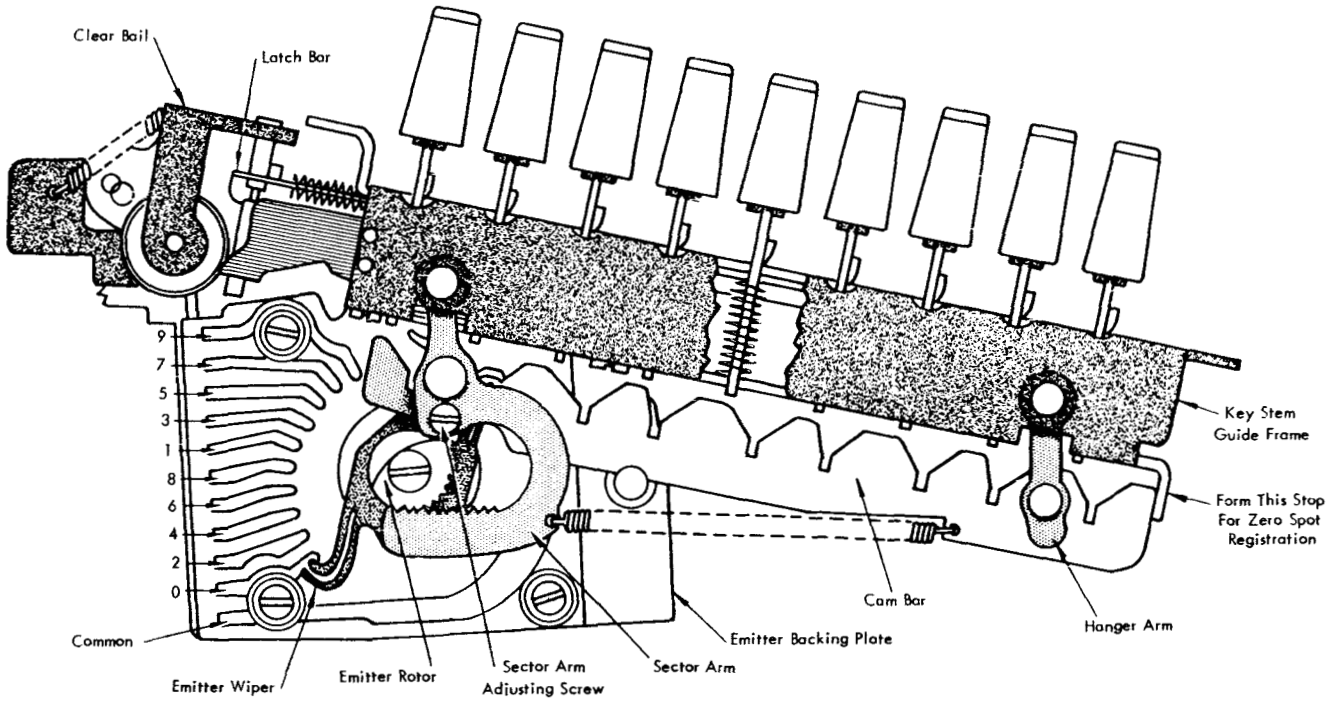


Figure 219. Address Key Bank

to release a depressed digit key by depressing another digit key in that key bank.

Motion to clear a column is imparted to the latch bar by the clear bail.

CONTROL KEY BANK (FIGURE 220)

The control key bank consists of five keys, the inquire key, clear key, and three format keys (1 - 2 - 3). Depressing the inquire key locks the entire keyboard until a pulse is applied to the inquire key release magnet. With the inquire key latched down, the following conditions exist.

1. The clear key is ineffective because the inquiry lockout pawl is in position to interfere with the clear lever.
2. The clear bail is holding the slide bar for each of the numeric key banks toward the rear, thereby preventing any of the keys from being depressed or cleared.
3. The selected format key is locked down.

The clear key operation when the keyboard is not locked is as follows:

1. The clear lever slips by the inquiry lockout pawl.
2. The clear lever pivots the clear bail, forcing the slide bars toward the front of the machine; this frees all of the numeric keys.
3. The control key slide bar releases the selected format key.

Selected Station Type Out

A selected station type out operation is initiated by a program exit impulse wired to one of the remote station hubs on the 305 control panel (Figure 217). The logic of selected station type out is illustrated by Figure 221.

A program exit impulse wired to the remote station #2 hub picks TYPE #1 and initiates a normal console type operation. The same program exit impulse latch picks the remote print relays for station 2 (RP2A, R8616 and R8270). During the first clutch cycle an impulse from the station 2 type exit hub on the 380 control panel is wired to COLUMN CONTROL ON to establish the proper typing format for the remote station. The selection of data from Q track and the pick of the common channel relays is identical to normal console type operation. The SCB-2 impulse that normally energizes a selected console key magnet is transferred by the station switching relay points to the corresponding key magnet at the remote station.

The data from Q track can be typed simultaneously at more than one station by wiring the program exit to more than one remote station type hub on the 305 control panel.

OBJECTIVES:

1. Initiate a console type operation.
   a. Pick TYPE #1 (R8151) (6.04.05).
2. Emit an impulse from the station 2 type hub (6.04.07).

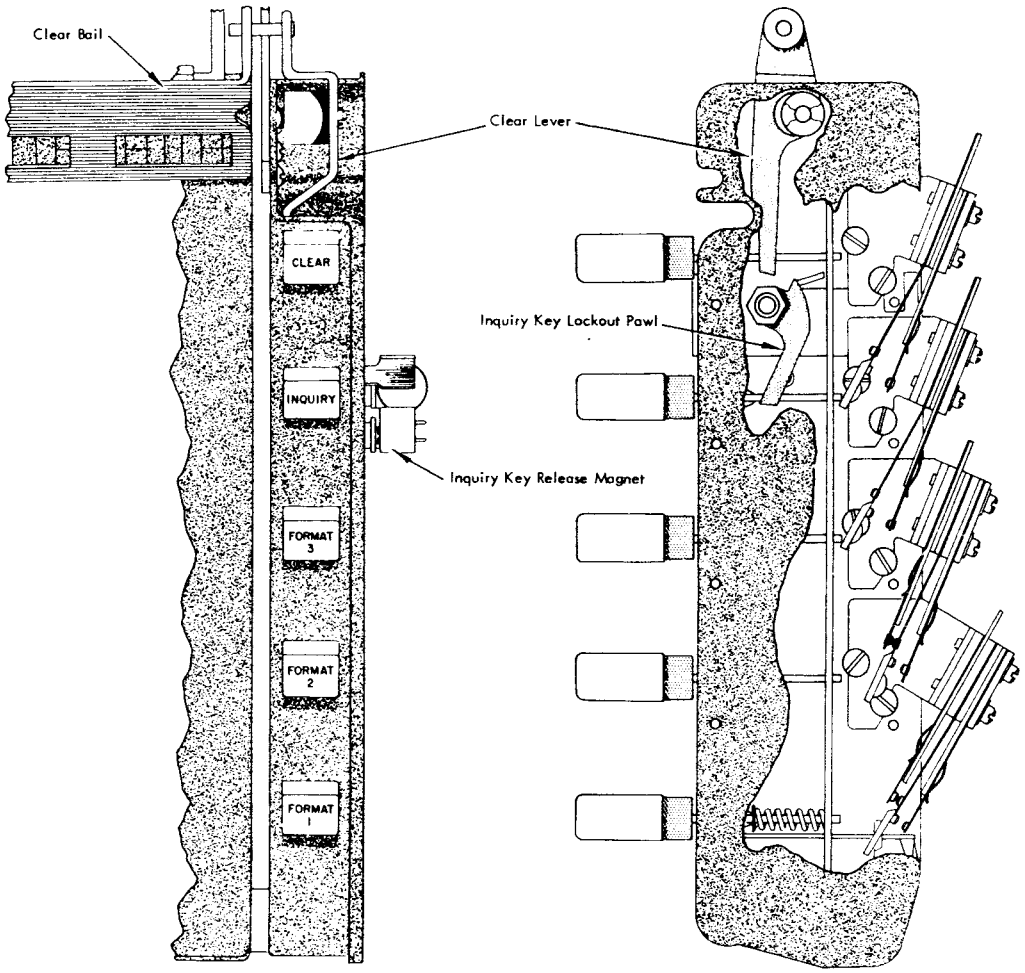


Figure 220. Control Key Bank

3. Energize the station 2 key magnets (6.20.02) (6.14.05).

Inquiry Transfer

Inquiries originating at the console can be directed to any of the remote stations in the console format. Operation is as follows:

1. Depress a format key on the console and wait for the inquiry light to come on.
2. Place the station select switch to the desired station.
3. Depress station select set.
4. Key in the five digit file address.

After depressing the last key, the information from the selected address will type out at the console and the selected station in the console format.

Only one modification of normal console inquiry operation is necessary in order to perform an inquiry transfer. The station switching relays for the station requesting the file data must be picked up before the actual typing of data begins. Under normal inquiry operation, after the format key has been depressed and the INQ ADR relays have been picked the inquiry is suspended until the operator enters the five digit file address. Before the file address is entered, the operator must position the station select switch and depress the station select set key. Depressing the station select set key picks the inquiry transfer select relay for the selected station (6.03.20). The entry of the file address from the console keyboard initiates a servo and file read operation in the normal manner (Figure 212). When the INQ TRF COMP relays are picked at the conclusion of the transfer of data to Q track, the inquiry transfer select relays pick the station switching relays for the selected remote station (6.04.08). With the station switching relays transferred, the data from Q track will be typed out at the remote station as well as at the console.

Remote Inquiry

Note: This discussion is written to "C" level System Diagrams. On later levels the relay designation will be changed from 1XXX to 8XXX.

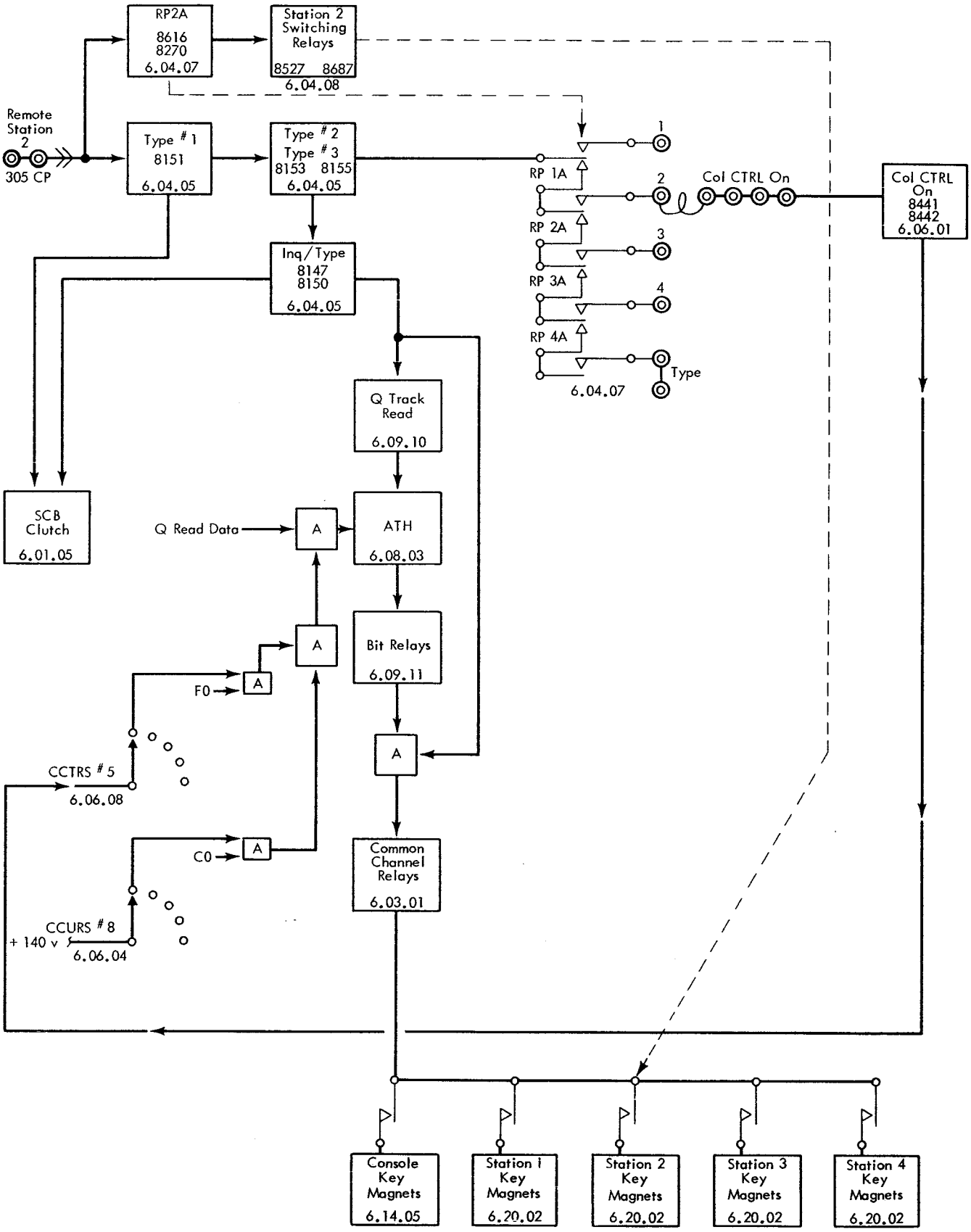


Figure 221. Selected Station Type Out

The Remote Inquiry feature allows direct inquiry from any of the Remote Printing Stations. Normal Inquire On and ITI interlocking are active. The remote inquiry is answered when a program exit impulse enters the inquiry in hub on the 305 control panel. Figure 222 illustrates the logic of remote inquiry operation.

Before the operator at a remote station can initiate an inquiry, the file address must be set up in the remote inquiry address keys and a format key must be depressed. These keys remain in the operated position until they are cleared manually or the inquiry is complete. Depressing the inquire key at the remote station initiates the inquiry operation by picking the KB 1 INQ relay in the 380 console.

In order to allow time sharing of the console inquiry circuits, a station request scanner (SRS rotary switch) is used. The KB 1 INQ relay activates the SRS drive magnet to advance the rotary switch to the position that corresponds to the requesting station. If the same station initiates a second inquiry, the SRS advances through the remaining positions of the rotary switch and checks for requests at the other stations before answering a second request from the same station.

When the SRS reaches the requesting position, a test impulse is directed to the latched format key at the remote station. The test impulse through the 381 format key picks the corresponding format relays in the 380 console and sets up normal inquiry controlling circuits. A program exit impulse entering the inquiry in hub picks the INQ ADDR relays and conditions the console circuits for the entry of the file address.

The INQ ADDR relays activate the PCLRS drive magnet and the SCB clutch. During each clutch cycle the rotary switch advances one position to control the sequential scanning of the address key emitters at the remote station. The #8 wafer of the PCLRS picks the disk tens scan relay which directs a test impulse to the disk tens address key emitter at the remote station. A decoder at the remote station produces an output on four bit lines that corresponds to the numeric position of the address key emitter. The output of the decoder is returned to the 380 console to pick the corresponding supervisory buffer relays under control of the PCLRS. As the rotary switch is advanced to the next position a new scan relay is picked and the process is repeated for the disk units address.

As the PCLRS advances to the sixth position the INQ ADDR COMP relays are picked and normal inquiry operation is resumed. To direct the type impulses to the remote station, the station switching relays are picked by INQ TRF COMP just prior to the actual type out.

OBJECTIVES:

1. Search the SRS to the inquiring station.
   a. Energize the SRS drive magnet (6.03.21).
2. Pick the console format relays to initiate an inquiry (6.04.01).
3. Transfer the file address from the remote keyboard to the supervisory buffer relays.
   a. Energize the SCB clutch (6.01.05).
   b. Pick the scan relays (6.07.08).
   c. Test the remote inquiry address keys (6.20.01).
   d. Pick the supervisory buffer relays (6.05.01).
   e. Advance the PCLRS (6.07.07).
4. Initiate a normal inquiry.
   a. INQ ADDR COMP (6.04.02).
5. Emit an impulse from the station format hub (6.04.07).
6. Pick the station switching relays (6.04.08).

Interlocks

RAMAC READY (REMOTE INQUIRY)

Before a remote inquiry can be made, the RAMAC must be ready to accept the inquiry. The RAMAC is ready when it is in a reset position or when processing. On 6.02.06, if R1381 (RAMAC not ready) is down, the RAMAC ready condition exists. The relay (R1381) will pick through R1044-9 N/C (proc prog reset), and R1043-1 (proc prog stop). When processing, process program stop (R1043-1 N/O) will prevent the pick of the relay. The relay will also be down if the RAMAC is reset (R1044-9 N/C). The RAMAC ready lights at the Remote Stations (6.20.03) will be turned on through R1381-1 N/C (6.02.06). On 6.03.20, SCB5 impulses to the SCB clutch will be prevented through R1381-2 N/C if the RAMAC not ready condition exists.

STATION READY

On a selected station type out operation, the type must not be attempted unless:

1. The typewriter motor for the station is ON.
2. There is paper in the typewriter.
3. The control switch for the selected station is in the RUN position.

In order for the selected station type out to progress, it was necessary to pick the station switching relays. There must be a ground return circuit for these relays to pick. It will be shown that the three conditions listed above must exist, or the ground return for the switching relays will be open.

1. On 6.04.08, the ground side of the switching relays goes to 6.04.11. R8539 must be up to complete the ground circuit.
2. The station 2 ready relays (R8539, etc.) are picked through R8217-2 N/C (form stop) on

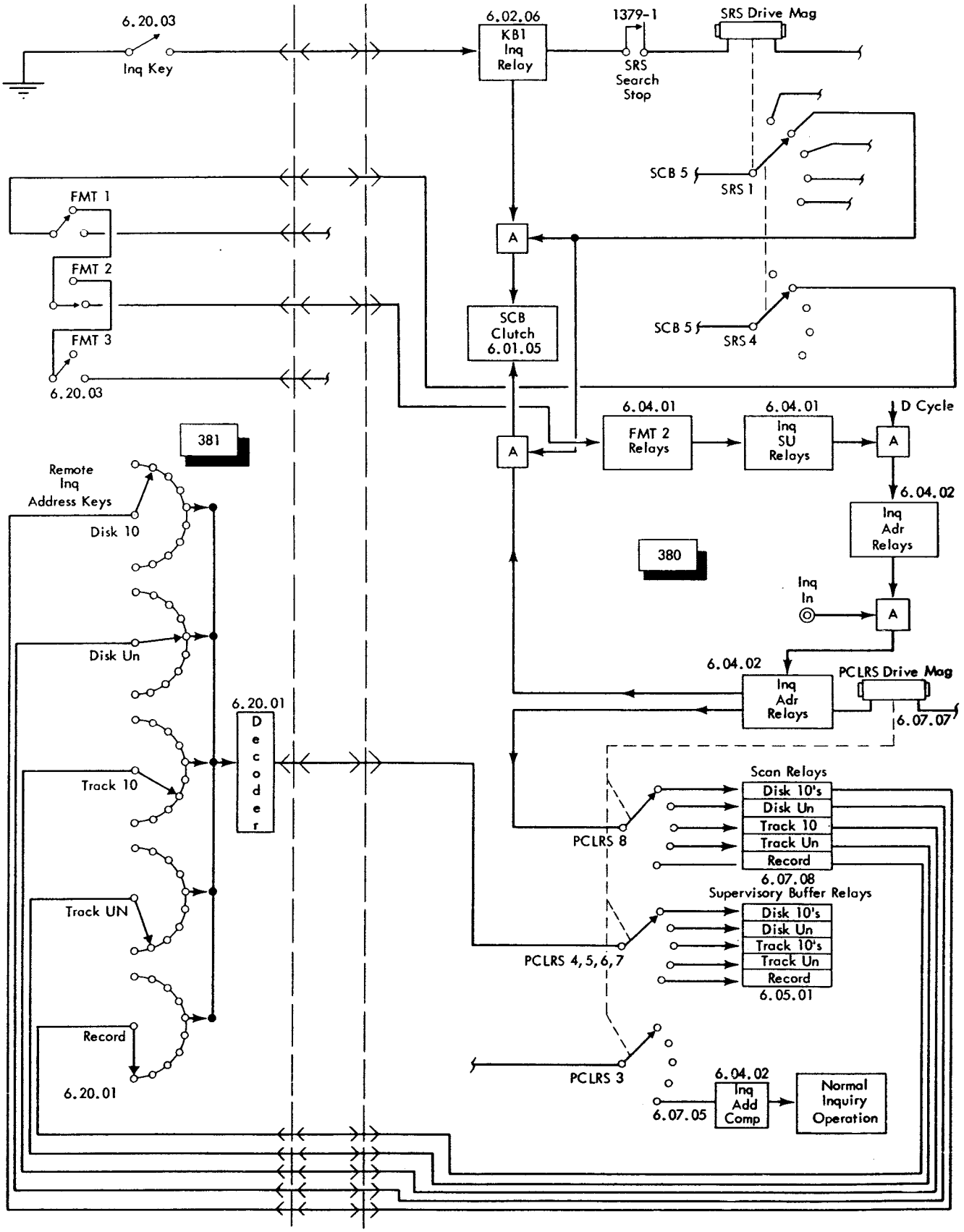


Figure 222. Remote Inquiry

6.04.09, to 6.20.03, through run-stop control switch in RUN, to the 40v DC supply.
3. The input to the 40v DC supply is the 115v AC that is across the typewriter motor.

If the station is not ready, the following conditions should occur:

1. Program should stop.
2. The interlock light should be ON.
3. Select light corresponding to the not ready station should "blink."

On 6.04.07, the impulse to the remote station hub will go through R8539-1 N/C (RP2 Ready) through D1097 to the program stop hub on the 305 control panel (1.02.09).

On 6.04.11 the remote printer interlock relay (R8379) will pick through the ground circuit supplied by D1219, R8616-3 N/O (RP2A), and R8539-2 N/C (station ready). The clutch interlock relay will open the SCB clutch circuit (6.01.05) preventing subsequent clutch cycles. On 6.04.10, the interlock light will come ON through R8379-12 N/O (RP interlock). The select station 2 neon will turn ON through R8616-4 N/O (RP2A) and R8253-3 N/C (RP2 ready). The 2 Meg resistor and .22 μf capacitor and the neon form a relaxation oscillator whose frequency is approximately 3 cycles/second. This causes the neon corresponding to the not ready station to blink.

Once the interlock condition described above is encountered, the operator has three options:

1. Perform a clear operation with console control switch ON. However, this will cancel type out of that data.
2. Turn run-stop control switch to STOP and correct the situation at the remote station (forms, switches, plugs, etc.). Type out will commence immediateiy. Depress the program start key at the console to resume operation.
3. Press the type release button on the console. The attempted type out will occur at the console. Depress the program start key to resume operation.

TYPE RELEASE

Depression of the type release button will cause a type out of the selected information at the console and release the interlocks on the machine.

1. On 6.04.07, the type release switch (SW15A) will latch pick type release relay (R8385) and console type A relay (R8536). R8536 will set up the pick to the console switching relays.
2. On 6.04.11, R8385-2 N/C will cause the RP interlock and clutch interlock relays to drop on the next SCB cycle.
3. On 6.01.05, R8385-3 N/O bypasses R8494-1 N/C (clutch interlock) and releases SCB clutch.
4. The selected information will type out at the console because the console switching relays are up.
5. On 6.02.06, the type release switch shorts out all carriage return and tab contacts and will release any tab or carriage return interlock conditions.

TYPE CHECK (selected station program type out only).

If a parity error is detected in the Q track data relays, a type check should occur. The type check neon should turn ON and subsequent transfers to Q track should be prevented.

1. On 6.09.01 a Q track parity will latch pick the type check relays (R8378, R8382). On 6.04.10 the R8382-3 N/O point turns on the type check light.
2. On 6.04.11 the SCB 3 impulse will pick the RP interlock (R8379) and the clutch interlock (R8494).
3. On 6.04.07 the latch trip of the remote station select relays is prevented.
4. On 6.04.10 the R8382-4 N/O point keeps the typewriter not ready line high, preventing a W cycle gate when T = Q.
5. Type release will release this interlock.

A type check interlock should also occur if the typewriter loses power during a program type out. The type check condition will not be recognized until the clear occurs. The station ready relays are picked with the 40v supply from the Remote Printing Station and the presence of this supply indicates typewriter power. If power is lost, the station ready relays will drop. This will open the ground to the station switching relays to prevent key piling (6.04.11). The N/C point of the station relay supplies a ground return for the latch pick of the station not ready relay (R8541) on 6.04.11. The R8541-1 N/O points pick the type check relays on 6.09.01 and the machine is type check interlocked.

FORMAT CHECK (Remote Inquiry)

If an operator fails to unlock the inquiry keyboard, or fails to depress a format key, the system should not respond to a remote inquiry. This is accomplished by impulsing the inquire key release magnet if either of these conditions exist.

1. The keyboard must be unlocked and a format key depressed (6.20.03) before a format "A" relay can be energized (6.04.01).
2. Failure to pick a format relay will result in not picking R1336 on 6.04.01.
3. The format check relay (R1337) will pick on 6.03.20 through R1336-1 N/C.
4. When the search to the selected station is completed, the inquiry key release magnet is ener-

gized (6.20.03) to 6.03.21, through R1337-X N/O (FMT check), R1379-4 N/O and R1336-3 N/C.

CONSOLE INTERLOCKING (Remote Inquiry)

If an error occurs at a Remote Station preventing the completion of a remote inquiry, the console operator must be able to clear the affected station at his discretion. This is accomplished by turning the console control switch ON. On 6.02.06, the switch will pick R1380 (console control). On 6.03.21 a search to the console position is initiated through the SRS interrupter contact and R1380-2 N/O. On 6.02.03 the clear key is activated through R1380-1 N/O and SCB-5.

The test lock is interlocked through the console position of SRS-8-11 (6.15.04).

Program load is also a console operation. In order to start an operation with the program load button, the circuit must be operative with + 48v through SW14A N/O (6.03.21). When the console control switch is turned on the SRS rotary switch advances to the console position and provides + 48v through SRS 7-11 and SW14A N/O (6.03.21) to SW5A N/O (6.04.12).

Decision Elements

The decision elements in the RAMAC system are as follows:

1. Accumulator sign.
2. Accumulator overflow.
3. Compare.
4. Field compare.
5. Blank transmission test.
6. Character selector.
7. Selectors.
8. Cycle delay.

Each of these decision elements has a special purpose selector with hubs on the 305 control panel. The selectors are tested with a program exit impulse at a predetermined point in the program routine. The status of the selector, whether normal or transferred, determines what the system will do next.

The first two of these decision element selectors, accumulator sign and accumulator overflow, are discussed in the Arithmetic section (Section 11) under "Accumulator Sign Control."

Compare

The compare feature is probably the most frequently used of the decision elements. In addition to its function as a source of logical decisions, this feature is often used by the programmer as a safeguard to prevent any possibility of obtaining and altering the wrong file record.

There are three types of compare operations, each of which is activated by the inclusion of a particular Q instruction. The three types of compare operations are illustrated below:

1. It is desired to determine whether the data in character positions 37-43 of track W is the same as the data in character positions 81-87 of track Y. The following instruction may be used: W43Y8707$1.

The Q instruction of "1" changes this program instruction from a transfer of data to a comparison. The P instruction causes the I, R, and W cycles to be followed by D and P cycles. It also causes an impulse to be emitted from the "$" hub on P cycle.

This impulse may be used to test any of the compare hubs (3.03.05).

2. It is desired to determine which fields of track X are equal to the corresponding fields of track A. The following instruction may be used: X99Z9900&2.

The Q instruction of "2" causes each field of track X to be compared with the corresponding field of track Z. Two sets of field compare hubs (3.03.04) are associated with each field. The field compare hubs are conditioned to indicate the result of the comparison within each field. After a compare operation, the state of the compare relays will not be altered until the next programmed comparison.

3. The programmer desires to compare the fields of track X with the fields of track Z, as in the preceding example. He also desires an indication of the equal or unequal condition of the two tracks taken as complete units. This requires a combination of two types of comparisons mentioned above, and is accomplished by using a Q instruction of "3," as in the following program instruction: W99Z9900P3.

With this instruction, the compare hubs (3.03.05) are conditioned to indicate the equal or unequal relationship between the two complete tracks, and the field compare hubs indicate the equal or unequal relationship between the individual fields.

Compare (Q = 1)

The instruction W43Y8707&1 will cause the following objectives to take place:

OBJECTIVES:

1. P flag causes D and P cycle with an impulse from "&" hub on P cycle.
2. W data from T_1 address to compare circuits on W cycle.
3. Read data from T_2 address to compare circuits on W cycle.
4. Pick R31 if unequal occurs.

D, P Cycles: D cycle is initiated, following W cycle by the P = not blank line. During P cycle the "&" program exit hub will emit an MR7 impulse (2.05.03) to test the compare selector.

W Data: The data from the T_1 address was placed in cores on R cycle. Then on W cycle it enters the compare circuits on 3.03.01 as W data.

Read Data: On a Q = 1 operation a special circuit is necessary to provide read data from the drum read matrix during W cycle. Normally this would be a write operation. The matrix write gate is blocked on 3.02.09 by the not Q compare line being low. The T_2 address selects the desired head. With the matrix write gate low the matrix circuits are conditioned for reading (see "Track to Track Transfer").

Pick R31: All compare hubs on 3.03.05 are conditioned by R31 points. R31, if previously energized, will be dropped out at I cycle end of a compare instruction at thyratron 3K5 on 3.03.01. During the W cycle gate, a difference between W data and read data will fire thyratron 3J6 through AI 3G6. This picks R31, which will remain up until another compare instruction.

Field Compare (Q = 2)

The table beneath the field compare hubs (3.03.05) shows that a separate relay is employed to condition the hubs for each field. These relays are energized on 3.03.02, with an individual thyratron for each relay. Each of the thyratrons receive + 70 volts through its respective relay on the line labeled P pick.

OBJECTIVES:

1. Drop all field compare relays on R cycle of compare operation.
2. Pick specific field compare relay during W cycle if unequal is detected.
3. Hold relays until next compare operation.

Field Compare Relays: On 3.03.02 the relays are held by field compare hold to the normally closed points of MR11 on 2.09.11. MR11 is energized on 2.09.02 at the start of R cycle on a compare operation and dropped at F4 of W cycle.

Pick field compare relay: Each of the ten thyratrons on 3.03.02 is conditioned by a field gate. An unequal condition existing between read data and W data on 3.03.01 will appear on the not compare line and pick the required field compare relay. The read data and W data are gated to the compare circuits on W cycle just as they were for Q = 1. P pick must be high during this W cycle to enable the thyratrons to fire. It is supplied through the normally closed points of MR1 on 2.09.10. MR1 will pick and open P pick at F6 of D cycle if P is not blank (2.09.01) and drop out at F4 of P cycle. Therefore it will be normal on a compare operation until after W cycle, at which time the field compare hold will be established.

The field compare feature may be used to compare a group of fields of the T_1 track to a different group of fields of the T_2 track. This may be illustrated with the instruction X59Z9960&2 which will cause a comparison between 6 fields. Fields 5, 4, 3, 2, 1, and 0 of track X will be compared to fields 9, 8, 7, 6, 5, and 4, respectively, of track Z. The result of the comparison will be indicated in selectors 9, 8, 7, 6, 5, and 4.

Compare and Field Compare (Q = 3)

A program instruction that has a Q instruction of "3" will cause triggers 2X10 and 2Y10 (2.06.00) to be turned ON. Since trigger 2Z10 will be OFF, the gates Q = 1 and Q = 2 will both be available from the special instruction register. With Q = 1 and Q = 2 both high, the compare and the field compare operations will both be accomplished on one program step.

Blank Transmission Test (Q = 6)

The blank transfer hubs are located on 3.03.05. From the chart on 3.03.05 it can be seen that a blank transfer has occurred if relay 30 is up. The blank transfer selector can be picked or dropped only during an instruction with a Q = 6. A test of W data is made during a Q = 6 instruction. If anything except bit 0 or bit R occurs, the transfer was not blank and relay 30 will be down. If the W data contained only bit R's or Bit 0's, a blank transfer has occurred and R30 will be up.

At I cycle end of a Q = 6 instruction, 3Q6 on 3.03.03 is set 3 pin high and 3M6 is fired, dropping R30. If 3N6 conducts, R30 will pick and a blank transmission will be indicated (3.03.03). If 3Q5 conducts, 3Q6 will be pulled 3 pin low and 3N6 cannot come up at W cycle end. 3Q5 conducts only on a transmission which has bits other than BR or B0 as W data. If only BR or B0 occurs as W data, 3Q5 will not conduct and 3Q6 will remain 3 pin high. 3N6 will conduct at W cycle end. This will pick R30 and indicate a blank transmission.

Character Selector

One of the most powerful decision elements within RAMAC is the character selector. This unit permits the selection of a particular routine from among several

possible program branches. These may be illustrated by the following instruction: K05-9901&b.

In the area of inventory control and billing, a particular program might require the processing of several different types of cards. Column 6 of the card might be reserved for a code character to identify the type of transaction which that card represents. The first step in the processing of each new set of card data could employ the following instruction: K05-9901&b.

The character "-" (hyphen) in the T_2 position would cause the code character in the 05 position of track K to be stored in the character selector relays. If the program exit from the & hub is wired into the character selector in hub (3.04.03), the out hubs might be wired as follows:

"A"—This card represents items ordered by a customer. Wire to program advance.

"B"—This card represents items returned for credit by a customer. Wire to program 50.

"C"—This card represents merchandise received to replenish stock. Wire to program 75.

"D"—This card represents price changes to be stored in item records. Wire to program 85.

"E"—This card represents a remittance received from a customer. Wire to program 95.

"F"—This card represents an alteration in customer's maximum credit allowance. Wire to program 105.

"G"—Etc.

In addition to the set of hubs on 3.04.03 which indicates actual alphabetic, numeric, or special character identification, the character selector also includes three standard and three optional sets of hubs on 3.04.04 and 3.04.06, which indicate the Hollerith elements that comprise the selected character. As an optional feature three positions each of "X" "no-X" bit and "0" "no 0" bit selection may be added to the function of the character selector. These selectors allow analyzing of a character for the presence or absence of X or 0 bits.

To enter a character into the character selector, T_2 must be "-" (hyphen) and MN must be 01. Although not essential, A_2B_2 should be 99 to allow maximum pick time for the character selector relays.

The character selector relays are energized by the six thyratrons on 3.04.01. P pick, which is MR1 N/C, applies + 70 volts through the character selector relays to the thyratron plates during W cycle. Since each of the relays has a particular bit value, the screen grid of each thyratron receives a particular bit pulse from the bit ring. Data to "-" is applied to the control grids.

Data to "-" is obtained on 3.02.12 at 3T8 from W data anded with T = "-" and ∅C's.

The hold circuit for the character selector relays (3.04.01) is supplied through the normally closed points of MR3 on the line labeled "-hold" (2.09.10). MR3 (2.09.01) is energized at the leading edge of R cycle when T_2 = "-" to F4 of W cycle. This drops all relays and then holds the new relays before their points are tested on P cycle.

Selector

The 305 control panel has hubs for ten standard and additional optional selectors. Each selector has two sets of points, with a common, normal, and transfer hub for each point as indicated on 2.08.03.

Latch type relays are used and there is a pickup and drop out hub for each selector. In addition there is a reset hub for each group of ten selectors. It can be seen on 2.08.04 that an impulse into the reset A hub picks R213. The points of R213 then apply + 48v to latch trip all relays of selectors 1 through 10.

Cycle Delay

It is frequently desirable to test the points of a selector and then to drop that selector (or pick it) before continuing to the next program step. If the same impulse which tests the selector is wired to the PU or DO hub, several ill effects would result. The state of the selector would be altered in the midst of the impulse wired through its points; hence, a fragment of the impulse would be emitted from the normal point and a fragment from the transferred point. This could cause an invalid program level to be stored in the program counter. The cycle delay unit provides a means of testing a selector and then dropping it (or picking it) 30 milliseconds later.

Figure 223 illustrates a typical application of the cycle delay unit. A program exit impulse tests a selector and, if the selector is transferred, it is desired to drop the selector as well as to set the program counter at the necessary level. In the event that the selector is transferred, the impulse passes from the transferred hub into the cycle delay in hub.

This causes an impulse to be emitted from the cycle delay out hub 30 milliseconds later. The cycle delay exit is wired to the DO hub and through a distributor to the desired program level.

The process unit control panel has 15 standard cycle delay positions. An impulse into a particular IN hub on 2.08.05 causes an impulse from the corresponding OUT hub on 2.08.06.

The cycle delay relays are arranged in binary fashion so that only four relays are needed to receive the inputs from 15 hubs. Four additional relays are needed to provide the impulse from the corresponding OUT hubs. For this reason the cycle delay selectors can be used to add binary numbers. For example, impulsing both delay 1 and 4 will result in an impulse from the cycle delay 5 exit hub on the second P cycle.

The cycle delay operation involves four mercury relays whose timings are shown on 0.09.04. It should be remembered that all control panel impulses are provided by MR7.

OBJECTIVES:

1. Store program exit impulse in cycle delay relays.
2. Cause D, D, P cycles to follow P cycle.
3. Impulse from cycle delay exit hub on second P cycle.

Store Program Exit Impulse: Using the sequence chart and control panel wiring in Figure 223, R101 and R102 will be picked on the first P cycle by the program exit impulse (MR7).

D, D, P cycles: The not new program line remains high since no impulse reaches a program entry hub or a program advance hub (2.01.06). This results in two D cycles followed by a P cycle.

Cycle Delay Exit: Relays 107 and 108 are picked during the second D cycle through the R101 and R102 points. On the second P cycle the R107 and R108 points allow an MR7 impulse at the cycle delay out hub. This impulse, if wired to program entry will raise the new program line (2.01.06) and allow cycling to advance.

Program Exit Split (optional)

Operation

The double program exit hubs can be split and placed under selector control, so that either the upper hub or the lower hub (but not both), will emit the corresponding program exit impulses. See Figure 224. This feature is divided into two groups: program exit hubs A-Z make up the first group, and program exit hubs 0 (zero) through 9, and special characters make up the second. The operation of this device consists of impulsing either the U (upper) or L (lower) pickup hubs (located in control panel positions C, 23-26) with a program exit, or similar impulse. If the upper

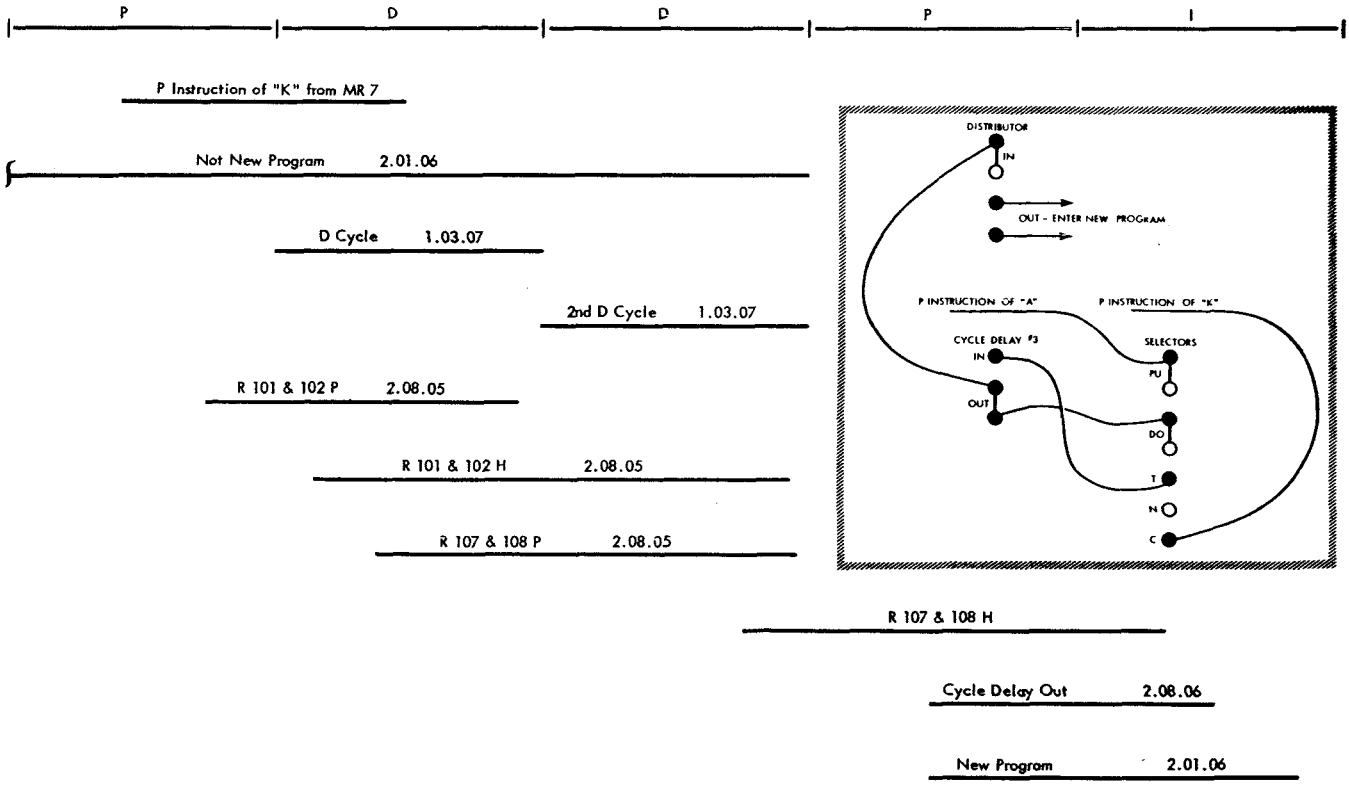


Figure 223. Cycle Delay

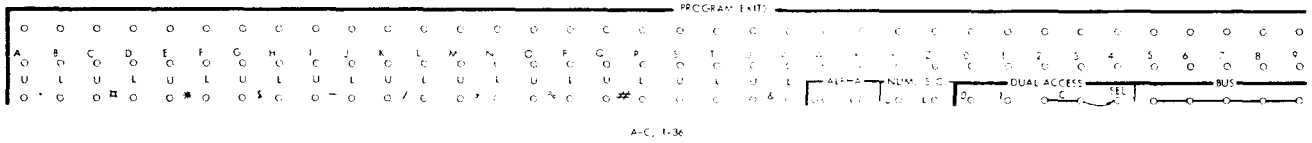


Figure 224. Split Program Exit Hubs

hub is impulsed, the corresponding program exit hubs of this group will emit until the lower hub is impulsed. If the lower hub is impulsed, the lower row will emit until the upper hub is impulsed. At the beginning of a job, a start, or similar impulse should be used to set up the group of exits desired. Reset and check reset have no effect on which exits are set up to emit. Two console neons, one for each group, indicate when the upper set of program exits are active. They are located just above the cycle neons.

Description of Circuits

System Diagram 2.05.03 indicates that when relays 82, 85, and 88 are deenergized the upper program exits are active. Control of these three relays (which control the first group of double program exit hubs) is accomplished on System Diagram 2.05.05. Relays 82, 85, and 88 are picked by an MR 8 line after R95 is latch picked. Relays 82, 85, and 88 remain held and the lower program exits are active until after R95 is latch tripped. The second group of program exits are controlled similarly.

340 Power Supply

The power input to the type 340 power supply must be from either a 208 or 230 volt, three phase, 60 cycle, four wire service. Variations from this input can be ± 10% for voltage and ± ½ cycle per second for frequency. All AC and DC power for operating the RAMAC 305 is obtained from the 340 Power Supply except the file power, compressor, and access motors. The 340 does not use three phase power as such, but arbitrarily distributes voltages to various loads which are not necessarily balanced across the phase lines.

340 Voltages

The AC voltages supplied by the 340 and the purpose of each is listed below:

1. Unregulated line (208 vac-230 vac)	Drum motor, drive motors for 370, 323 card reader, typewriter and 382, blower motors.
2. Regulated 230 vac (ACLR 1 & 2)	File filament transformer, file blower motor and flood lights.
3. 6.3 vac	305 tube filaments.
4. 115 vac	convenience outlets, AC sequencing circuits.

The DC voltages supplied by the 340 are listed below:

1. +270 vdc +140 vdc	electronic circuits.
2. +70 vdc	thyratron plate supply.
3. +48 vdc	relays and lights.
4. −60 vdc,−250 vdc	electronic circuits.
5. −250 vdc reset	reset of triggers.

File Voltages

The 340 power supply provides + 270v, + 48v, + 140v, − 60v, and − 250v to the 350 file (s). The − 250v and + 270v are used to develop 3 regulated DC voltages within the file, + 215v, + 140v and − 210v, for use in the track and disk null detector circuits. Regulated 236 vac is also sent to the file for the tube gate blower motor, the flood lights, and to develop 6.3 vac filament voltage. The floating power supplies in the file are driven solely by the 6.3 vac. All other file motors (access, compressors, compressor blowers) are supplied 230 vac from the line cord on the remote compressor cabinet.

Control Functions and Monitoring

The power supply is normally operated by the remote controls at the console. It can also be operated by a set of controls at the rear of the 340. The following push buttons are used:

On the Console	*On the Power Supply*	*Purpose*
MASTER POWER OFF	IMMEDIATE OFF	Remove all power instantaneously.
POWER ON	POWER ON	Initiates normal cycling up sequence.
(Use POWER ON button)	DC ON	Re-establishes all DC voltages
POWER OFF	POWER OFF	Initiates normal cycling down sequence.
DC OFF	DC OFF	Removes all DC voltages.
	RESET	Removes blown fuse or electronic gate thermal trip condition.

The immediate off button cuts off all power instantaneously regardless of sequencing, and should be used only in an emergency. The reset button removes the blown fuse or the electronic gate thermal trip condition. It will not reset the process unit.

In addition to the above controls, a DC off toggle switch and a DC on push button are mounted on the CE sync panel. The toggle switch may be thrown to cause a DC off sequence. With this switch transferred, the power on and the DC on buttons are inactive. The toggle switch must be returned to the normal running position before DC can be reapplied.

Meters

There is an AC and a DC voltmeter located on the power supply panel. A selector switch is provided for each meter. The switch not only selects the proper input, but also selects the proper range.

The AC meter measures the input voltage across each of the three phase lines and the output voltages of both AC line regulator transformers. It is a 167 ohm per volt meter with a range of 0-300 volts.

The DC volt meter measures the output of the DC regulators for each of the DC supplies. The ranges for the meter are 0-150 and 0-300 volts.

Phase Sequence

The sequence of phase rotation at the power input terminals must be 3, 2 and 1 on lines 1, 2, and 3

respectively. A resistance-capacitive network monitors this sequence and causes the AC sequence light on the 340 panel to glow brightly when the sequence of rotation is correct. The improper sequence will cause the light to be very dim or out. When the sequence is wrong, there is an unbalanced current distribution across the individual phases. This unbalanced condition has no noticeable effect on the RAMAC system.

The following chart shows the variations in current load for both sequences:

	No Load	*Correct Sequence*	*Wrong Sequence*
Phase 1	28.7 Amps	33.5 Amps	25.8 Amps
Phase 2	33.8 Amps	36.0 Amps	43.2 Amps
Phase 3	29.5 Amps	34.0 Amps	36.0 Amps

Blower Timer

The electronic panel blowers should continue to run for 3 to 5 minutes after the machine power is turned off. A timer motor on the power supply panel starts after all voltages have been removed from the RAMAC system by a depression of the power off button.

The time required to open the normally closed timer micro-switch contacts is controlled by the time dial setting on the front of the timer. Each dial division is equal to 30 seconds. The timer is spring reset when the blower timer motor is de-energized.

Regulation

The AC voltage regulators are step-up type transformers, whose outputs are used as filament transformer inputs. The primary windings of the voltage regulators are non-saturated inductors. In normal transformer operation, changes in primary voltage are reflected as changes in secondary voltage due to the changing magnetic lines of force or flux density. The voltage regulators use the saturable reactor principle of a saturated core for the secondary winding.

When the core is saturated, there is little or no change in the lines of force (flux density) across the coil. An inductor operating at saturation maintains a nearly constant magnetic flux density through a comparitively wide variation in current flow, and therefore maintains a nearly constant voltage across its output terminals.

The ACLR 1 and 2 saturable reactors are shown on 9.04.01 and 9.04.02. The capacitor and the secondary winding form a resonant circuit which will cause saturation of the secondary core. Up to 500 volts AC may appear across the secondary winding. The secondary is tapped to provide 236 vac.

All eight DC power supplies also use saturable reactors for voltage regulation. In addition, a buck-boost transformer is used on the output of the secondary (for example, T9 on 9.05.01). This transformer takes an increase or a decrease in secondary voltage, transforms it to a bucking or a boosting current, respectively, and couples it back to the secondary.

The primary windings of the AC and DC regulators have tapped windings to provide for either of two input voltages (208 or 230 volts). Design requirements dictate the actual arrangement of the secondary windings on the reactors.

The regulation of the AC regulators is $\pm 3\%$ for input voltage variations of $\pm 10\%$. The regulation for the DC power supplies is generally $\pm 1\%$ for the input voltage variations of $\pm 10\%$.

Adjustment of DC Levels

The output voltage may be adjusted over a range of $\pm 10\%$ of input voltage. Initially the variac is adjusted until a nominal voltage, as stated on the meter caibration chart, is read on the DC meter. The DC loads will vary according to the type of operation performed by the machine at any given instant. Thus, the DC voltage must be set initially and checked periodically under specified machine conditions. (These are covered in the 305 CE Reference Manual.)

Sequencing

The 340 sequencing circuits are both AC and DC, therefore extra care should be used when servicing this equipment. Heavy duty AC contactors must be used to supply AC power to the various motors, to the DC power supplies and the filament transformers. The energizing of these contactors is controlled by a group of standard 48 volt duo relays. The contactors, K1 to K8 are listed on System Diagram 0.46.01 and the duo relays, 1 to 32, on 0.46.00. For discussing all sequencing circuits the function charts on System Diagrams 0.43.00, 0.43.01 and 0.43.02 will be used.

Power On

When either the 340 or the 380 power on button is depressed the indivdual machine components must receive power in a definite sequence to prevent damage to circuitry or overloading of the line. The function chart for this sequence is shown on 0.43.00.

OBJECTIVES:

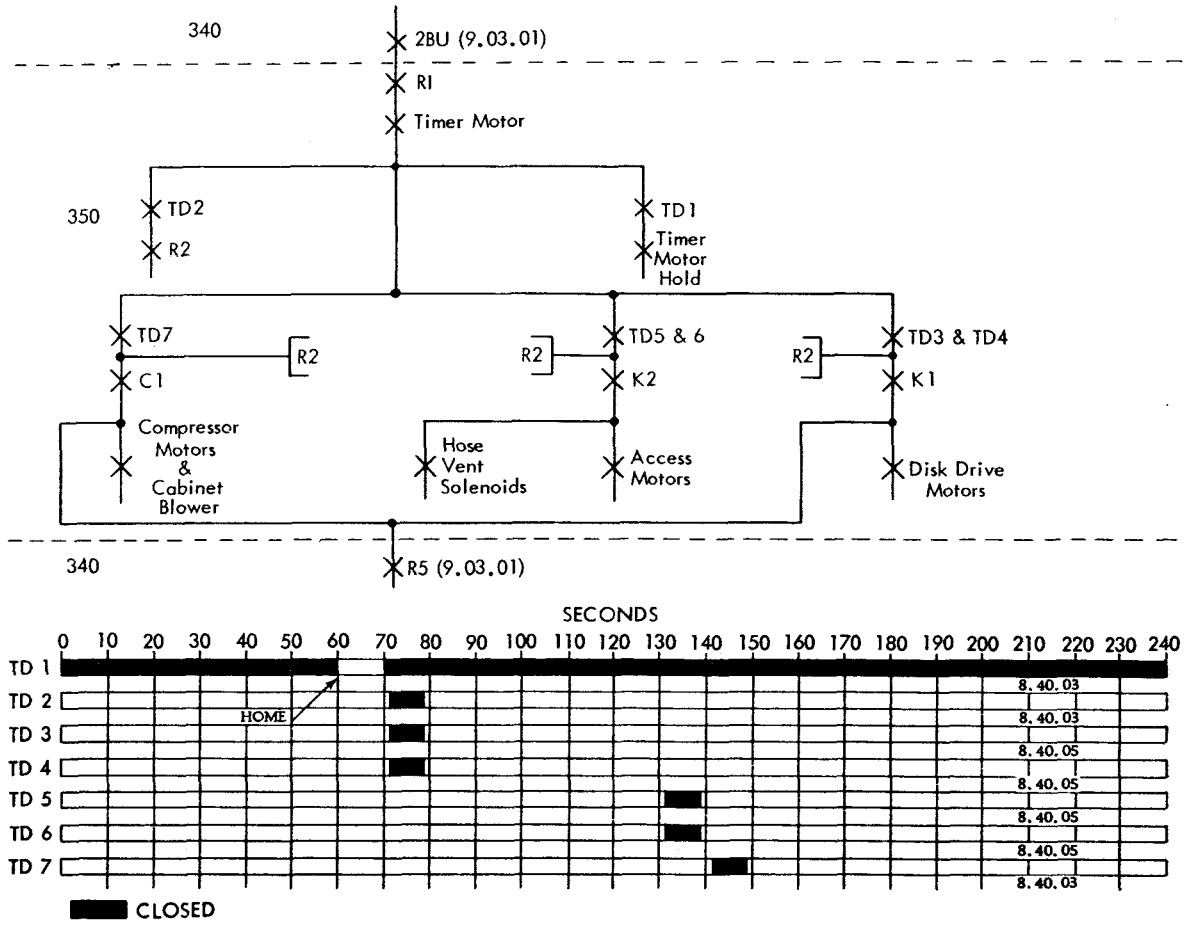
1. Depress power on switch (9.02.02).
2. Power to AC and DC sequencing circuits, K2 (9.03.03).
3. Start file power on sequence, R1 (9.03.00).
   a. Start file timer (8.40.03).
   b. Start disk drive motor (8.40.06).
   c. Start access motors and hose vent valves (8.40.06 and 8.40.05).
   d. Start compressor motors and compressor cabinet blowers, C1 (8.40.04).
4. Start 305 sequencing, R5 (9.03.01).
5. Blowers on, K4 (9.01.03).
6. Drum and unregulated AC, K1 (9.01.02).
7. Filament build up for 30 secs, K7 (9.01.01).
8. Full filament for 30 secs, K8 (9.01.01).
9. Negative DC on, K3.
10. Plus DC on, K6.
11. −250 vdc reset on, R3 (9.05.01).
12. Ready light, R3 (9.03.02).

File Power On Sequence: This sequence is controlled by the timer located in the compressor cabinet sequence control box (8.40.03). The function and timings of the seven TC contacts are shown in Figure 225. These contacts test the file remote local control switches (8.40.05) and compressor remote local switch (8.40.03). If set to REMOTE the motors will start during the power on sequence. On LOCAL or OFF the file motors or compressor motors will be bypassed. The file sequence complete circuit, labeled INTLK also is conditioned by these switches, checking C1 and K1 only if the control switches are on REMOTE.

For dual file operation the TC contact timings are changed to start disk motor 1 sixty seconds before disk motor 2 to prevent loading of the line. For dual process there is still a single timer located in the master compressor cabinet. It is energized by a power on sequence from either 340.

DC Off Sequence

When servicing the RAMAC it is often desirable to remove all DC voltages. The function chart for this operation is on 0.43.01.



NOTE: Chart shows single file installation timing. For dual file retime TD1, TD2 and TD3 to make 60 secs earlier.

Figure 225. File Power On Sequence

OBJECTIVES:

1. Depress DC off switch dropping R4 (9.03.01).
2. Remove -250v reset voltage, R3BL (9.05.01).
3. Remove all positive voltages, K6 (9.02.01).
4. Remove all negative voltages, K3 (9.02.01).

The DC voltages will remain off after the DC off switch is released since R4 can only be repicked through R5BL. R5 has no hold circuit. Notice that R3 on 9.03.01 will drop if any DC voltage is lost. This also initiates a DC off sequence.

DC On Sequence

If a DC off sequence was initiated by the DC off toggle switch on the CE panel (9.03.01), this switch must be returned to normal before any DC on switch is operative.

OBJECTIVES:

1. Depress any DC on switch, picking R5 (9.03.01).
2. Positive voltages on, K3 (9.02.01).
3. Negative voltages on, K6 (9.02.01).
4. -250v reset line high, R3BL (9.05.01).

Power Off Sequence

Depressing either power off switch (9.03.01) will remove all AC and DC from the RAMAC. As in a DC off sequence the positive DC voltages will be removed before the negative DC voltages with the exception of the -250v reset voltages. When the filaments go off, a timer motor in the 340 is started, (9.02.01) opening the TC1 points 3 to 5 minutes later. These normally closed points keep the blowers in operation. The points are spring reset as soon as the timer motor is de-energized. The function chart for this operation is on 0.43.00.

DC Fuse Blow and Restore

The function charts are on system diagram 0.43.01. If any DC fuse blows the indicating plunger makes contact on an alarm bar picking R30 or R29 (9.05.06). Either relay picking will latch pick the AC and DC fail relay, R26, (9.03.02) which turns on the fuse light and initiates a DC off sequence. Also, a loss of any DC voltage without a blown fuse will latch pick R26, turning on the fuse light.

To restore power after the fuse light is on, the defective fuse (if one exists) must be replaced. Then the reset button (9.03.02) must be depressed to latch trip R26. The DC on button may then be depressed.

AC Fail Sequence

There are four types of AC failures which will initiate a power off sequence. The function chart is on 0.43.02. The four failures are:

1. File failure.
2. Blown AC fuse.
3. Filament supply failure.
4. Closing of the thermal circuit breakers in the electronic gates.

In all cases the power off sequence will proceed as normal, however, K2 will remain energized on 9.02.02 through the 2AU N/O points. This will provide + 45 volts to the DC sequencing circuits and for the power on and fuse lights.

File Fail: Relay 4 and 6 are dropped on 9.03.01 when the file interlock circuit is opened. This circuit tests the condition of the K1 contactor (8.40.06) and the C1 contactor (8.40.03). These contactors will drop if the thermal in the disk motor (shaft) opens or any of the thermals for the compressor cabinet motors open (8.40.04).

Blown AC Fuse: Any of the indicating AC fuses will pick one of six relays (R20, R21, R22, R23, R24, R25) if it blows. This drops relay 1 initiating the power off sequence (9.03.01).

Filament Failure: Failure of either filament supply will drop R29 (9.04.01) or R28 (9.04.02). These relays in turn drop R1 (9.03.01).

Thermals: The three thermal points in the 305 tube gates can drop R7 if overheating causes them to open (9.03.01). The R7AL points will drop R1.

In all cases above R26 must be latch tripped with the restore key before power can be restored to the system.

Immediate Off

The immediate off switch on the power supply panel, or the master power off switch on the console are to be used only in case of emergency. Operation of either switch (9.02.02) will pick K5 by removing L1 from the B side of this contactor. The K5 points energize the shunt trip coil in the main CB on the 340 (9.01.01) and the shunt trip coil in the main CB in the compressor cabinet (8.40.03). This removes all AC and DC power immediately. These two CB's must be manually reset before power on is effective.

Servicing

Extreme CAUTION should be exercised when servicing or inspecting the power supply. Dangerous voltages are present at various points within the power supply, even when the machine is in a power off status. If it is necessary to make a test instrument connection within the power supply, or to reach into it for any reason, the commercial power input should be disconnected.

Servicing Aids

Several self-contained servicing devices have been incorporated in the RAMAC. The ability to effectively use these devices will facilitate the analysis of reported failures. Good customer engineering logic while using the oscilloscope and the built-in aids should result in a minimum of down time for the system.

Supervisory Console

The supervisory console has great potential for the preliminary analysis of machine failures. The Customer Engineer should be thoroughly familiar with the indications provided by the signal neons and should develop an intimate knowledge of the various operations that may be performed at this station.

The particular cycle during which a failure occurs can often be determined by monitoring the signal neons while operating RAMAC in SINGLE OPERATION, SINGLE CYCLE, or FORMAT TEST. If the failure is one that will not be immediately indicated on the signal panel, the point at which failure occurs can generally be determined by investigating the affected process drum tracks between successive program steps.

The console may be used to alter program instructions or process drum data after the test lock switch has been turned ON. Such changing should be done if necessary to determine the exact conditions under which failure occurs.

If a failure involves a transfer of data to or from the file, the testing operations should be restricted to the Customer Engineering tracks on the disk. One of these tracks is addressed automatically by turning the test lock ON.

The test lock switch energizes R8056 (6.15.04) and R5119 (8.11.01). R5119-2 then picks R5118. If the file address register relays store an odd track address, R5119-4 and R5134-12 (8.02.02) will address the access arm to track −1; if an even track address is stored in the address register, R5119-4 and R5119-5 address the arm to track 100. The track null is thus destroyed. The loss of the track null without dropping the servo start relays will cause the clutch power relay, R5035 (8.04.02), to be energized. A servo is thus initiated to one of the CE tracks.

With the test switch ON, data may be read from or stored at the addressed CE track. A new servo may not be initiated, however, as long as the test switch is ON, unless the remote cycling box is connected into its receptacle on the synchronizing panel. The CE test relay, R8056-4 (6.15.04), opens the MR6 circuit so that a file pick pulse cannot be supplied to the file. If a servo to another CE track is desired, the remote cycling box must be plugged in. This will pick R163 (1.02.03). R163-6 (2.09.11) will then shunt R8056-4 (6.15.04).

305 Synchronizing (Sync) Panel

Since the oscilloscope is used almost invariably in the analysis of the electronic circuits, an appreciable saving in total service time can be accomplished by reducing scope set-up time to a minimum. In order to facilitate scope setup, a synchronizing panel is located behind the front relay gate on the process unit. An assortment of pulses and gates which are frequently used in triggering or gating the scope signal are available from hubs on this panel. A 4-input AND inverter switch is also included so that the scope may be triggered by the coincidence of two or more of the sync panel signals.

A diagram of the sync panel is shown in Figure 226. The System Diagram location and identification of each of the sync panel hubs follows:

CE-1	(1.01.00)	Reference Mark.
CE-2	(3.01.04)	Record Start.
CE-3	(1.03.04)	I Cycle.
CE-4	(1.03.05)	R Cycle.
CE-5	(1.03.06)	W Cycle.
CE-6	(1.03.07)	D Cycle.
CE-7	(1.03.08)	P Cycle.
CE-8	(1.01.05)	Bit 0.

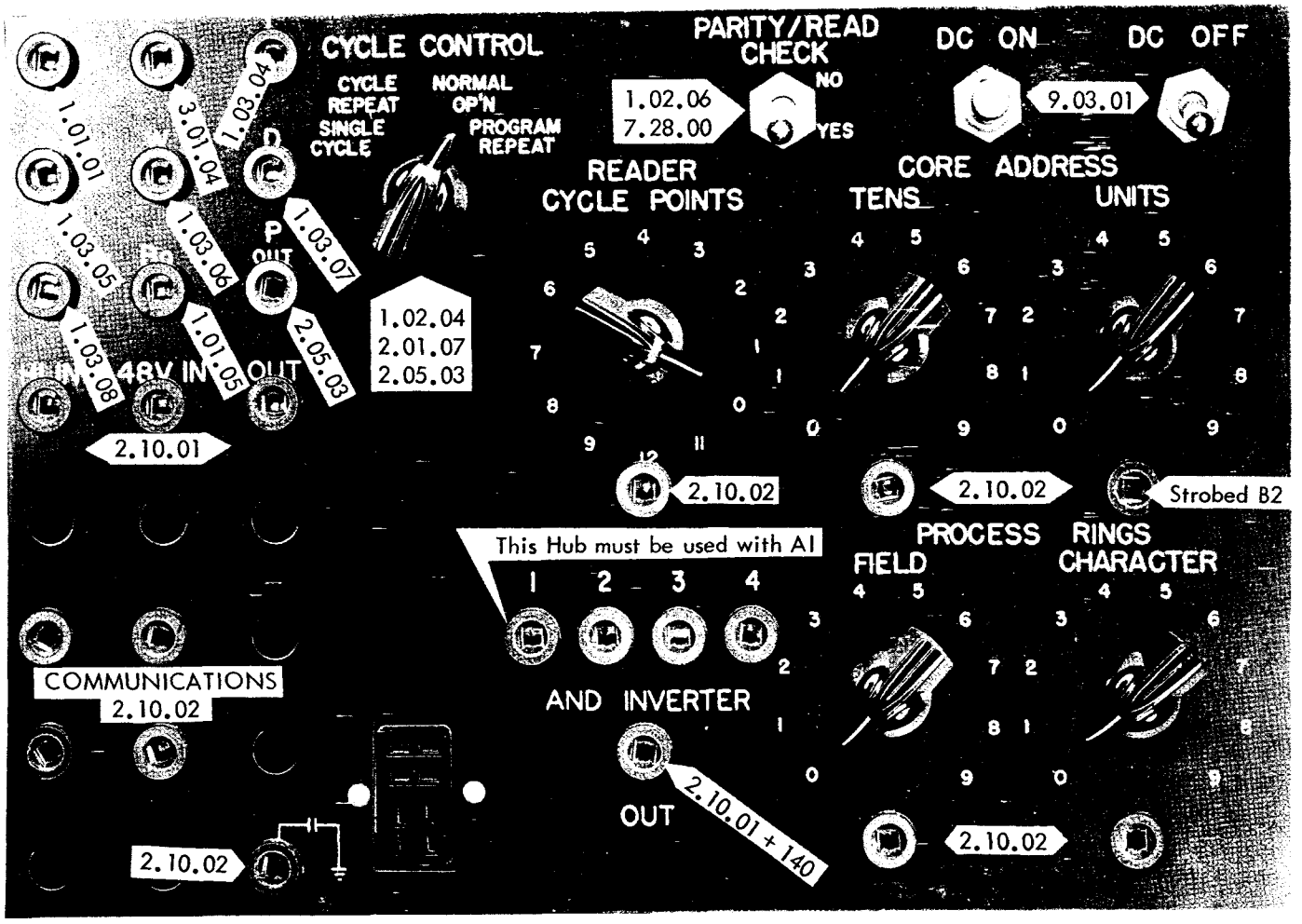


Figure 226. 305 Sync Panel

CE-9 (2.05.03) Program repeat exit – used in conjunction with program repeat switch.

CE-10 (2.10.01) High input to voltage divider.

CE-11 (2.10.01) 48 volt input to voltage divider.

CE-12 (2.10.01) Standard (low) level output from voltage divider.

CE-13 (2.10.02) Reader cycle point gate used in conjunction with dial switch.

CE-14 (2.10.01) Core buffer tens ring gate used in conjunction with dial switch.

CE-15 (2.10.01) Core buffer units ring gate used in conjunction with dial switch.

CE-16 (2.10.01) Input to 4-input AI.

CE-17 (2.10.01) Input to 4-input AI.

CE-18 (2.10.01) Input to 4-input AI.

CE-19 (2.10.01) Input to 4-input AI.

CE-20 (2.10.01) Output from 4-input AI.

CE-21 (2.10.02) Field ring gate—used in conjunction with dial switch.

CE-22 (2.10.02) Character ring gate—used in conjunction with dial switch.

CE-34 (2.10.02) Tweaker hub used in conjunction with the tweaker probe.

CE-26, CE-27, CE-29, CE-30 (2.10.02) Communication hubs providing circuits to file test panel.

Use of the Cycle Control Switch

Single Cycle: This setting simply parallels the single cycle setting of the console control selector switch (1.02.04), allowing processing to advance one cycle with each depression of the program start key.

Cycle Repeat: This setting will prevent a cycle complete gate on 1.02.04. The previously set cycle ready and cycle triggers will remain ON, repeating the established cycle until the CE stop button is depressed. The desired cycle may be set up by first using the SINGLE CYCLE position of the switch.

Program Repeat: To cause the RAMAC to repeat a particular program step, this switch setting blocks the normal program advance pulse and the P cycle program counter reset pulse on 2.01.07. If the program being repeated has a P flag, the MR7 impulse will be directed to the P-out hub on the sync panel (2.05.03) rather than to the 305 control panel program exit hubs. This prevents any program exit impulses from reaching the program entry hubs, and setting up a new program level. To check any of the decision elements during this repated program, a wire may be taken from the P-out hub on the sync panel to the desired 305 control panel hub.

To enable I cycle ready to be turned ON at P cycle end (1.03.04) an MR7 impulse is used to force the new program line high on 2.01.06. This impulse is directed through the program repeat switch points on 2.05.03.

Use of the Sync Panel Hubs

The sync panel hubs, CE-10, CE-11, and CE-12, are points on a voltage divider (2.10.01). The principal purpose of this divider is to convert plate level or 48 volt level signals to approximately standard level for entry into the 4-input AI switch.

The four input AI at 4T1 (2.10.01) employs sync panel hubs, CE-16, 17, 18, and 19, as inputs and CE-20 as an output. If this unit is used, CE-16 must be wired to prevent the triode grids from floating. The other three input hubs may be wired or may be left open.

CE-21 and CE-22, with their associated dial switches, provide process unit field ring gates and character ring gates. These signals are available at their specific process drum timings. For example, if it is desired to examine the data bits entering the core buffer during character 49 time of R cycle, it would be desirable to trigger the scope through the AI. R cycle, F4, and C9 could be wired to the AI input hubs, and the output hub wired to the trigger input of the scope. Since the output from CE-20 would consist of a negative shift at the leading edge, it would be necessary to adjust the scope to trigger on the negative slope. If the scope is triggered with the positive shift, C48 will be displayed instead of C49.

The gates provided by the tens and units rings of the core buffer address counter must be used when it is desired to examine particular characters of data which are being stored into or read from the file. The process unit character and field ring gates cannot be used to trigger the scope. The reason for this is that the rotation of the disks is not synchronized with the process drum clock. By selecting the proper core tens ring gate from CE-14, and the proper core units ring gate from CE-15, the scope may be triggered to inspect any character of the data transfer.

The units position of the core address counter is "anded" with a bit 2. This is to prevent early triggering of the scope by spikes due to the overlap of the falling character 9 and the rising new field gate. Later triggering could be caused by the spikes due to overlapping of the falling field and the rising character 0 gate. The overlap is due to the varying time constants for the changing states of triggers. The bit 0 hub, CE-8, should be used in the event that such extraneous triggering is troublesome while using the units ring and the tens ring hubs.

If it is desired to examine the data bits being decoded from the card at a particular digit impulse time, the corresponding reader cycle point gate may be selected from CE-13 (2.10.02). The selection is accomplished by the associated dial switch. It should be noted that the signals available from CE-13 are at the + 48 volt level.

The trigger tweaker hub, CE-34, provides a means of grid flipping or plate pulling triggers. The resistive-capacitive circuit ties to ground.

When servicing the RAMAC, it is frequently desirable to prevent machine operation from being interrupted by a parity error, compare failure, or read check failure. The Customer Engineer can accomplish this by throwing the parity stop switch to NO (1.02.06), if the remote cycling box is plugged into its receptacle on the sync panel. With both R163-5 and the parity stop switch open, neither a parity error nor a compare failure will halt system operation. The 1B point of the parity stop switch (7.28.00) completes a circuit through R163-10 to insure that R8036 picks on each feed cycle. This will prevent a read check from stopping the system.

The communication hubs provide direct circuits to the file test panel. Scope triggering pulses and gates may be sent from the 305 to the 350 or vice-versa through these lines.

In addition to the switches and hubs discussed above, the sync panel includes a DC on and a DC off switch. With the DC off switch in the OFF position, the DC on and POWER on switches at the power supply panel and at the supervisory panel are crippled. This prevents the DC from being applied inadvertently while the Customer Engineer is working on the system.

305 Remote Cycling Box

The 305 remote cycling box has five push-button switches. This device is connected through a flexible

cable to a Jones plug which may be plugged into a receptacle on the sync panel.

When the remote cycling box is attached, R163 (1.02.03), is energized. The points of R163 make active the CE check reset switch, the CE program set switch, the CE program start switch, the CE program stop switch, and the CE manual reset switch. The corresponding switches at the console are made inactive by transfer of the R163 points.

Other points of R163 perform certain auxiliary functions as follows:

1. R163-5 (1.02.06)—Parallels the parity stop switch 1A point to suppress parity error stops.
2. R163-6 (2.09.11)—Parallels R8056-4 to provide MR6 impulses to file pick common even though test lock is ON. Servo operations can be performed.
3. R163-7 (2.05.03)—Transfers all program exit impulses to the P-out hub on the sync panel when the CE cycle control switch is set to PROGRAM REPEAT.
4. R163-9 (1.02.03)—Permits inquiry even though test lock is ON.
5. R163-10 (7.28.00)—Prevents read check error stops when the parity read check switch is at NO.
6. R163-12 (2.01.07)—Blocks program counter advance pulse when the CE cycle control switch is set to PROGRAM REPEAT.

370 Dynamic Timer (Figure 227)

The 370 dynamic timer index is in continuous operation and is therefore synchronized with the CR index at all times; however, it is not in automatic synchronism with the program shaft index and with the emitter shaft. Since the dynamic timer index is based on a 400 millisecond cycle, there is a possibility of engaging the program shaft clutch at ten different points in the dynamic timer cycle. Thus when the dynamic timer is to be used in servicing the printer, the impulse to energize the PS clutch must be timed to cause the clutch to engage when the dynamic timer is at its zero index line.

The dynamic timer CB, DTCB (7.74.11), is normally shunted by the dynamic timer interlock switch. If this switch is opened, R3 will be energized at the proper point of the dynamic timer cycle to cause the program shaft clutch to engage in synchronism with the dynamic timer index.

The interval from 17 to 19 on the dynamic timer index is identified as print position #1 (Figure 227). It is during this interval of time that impulses are available from print position exit emitter spot #1 and print control exit emitter spot #1. Thus, the print positions as indicated on the dynamic timer index refer to the position of the emitter shaft when a character is selected for printing. Actual printing time comes somewhat later.

The dynamic timer has a 400 millisecond cycle; printing takes place at the rate of 20 characters per cycle. Therefore, the interval which represents print position #1 on the first cycle will represent print positions #21, #41, and #61 on succeeding cycles.

If it is desired to use the dynamic timer to examine the relay circuit actions occurring in the area of print position #41, it would be desirable to prevent print position #21 or #61 from lighting the dynamic timer neons. A method is provided whereby this may be accomplished.

The socket connections for the dynamic timer power pack and the dynamic timer neons are shown on 7.74.81. Note that R15 must be energized in order to complete a circuit to the neons. Relay 15 has a latch pick and a latch trip coil on 7.74.11. The pick-up and drop-out hubs are located on the timer panel above the socket for the power pack. Leads may be taken to these hubs from print control exit emitter hubs on the control panel to make the dynamic timer effective only during the desired interval.

Relay 15 may also be picked prior to the beginning of the PS cycle with the same impulse which holds R3 (7.74.11). The dynamic timer control pulse hub is provided on the timer for this purpose.

A jack for an auxiliary start key is also available on the 370 timer panel. When this key is inserted, the circuit to relay 1 is broken; hence neither of the ready relays, R1 nor R2, will be energized (7.74.11). The auxiliary start key is placed in the circuit so that, when depressed, it will energize R32. R32-1 bypasses R2-1 and R172-3 in the circuit to R3.

The dynamic timer index should not be used to adjust or manually check a timing. The timer index will not agree with the CRCB index when the machine is operated by hand. This variance is due to gear play and belt stretch in the drive mechanism. Refer to the 305 CE Reference Manual for complete details.

Dynamic Timers for Reader and Punch

A dynamic timer is included with both the reader and punch. Unlike the 370, these dynamic timer indexes are continuously synchronized.

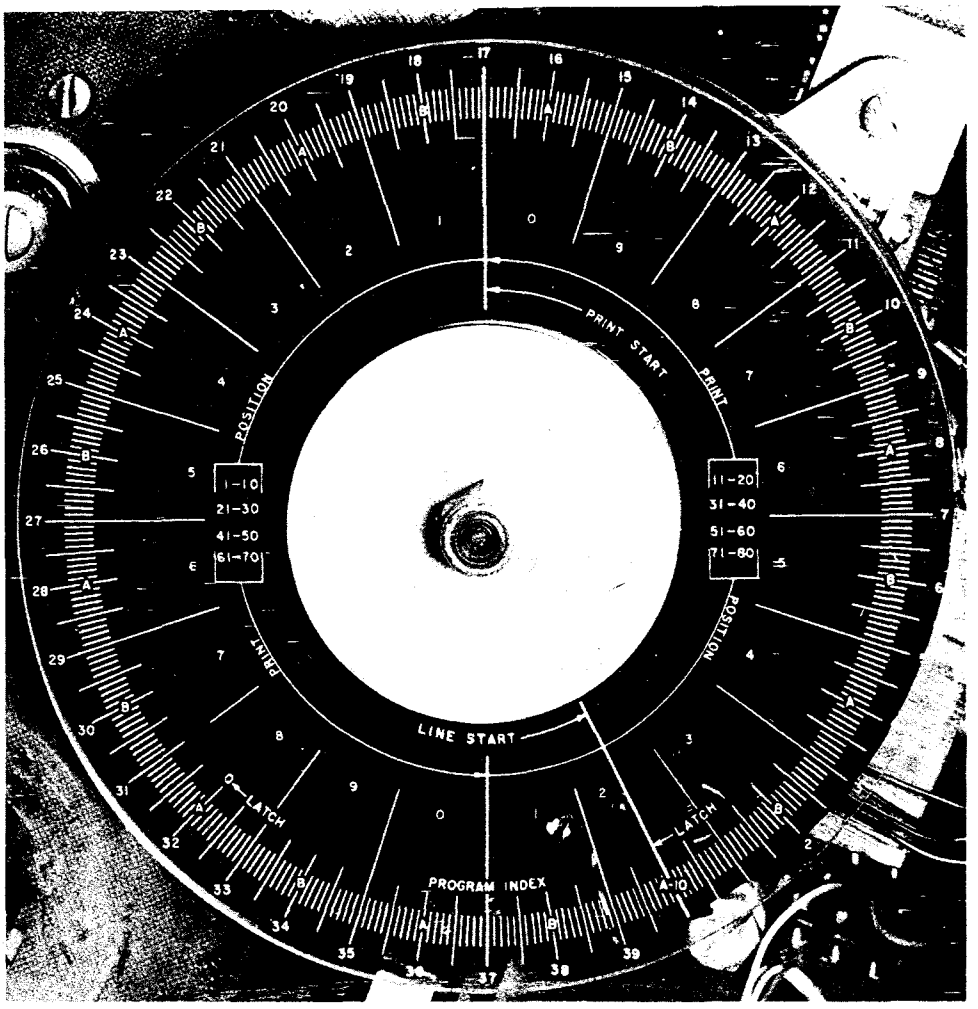


Figure 227. 370 Dynamic Timer

File Test Panel (Figure 228)

The 350 file has been designed with a built-in test panel. All normal electronic adjustments and most file trouble analysis can be performed at this station. The file test station includes 7 adjustable potentiometers, 46 indicating neons and 6 spares, 16 servicing hubs and 5 spares, 5 fuses, 3 toggle switches and 1 push-button switch. The System Diagrams locations for the various test station items can be found on 0.55.01.

The specific adjustment procedure for each of the potentiometers will be found in the 305 CE Reference Manual. The purposes of neons and fuses are self-explanatory on Figure 228. Except for the communication hubs and the ground hub, the servicing hubs are monitor points placed in the file circuits.

The safety off push-button (8.06.01) is used to drop the logic safety relay 5116. R5116-5 then drops the bias safety R5007 (8.06.02). The file should be in a SAFETY OFF condition when working around the access mechanism.

The three toggle switches are the double-pole double-throw type with the center position OFF. The safety reset adjust switch in the SAFETY RESET position completes the pick circuit to the logic safety R5116 (8.06.01). The ADJUST position of this switch completes the circuit to pick the adjust relay 5052 (8.06.01) in the electronic gate. When this relay is energized the following objectives are accomplished:

1. R5052-1 turns on the adjust neon on the file test panel (8.08.01).
2. R5052-2 drops the head solenoid relay (8.01.07).
3. R5052-10 applies ground level to the clutch amplifier wiper signal input (8.05.01).
4. R5052-7 connects a 6.3v AC signal to the track null detector input (8.02.03).
5. R5052-8 connects a 6.3v AC signal to the disk null detector input (8.01.03).

The no null toggle switch (8.01.04) removes either the disk null condition or the track null condition. It does this by supplying −60 volts to the last stage of the disk or track null amplifier (8.02.04). Loss of the track null will cause the track detent solenoid to be de-energized. This permits the access arm to be moved manually.

The null adjust switch (8.01.04) controls the output of the null adjust signal hub. It makes an amplified disk potentiometer signal available when up. An amplified track potentiometer signal is available when the switch is down.

File Robot (8.20.00)

The testing of file servo operations can be facilitated by operating the access mechanism as a separate machine, free of control from the process unit. If this is to be done, an additional set of controls must be available to the Customer Engineer. These additional controls are included in a portable box which is called the robot. This device is illustrated in Figure 229.

The functions of the front panel switches, jacks, and lights are as follows:

Address: Two sets of rotary switches permit addresses "A" or "B" to be made active. The access mechanism may be caused to servo alternately between the two addresses. Five rotary switches are used to set up each address. Each switch connects one side of an address relay coil to ground. Any address from 00000 to 99999 may be selected.

Track Solenoid: This switch may be opened to remove the + 48 volt input to the track solenoids. It is a SPST toggle switch which prevents either track solenoid from being energized when in the down position.

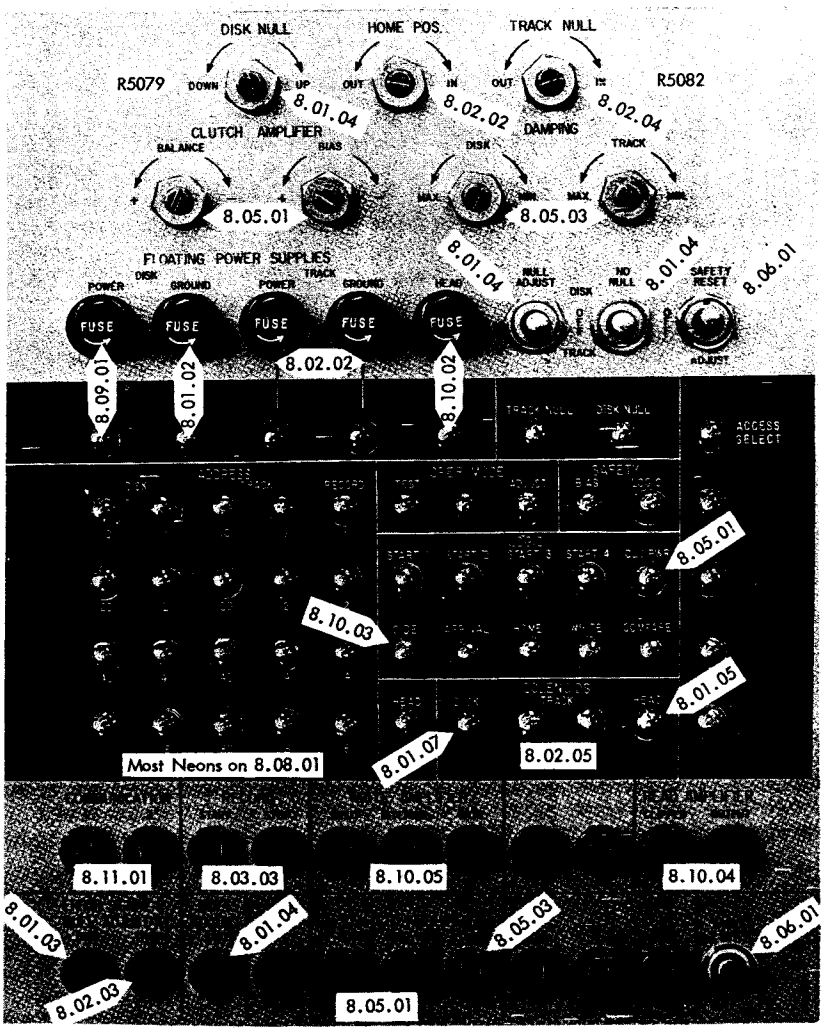


Figure 228. File Test Panel

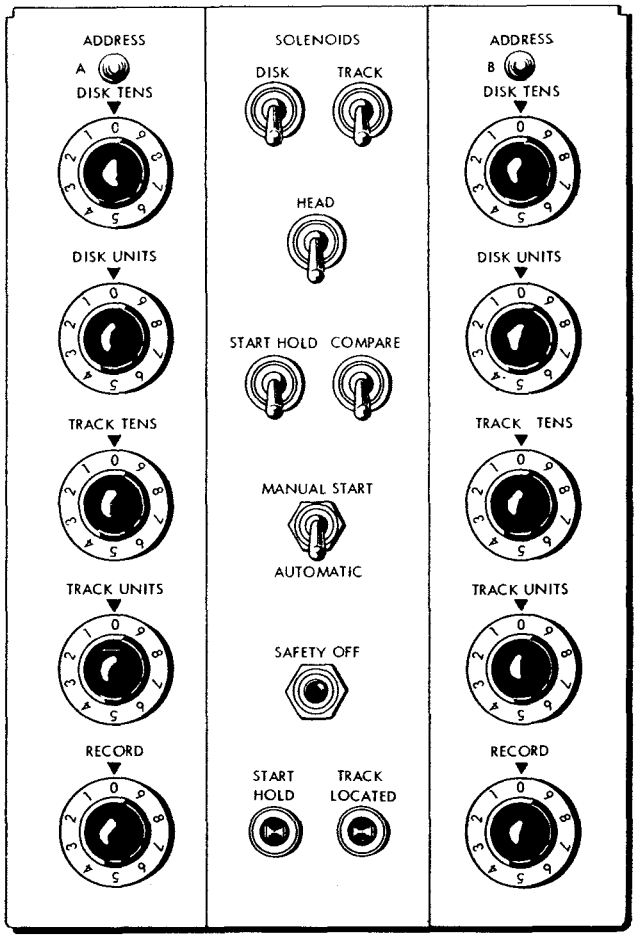


Figure 229. File Robot

Disk Solenoid: This switch prevents either disk detent solenoid from being energized when in the down position. When opened, this SPST switch removes the + 48 volt potential from the disk detent solenoid line.

Head Solenoid: This SPST switch makes it possible to remove the air supply to the file read/write heads. When down it prevents the + 48 volt line from being applied to the air head solenoid. This keeps the air heads away from the disks at all times.

Compare: This is a spare SPST switch placed in the robot for future use.

Start Hold: This switch breaks the hold circuit for the start relays when in the down position. It is a SPST toggle switch.

Manual Start-Automatic: When this double pole-double throw toggle switch is in the AUTOMATIC position, it completes the circuit so the track located signal will cause a change of address. The access mechanism will then servo automatically between the two addresses set up by the rotary switches.

When in the MANUAL START position, the switch provides a + 48 volt impulse to initiate a servo to the alternate address. The switch is spring loaded to return from the MANUAL START position to the center OFF position.

Safety Off: The safety-off switch is the push-button type which will open the + 48 volt potential to the logic safety relays when depressed. Dropping the logic safety relay will cause the bias safety relay to drop also.

Start Monitor Point: This is a hub on the robot which permits observing the "start hold" signal with the oscilloscope.

Track Located Monitor Point: This hub on the robot permits observing the "track located" signal with the oscilloscope.

"A" and "B" Address Lights: These two neon lights indicate which of the two addresses is active.

Operating Procedure for the File Robot

The following procedure should be followed in connecting the robot for servicing the 350 file:

1. Turn off the DC power.
2. Put the manual start-automatic switch at its center position.
3. Put the remaining toggle switches in the down position.
4. Connect the H and K connectors from the electronic gate to the receptacles in the back of the robot.
5. Turn on the DC power.

The following procedure may be employed to operate the access mechanism under manual control:

1. Verify that the safety relays in the electronic gate are energized.
2. Position the five rotary switches of the "A" group at the desired record position. Place the "B" address switches at a different record position.
3. Place the track, disk and head solenoid switches in the up position.
4. Place the start hold switch in the up position.
5. Flip the manual start switch up momentarily. The access arm will go to the address indicated by the lighted neon address light on the front panel of the robot.
6. After the access arm has reached the selected address, a second deflection of the manual start switch will cause the access arm to servo to the alternate address selected in step 2.

The System Diagrams page 8.20.00 shows that nine relays are included in the robot. Two of these, MR1 and MR2, are mercury relays. MR1 (8.20.00) supplies the hold circuit for the address register relays and for the file start relays. MR2 supplies + 48 volts to the common pick circuit for these. We learned from the previous discussion of the file circuits that a servo is initiated by first dropping and then repicking the