Lecture 20: Memory Technology

COS 471a, COS 471b / ELE 375

Computer Architecture and Organization

Princeton University
Fall 2004

Prof. David August

Program Notes

Homework #3

- Due December 6th (Monday)
- Out this week

Reading

- Chapters 1-8, A-C

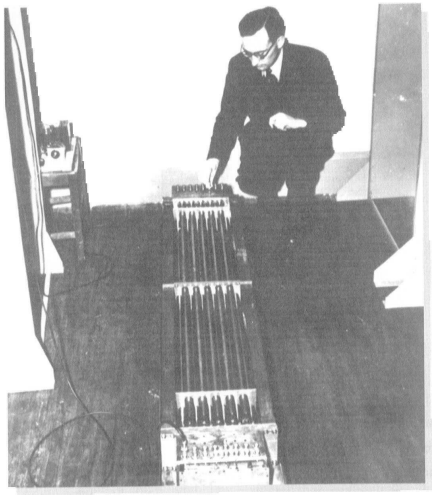
Today

- Short Lecture

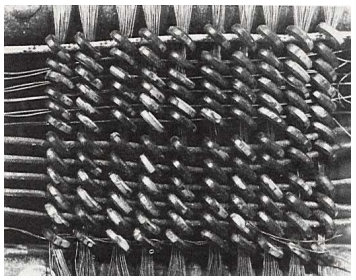
Old Stuff Revisited

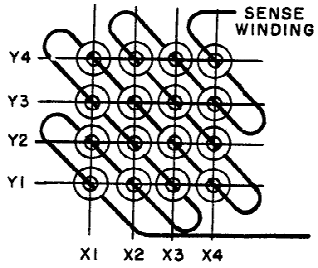
Mercury Delay Line Memory

Maurice Wilkes, in 1947, with first mercury tank memories built for EDSAC.

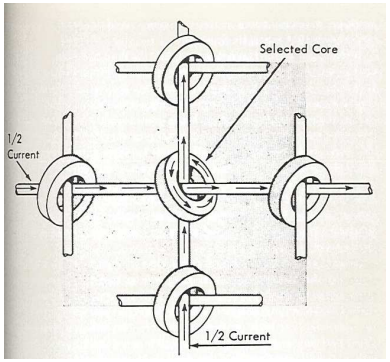


Core Memory

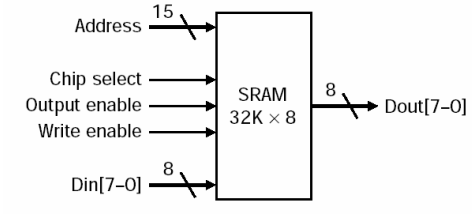




- Theory of operation
- Threaded by hand!
- The Lifesaver connection
- Refresh



Static RAM (SRAM)

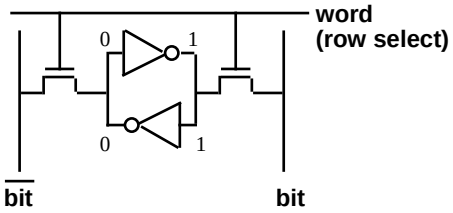


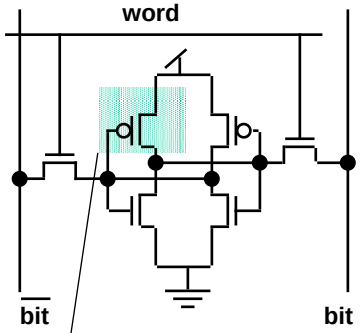
- SRAM - Fast, but not the most dense (better than core!)
- Chip select can be viewed as another address line
- Din and Dout are often combined to save pins
  - Need output enable (OE_L - enable low)
  - Need write enable (WE_L - enable low)
- Don't assert both write enable and output enable
  - Result is unknown.
  - This is bad.
  - Don't do it!!!

The Transistor Makes It Possible!

Static RAM (SRAM) Cell

6-Transistor SRAM Cell





Replaced with pullup resistor to save area

Write:

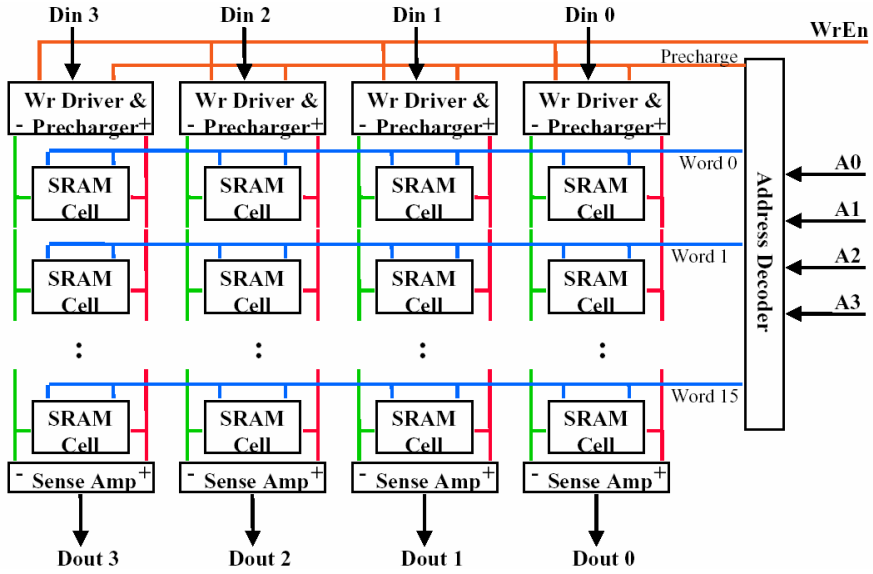
1. Drive bit lines (bit=1, bitbar=0)
2. Select row

Read:

1. Precharge bit and bitbar to Vdd
2. Select row
3. Cell pulls one line low
4. Sense amp on column detects difference between bit and bitbar

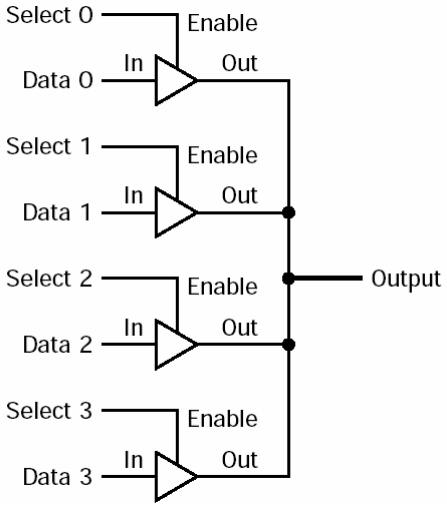
Why is it Static?

Typical SRAM Organization

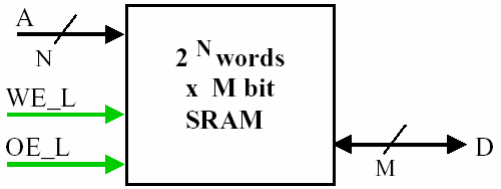


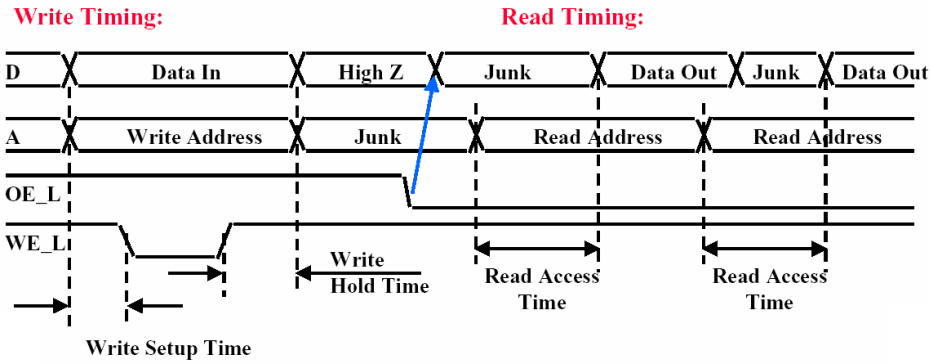
Three-State Buffers

Avoid HUGE MUX using three-state buffers



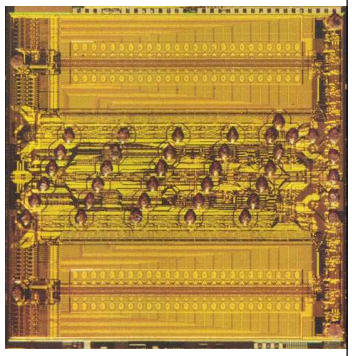
Typical SRAM Timing





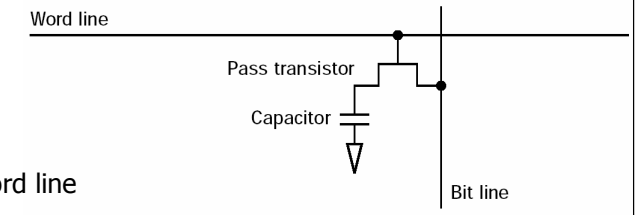
Dynamic RAM (DRAM)

- Slower, cheaper, more dense than SRAM
- Dynamic?



Dynamic RAM Cell

DRAM



Write:

1. Drive bit line
2. Select row/word line

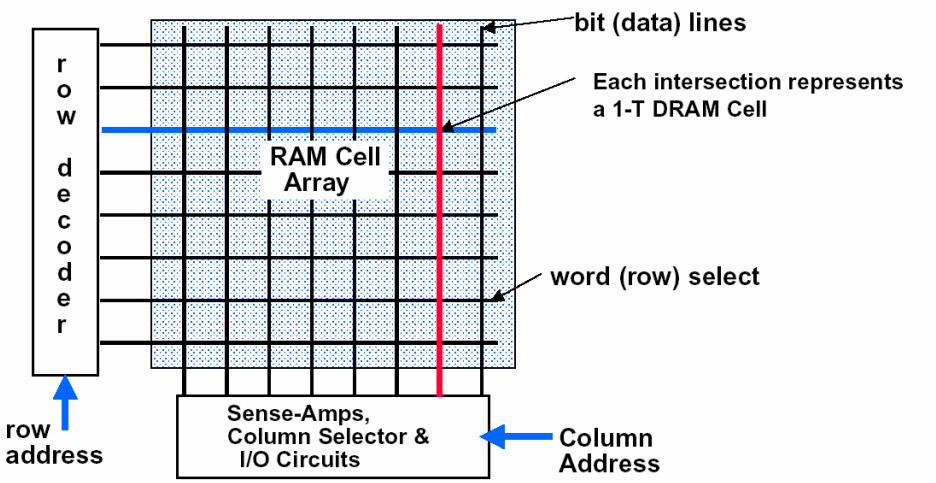
Read:

1. Precharge bit line to Vdd
2. Select row/word line
3. Cell and bit line share charge
4. Sense (sense amp can detect changes of ~10-100k electrons)
5. Write: restore the value

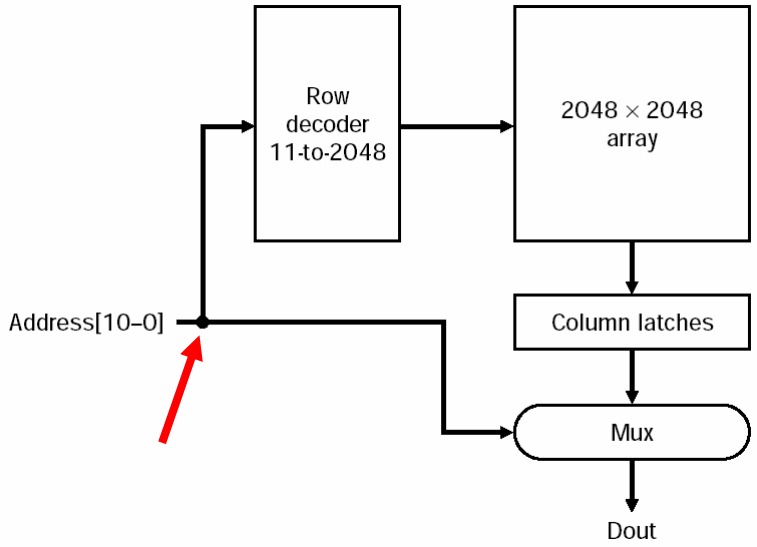
Refresh (capacitor leaks):

1. Just do a dummy read to every cell.

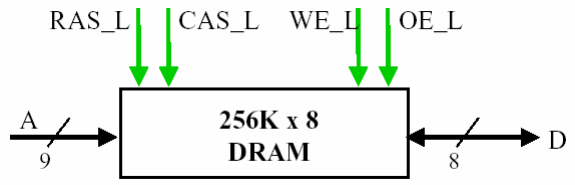
Classical DRAM Organization (Square)



4Mx1 DRAM Organization

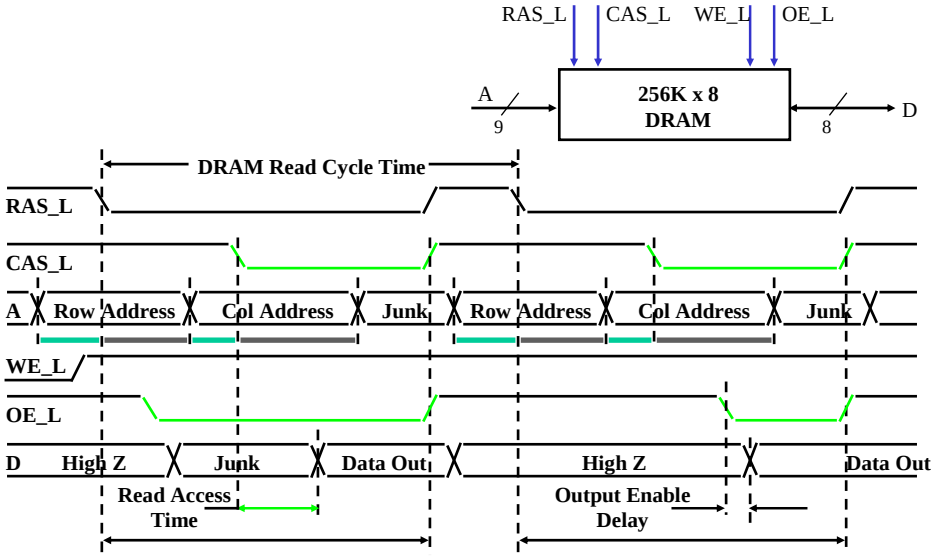


Logic Diagram of a Typical DRAM



- Row and column addresses share the same pins (A)
  - RAS_L goes low: Pins A are latched in as row address
  - CAS_L goes low: Pins A are latched in as column address
  - RAS/CAS edge-sensitive
- Din and Dout share the same pins (D)
- Control Signals (RAS_L, CAS_L, WE_L, OE_L) typically active low

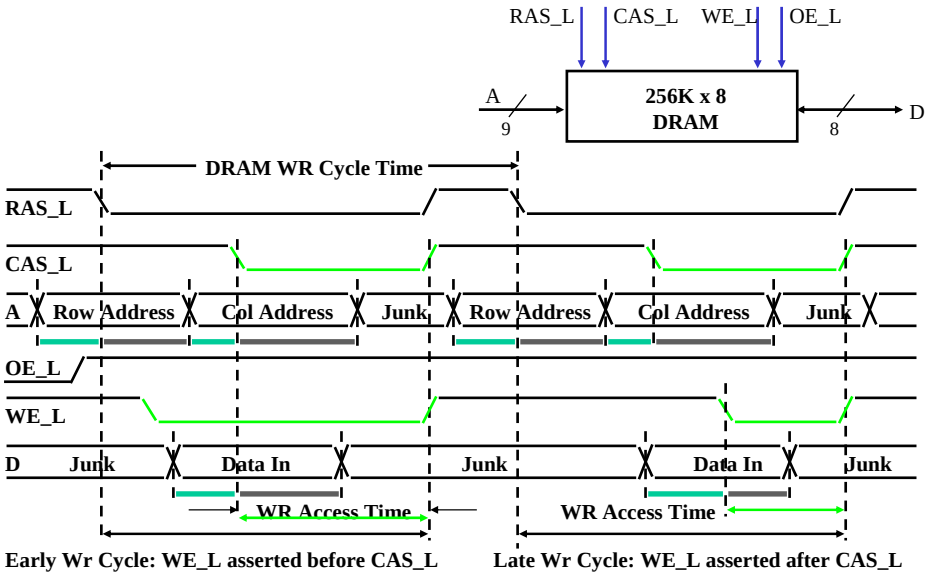
DRAM Read Timing



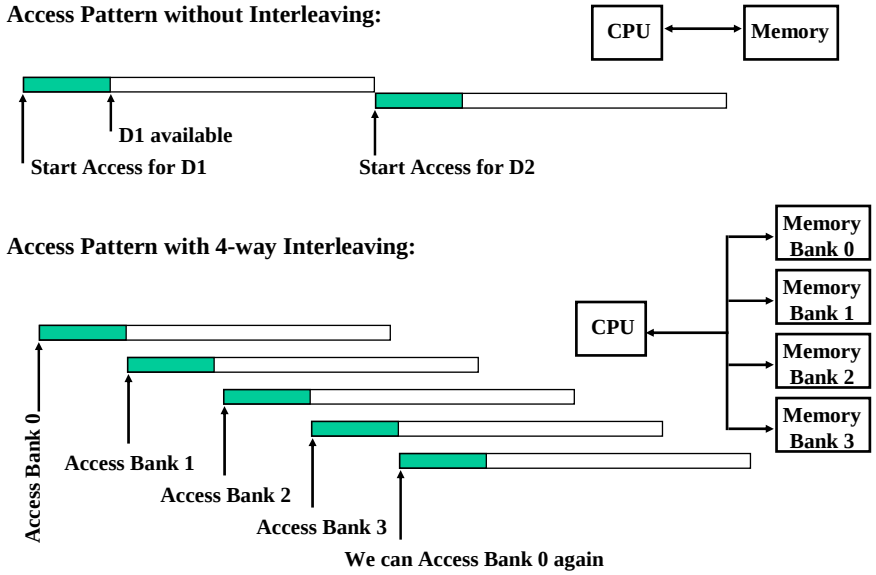
Early Read Cycle: OE_L asserted before CAS_L

Late Read Cycle: OE_L asserted after CAS_L

DRAM Write Timing

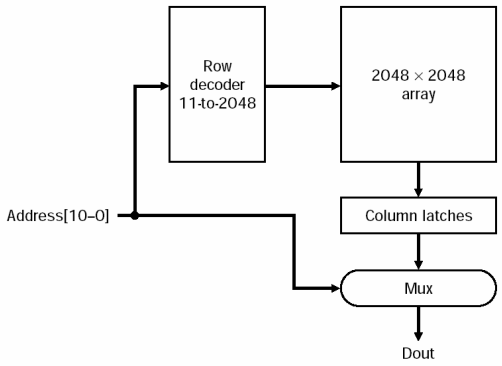


Increasing Bandwidth - Interleaving



"New" DRAMs

- For decades, DRAM Interface was stable (RAS, CAS, etc.)
- Only in past decade has it begun to evolve again
  - Especially in systems with few DRAM chips
  - Bandwidth/Througput
  - Ease of design
- Two key contenders:
  - Synchronous DRAM
  - Rambus DRAM



Summary

DRAM à slow, cheap, dense
- Good for BIG main memory
- Must be refreshed

SRAM à fast, expensive, not very dense
- Good choice for fast memory like caches!
- Holds state while power applied

Memory hierarchy to get the best of both!

Enjoy Your Thanksgiving Break!