μPB8288
CPU SYSTEM BUS CONTROLLER

Description

The μPB8288 bus controller is used in medium to large μPD8086/μPD8088 systems. This 20-pin bipolar component provides command and control timing generation, as well as bipolar drive capability and optimal system performance. It provides both Multibus® command signals and control outputs for the microprocessor system. There is an option to use the controller with a multimaster system bus and separate I/O bus.

Features

- ☐ System controller for μPD8086/μPD8088 systems
- ☐ Bipolar drive capability
- ☐ Provides advanced commands
- ☐ Three state output drivers
- ☐ Can be used with an I/O bus
- ☐ Enables interface to one or two multimaster buses

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPB8288D	20-pin cerdip	10 MHz

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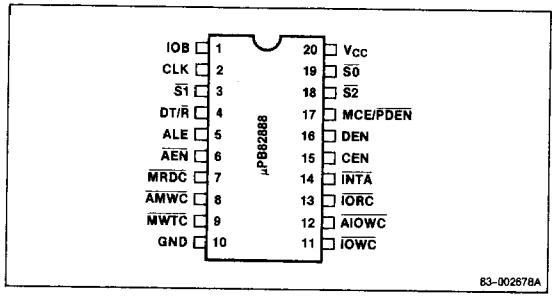
Pin Configuration



Pin Identification

No.	Symbol	Function
1	IOB	I/O bus mode selector input
2	CLK	Clock input
3	$\overline{S1}$	Status input
4	DT/$\overline{R}$	Data transmit/receive
5	ALE	Address latch enable output
6	$\overline{AEN}$	Address enable input
7	$\overline{MRDC}$	Memory read command output
8	$\overline{AMWC}$	Advanced memory write command output
9	$\overline{MWTC}$	Memory write command output
10	GND	Ground
11	$\overline{IOWC}$	I/O write command output
12	$\overline{AIOWC}$	Advanced I/O write command output
13	$\overline{IORC}$	I/O read command output
14	$\overline{INTA}$	Interrupt acknowledge output
15	CEN	Command enable input
16	DEN	Data enable output
17	MCE/$\overline{PDEN}$	Master cascade enable/peripheral data enable output
18	$\overline{S2}$	Status input
19	$\overline{S0}$	Status input
20	V_{CC}	+5 V power supply

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Pin Functions

$\overline{AEN}$ (Address Enable)

In the I/O system bus mode, $\overline{AEN}$ enables the command outputs of the μPB8288 105 ns after it becomes active. If $\overline{AEN}$ is inactive, the command outputs become high impedance outputs.

$\overline{AIOWC}$ (Advanced I/O Write Command)

This write command occurs earlier in the machine cycle than the $\overline{IOWC}$ command.

ALE (Address Latch Enable)

This signal is used for controlling transparent D-type latches (μPB8282/μPB8283). It will strobe in the address on a high to low transition.

$\overline{AMWC}$ (Advanced Memory Write Command)

This is an advanced write command which occurs early in the machine cycle, with timing the same as the read command.

CEN (Command Enable)

This signal enables all command and control outputs. If CEN is low, these outputs are inactive.

CLK (Clock)

The clock signal from the μPB8284 clock generator synchronizes the generation of command and control signals.

DEN (Data Enable)

This signal enables the data transceivers onto the bus.

DT/$\overline{R}$ (Data Transmit/Receive)

This signal is used to control the bus transceivers in a system; high for writing to I/O or memory and low for reading data.

$\overline{INTA}$ (Interrupt Acknowledge)

INTA is used to signal an interrupting device to put the vector information on the data bus.

IOB (I/O Bus Mode)

Sets mode of μPB8288; high for the I/O bus mode and low for the system bus mode.

$\overline{IORC}$ (I/O Read Command)

This signal enables the CPU to read data from an I/O device.

$\overline{IOWC}$ (I/O Write Command)

This command is for transferring information to I/O devices.

MCE/$\overline{PDEN}$ (Master Cascade Enable/ Peripheral Data Enable)

Dual function pin system. (MCE) In the bus mode, this signal is active during an interrupt sequence to read the cascade address from the master interrupt controller onto the data bus. ($\overline{PDEN}$) In the I/O bus mode, it enables the transceivers for the I/O bus just as DEN enables bus transceivers in the system bus mode.

$\overline{MRDC}$ (Memory Read Command)

This active low signal is for switching the data from memory to the data bus.

$\overline{MWTC}$ (Memory Write Command)

This signal is used to transfer the data bus to memory, but not as early as $\overline{AMWC}$. (See timing waveforms).

GND (Ground)

Ground.

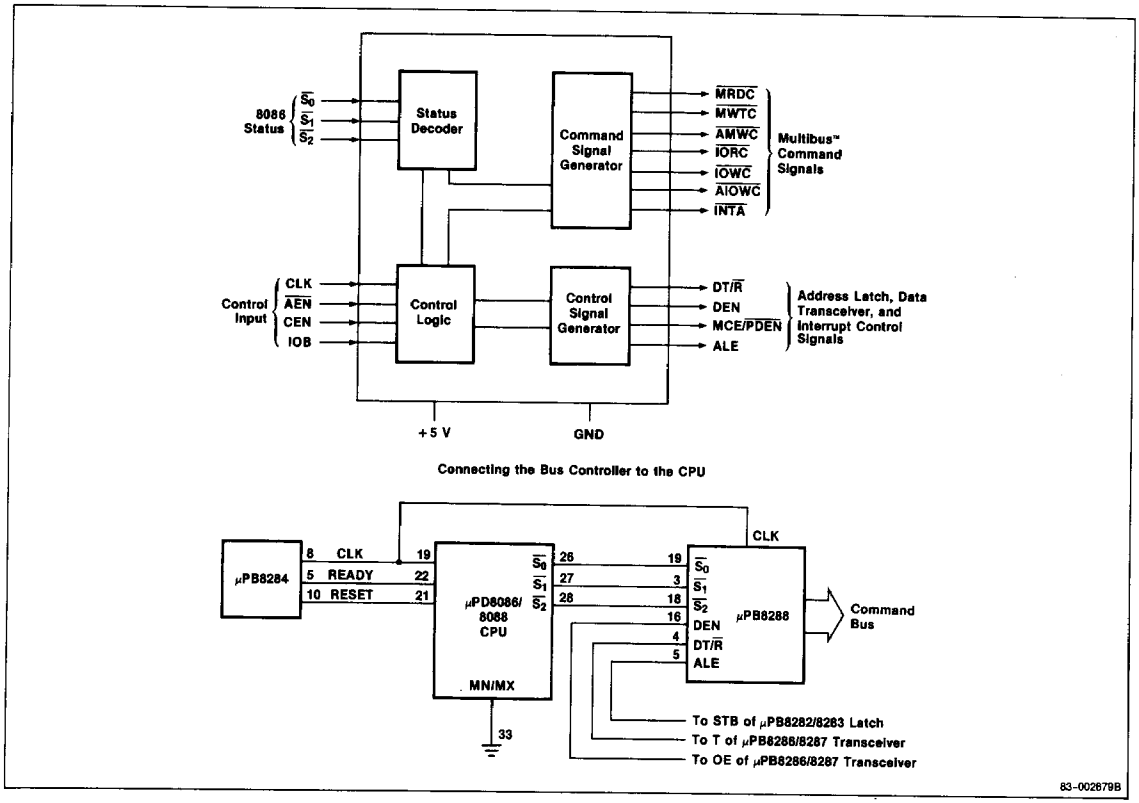
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$ (Status Input Pins)

The μPB8288 decodes these status lines from the μPD8086 to generate command and control signals. When not in use, these pins are high.

V_{CC} (Power Supply)

+5 V power supply.

Block Diagram



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Absolute Maximum Ratings

T_A = 25°C

Power supply voltage, V_{DD}	−0.5 to +7.0 V
Input voltage, V_I	−1.0 to +5.5 V
Output voltage, V_O	−0.5 to +7.0 V
Operating temperature, T_{OPT}	0 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum ratings for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5 V ±10%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input high voltage	V_{IH}	2.0		V	
Input low voltage	V_{IL}		0.8	V	
Input clamp voltage	V_C		−1	V	I_C = −5 mA
Output high voltage (command)	V_{OH}	2.4		V	I_{OH} = −5 mA
(control)		2.4		V	I_{OH} = −1 mA
Output low voltage (command)	V_{OL}		0.5	V	I_{OL} = 32 mA
(control)			0.5	V	I_{OL} = 16 mA
Forward input current	I_F		−0.7	mA	V_F = 0.45 V
Reverse input current	I_R		50	μA	V_R = V_{CC}
Output off current	I_{OFF}		100	μA	V_{OFF} = 0.4 V to 5.25 V
Power supply current	I_{CC}		230	mA	

AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5 V ±10%

Timing Requirements

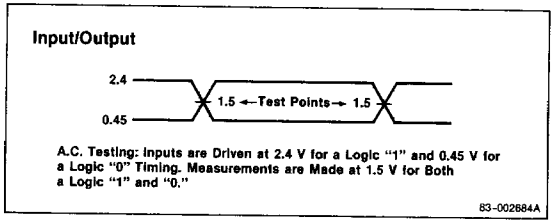
Parameter	Symbol	Limits Min	Limits Max	Unit	Loading
CLK cycle period	t_{CLCL}	100		ns	
CLK low time	t_{CLCH}	50		ns	
CLK high time	t_{CHCL}	30		ns	
Status active setup time	t_{SVCH}	35		ns	
Status active hold time	t_{CHSV}	10		ns	
Status inactive setup time	t_{SHCL}	35		ns	
Status inactive hold time	t_{CLSH}	10		ns	
Input rise time	t_{ILIH}		20	ns	
Input fall time	t_{IHIL}		12	ns	

Timing Responses

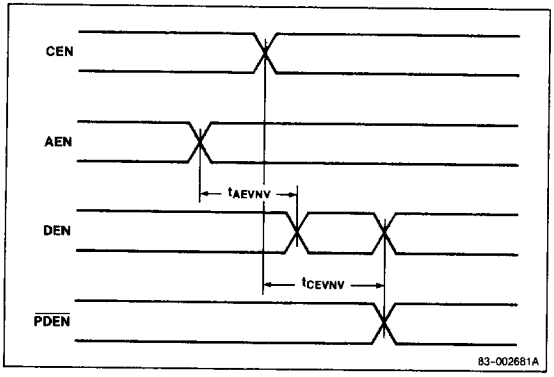
Parameter	Symbol	Limits Min	Limits Max	Unit	Loading
Control active delay	t_{CVNV}	5	45	ns	
Control inactive delay	t_{CVNX}	10	45	ns	
ALE MCE active delay (from CLK)	t_{CLLH}/ t_{CLMCH}		20	ns	$\overline{MRDC}$
ALE MCE active delay (from status)	t_{SVLH} t_{SVMCH}		20	ns	$\overline{IORC}$ $\overline{MWTC}$ I_{OL} = 32 mA
ALE inactive delay	t_{CHLL}	4	15	ns	$\overline{IOWC}$ I_{OH} = −5 mA
Command active delay	t_{CLML}	10	35	ns	$\overline{INTA}$ C_L = 300 pF
Command inactive delay	t_{CLMH}	10	35	ns	$\overline{AMWC}$
Direction control active delay	t_{CHDTL}		50	ns	$\overline{AIOWC}$
Direction control inactive delay	t_{CHDTH}		30	ns	
Command enable time	t_{AELCH}		40	ns	
Command disable time	t_{AEHCZ}		40	ns	
Enable delay time	t_{AELCV}	115	200	ns	I_{OL} = 16 mA
AEN to DEN	t_{AEVNV}		20	ns	Other} I_{OH} = −1 mA
CEN to DEN, PDEN	t_{CEVNV}		25	ns	C_L = 80 pF
CEN to command	t_{CELRH}		t_{CLML}	ns	
Output rise time	t_{OLOH}		20	ns	
Output fall time	t_{OHOL}		12	ns	

Timing Waveforms

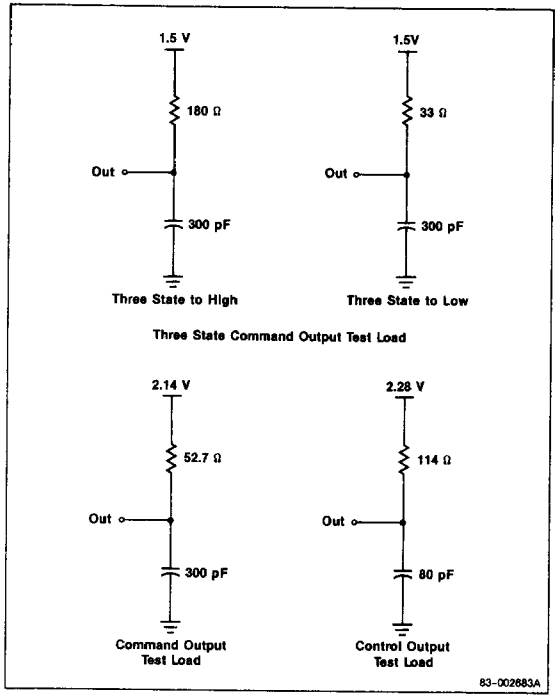
Timing Measurement Points



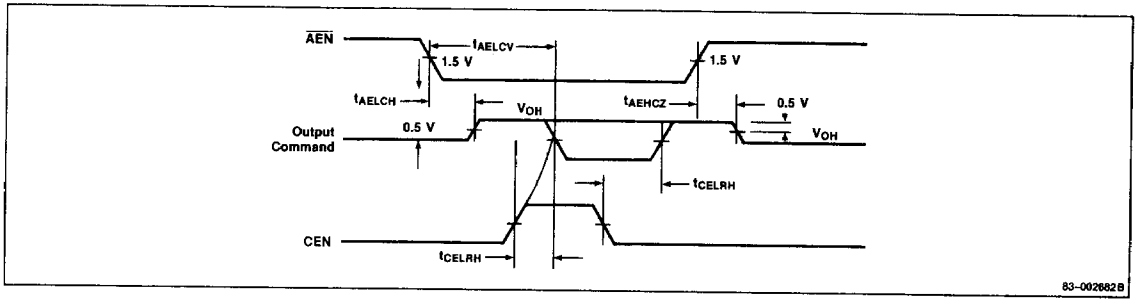
DEN, PDEN Qualification Timing



Test Load Circuits



μPD8288 Address Enable (AEN) Timing (Three State Enable/Disable)



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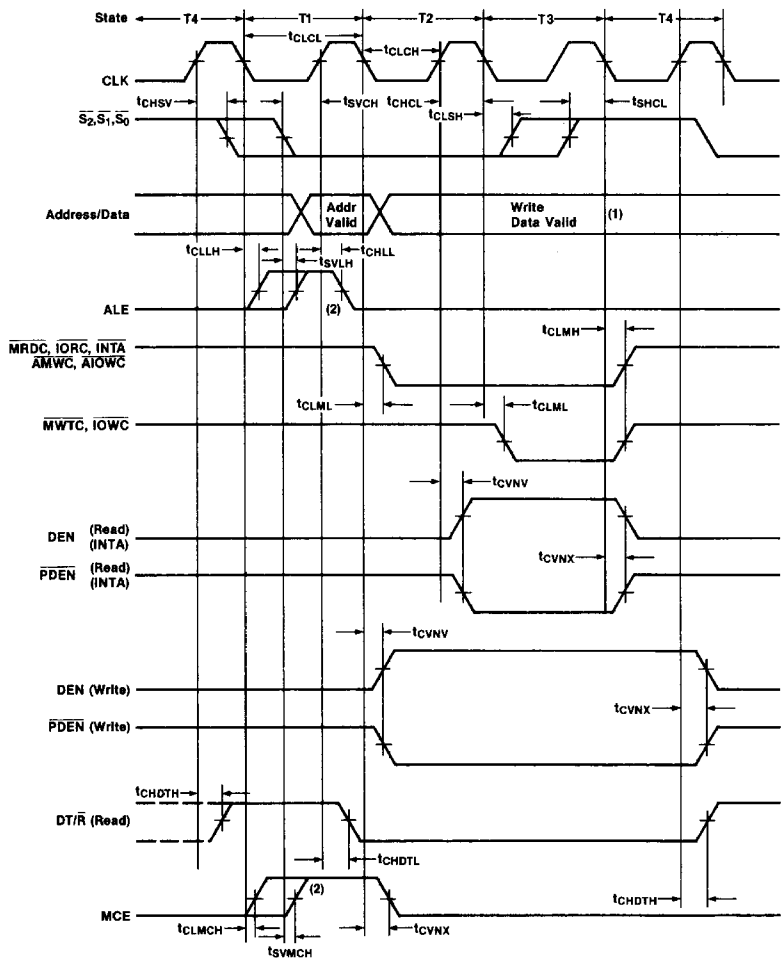
Timing Waveforms (cont)

State Timing



Note:

(1) Address/data bus is shown only for reference purposes.

(2) Leading edge of ALE and MCE is determined by the falling edge of CLK or status going active, whichever occurs last.

(3) All timing measurements are made at 1.5 V unless specified otherwise.

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Functional Description

The three status lines ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$) from the μPD8086 CPU are decoded by command logic within the μPB8288 to determine which command is to be issued. Table 1 below illustrates the decoding and command generation of the status lines.

Table 1. Status Line Decoding

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	μPD8086 State	μPB8288 Command
0	0	0	Interrupt acknowledge	$\overline{INTA}$
0	0	1	Read I/O port	$\overline{IORC}$
0	1	0	Write I/O port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Code access	$\overline{MRDC}$
1	0	1	Read memory	$\overline{MRDC}$
1	1	0	Write memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

There are two ways the command is issued depending on the mode of the μPB8288.

The I/O bus mode is enabled if the IOB pin is pulled high. In this mode, all I/O command lines are always enabled and not dependent upon AEN. When the processor sends out an I/O command, the μPB8288 activates the command lines using $\overline{PDEN}$ and DT/$\overline{R}$ to control any bus transceivers.

This mode is advantageous if I/O or peripherals dedicated to one microprocessor are in a multiprocessor system, allowing the μPB8288 to control two external buses. No waiting is required when the CPU needs to access the I/O bus, as an $\overline{AEN}$ low signal is needed to gain normal memory access.

If the IOB pin is tied to ground, the μPB8288 is in the system bus mode. In this mode, command signals are dependent upon the $\overline{AEN}$ line. Thus the command lines are activated 105 ns after the $\overline{AEN}$ line goes low. In this mode, there must be some bus arbitration logic to toggle the $\overline{AEN}$ line when the bus is free for use. Here, both memory and I/O are shared by more than one processor, over one bus, with both memory and I/O commands waiting for bus arbitration.

Among the command outputs are some advanced write commands which are initiated early in the machine cycle and can be used to prevent the CPU from entering unnecessary wait states.

The $\overline{INTA}$ signal acts as an I/O read during an interrupt cycle. This is to signal the interrupting device that its interrupt is being acknowledged, and to place the interrupt vector on the data bus.

The control outputs of the μPB8288 are used to control the bus transceivers in a system. DT/$\overline{R}$ determines the direction of the data transfer, and DEN is used to enable the outputs of the transceiver. In the IOB mode the MCE/$\overline{PDEN}$ pin acts as a dedicated data enable signal for the I/O bus.

The MCE signal is used in conjunction with an interrupt acknowledge cycle to control the cascade address when more than one interrupt controller (such as a μPD8259A) is used. If there is only one interrupt controller in a system, MCE is not used because the $\overline{INTA}$ signal gates the interrupt vector onto the processor bus. In multiple interrupt controller systems, MCE is used to gate the μPD8259A's cascade address onto the processor's local bus, where ALE strobes it into the address latches. This occurs during the first $\overline{INTA}$ cycle. During the second $\overline{INTA}$ cycle the addressed slave μPD8259A gates its interrupt vector onto the processor bus.

The ALE signal occurs during each machine cycle and is used to strobe data into the address latches and to strobe the status ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$) into the μPB8288. ALE also occurs during a halt state to accomplish this.

The CEN (Command Enable) is used to control the command lines. If pulled high, the μPB8288 functions normally, and if grounded, all command lines are inactive.