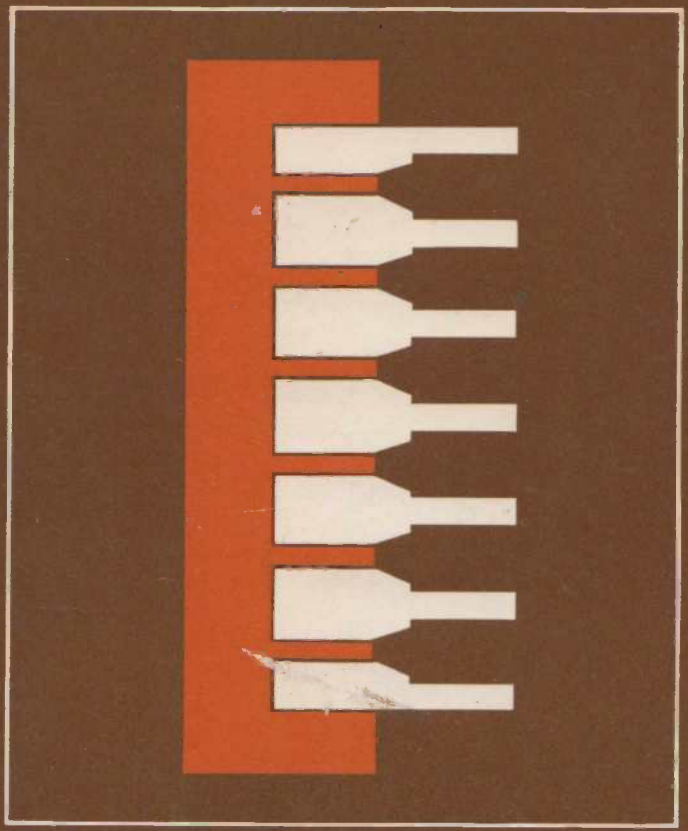
50 CMOS IC Projects

R. A. PENFOLD



50 CMOS I.C. PROJECTS

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by

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Chapter 1

INTRODUCTION TO CMOS I.C.s

Although CMOS I.C.s are a range of digital devices, they are suitable for a range of applications which is far more diverse than one might expect. In fact, there can be little doubt that these I.C.s are the most useful range of digital devices for the average amateur user, and are perhaps even the most useful range of I.C.s of any type.

When CMOS devices were first introduced in the early 1970s they were much more expensive than their alternatives in other logic families. This is not the case these days, and they are now about the cheapest I.C.s available. The more simple of the devices in the CMOS range cost less than many ordinary transistors, and on a cost basis these I.C.s are just about unbeatable.

Earlier families of digital devices suffer from three main disadvantages which limit their usefulness to the amateur. They require relatively high supply currents (about 20 mA for a simple quad gate I.C.), supply voltages are rather critical (5 V ± 10% for TTL devices for instance), and input impedances are usually rather low, often being only in the region of a few hundred ohms.

CMOS devices do not have any of these disadvantages. They require only very modest supply currents, and even some quite complex devices, such as the 4046 low frequency phase locked loop will operate at supply currents of less than 1 mA. Simple gates, when they are in a static condition, use virtually no power at all.

The supply voltage range over which a CMOS device will operate depends upon the suffix given after the type number. The devices usually supplied to amateur users, and specified for the projects in this book, have an 'AE' suffix. The 'A' of the suffix denotes that the unit has an operating voltage range of 3 to 15 V, and the 'E' indicates that it is contained in a standard DIL plastic encapsulation.

Input impedances of CMOS I.C.s are extremely high indeed, being something in the order of 1,000,000 Megohms. For all practical purposes they can be regarded as having an infinite input impedance, and are voltage rather than current operated devices.

Basic Gates

The most simple of CMOS devices is the inverter, which uses only two active devices. The circuit of an inverter is shown in Figure 1. This uses a single P Channel Igfet (insulated gate field effect transistor) and one N Channel Igfet. This is, of course, a switching device and the input is therefore only maintained in one of two states. It is either

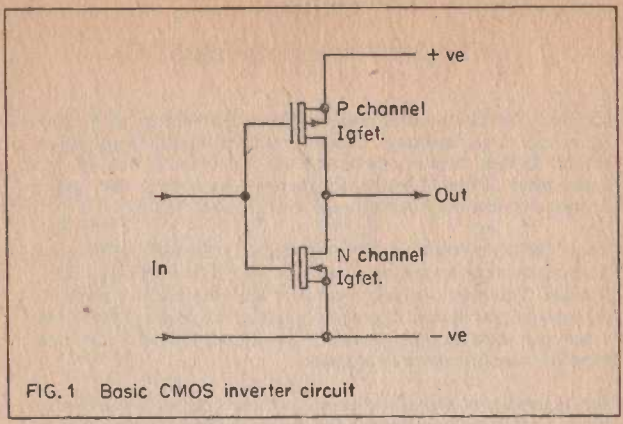

FIG. 1 Basic CMOS inverter circuit

high, which means that it is at or near the positive supply potential, or it is low, which means that it is at or near the negative supply potential. These states are often referred to as logic 1 and logic 0 respectively.

The output of the circuit can also have only two stable states, and again these are the high and the low states. The purpose of the inverter, as its name suggests, is to have an output state which is the opposite of the input one.

Operation of this circuit is quite simple to understand. An Igfet has a very high drain to source resistance when its gate is at around the same potential as its source. If a forward bias of a couple of volts or more is applied to its gate then the drain to source resistance falls to a value of only a few hundred ohms.

Thus, when the input of the inverter is low, Tr1 is turned hard on and Tr2 is hard off, and the output of the device is in the high state. When the input is high, Tr1 is off and Tr1 is on, and the output is low. The transistors are acting as simple S.P.S.T. switches, and Figure 2(a) shows the effective circuit of the unit in the high output state, and Figure 2(b) shows the effective low output circuit.

One could gain the impression from this that the circuit never consumes any current, but this is not the case. The transistors do not form perfect switches, and they have a resistance of a few hundred ohms when on, and a few thousand Megohms when off. Thus a minute, but for most purposes an insignificant current does flow through a static inverter.

A very brief pulse of current is consumed by the device as it changes state, as in effect, one switch closes before the other opens as the

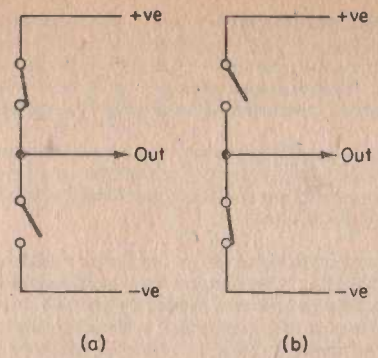

FIG.2(a) The effective high output circuit, and (b), the effective low output circuit

circuit goes from one output state to the other. Therefore, the more frequently the device changes state, the higher its current consumption. When used at fairly low frequencies CMOS I.C.s have very low current consumptions, but when used at high frequencies the current consumption can rise to many mA per device. Because of this it is usual to confine the use of CMOS I.C.s to medium and low speed applications.

Many of the projects described in this book are based on inverters, but these are not of the type just described. Instead, it is more convenient in use to use NOR and NAND gates with the inputs connected in parallel. For most circuits either a 4001 quad two input NOR gate or a 4011 quad two input NAND gate is specified. Four inverters can be made from each device, and they have the same characteristics as the basic inverter just described.

Manufacturers

CMOS I.C.s are manufactured by more than one company, and each company uses a different prefix to the type number. Most CMOS I.C.s offered to the amateur seem to originate from R.C.A. and have their CD prefix (CD4011AE for example). Some firms offer Motorola devices which have a 1 prefix (such as 14011), and others just give the basic type number.

Any of these I.C.s will work perfectly well in the circuits described here.

CMOS Protection

As many readers will be aware, Igfets are easily damaged by high voltage static charges. Such charges exist in most households these days due to the widespread use of plastics which tend to generate static charges. Even someone wearing a nylon shirt is said to be a potential source of destruction as far as an Igfet is concerned.

One might think that CMOS devices were very delicate, and virtually impossible to use. This is not in fact the case, as all recent CMOS I.C.s are equipped with internal protective diodes which limit voltages at the inputs to a safe level.

Even so, it is still advisable to obey a few simple rules when handling and using CMOS I.C.s. These devices are usually supplied with their leadouts embedded in a piece of conductive foam. It is a good idea to leave the device in this foam until it is actually going to be used. Do not plug or unplug a CMOS I.C. from an I.C. holder while the supply is connected. Make quite sure that the supply is connected with the correct polarity. When using I.C. holders it is an easy matter to accidentally plug an I.C. into a socket the wrong way round. This results in the supply being connected with incorrect polarity, and almost certainly causes the destruction of the device when the power is switched on.

In many of the circuits to be described here, some of the gates of an I.C. are not used. It is not a good idea to simply ignore the unused gates. There is little risk of the gates being damaged by static charges and other sources of electrical signals, but these will operate the inputs of the gates.

As mentioned earlier, a static gate uses no significant current, but it is switching continually from one state to the other, it will use supply current. Therefore, the inputs of unused gates should be connected to one or other of the supply lines (whichever happens to be the most convenient), as otherwise stray pick up will operate the gates causing a waste of power.

Final Points

CMOS devices have a wide operating temperature range, the actual range being −40 to +85 degrees centigrade for the plastic DIL versios (−55 to +125 degrees centigrade for the ceramic and flatpack versions). They are therefore perfectly suitable for use in automotive and similar outdoor applications.

If the output of a CMOS device should happen to be accidentally short circuited to one of the supply lines, a current of many mA will flow. The amount of current that flows will depend upon the power supply voltage used, but the resistance of the output transistor which is turned

on will limit the output current to a safe level, and will protect the device against damage.

CMOS I.C.s have a high level of fanout as although they have only a comparatively low output current drive capability, input current requirements are extremely low. The level of fanout is only really limited by the input capacitance of the devices, and the minimum fan-out figure for CMOS devices is 50.

Chapter 2

MULTIVIBRATOR PROJECTS

CMOS inverters can be connected to form any of the three types of multivibrator circuit (astable, bistable, and monostable). In this chapter each type of multivibrator will be dealt with in turn, and apart from basic circuit details of each type, several practical projects will also be covered.

ASTABLE CIRCUITS

Astable, or free running multivibrator circuits are one of the most frequently used electronic building blocks in amateur electronics. This type of circuit merely consists of two inverting amplifier stages with cross coupling between the inputs and outputs. The positive feedback through the cross coupling causes the circuit to oscillate continuously and violently with a squarewave output being produced.

The circuit diagram of a CMOS equivalent of a conventional discrete multivibrator is shown in Figure 3. Resistors R1 and R2 are used to bias the inverters as linear amplifiers, and the two capacitors provide the cross coupling.

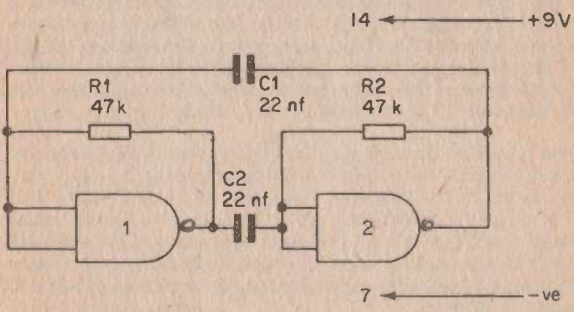

FIG. 3 Basic conventional 1 kHz astable multivibrator

This circuit can be simplified slightly by using direct coupling between inverter 1 and inverter 2. This does away with the need for the coupling capacitor which was formerly used here, and it also obviates the need for the bias resistor for inverter 2 (see Figure 4).

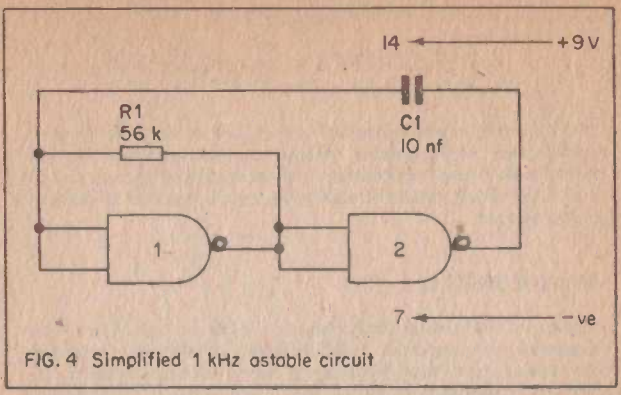

FIG. 4 Simplified 1 kHz astable circuit

The circuit operates in the following manner. When the supply is initially connected the output of one gate will go to the high state while the other will go to the low state. Which of these states the circuit assumes is unpredictable since it depends upon the characteristics of the two gates. For the sake of this explanation we will assume that inverter 1 has a high output, and inverter 2 has a low output.

C1 will begin to charge up from the high output of inverter 1 via R1. After a length of time which is determined by the values given to R1 and C1, the voltage across C1, and thus also at the input of inverter 1, will reach the transfer voltage of inverter 1. This results in the output of inverter 1 going low, and in doing so drives the input of inverter 2 low. This causes the previously low output of inverter 2 to go high. As this occurs C1 is discharged into the inverters.

Now C1 starts to charge up from the negative supply through R1, which is connected to the now low output of inverter 1. As C1 charges up, the voltage at the inverter 1 will gradually fall, and after a time determined by the time constant of C1 and R1, the transfer voltage of the gate will be reached. This drives the output of inverter 1 high, which in turn takes the input to inverter 2 high. This causes the output of inverter 2 to go low, and C1 is again discharged through the inverters as this all happens.

The circuit operation then commences at the beginning again with C1 charging via R1 from the high output of inverter 1. The circuit thus continually oscillates with antiphase squarewave outputs being produced at the outputs of the inverters.

This circuit has several advantages over a conventional discrete component multivibrator. As we have already seen, it has only two frequency

determining components rather than the usual four. Also it can be made to operate over a very wide frequency range. At the low frequency end of the spectrum this is due to the very high input impedances of the inverters. This enables very high values to be used for R1, which when used in conjunction with a high value for C1 enables an operating frequency of less than one cycle per hour to be attained. On the other hand the circuit will operate reliably using a capacitor of a few pF in value and a resistor of a few K ohms. Operating frequencies into the Meg Hertz region are then possible.

Another advantage of this circuit is its low level of current consumption. At frequencies within the audio frequency spectrum, or below it, the circuit has a current consumption of less than 500 microamps from a 9 volt supply.

One drawback of the circuit is that the frequency of operation tends to vary with fluctuations in the supply voltage, and it also varies somewhat between individual circuits built to the same design due to variations in the transfer voltages of individual inverters. However, in most applications this is of no great significance.

Squarewave Generator

Perhaps the most obvious use for an astable multivibrator is as the basis of an audio squarewave generator. The circuit diagram of such a unit is shown in Figure 5.

This is basically just the circuit which was described in the previous section, except that the timing capacitor is actually three switched components, and the timing resistance has been made variable. The three switched capacitors provide the unit with three ranges, the output frequency being variable over these ranges by means of VR1. The three ranges are as follows:—

Range 1	20Hz	to	200Hz
Range 2	200Hz	to	2kHz
Range 3	2kHz	to	20kHz

Thus the unit covers the whole of the audio frequency spectrum. There is actually a slight overlap between ranges so that any variations in frequency coverage between individual units should not create any gaps in the frequency coverage.

As is common to all astable multivibrator circuits, the output waveform of this circuit is not a very good squarewave, with severe rounding at the top of the leading edge of the waveform. This is illiminated by using a third inverter as a buffer at the output. The multivibrator chops this from one state to the other with a high quality squarewave being produced at the output. VR2 is the output level control, and the maximum peak to peak output voltage of the unit is fractionally less

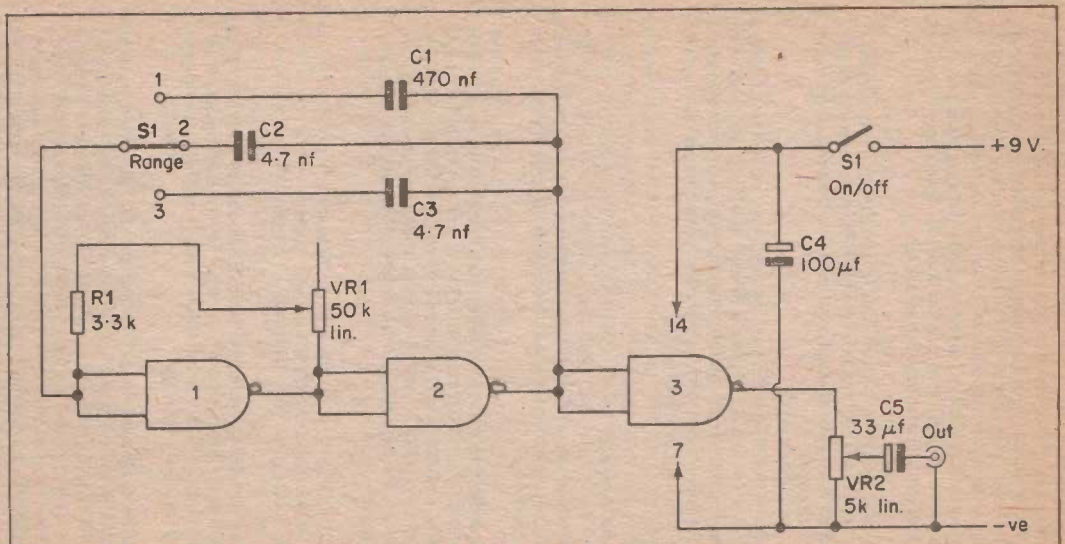

FIG. 5 Wide range squarewave generator

than the power supply voltage.

A dial calibrated in frequency can be marked around the control knob of VR1 using any of the usual methods for output frequency determination. Provided C1 to C3 have reasonably low tolerances, say 5% or less, a single 20 to 200 scale will suffice for all three ranges (multiply by ten for range 2, and by 100 for range 3).

The pin identification diagram for the 4001 and 4011 devices is shown in Figure 6. These both use the same leadout arrangement.

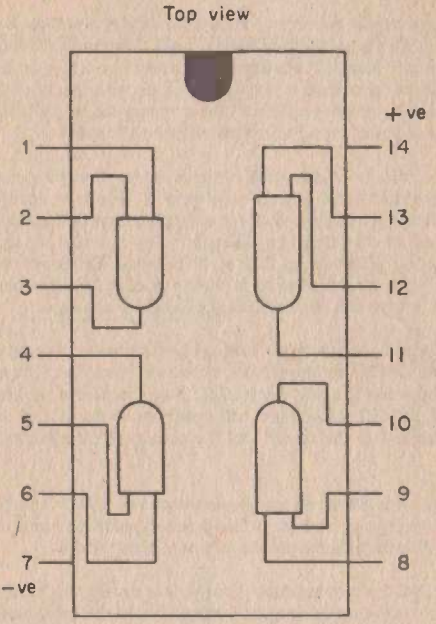

FIG. 6 Details of the pinning of the 4001 and 4011 I.C.s

Water Level Alarm

One of the most widespread uses of astable multivibrators is in the generation of alarm signals of various types. The squarewave output is very strident and is not easily missed.

Ordinary CMOS gates are unable to provide sufficient output power to properly drive even a minature loudspeaker, and it is necessary to use a stage of amplification between the output of the tone generator and the loudspeaker.

Figure 7 shows the circuit diagram of a water level detector which uses a CMOS multivibrator. This type of alarm can be used in various applications, such as for monitoring the water level in the bilges of a boat, and sounding a warning if the level rises above a predetermined point. They also have household applications, and can be used as rain alarms, or to indicate when the water level in a bath has reached the required level.

Basically the circuit consists of an astable driving a common emitter transistor stage via an inverter/buffer stage. R3 limits the base current to Tr1 to a safe level. The loudspeaker forms the collector load for Tr1, and in consequence a large pulse of current is passed by the speaker each time the output of the inverter/buffer goes high. This causes a loud audio tone to be emitted from the speaker.

The timing resistor of the multivibrator is not directly connected between the input and output of inverter 1, but is connected via a sensor. The sensor is a simple device that has two electrodes which are arranged so that they are bridged by water when it reaches the required level (or rain drops fall on the sensor). The sensor normally acts as an open circuit, and so it does not complete the bias circuit of inverter 1 with the circuit failing to oscillate as a result.

When the sensor contacts are bridged by the water, the sensor will exhibit a relatively low impedance as the water will provide a conductive path between the two electrodes. This completes the bias circuit and the alarm will sound, and will continue to do so for as long as power is applied to the circuit and the sensors electrodes are bridged by water.

It is worth noting that although pure water is a poor conductor of electricity, rain, tap, and sea water contain sufficient impurities to produce a low impedance path between the electrodes.

R2 is required for two reasons. Firstly, it is not a good idea to leave an inverter's input open circuit, as would otherwise be the case here when the alarm is not sounding. This is because it will tend to pick up stray interference which would cause a continuous noise to be produced from the speaker. It would also result in wasted power.

Secondly, this resistor ensures that when the alarm is not operating, no current flows through the speaker. By taking the input of inverter 1 high under static conditions R2 ensures that the output of inverter 3 is low, and Tr1 is cut off. If the circuit was to latch in the opposite state (inverter 3 output high) a considerable quiescent output current would flow.

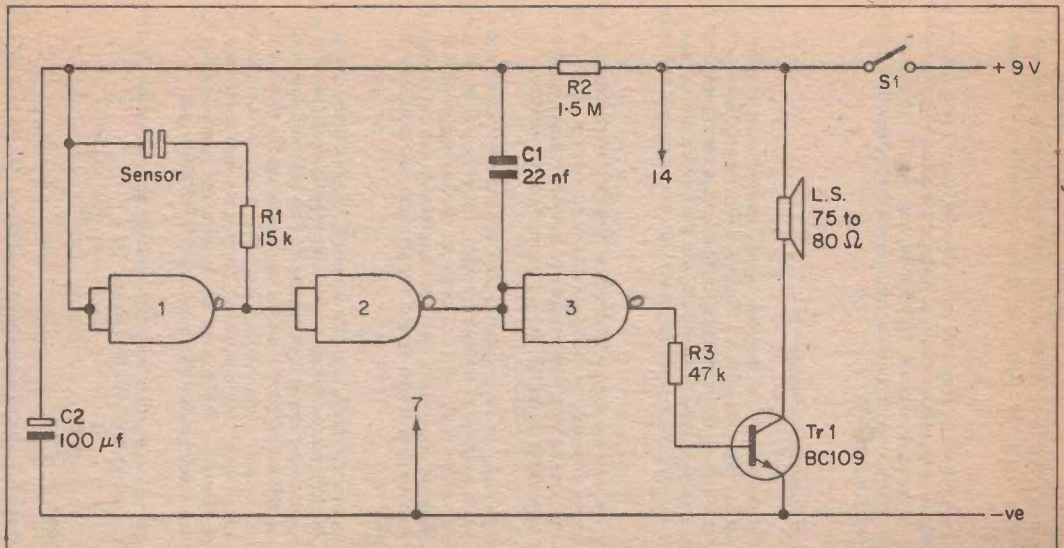

FIG. 7 Water level alarm circuit

The circuit has a static current consumption of only a minute fraction of a micro-amp, and it is economically viable to power the unit from a battery even if it is to be used for very prolonged periods. The current consumption when the alarm is operating is something in the region of 18 mA.

Unless the leads to the sensor are exceptionally long, or pass close to a mains lead or some similar source of electrical interference, there is no need for them to be screened. If this cable does need to be of the screened variety, a single screened type can be used (outer to R1, inner to inverter 1 input).

Christmas Tree Lights Flasher

Several useful gadgets can be made using a multivibrator to drive a relay, and a popular example is a Christmas Tree Lights Flasher. This will provide a much more regular flashing rate than can be obtained by using a bi-metal type flashing bulb, and the flashing rate can also be made variable. The circuit diagram of this device appears in Figure 8.

The two inverters are connected as a low frequency astable circuit, and the operating frequency of this is variable over a range of about 0.5 to 1.5 Hz by means of R1. The output of inverter 2 drives common emitter amplifier Tr2, via R3. R3 is a current limiting resistor.

Tr1 has the relay coil as its collector load, and the relay will be energised when the output of inverter 2 is high. The relay will be off when the output of inverter 2 is low. A single set of relay contacts (either normally closed or normally open ones) are used to control the lights. These will therefore switch on and off at a rate determined by the setting of R1.

D1 is a protective diode, and this is needed to protect the circuit against the high reverse voltage which is developed across the relay coil as the power to the circuit is switched off. This voltage is generated by the magnetic lines of force quickly decaying and cutting through the relay coil. Because of the speed at which this magnetic force dies away, quite a high voltage can be produced, but it is at a high impedance. D1, in effect, shorts out this voltage, and is protected against passing an excessive current by the high source resistance of the signal.

D1 should not be omitted from the circuit as this voltage spike is quite capable of destroying both the I.C. and Tr1.

Metronome

A low frequency astable multivibrator can be used as the basis of a very simple metronome, and the circuit diagram of such a metronome appears in Figure 9.

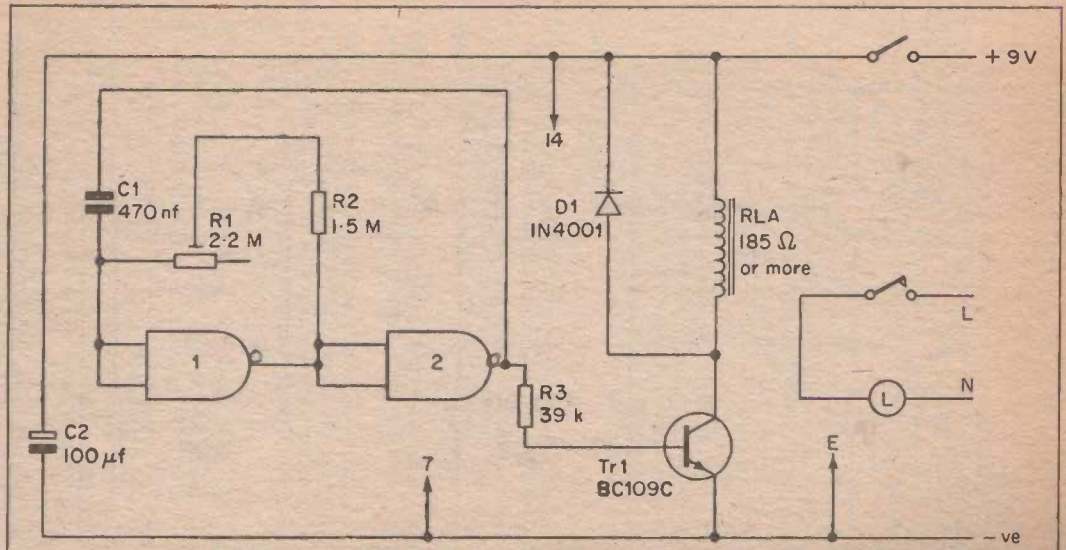

FIG. 8 Christmas tree lamps flasher

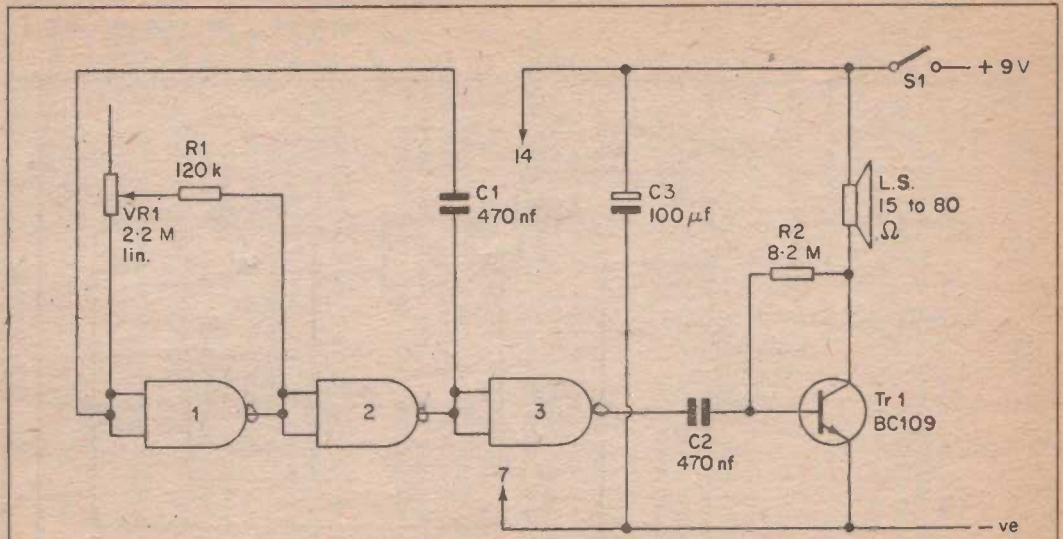

FIG. 9 Metronome circuit

Inverters 1 and 2 are used to form the astable circuit, which has a continuously variable frequency range of approximately 0.5 to 5Hz. The frequency is adjusted by means of VR1.

The output of the multivibrator is fed to an inverter/buffer stage, and the output of this drives a single transistor output stage. R2 is the base bias resistor for the output transistor (Tr1), but this has a very high value and it does not bias Tr1 into class A operation. It only takes Tr1 just beyond the threshold of conduction, and this stage actually works in the class B mode.

When the output of inverter 3 goes positive, a brief positive pulse is fed to the base of Tr1 by way of C2, and this turns Tr1 hard on for the duration of the pulse. This causes a brief but fairly large pulse of current to be passed by the speaker which forms the collector load for Tr1. C2 has purposely been given a fairly low value so that the duration of this pulse is short, and a click of a fairly high pitch is produced from the speaker. This makes a very good simulation of the click produced by a conventional metronome. Of course, a click is produced each time the output of inverter 3 goes high, and this results in about 40 to 300 clicks being produced each minute, the required rate being set using VR1. A beat rate of 40 to 300 per minute covers all normal musical requirements.

When the output of inverter goes negative, no significant audio output is produced. This is because the output transistor will be cut off by the negative voltage pulse which is supplied to its base. Being biased into class B operation, Tr1 is virtually cut off anyway, and the negative pulses therefore have no real effect on the output stage.

This gives the unit a very low average current consumption, and the current consumption of the prototype is only about 2 mA.

A dial calibrated in beats per minute should be marked around the control knob of VR1, and this is quite simple to accomplish. The range of operating frequencies is so low that it is quite easy to count the number of beats per minute produced with VR1 at various settings. The dial is then calibrated at these settings.

It is advisable to try to find settings that correspond to beat rates that are divisible by five or ten, as a dial calibrated at points such as 40, 70, 100, 150 etc., will look more neat than one calibrated at points such as 42, 71, 98, 153 etc. Unfortunately, the only way to find the desired calibration points is by trial and error, and this is likely to be time consuming. It is possible to save a certain amount of time by counting the number of beats in a 15 second period and then multiplying this by four to find the numbers of beats per minute, rather than by doing a straight forward minute count. This should not be done at the lower calibration points because accuracy could suffer as a result of this.

Transistor Tester

Most transistor testers are designed to test a transistor which has been removed from its circuit, or to test it prior to being connected into circuit. Provided one does not want to actually measure the gain or some other parameter of the device under test, it is usually quite possible to test the device while it is connected into circuit. The circuit diagram of such a 'Go' – 'No Go' tester is shown in Figure 10.

The idea of this circuit is simply to apply a periodic forward bias to the base of the transistor while monitoring its collector current. The bias signal is obtained from the output of an inverter which is driven from a low speed astable circuit. The collector current is monitored by a light emitting diode indicator (D1).

If we consider the circuit first in the p.n.p. testing mode. When the output of the inverter is high, the base of the transistor will be at virtually the same potential as its emitter, and it will therefore not conduct. The L.E.D. will not light up since it will receive no significant current.

When the output of inverter 3 goes low, a large forward bias is applied to the test transistor which should, in consequence, be biased into saturation. A large current will flow through D1 which will light up.

Thus if the transistor under test is a good operational device, upon connecting the test prods to it, the L.E.D. indicator should flash on and off (at a rate of around 1 Hz).

If the test transistor is a closed circuit device, then of course the bias will have no effect, and D1 will be on all the time. If the transistor is an open circuit device, then D1 will not come on at all.

The circuit operates in precisely the same manner when it is switched to the n.p.n. mode, except that the transistor is cut off when the output of inverter 3 is low, and saturated when it is high. The unit is used in exactly the same way whichever mode it is in.

It should perhaps be pointed out that this circuit is not fool-proof, and it can give misleading results. This is because the base and emitter of the test transistor are not genuinely short circuited together when the device is supposed to be cut off. It is therefore just possible that circuit resistances could bias the transistor on. It is also possible that circuit resistances could supply a path for the L.E.D. current flow. Thus the L.E.D. could be continually on even though the test transistor is sound.

It is also possible that the L.E.D. could fail to come on even if the transistor is operational. This could occur if it has a low resistance in its base – emitter circuit, as the potential divider effect between this and R2 of the tester could produce a base – emitter voltage of insufficient level to turn the transistor on.

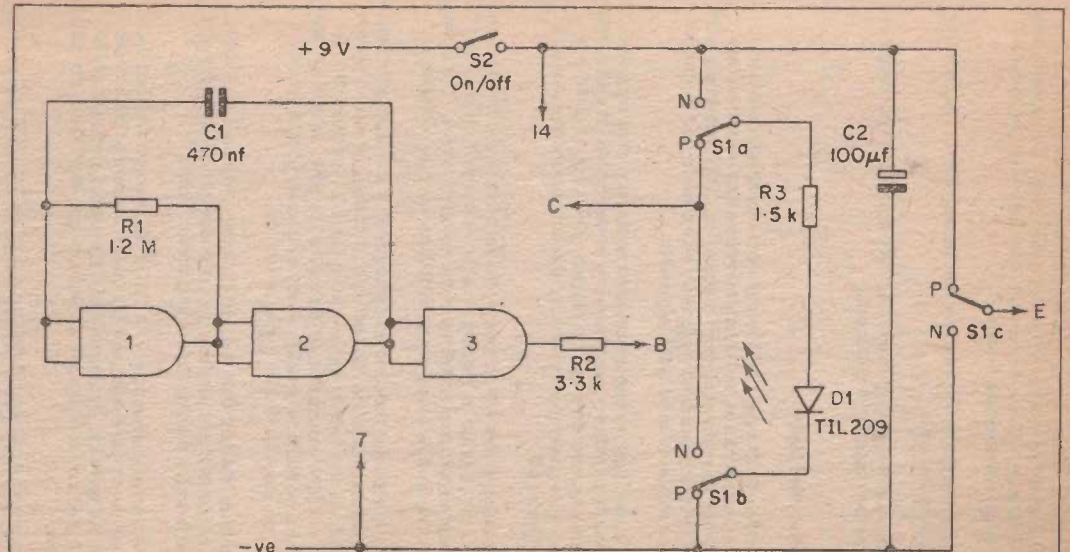

FIG. 10 Transistor tester circuit

Results obtained with this tester should not, therefore, be regarded as being infallible. When testing ordinary low level transistor stages the device is unlikely to produce erroneous results, since the necessary low circuit resistances will not be present. Caution should be exercised when testing power devices though.

It can be said in favour of this tester that its usefulness is disproportionate to its very low cost.

One final point is that no power should be connected to the circuit in which the test transistor is employed.

Low Power Pilot Light

It is advisable to fit a pilot light to any item of electronic equipment, such as signal generators, and electronic voltmeters, where it is easy to inadvertently leave the equipment switched on. This is especially so in the case of battery operated equipment, where leaving the equipment turned on will prove to be rather expensive.

Fitting a pilot light to battery operated equipment does represent something of a problem since in order to be worthwhile, the pilot light must consume very little battery current. Otherwise it could well consume more power than is saved by always remembering to switch the equipment off.

Light emitting diodes will provide visible light from quite low operating currents, but in order to provide a really noticeable light level they really need to consume something in the region of 10 mA. This is more than is consumed by many pieces of battery operated equipment.

One way of reducing the current consumption of an L.E.D. pilot light is to use a pulsing technique. For example, if during one second periods the L.E.D. is only briefly turned on for (say) 0.1 seconds, then the average current consumption will be reduced by 90%. In this way the L.E.D. can be made to produce a very noticeable pilot light with a current consumption of only 1 mA or even less.

Furthermore, the fact that the light is flashing will tend to make it more noticeable than one which is on continuously. Thus, although it uses less power, a flashing pilot light is more efficient.

The low current consumption of a CMOS I.C. makes it the ideal basis for a low power pilot light, and the circuit diagram of such a unit appears in Figure 11. Inverters 1 and 2 are used as an astable multivibrator, and inverter 3 is used as a buffer stage which drives the L.E.D. indicator.

It will be seen from Figure 11 that the astable circuit is a modified version of the type used in the previous circuits. The timing resistor

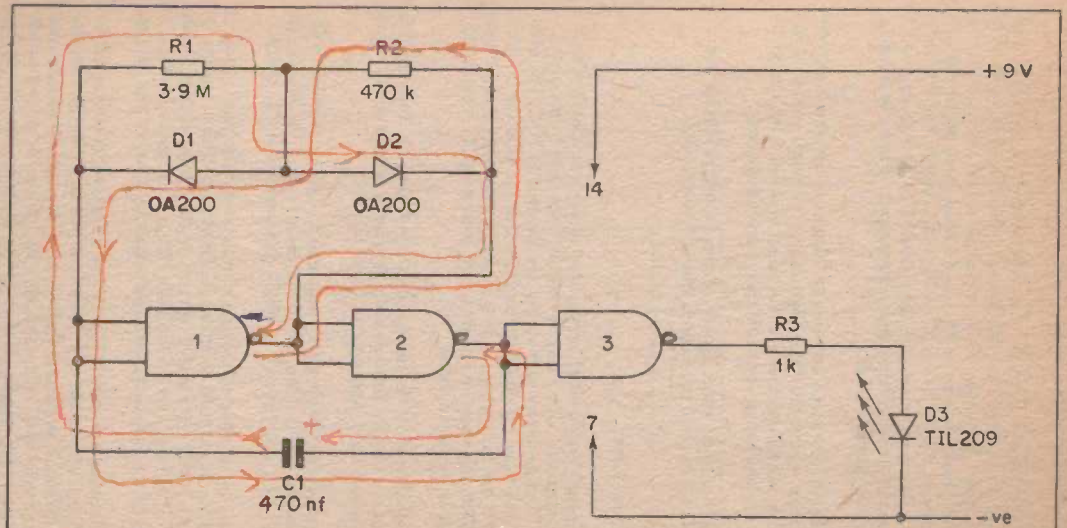

FIG. 11 The low power pilot light

has been divided into two separate components (R1 and R2), and steering diodes have been added (D1 and D2).

In effect, these diodes short out one resistor when C1 is charging from the positive supply, and the other resistor when it is charging from the negative supply. It charges from the positive supply via R1, and from the negative supply by way of R2. As R1 has a much higher value than R2, the output of inverter 2 is in the high state longer than it is in the low state. This must be the case since it will take the voltage across C1 longer to reach the transfer voltage of inverter 1 when C1 is charging through the higher resistance.

An inverter in interposed between the output of inverter 2 and the L.E.D. circuit, and so the voltage here is low for longer periods than it is high. The circuit operates at a frequency of about 1 Hz, and so D1 is briefly switched on at approximately 1 second intervals.

The average current consumption of the prototype circuit was measured at about 900 micro-amps from a 9 volt supply.

0–10 Second Timer

This is a simple device which produces an audio tone shortly after a switch is operated. The delay is variable from zero to about ten seconds. Simple timers such as this can be used in T.V. type quiz games where there is a time limit during which the question must be answered if one is to score. They can also be employed in other games, such as lightning chess or draughts, and there must be many other possible uses for such devices.

The circuit diagram of the timer is shown in Figure 12. Inverters 1 and 2 are used as a straight forward audio frequency astable circuit which actually operates at a frequency of about 500 Hz.

The output of the astable is fed to a common emitter amplifier via a pulse enabling circuit. This merely consists of one of the NAND gates of a 4011 I.C., and the way in which this operates is very simple.

When the control input of the gate is in the low state, input signals at the signal input will have no effect on the output. This is because the output of a NAND gate is high unless both the inputs are high, in which case the output takes up the low state. Thus if the control input is low, the state of the signal input is irrelevant as the output will be high.

Therefore, when the control input of gate 3 is low, its output will be high and Tr1 will be cut off. No sound will be produced from the speaker. When S1 is opened, the voltage at the control input of gate 3 will begin to rise as C3 charges up via VR1. When the voltage across C3 goes above the transfer voltage of the enabling gate, the output state of this gate will be dependent upon the signal at its other input

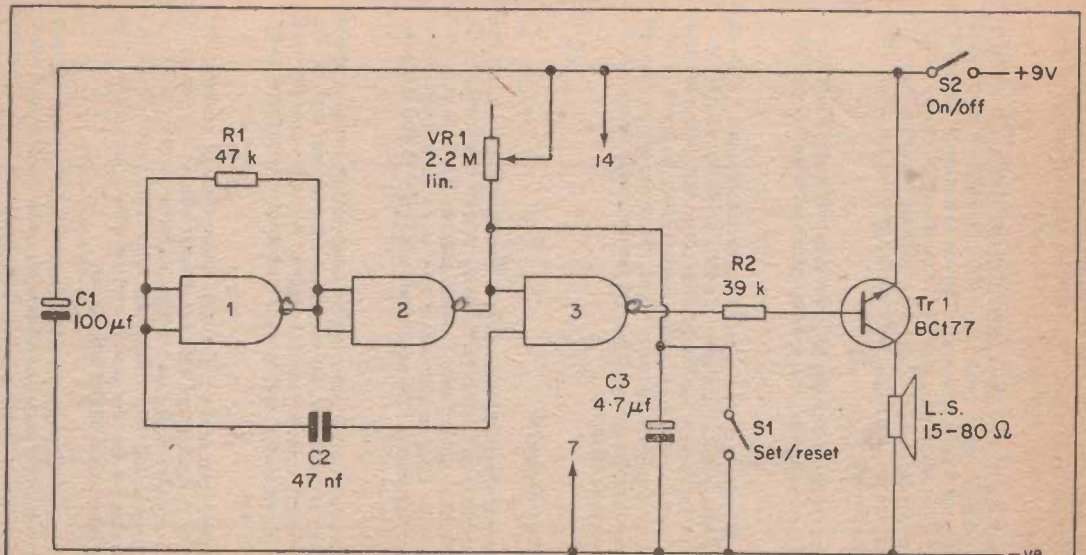

FIG.12 0–10 sec. timer. Only use IC 4011 in this circuit

When the signal input is low the output is high, and the output is low when the signal input is high. Tr1 will then be pulsed on and off and an audio tone will be produced from the speaker.

The time taken for the voltage across C3 to reach the transfer voltage of gate 3 depends upon the setting of VR1. When this is adjusted for zero resistance there is zero delay. This can be increased to a maximum delay of about ten seconds with VR1 at maximum resistance. Note, however, that the maximum time delay will vary somewhat between individual circuits due to the wide tolerances of certain components (C3 in particular).

The circuit is reset by closing S1 which then discharges C3 and thus cuts off the audio tone. A new timing period is started by opening S1 again.

A 4001 I.C. Is not suitable for use in this circuit since gate 3 is not used as an inverter, and the NOR gates of a 4001 would not provide the required circuit action. Although in this circuit explanation the inputs of gate 3 were termed the signal and control gates, the inputs to this gate can be connected either way round. Whichever one is connected to C3 becomes the control input and the one connecting to gate 2 becomes the signal input.

Pulsed Tone Generator

Two circuits using audible alarms have been described so far, and these both use simple continuous tone circuits. A more effective alarm can be produced by either having a tone of varying pitch (such as police car sirens), or by using an intermittent tone (as do many burglar alarm systems for instance). The circuit shown in Figure 13 is of the latter type.

Here inverters 1 and 2 form a low frequency astable having an operating frequency of about 1 Hz, and inverters 3 and 4 are used as an astable tone generator operating at a frequency of very approximately 800 Hz. Gate 3 is not used as a straight forward inverter, but is used as an enabling gate.

When the output of the L.F. astable is low, the tone generator will obviously be blocked and will be unable to oscillate. When output of the L.F. astable is high, gate 3 will function as an ordinary inverter and the tone generator will function normally. Thus the low frequency astable switches the tone generator on and off at a rate of about 1 Hz, and an intermittent output is produced.

Gate 3 is used as the control gate rather than gate 4, as with the alternative method the output of the tone generator would be high when the circuit was in the muted state. This would turn Tr1 on and would result in increased current consumption.

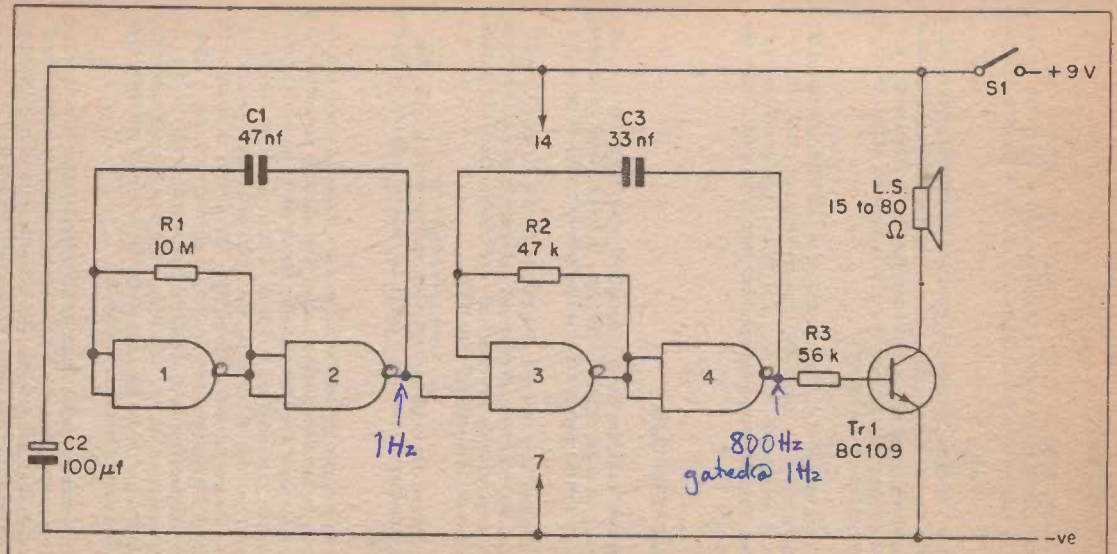

FIG. 13 Pulsed tone generator circuit (use only 4011)

Pulsed Output Timer

It is a simple matter to modify the pulsed tone generator circuit to produce a simple timer of the type described earlier, but with a pulsed output of course. The circuit diagram of this device appears in Figure 14.

Here gate 1 is used as an enabling gate, and the control input is normally held in the low state by S1. This prevents the low frequency astable from oscillating, and causes its output to be in the low state. This causes the tone generator astable to also be blocked, and so no output is produced from the speaker.

When S1 is opened, C4 begins to charge up via VR1, and when the potential across C4 exceeds the transfer voltage of gate 1, the low frequency astable will turn on. The pulsed tone generator then functions normally with an intermittent tone being emitted from the speaker.

BISTABLE CIRCUITS

The bistable is the simplest of the multivibrator family, but it is not used nearly as much as the astable type. In fact it is rarely encountered in circuits for the amateur, but it can be very useful on occasions.

A bistable can be very easily constructed from a couple of CMOS inverters, and only two resistors and two push button switches are needed in addition to the inverters. The circuit diagram of a basic CMOS inverter is shown in Figure 15.

In this type of circuit one output is low and the other is high. The circuit therefore has two stable states, and it is from this that it derives its name.

Which output goes high and which goes low when the power is initially connected to the circuit depends upon unpredictable parameters. It is mainly dependent upon the operating speeds of the inverters. Assume for example, that inverter 1 is capable of faster operation than inverter 2. When the supply is turned on, the inputs of both inverters will be low, and the outputs will try to go high. The output of inverter 1 will go high at a faster rate than the output of inverter 2, and a rising voltage will therefore be coupled from the output of inverter 1 to the input of inverter 2 via R1. This voltage will have the effect of holding inverter 2 output in the low state while the output of inverter 1 goes high. The circuit then rests in this state.

The circuit can be made to take up the opposite state by momentarily operating push button switch S2. This takes the input of inverter 2 low and its output to go high. This takes the input of inverter 1 high as this is connected to the output of inverter 2 via R2. In consequence

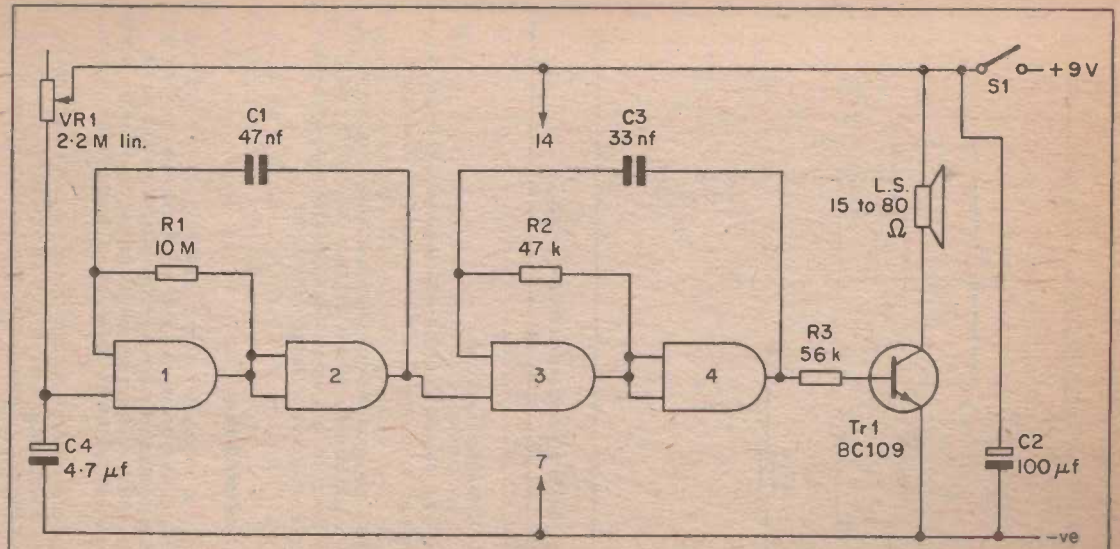

FIG. 14 Pulsed output 0–10 second timer (use only 4011)

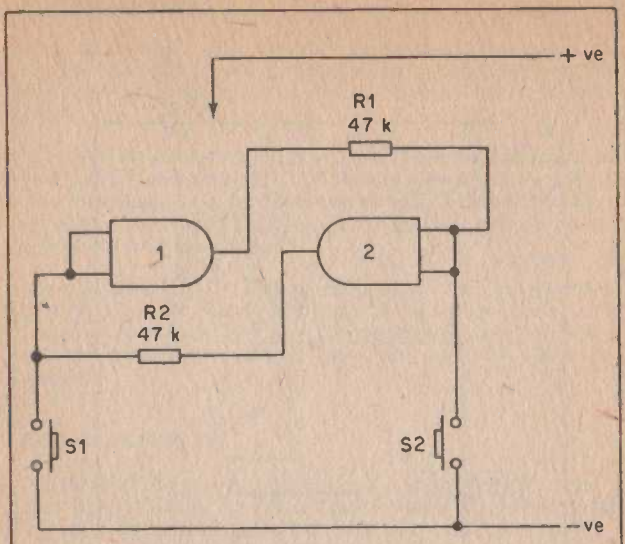

FIG. 15 Basic bistable multivibrator circuit

the output of inverter 1 goes high.

Even when S2 is released, the circuit will remain in its new state. It can be returned to its original state by operating S1 momentarily.

This circuit forms a sort of simple electronic memory, because once it is set in a certain state it remains in that state, and could be said to remember that state. It is also sometimes referred to as a latch, since once set in a certain state it latches in that state.

Switch Precedence Indicator

One popular use of bistable circuits is in switch precedence indicators. This is the type of device which is used in T.V. type quizzes where the first person to press his or her switch has the first opportunity to answer the question. The purpose of the device is to render the unoperated switches inoperative the instant one of the switches is closed.

Similar games are often played in the home, and such a device can be used when playing games such as snap, the well known card game. The circuit diagram of a simple switch precedence indicator is shown

in Figure 16.

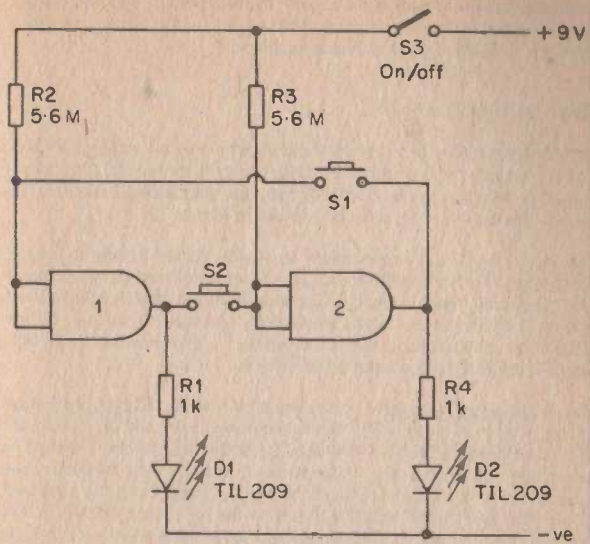

FIG. 16 Circuit diagram of the switch precedence ind.

Both lamps are off when neither of the switches are closed, since the input of each inverter will be taken high by its bias resistor (R2 and R3). The output of each inverter will therefore be low, and neither L.E.D. indicator will be supplied with any current.

If one of the push button switches is operated, say S1, then the appropriate indicator lamp will come on. In this case it will be D1 that will come on, as the input of inverter 1 will be taken low by being connected to the low output of inverter 2.

If S2 is now operated, D2 will not come on because the output of inverter 1 is high, and closing S2 will merely keep inverter 1 input in its present state. Thus when a push button is operated the appropriate lamp will come on, and the other push button is blocked, and will have no effect on the circuit.

The circuit is reset ready for a new round to commence by simply releasing the push buttons.

This circuit, together with the simple timer described earlier, could form the basis of a simple reaction testing game. The timer would be set to give a delay of a few seconds and then it would be started. The two players would each have a push button switch, and the winner would be the person who operated his or her switch the most quickly once the audible alarm had begun to sound.

Heads Or Tails Simulator

Another popular type of novelty circuit which often employs a bistable circuit in some form or other is a heads or tails simulator. This kind of circuit is designed to electronically simulate the tossing of a coin. The circuit diagram of such a device appears in Figure 17.

Inverters 1 and 2 are connected as an astable circuit having an operating frequency of a few hundred Hz. The other two inverters are connected as a simplified bistable circuit. The simplification is merely that inverter 3 output and inverter 4 input are directly connected together, rather than being connected by way of a resistor. This is possible as no input signal is applied to the input of inverter 4.

The input signal is coupled to the input of inverter 3 from the output of the astable circuit via S1. When the power is turned on the input of the bistable will be rapidly switched from the high to the low state by the astable multivibrator. The input and output of the bistable are in phase, and so the output will also be rapidly going from the high to the low state. Each time the output goes to the high state, D1 will briefly be pulsed on. It will be flashing on and off at such a fast rate though, that to a human observer the flashing will not be perceivable, and the lamp will appear to glow continuously.

When S1 is opened, the bistable will latch in whatever state it was in at the instant S1 broke the continuity of the circuit. For instance, if the output of the bistable was in the high state when this occurred, its input will be held in the high position by the voltage which is coupled from output to input by R2. The L.E.D. indicator will therefore remain on.

The input of the bistable will similarly be held in the low state by this coupling if the output happened to be low at the instant S1 went open circuit, and in consequence the L.E.D. would go off.

The output from the astable circuit is a squarewave, and so the bistable is driven to the high and low states for equal lengths of time. It is therefore purely a matter of chance whether the indicator lamp remains on or switches off when S1 is operated. There is a 50-50 chance of it assuming any one of the two possible states, just as there is when one tosses a coin.

By classing the on state of the lamp 'heads', and the off state 'tails', the unit will thus simulate the tossing of a coin. Unlike some other heads

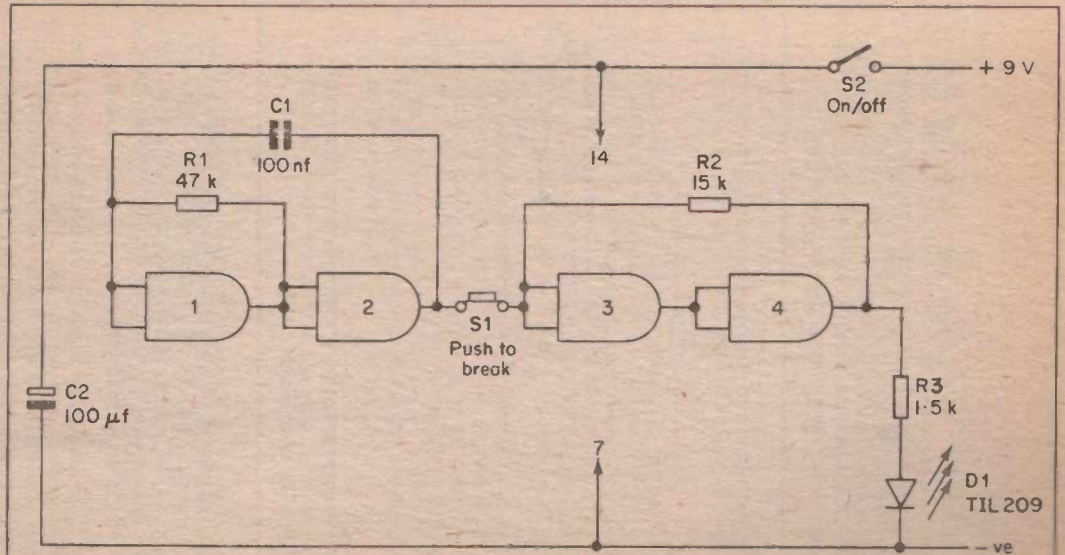

FIG. 17 Heads or tails simulator

or tails circuits, this one requires no adjustment or experimentation with circuit values in order to obtain proper 50–50 operation.

Touch Switch

Touch switches seem to have become quite popular these days, and although this is probably mainly due to their novelty value rather than any practical advantage, they do have certain practical advantages over more conventional forms of switch. Probably the main one in most applications is that they can be designed to have no moving parts to wear out. This makes them as reliable and hard wearing as the main (electronic) part of the equipment they are controlling.

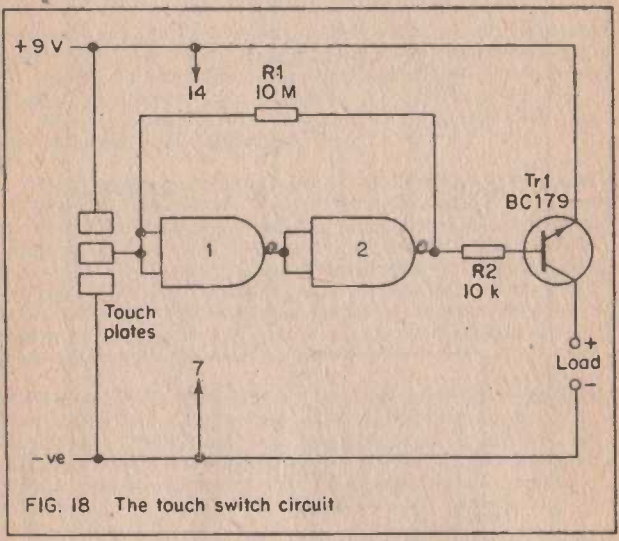

FIG. 18 The touch switch circuit

The circuit diagram of a simple touch switch using a CMOS bistable circuit is shown in Figure 18. This will provide on/off switching for any piece of 9 volt battery operated equipment which does not have a current consumption of more than 100 mA (the maximum operating current for the BC179 transistor).

CMOS I.C.s are ideal for use in this particular application since they can easily provide the necessary very high input impedances, and they also consume no significant current when they are not driving a load. The current consumption of this circuit in the off state is very low, being actually less than 1 micro-amp. There is subsequently no significant battery drain when the equipment is turned off, and the

battery life should not be significantly less than if a mechanical switch were used.

Extra current is consumed when the unit is in the on state, this mainly being the base current to turn on Tr1. This is unavoidable, but the additional current consumed is less than 1 mA, and is likely to be of no significance in the majority of applications.

The circuit operates in the following manner. When the power is initially connected to the device the output of the bistable will go into the high condition. Tr1 is cut off and no power is applied to the load.

It is possible to alter the state of the bistable by touching the lower set of touch contacts. The resistance of the operators skin then takes the input of the bistable low, and the output of the bistable will then also go low. A base current is then applied to Tr1 which is biased into saturation, and virtually the full supply rail potential is supplied to the load.

The unit can be switched off again by touching the upper set of touch contacts. The input of the bistable is then connected to the positive supply by way of the skin resistance of the operator's finger, and in consequence both the input and output of the bistable take up the high condition. Tr1 is therefore cut off once again, with no significant current being supplied to the load.

R1 provides the necessary latching action by holding the input in whatever state it was in when the finger of the user is removed from the touch contacts. If necessary, the sensitivity of the circuit can be boosted by raising the value of R1. Resistors having values of more than 10 Megohms are not readily available, and so an increased value for R1 can only be obtained by adding two of more resistors in series to make up the required value.

R2 is needed in order to prevent Tr1 from passing an excessive base current. It also limits this current to an economical level. If the unit is being used to control a fairly high current load, say 25 mA or more, it is necessary to reduce the value of R2 to 1 k.

With a little ingenuity it should not be too difficult for the constructor to fabricate suitable touch contacts. A piece of stripboard can be used to make a very simple but effective touch plate, or an even better one can be etched from a piece of copper laminate board. Even three screws (Pan or Countersunk heads) mounted on the front panel of the main equipment could be used if they are suitable positioned.

Relay Version

In some applications the above circuit will not be suitable since it will only control 9 volt equipment which has a current consumption of

100 mA or less. If one wishes to control a higher power, or an alternating current, this can be accomplished by controlling the load via a relay having suitable contacts. In this way it is also possible to have change over switching, and such things as touch controlled wavechange switches become a possibility.

The circuit diagram of the relay version of the touch switch appears in Figure 19. This is the same as the original circuit except that Tr1 now have a relay as its collector load in place of the controlled equipment. Protective diode, D1, has also been added.

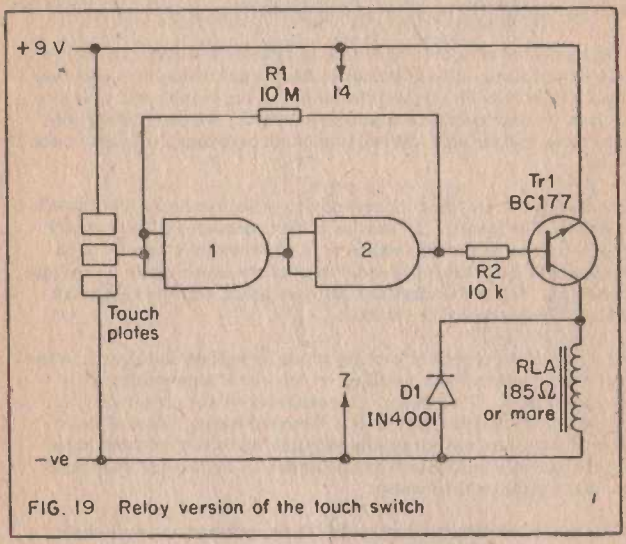

FIG. 19 Reloy version of the touch switch

The relay can be any type which is suitable for 6 volt operation and has a coil resistance of 185 ohms or more, provided it has suitable contacts for its intended application, of course.

MONOSTABLE CIRCUITS

It is probably true to say that monostable circuits are among the least used of all electronic building blocks, as far as circuits for the amateur are concerned anyway. They are perhaps used more often now than they were a few years ago as monostable I.C.s such as the NE555 and 74121 have proved to be very versatile.

CMOS monostable devices are available, and an example is the 4047 I.C. However, when only a simple monostable is required it is usually

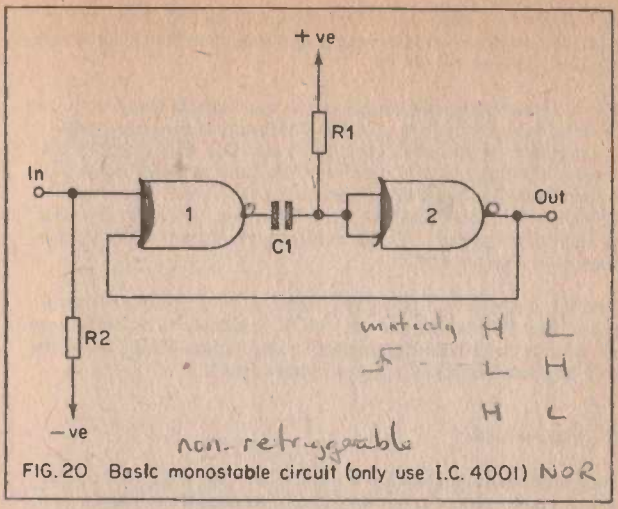

FIG. 20 Basic monostable circuit (only use I.C. 4001) NOR

easier and cheaper to connect a couple of gates to form a monostable circuit. A simple monostable can be produced from an inverter and a 2 input NOR gate. It is therefore possible to make one (or two) from a 4001 I.C. The relevant circuit diagram is shown in Figure 20.

The input of the inverter (gate 2) goes low when the power is initially connected to the circuit. This is because its input is taken high by R1. The output of gate 1 will also be high since both the inputs are low. If either or both of the inputs of a NOR gate go high, the output will go low.

If a brief pulse is applied to the input of the circuit, this will momentarily take one input high and gate 1 output will therefore go low. This output pulse is fed via C1 to the input of the inverter, and in consequence the output of the monostable goes into the high state. This takes the second input of gate 1 high, and even if the other input now goes low, the output of gate 1 will remain in the high state.

C1 will begin to charge up via R1 the moment the output of gate 1 goes low, and eventually the voltage on C1 will reach the transfer voltage of gate 2, and its output will go low. This takes the second input of gate 1 low, and the circuit has now returned to its original and only stable state. It is from this that the name monostable is derived.

It is worth noting that even if the input to the circuit is taken positive for a long period, rather than just momentarily, the output waveform will be the same. This merely has the effect of holding the output of

gate 1 low if a positive input is still present at the end of the output pulse. When this input is eventually removed, then the circuit returns to its original state.

Thus a monostable multivibrator can be used to either lengthen a brief input pulse or shorten a long pulse. The length of the output pulse is controlled by the values given to C1 and R1. The length of the output pulse can be varied over very wide limits as it can be less than a micro-second to more than an hour. R1 can have a value of anywhere between about 10 k and many Megohms. C1 can be any value of more than a few pF. If C1 is an electrolytic type it has its positive terminal connected to R1.

With R1 at a value of 1.8 Meg the prototype gave an output pulse of approximately 1 second per mfd, but there is likely to be afairly large variation between individual circuits in this respect. This is about the only real disadvantage of this very simple circuit.

Capacitance Meter

Most multimeters are equipped to measure wide ranges of voltage, current, and resistance, but few, if any, are capable of capacitance measurements. As a result of this, most electronics enthusiasts are unable to undertake capacitance measurements, and this must lead to many useable capacitors being discarded simply because their identification markings have become erased. Some means of testing capacitors is also very useful when one is engaged on servicing faulty equipment.

A capacitance meter is therefore a very useful piece of equipment to have in the workshop. A simple capacitance meter can be based on an astable and a monostable multivibrator, and it is possible to make one using a single CMOS I.C. as the only active device. The circuit diagram of such a unit is shown in Figure 21, and this uses a single 4001 I.C.

Gates 1 and 2 are connected as the astable circuit and gates 3 and 4 form the monostable multivibrator. The astable operates at a frequency of about 100 Hz, and its output is fed to the trigger input of the monostable. Thus one hundred times per second the monostable will produce an output pulse. The length of this output pulse is determined by the values of the timing components, and the timing capacitor under test. The timing resistor is one of the four resistors, R3 to R6, and is whichever one is switched into circuit by S1.

By using four timing resistors the unit is able to provide four measuring ranges. These are as follows:–

Range 1	0 to 500 nF
Range 2	0 to 50 nF
Range 3	0 to 5 nF
Range 4	0 to 500 pF

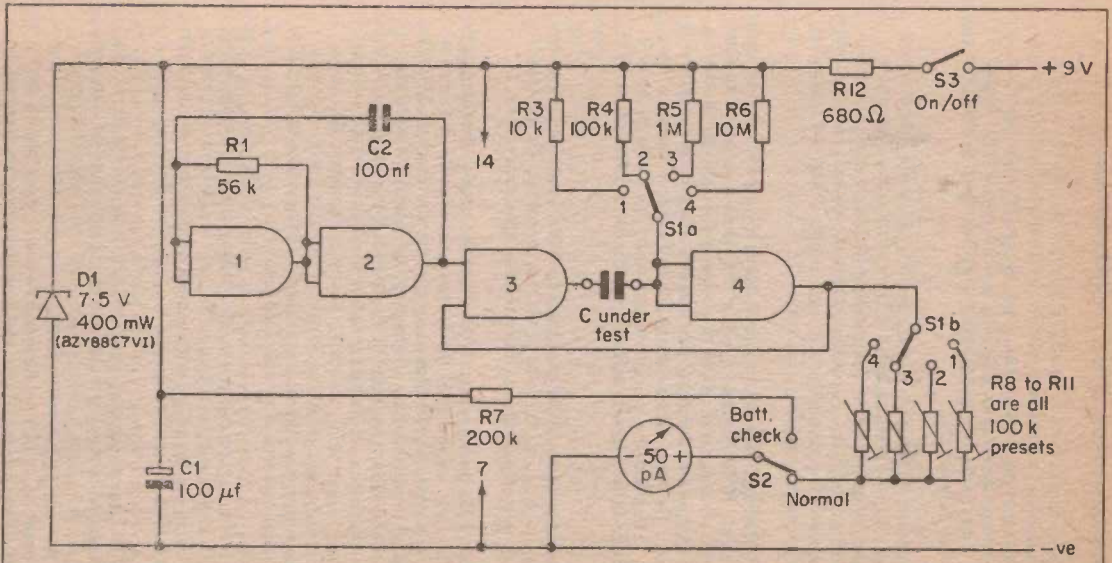

FIG. 21 The direct reading capacitance meter circuit (use only I.C. 4001)

The unit thus covers most normal amateur requirements.

The circuit value have been chosen so that the monostable acts as a pulse shortener. For instance, with the unit switched to Range 1 and a 500 nF test capacitor in circuit, the output pulse from the monostable will only be about half the length of the trigger pulse from the astable. Lower values of test capacitance will produce an even shorter monostable pulse length.

A voltmeter circuit consisting of M1 and one of the set of four preset resistors (R8 to R11) is connected at the output of the monostable. Each time the output of the monostable goes high, a pulse of current will be fed to the meter. A constant string of pulses are generated when a test capacitor is connected to the unit, and the meter will respond to the average output voltage.

With a 500 nF test capacitor in circuit, R9 is adjusted to produce f.s.d. of the meter. If, for instance, a 100 nF capacitor is connected in place of the 500 nF one, the length of the output pulses will only be one-fifth of the previous duration. The rate at which the monostable is triggered is the same, and so the pulses still occur at the same frequency. Therefore the average voltage across the meter circuit will only be one-fifth of its original level, and the meter will read one-fifth f.s.d.

It will be apparent from this that there is a linear relationship between the meter reading and the value of the test capacitor. The unit thus functions very effectively as a linear reading capacitance meter.

On Range 2 the timing resistor is ten times the value of that used on Range 1. Only one-tenth of the previous test capacity is therefore needed to produce an identical meter reading. For example, 500 nF was needed to produce f.s.d. of the meter on Range 1 whereas only 50 nF will be needed on Range 2. In practice this is not quite the case since the tolerances of the timing resistors will prevent such a precise relationship from being obtained. In order to ensure that good accuracy is obtained on all four ranges, a different preset resistor for each range is provided in the meter circuit. This enables each range to be calibrated against a close tolerance capacitor.

An alternative approach is to use 1% tolerance components for R3 to R6, and a single calibration preset. The unit would then only need to be calibrated on one range, with good accuracy being automatically obtained on the other three ranges.

D1 and R12 are used to stablise the supply voltage of the circuit, and this is essential if consistent and reliable results are to be obtained. There are two reasons for this. Firstly, the frequency of the astable circuit will vary slightly with variations in supply rail potential. If it should speed up at all, then there will be more pulses applied to the meter in a given period of time, and increased meter readings will be

obtained. If the speed of the astable should decrease, then obviously all meter readings will be low.

Secondly, the more importantly, the output voltage pulses of the monostable are virtually equal in amplitude to the supply rail voltage. If the supply rail alters (due to battery ageing for example), then the meter readings will alter proportionately.

A simple battery check facility is incorporated in the circuit, and this merely consists of S2 and R7. When S2 is in the position shown, the circuit functions normally. The meter is connected across the stabilised supply rail when S2 is in the other position. It is connected via R2 which converts the meter into a 0 to 10 V voltmeter. This can be used to monitor the supply potential, and when it falls below its nominal level of 7.5 V, this indicates that a new battery is required.

Calibrating the unit is quite straightforward, and four close tolerance capacitors are required for this. For example, a 470 nF 2% capacitor could be used to calibrate Range 1. With this connected across the test terminals and the unit set for normal operation on Range 1, R10 would be adjusted for a reading of 47 on the meter.

It is best not to use a calibration capacitor which has a value corresponding to less than half f.s.d. of the range being calibrated, as this will result in inferior accuracy being obtained. It is advisable to initially adjust all the preset resistors for maximum resistance before commencing calibration of the unit.

Enlarger Timer

Perhaps the most obvious use for a monostable is as a simple timer. This type of circuit is ideal for this application, and the circuit diagram of a simple enlarger timer employing a CMOS monostable is shown in Figure 22. This has a timing period which is continuously variable from about 1 second to 2 minutes.

The two gates are connected as a straightforward monostable which can be manually triggered by operating push button switch S1. VR1 enables the timing resistance to be varied on a wide range of values, and this enables the required timing period to be set.

Tr1 is normally shut off but it is turned hard on when the output of the monostable goes high. In doing so it energises the relay coil, and the normally open contacts of the relay connect the power to the enlarger lamp. Of course, at the end of the timing period the output of the monostable goes low and the enlarger lamp is turned off. D1 is the usual protective diode.

S2 enables the enlarger lamp to be switched on independently of the timing circuit, and this is a useful feature when it comes to the focusing

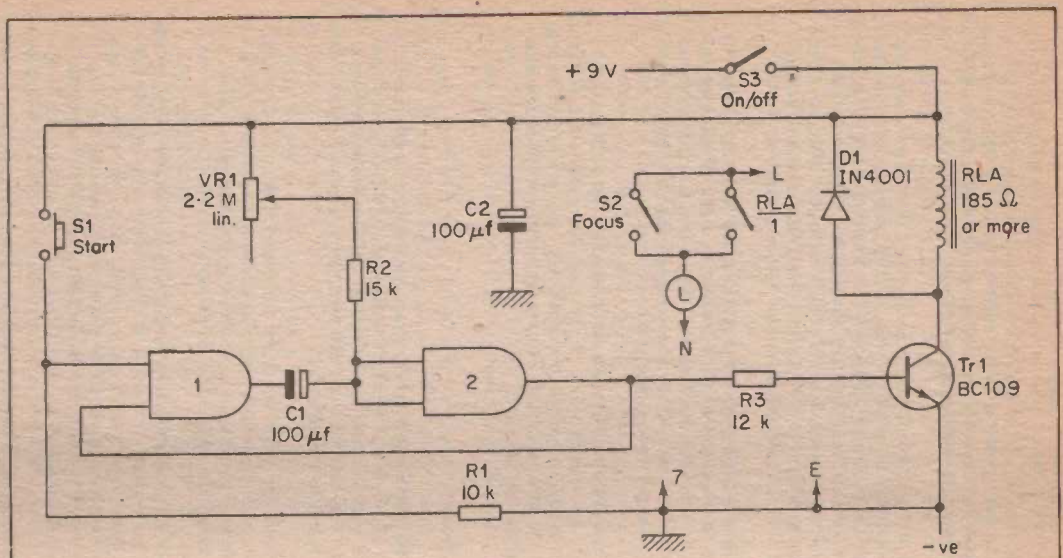

FIG. 22 Enlarger timer (use only I.C. 4001)

of the enlarger.

C1 must be a high quality component having a low leakage current if reliable and consistant results are to be obtained.

It is necessary to mark a dial around the control knob of VR1, and this should preferably be calibrated at one second intervals. Marking this out is rather time consuming since the only way to find the calibration points is to use trial and error.

Peak Level Indicator

A peak level indicator is a device which will give a warning of an overload in an amplifier, tape recorder, mixer, or some other piece of audio gear. Unlike the usual average reading VU meter, this type of indicator has a very fast response and it will respond to even very brief transients as it is operated by peak rather than average or R.M.S. levels.

It must be emphasised that a peak level indicator is not intended to be used instead of a VU meter, but is intended to be used in conjunction with one. A single peak level indicator will only show when an overload has occurred. It does not show the signal level.

The circuit diagram of a peak level indicator which utilises a CMOS monostable is shown in Figure 23. Gates 2 and 3 form the monostable, and the output of this is used to drive L.E.D. indicator D1 via current limiting resistor R6. The L.E.D. indicator will come on when the output of the monostable goes positive. The circuit values have been chosen to produce an output pulse of about 0.2 seconds in duration.

R3 and R4 are used to bias the input of the monostable towards its trigger voltage, but the voltage produced by this potential divider is insufficient to actually trigger the circuit. The reason for using this network is that it reduces the peak input voltage which is required in order to trigger the monostable, and it thus increases the sensitivity of the circuit.

It does not increase the sensitivity quite enough to enable the unit to be used with some pieces of equipment, and so an amplifier stage has been included ahead of the monostable. This is based on gate 1, and the use of the CMOS gates as linear amplifiers will be covered more fully later. R1 is a sensitivity control, and this enables the unit to be adjusted to respond to any input signal level of about 500 mV peak to peak or more.

The amplified input signal will modulate the voltage at the input of the monostable, and when a positive peak takes the input above the transfer voltage of the gate the monostable will be triggered. This will cause D1 to be briefly pulsed on.

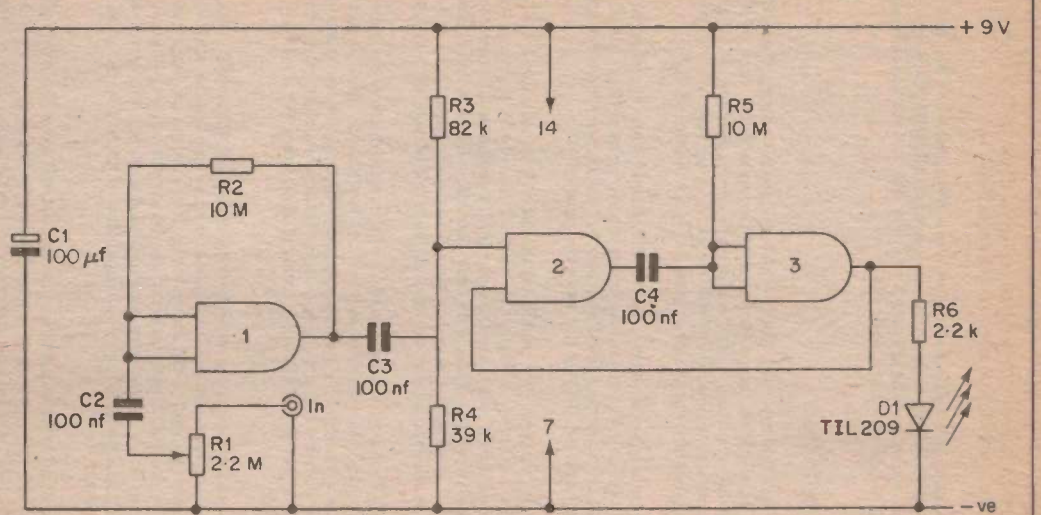

FIG. 23 Peak level indicator circuit (only use I.C. 4001)

It is an essential feature of the circuit that it is the peak level of the signal which the circuit responds to, the input waveshape and its mean level being irrelevant. In order to obtain consistant operation from this circuit it is necessary to power it from a stabilised supply.

An input for the unit is taken from any suitable point in the VU meter circuit, and as the unit has an input impedance of around 2 Megohms it will not significantly load the VU meter circuit. Because of this very high input impedance it may be beneficial to use screened input cable, although this will not be necessary if the unit is fed from a fairly low source impedance.

R1 is adjusted in the following manner. Connect a sinewave generator to the input of the main equipment and adjust the controls to indicate the required overload level on the VU meter (usually either +3 or +6 dB). Adjust R1 for the lowest sensitivity which causes the L.E.D. indicator to be continuously on.

Stereo Version

For stereo operation it is possible to use two of these peak level indicators, one to monitor each channel. It is more convenient however, to use a circuit which uses one indicator lamp for both channels. This can be accomplished by feeding the outputs of two of the circuits described above to the circuit shown in Figure 24. R6 and D1 of each of the original circuits are omitted, and the present circuit is fed direct from the outputs of the monostables.

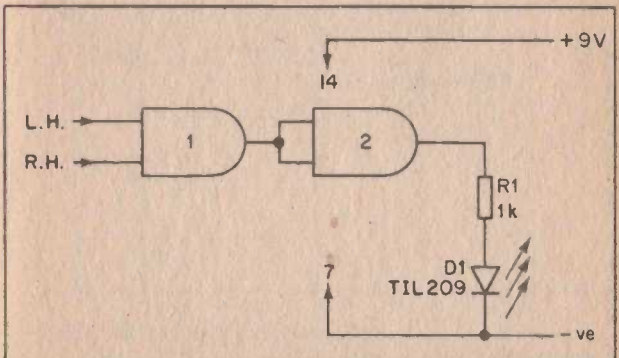

FIG. 24 When used in conjunction with two modified versions of Fig. 23 this produces a stereo P.L.I. (use only I.C. 4001)

Here a NOR gate and an inverter are connected to form an OR gate. When both the inputs to gate 1 are in the low state, its output will be high. The output of the inverter will therefore be low and D1 will not light up. If either or both the inputs to the NOR gate go high, then its output will go low. This will cause the output of the inverter to go high and D1 will be turned on.

The circuit as a whole (including the two monostables) will therefore cause the indicator lamp to come on if the peak level threshold of either channel is exceeded.

Chapter 3

AMPLIFIERS AND OSCILLATORS

For non-critical amplifier applications, and as the basis of many types of oscillator, CMOS I.C.s are a very attractive proposition due to the simplicity of the circuitry and their low cost.

Simple Amplifier

The circuit diagram of a very simple CMOS amplifier which uses a single inverter is shown in Figure 25. R1 is used to bias the inverter as a linear amplifier. The output of the device will begin to go high when the supply is initially connected, since the input will be low. When the voltage at the output reaches the transfer voltage of the gate, the input will try to take the output low as the input will be taken high by the voltage obtained via R1 from the output. The output voltage will be stabilised at about half the supply potential by this negative feedback action. The gate is thus biased into a linear mode.

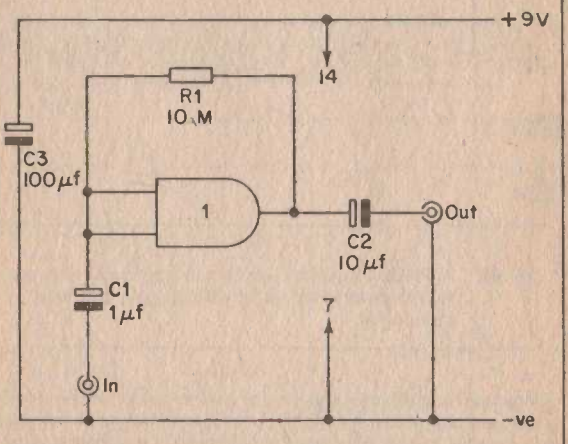

FIG. 25 Basic CMOS linear amplifier

At audio frequencies this circuit offers a voltage gain of about 50 times, and even at a frequency of many MHz it will still provide a degree of gain. It is not intended for use in Hi-Fi circuits, and is really only suitable for non-critical applications, such as in the peak level indicator

which was described earlier.

The value of R1 is not critical, but it should be in the Megohm region if the full voltage gain of the circuit is to be realised. C1 and C2 are the input and output D.C. blocking capacitors respectively. It is not a good idea to use this circuit with a nominal supply voltage of less than about 9 V as it could then become unstable.

Operational Amplifier

A more sophisticated amplifier can be produced by cascading three inverters together, as shown in Figure 26. This circuit is biased into a linear operating condition by R2, which operates in much the same way as R1 of Figure 25.

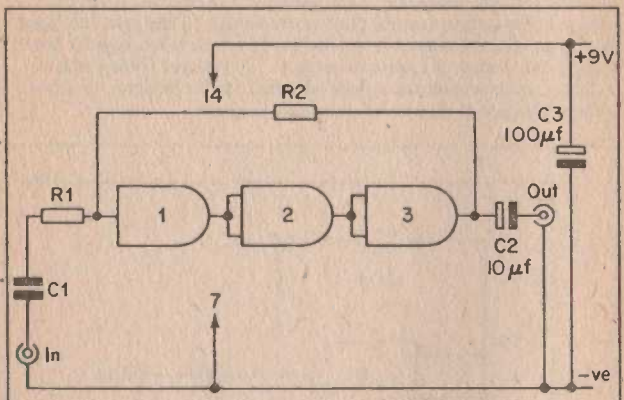

FIG. 26 A CMOS amplifier which uses op. amp. teqniques for the determination of voltage gain and input impedance

Operational amplifier techniques are used to select the desired input impedance and voltage gain of the circuit, and this makes the circuit very versatile indeed. The input impedance of the circuit is equal to the value given to R1, and the value of R2 is calculated by multiplying that of R1 by the required voltage gain.

Input impedances in the Megohm region are easily attained, as are very high voltage gains, but it is not really practical to obtain both of these in the same amplifier. There is the problem that the necessary high value resistor for R2 would simply not be obtainable, and stability

would probably be lost even if a suitable component was used.

The circuit has an open loop gain of typically 125,000 times (50 x 50 x 50 = 125,000), and a considerable amount of negative feedback is thus applied to the circuit when it is used in a practical situation with a closed loop gain of perhaps only 10 or 20. This provides the circuit with a reasonable level of performance with regard to noise and distortion, but it is not intended for high quality audio use. It is necessary to use a sensible component layout which is free from excessive stay capacitances, especially when the circuit is being used with an input impedance of more than a few k. Otherwise there is a risk of the circuit becoming unstable.

Crystal Oscillator

Crystal oscillators have been used since the early days of entertainment broadcasting whenever a highly stable R.F. oscillator is required. They are probably used more now than at any time in the past, and apart from use in crystal calibration oscillators and similar radio applications they are often used in digital clocks and other digital equipment where they generate a stable timebase signal.

CMOS I.C.s can be used as the active devices in good quality crystal oscillators having operating frequencies up to about 10 MHz or so. Figure 27 shows the circuit diagram of a simple CMOS crystal oscillator which uses a couple of inverters.

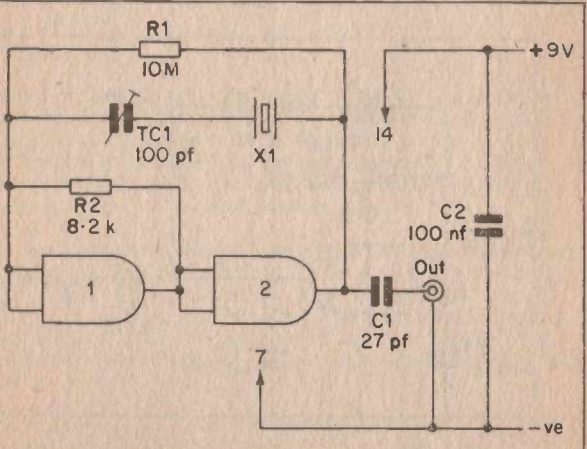

FIG. 27 A simple crystal oscillator

The two inverters are used to provide an amplifier which has its input and output of the amplifier via TC1, and at the series resonant frequency of the crystal (where it has a very low impedance) positive feedback will be applied to the circuit and it will oscillator.

TC1 enables the oscillation frequency of the circuit to be finely trimmed to the nominal frequency of the crystal. If this feature is not required TC1 can be omitted, with the crystal then being connected in parallel with R1.

At first sight R1 may appear to perform no useful function, but it was found to be necessary to add this as otherwise the oscillator often failed to start when power was applied to the circuit. C1 is the output D.C. blocking capacitor and C2 is a supply decoupling capacitor.

This circuit seems to operate satisfactorily over a wide range of frequencies with the component values shown, and the prototype oscillated properly with any crystal having a frequency from a few tens of kHz to many MHz.

Pierce Oscillator

It is possible to use a single inverter to provide the basis of a crystal oscillator, and such a circuit appears in Figure 28. This uses the well known Pierce oscillator configuration.

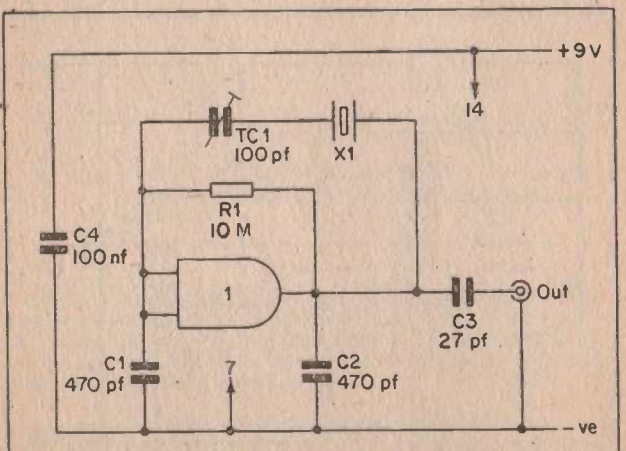

FIG. 28 A CMOS Pierce oscillator

The inverter is biased into a linear amplifying mode by R1, and the crystal is connected between the input and the output of the circuit by way of TC1. This circuit, like the previous design, operates at the series resonant frequency of the crystal.

There is no obvious positive feedback loop between the output and input of the circuit, just the opposite in fact, since the input and output of the amplifier are in antiphase. At series resonance it would appear as though the crystal provides negative feedback to the amplifier.

This is not actually the case since C1 and C2 form a capactive centre tap on the crystal, with the centre tap being earthed. The crystal thus acts as a sort of transformer at series resonance, with its two connections in antiphase. There is therefore a 180 degree phase shift through both the amplifier and the crystal, and the feedback is positive.

TC1 is used to trim the oscillation frequency of the circuit to the crystal's nominal frequency, and again, this feature can be left out if desired. TC1 is then omitted and the crystal is connected across R1.

C1 and C2 are shown as having values of 470 pF each in the circuit diagram. Using these values the circuit should oscillate satisfactorily over a wide range of frequencies. At frequencies above a few MHz it may be necessary to reduce the value of these components somewhat in order to obtain oscillation. Conversely, at frequencies below a few hundred kHz a slightly higher value may be required for these components. Also, if maximum output is required it will be necessary to find the values of these capacitors by empirical means.

L–C Oscillator

A crystal oscillator is, of course, intended to provide high stability at a single frequency, and is of no use if a tuneable wide range oscillator is required. This category of oscillator is almost invariably of the L–C variety for operating frequencies of a few hundred kHz and above. CMOS I.C.s can be used as the basis of simple L–C oscillators, and an example of such a circuit is shown in Figure 29.

This operates at a frequency of around 465 kHz, and T1 is an ordinary broadcast receiver I.F. transformer. In normal use the tuned winding is the primary and the untuned one is the secondary, but here the windings are used in the opposite roles. This is just a simple feedback circuit with the CMOS inverter being used as a linear amplifier. The circuit can be tuned over a fairly narrow range of frequencies by means of VC1.

As it stands here, the circuit is suitable for use as an I.F. alignment generator or as a B.F.O. for a communications receiver. However, it will work at frequencies beyond 10 MHz if a suitable coil is used (virtually any coil with a tuned winding plus a low impedance winding).

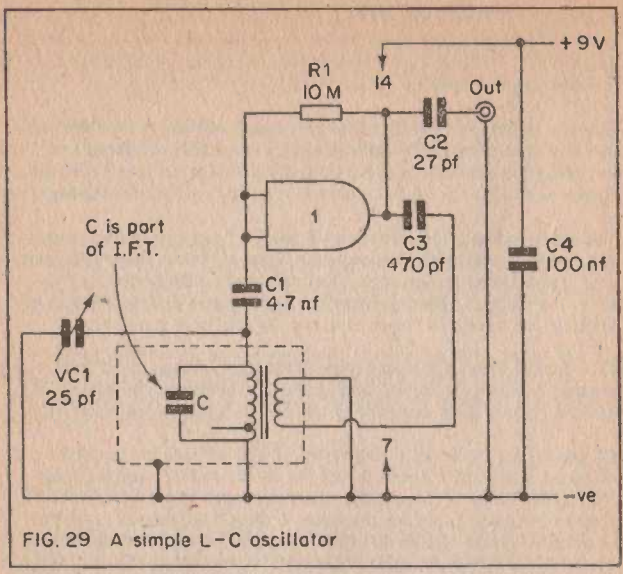

FIG. 29 A simple L-C oscillator

By increasing the value of VC1 to a few hundred pF the circuit can also be made to cover a wide tuning range. Note that the circuit will not oscillate unless T1 is connected with the phasing shown in the circuit diagram.

Hartley Oscillator

A CMOS inverter can be used in the well known Hartley type oscillator, and this has the advantage over the previous design that only a single winding is needed on the coil. However, this must be a centre tapped winding. The circuit diagram of a CMOS Hartley oscillator is shown in Figure 30.

This is very similar in operation to the pierce oscillator which was described earlier, the main difference being that a centre tapped L-C circuit is used in place of the capactively centre tapped crystal. The coil provides a D.C. path between the input and output of the inverter, and so no bias resistor is needed.

The circuit will operate over a frequency range of a few hundred kHz to more than 10 MHz, and the values of L and C are selected to suit the desired operating frequency. C can be a variable capacitor if a variable frequency oscillator is required. Note that the tapping does not have to

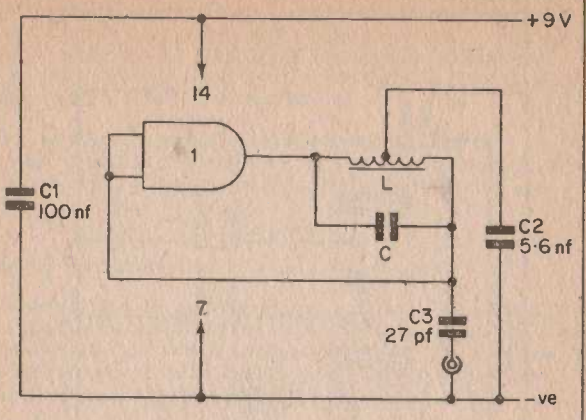

FIG. 30 A CMOS Hartley oscillator circuit

be at precisely the centre of the winding, and that for instance, the circuit will operate perfectly well using the primary of an I.F. transformer.

Phase Shift Oscillator

An audio squarewave generator was covered in the previous chapter, and this is not the only type of audio waveform generator which can be produced using CMOS inverters. It is possible to generate a sinewave using a phase shift oscillator, and such a circuit is shown in Figure 31.

Here three inverters are wired in cascade to form a high gain inverting amplifier. The actual gain of the circuit is controlled by the feedback network consisting of R1 and R4. R1 has been made variable so that the gain of the circuit can be set at precisely the required amount.

The output of the amplifier is coupled to the input by way of the three 60 degree phase shift networks which consists of C4 – R2, C5 – R3, C6 – R4. Thus, at the operating frequency of this network there is positive feedback between the input and output of the circuit, and provided the gain of the amplifier is sufficient, the circuit will oscillate. The gain should be no more than is absolutely necessary as otherwise the output waveform will be distorted. R1 is therefore adjusted for the lowest resistance that provides reliable oscillation.

An operating frequency of about 1 kHz is obtained with the specified values in the phase shift networks. This can be altered if required, by

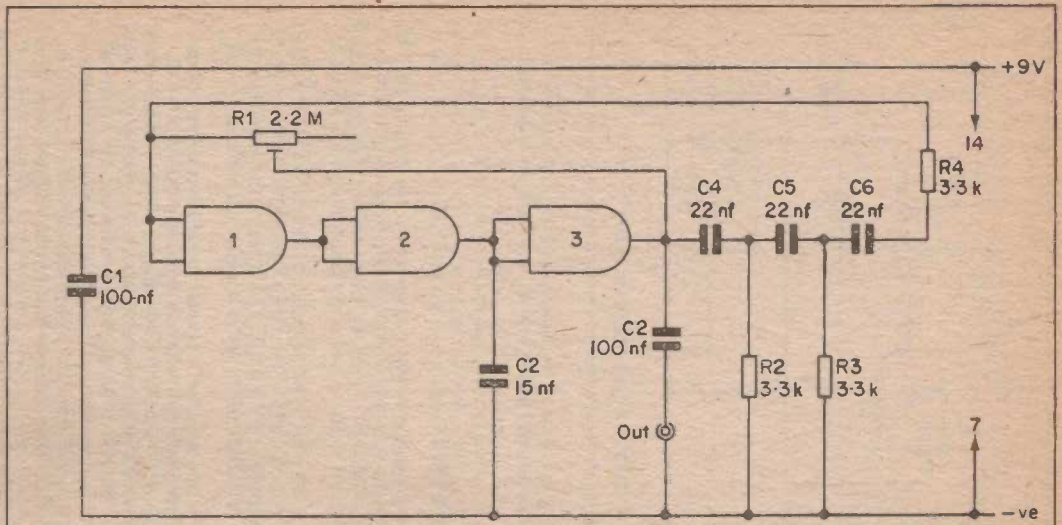

FIG. 31 A 1 kHz phase shift oscillator circuit

changing the values of C4 to C6. These should always be equal in value, and their value is inversely proportional to the operating frequency of the circuit. Thus using 220 nF capacitors gives an operating frequency of about 100 Hz, and 2.2 nF capacitors would provide oscillation at about 10 kHz. The circuit will function satisfactorily over a frequency range of less than 1 Hz to more than 20 kHz.

C2 is a stabilisation capacitor and C3 provides output D.C. blocking. The value of C3 should be increased if the unit is used to feed a fairly low impedance or if it is used at a lower operating frequency than 1 kHz.

Schmitt Trigger Oscillator

The circuit diagram of this unusual circuit is shown in Figure 32. The three inverters are connected as a form of Schmitt trigger, and this type of circuit is fully dealt with in the following chapter. Therefore only the characteristics of the Schmitt trigger circuit will be considered, rather than how this circuit actually operates.

A Schmitt trigger has an output which has only two stable states, and in this case the output is normally high. By applying a suitable input voltage the output can be made to go to the low state. With this circuit the input must be taken to about half the supply rail potential before the output will be triggered to the low state.

The output will return to the high state again if the input voltage is reduced to a suitable level, but the voltage at which the circuit triggers back to the high state is less than the original threshold voltage. This feature is termed hysteresis.

It is quite simple to understand the way in which this circuit operates. The output goes to the high state when the supply is initially connected since the input will be low. Capacitor C then begins to charge up via resistor R. When the voltage across C reaches the upper trigger threshold voltage, the output of the circuit goes low. C then begins to discharge through R and the output circuitry of inverter 3. When the voltage across C equals the lower threshold voltage of the Schmitt trigger, the output of the circuit will go high.

C then begins to charge via R once again until the voltage across C reaches the upper threshold voltage of the circuit. The output then goes low again. C then begins to discharge, and the circuit continuously oscillates in this fashion for as long as power is applied to it.

Two output waveforms are generated, a squarewave at the output of inverter 3, and a triangular waveform at the junction of R and C. Variations in output load impedance and supply voltage result in comparatively large variations in operating frequency, and so in critical applications it is necessary to use a buffer amplifier at the output and a stabilised power supply.

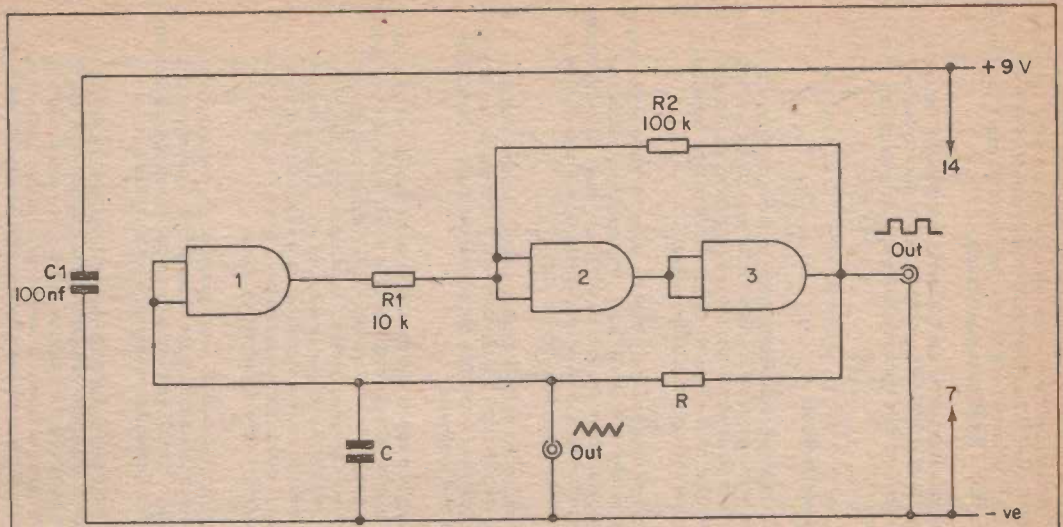

FIG. 32 A Schmitt trigger oscillator

An unusual feature of this circuit is the wide frequency coverage which can be obtained in a single range if R is a variable resistor. For example, using a 2.2 Megohm potentiometer forR and a 470 nF capacitor for C, the circuit has an operating range of a few Hz to many tens of kHz. The circuit will oscillate at a frequency of about 1 kHz with C at 100 nF and R at 470 k.

A peak to peak output amplitude virtually equal to the supply rail potential is obtained at the squarewave output, but the triangular output amplitude is much lower, being something in the region of 100 mV peak to peak. Also, the triangular output is at a relatively high impedance unless R has a low value. The circuit will oscillate with R having a value as low as a few tens of ohms, but for maximum reliability it should have a value of a few hundred ohms or more (the upper limit being many Megohms).

Chapter 4

SCHMITT TRIGGER CIRCUITS

A Schmitt trigger is a fairly simple type of circuit, but it is one of the most useful of all electronic building blocks and is widely used in home constructor projects. Basically a Schmitt trigger is a circuit which can only have one of two stable states (high or low) at its output. Which of these states the output assumes depends upon whether the input of the circuit is above or below a certain threshold voltage.

Most Schmitt trigger circuits have a degree of hysteresis, and so the threshold voltage at which the output goes high is above the threshold voltage at which it returns to the low state. In many applications this is a highly desirable feature, and in few it is absolutely essential, but it is usually necessary to have at least a small degree of hysteresis as otherwise the circuit would tend to become unstable with the input at or very close to the threshold voltage. Thus hysteresis is usually used whether it is essential to the basic operating principle of the circuit or not.

CMOS Schmitt trigger I.C.s are available, and the 4093 quad Schmitt trigger is one example. However, in most applications only a single Schmitt trigger is required, and it is more economical to connect a couple of inverters to form the circuit than it is to use a special I.C. (which are not as cheap as simple gates). Either one or both of the unused inverters can sometimes be usefully employed in some other section of the circuit.

Simple CMOS Schmitt Trigger

There are several ways of connecting gates to form a Schmitt trigger circuit, and the method shown in Figure 33 is probably the simplest. Here the input of inverter 1 is tied to ground via R1, and so the output of this inverter is high. The output of inverter 2 will therefore be low.

If a positive input signal is now applied to the circuit this will take the input of inverter 1 positive, but it will not have any effect upon the circuit other than this unless the input signal reaches an amplitude which is equal to the transfer voltage of inverter 1. When this happens, the output of inverter 1 will swing down towards the negative supply rail voltage, and this will cause the output of inverter 2 to start to go high. As it does so it feeds a positive voltage to the input of inverter 1 via R2, and this causes the output of inverter 1 to go more negative. This in turn sends the output of inverter 2 more positive. This causes a further positive voltage to be fed to inverter 1 input by way of R2, and this regenerative action will continue until the output of the circuit is fully positive.

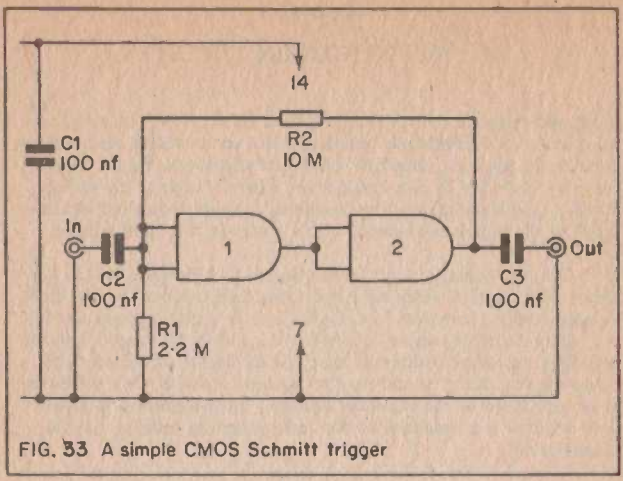

FIG. 33 A simple CMOS Schmitt trigger

In practice this all happens extremely rapidly, and virtually the instant the input voltage reaches the transfer voltage of inverter 1, the output assumes the high state.

If the input signal now begins to swing back towards the negative supply rail, a point will of course be reached where the input of inverter 1 is taken below the transfer voltage, and the output will start to swing negative. A regenerative circuit action will then once again take place and the output will quickly go fully low.

Hysteresis is introduced by the fact that once the output has gone high, the voltage through R2 is added to the input signal. This means that the input signal must go well below the transfer voltage before the circuit will return to its original state. The circuit will not normalise until the voltage from the output plus the input signal voltage equals a total which is less than the transfer voltage of inverter 1.

This basic circuit has many uses, and it can, for example, be used to produce a squarewave output from a sine or triangular input waveform. It can also be used to speed up a slowly rising or falling waveform, and it is often necessary to do this when using logic devices. This is due to the fact that many logic devices will not function reliably unless they are operated by a fast rising waveform, and CMOS counters and flip flop for example, must be driven by an input signal having a risetime of 5 micro-seconds or less.

Light Detector

Schmitt triggers are not only used in A.C. applications, and are frequently used in D.C. circuitry. In this type of application it is usually the role of the circuit to ensure that a definite output state is obtained, with no intermediate ones being possible.

An example of this is the simple light detector circuit which is shown in Figure 34. This type of circuit is used to close a set of relay contacts when the light level falling on a photocell exceeds a certain level. Such devices can be used in burglar alarms and for many other purposes.

It is usually necessary for the unit to draw a very low standby current so that economic battery operation is feasible. In the circuit of Figure 34 the Schmitt trigger ensures that this is achieved. VR1 is adjusted so that the output of the Schmitt trigger circuit is normally low, and no significant base current is supplied to Tr1. This transistor is therefore cut off and the relay is not activated.

When the light level falling on PCC1 exceeds a certain threshold level, the resistance of this cell will have dropped to a low enough level to cause the voltage at the junction of VR1 and PCC1 to rise above the trigger voltage of the Schmitt trigger. Its output will quickly go to the high state and Tr1 will turn on. The relay will then be activated.

Under normal conditions the Schmitt trigger and the output transistor draw no current, and the only supply current which flows is the small current through PCC1 and VR1. The circuit would still work if the trigger circuit and R3 were to be omitted, with the junction of PCC1 and VR1 then being connected direct to Tr1 base. However, with the circuit in the normal or off state it would be quite possible for a small base current to be fed to Tr1. This would cause it to draw a significant collector current which although too small to activate the relay, could discharge the batteries over a period of time.

Darkness Detector

In many applications it is necessary to have a circuit which operates a relay when the light level goes below a certain level, rather than when it goes above a certain level. It is quite simple to convert the circuit of Figure 34 to do this and there are several ways of doing it. Probably the most simple one is simply to transpose VR1 and PCC1. The voltage at the junction of these two devices will then rise with decreasing light level, and the required circuit action is thus provided.

Latching Version

In alarm circuits and certain other applications it is necessary to have a circuit that will remain on once it has been triggered. It is an easy

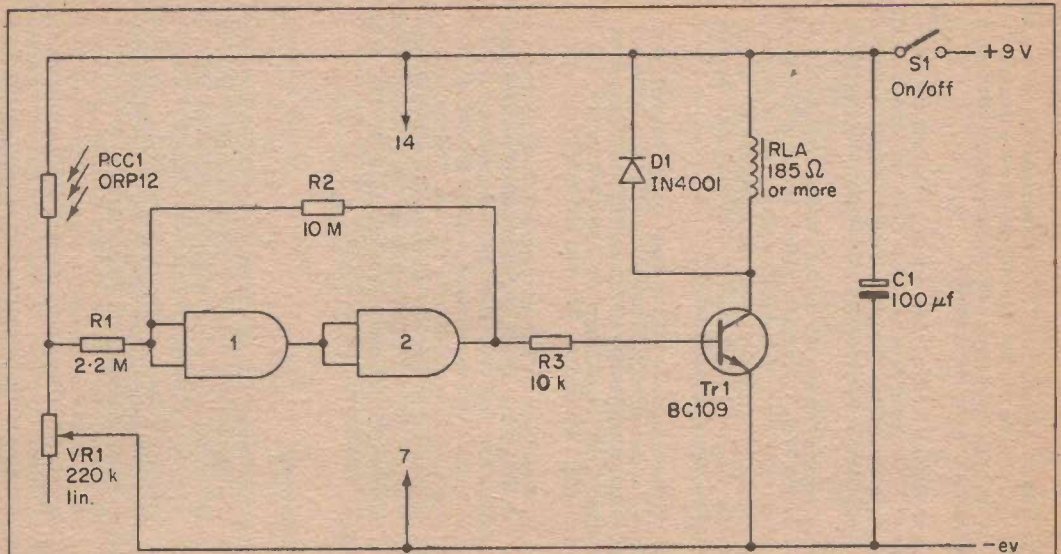

FIG. 34 A simple light detector circuit

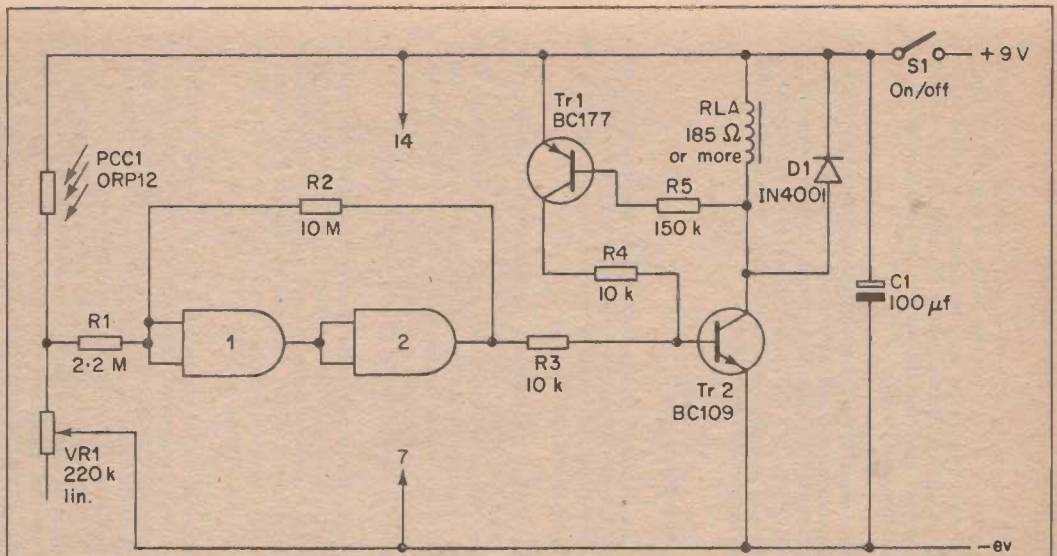

FIG 35 A latching light detector circuit

matter to modify the circuit of Figure 34 to provide latching, and the revised circuit diagram appears in Figure 35.

This operates in exactly the same way as the original circuit until the relay is activated. Then the voltage across the relay, which was previously zero, rises to several volts, and a base current is supplied to Tr1 by way of current limiting resistor R5. This turns Tr1 on, and a base current will be supplied to Tr2 via Tr1 emitter and collector and current limiting resistor R4.

Even if the output of the Schmitt trigger now returns to the low state, Tr2 will not be switched off as it will still be receiving a base current from Tr1. The circuit therefore latches in the on state once it has been triggered, with Tr1 and Tr2 providing a sort of thyristor action. Like the circuit of Figure 34, this circuit can be built as a darkness detector by swopping over VR1 and PCC1.

Automatic Parking Light

In applications where a light switch is to be used to operate a low voltage D.C. load it is usually possible to use a relayless circuit. An automatic parking light for a car is one such example, and a suitable circuit is shown in Figure 36.

Here the circuit is triggered when the light level falls below a level which causes the voltage at the junction of VR1 and PCC1 to exceed the trigger voltage of the Schmitt trigger. The trigger circuit then provides a base current to a high gain Darlington pair using Tr1 and Tr2. Tr2 is a power transistor which is capable of handling the relatively high current drawn by a parking light. S1 enables the light to be turned on independently of the automatic circuitry.

In this circuit the current consumption of the device is of secondary importance since it will be powered from a high capacity car battery. However, it is obviously desirable to have the lamp switching cleanly from one state to the other. Perhaps less obviously it is necessary for the circuit to avoid intermediate output states in order to illiminate the possibility of damage to Tr2 due to overheating.

This could occur if Tr2 was partially swtiched on with about half the supply voltage being present at its collector, as it would then have to dissipate several watts of power. This could be overcome by using a large amount of heatsinking for Tr2, but it is probably better to use a trigger circuit, as Tr2 can then only rest in the hard on or fully off state. The dissipation in either case can only be low, as when it is turned hard on very little voltage is produced across it, and when it is turned hard off it passes no significant current. It will dissipate a significant amount of power when it is turned on, and if a high current lamp is being controlled a certain amount of heatsinking will be necessary, but this will only need to be minimal.

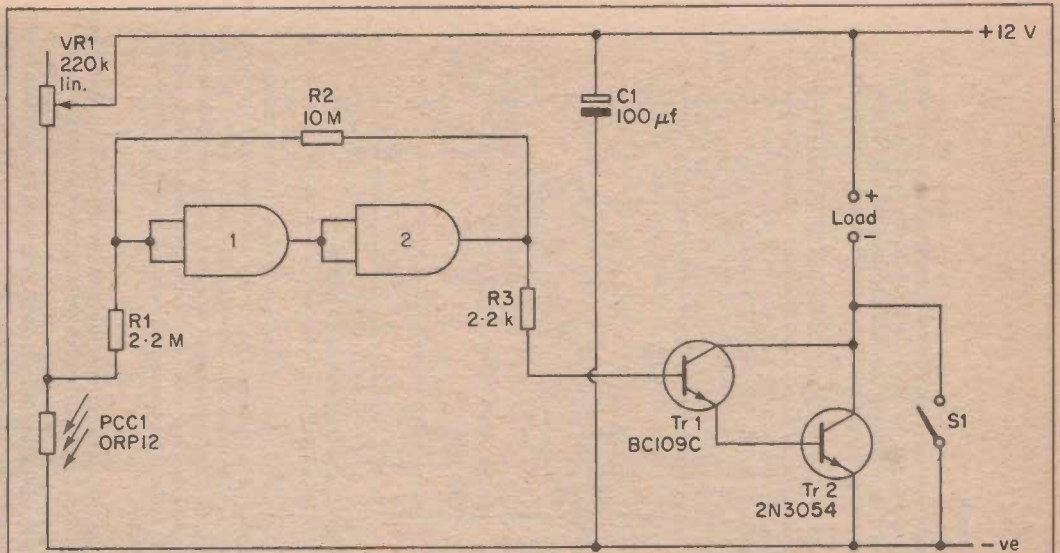

FIG. 36 An automatic parking light

In all the light switches just described it is possible to adjust the circuit by means of VR1 to produce a switching threshold at almost any required light intensity.

Touch Switch

A Schmitt trigger can be used as the basis of a simple touch switch, where it ensures that the circuit switches briskly from one state to the other and does not take up a stable intermediate state. It thus provides an action which is very similar to a conventional mechanical switch.

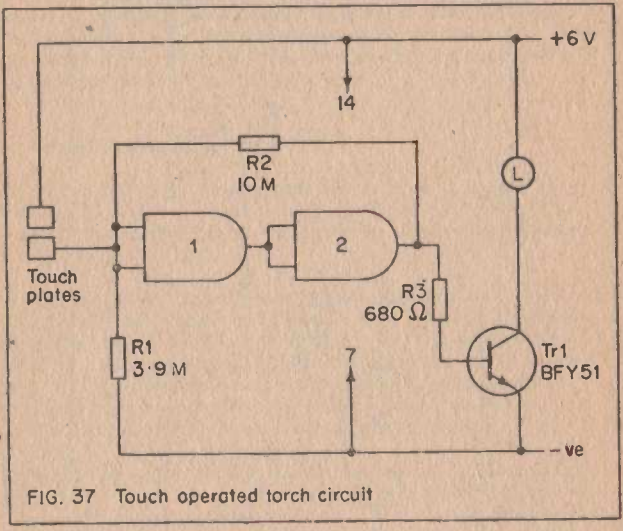

FIG. 37 Touch operated torch circuit

A simple touch switch circuit is shown in Figure 37, and this shows how a CMOS Schmitt trigger can be used as the basis of a novel home made torch. The circuit has other possible uses of course, and any small D.C. load can be connected in place of the lamp. Other loads can be controlled by using a relay in the collector circuit of Tr1, and if this is done it will also be necessary to include a protective diode in this part of the circuit.

Operation of the circuit is very straightforward. The Schmitt trigger is arranged so that its input and output are both normally in the low condition, and Tr1 is therefore normally cut off. When the touch contacts are bridged by the operator's finger a current will flow from the positive supply rail and through R1. In effect, the skin resistance of the operating finger and R1 together form a potential divider, and

provided the voltage at their junction is above the threshold voltage of the Schmitt trigger, this circuit will assume the high state at the output. It then supplies a base current to Tr1 which is, in consequence, biased hard on. Power is then supplied to the lamp which should have a current consumption of no more than about 100 mA.

When the operator's finger is removed from the touch contacts the Schmitt trigger reverts to its original state and the lamp is switched off.

Over Temperature Indicator

In this application it is the purpose of the Schmitt trigger to ensure that an erroneous indication is not produced. This is simply a circuit which indicates by means of a lamp any rise in temperature above a preset threshold level. If the triggering were to be left out, then the lamp would begin to glow dimly as the temperature approached the threshold level. This could be confusing, and if the unit is battery powered it could result in the batteries having a very short working life. The circuit diagram of the unit appears in Figure 38.

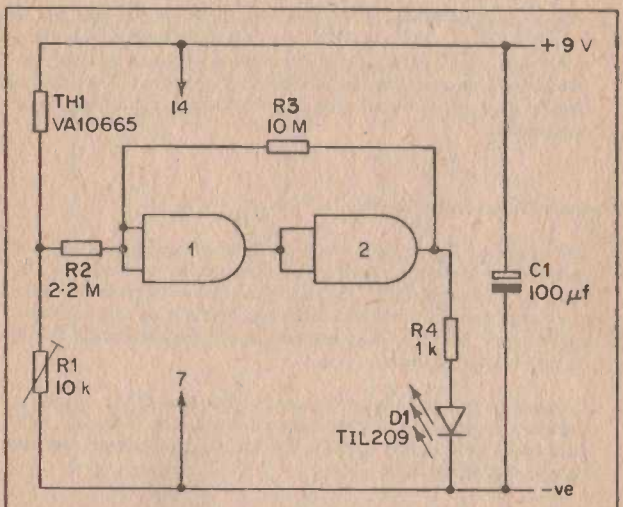

FIG. 38 Over temperature indicator circuit

TH1 and R1 are connected as a potential divider at the input of the trigger circuit. TH1 is a negative temperature coefficient thermistor, and its resistance therefore decreases with increasing temperature. R1

is adjusted so that the voltage produced by this potential divider reaches the trigger threshold of the Schmitt trigger at the required threshold temperature. When the output of the Schmitt trigger goes high, power is supplied to the L.E.D. indicator, D1.

When the lamp is in the off state the circuit only consumes about 1 mA from the supply lines, and this is the power which flows through the thermistor and R1. A reasonable battery life can be obtained by using a large capacity battery to power the unit, but in many cases it will be better to use a small battery and connect a push to make non-locking push button switch in series with the positive supply lead. The unit will then only consume power when this push switch is operated. Obviously in some applications this form of periodic monitoring will not be suitable, but it is preferable to use it wherever it is practical to do so.

A wide range of threshold temperatures can be provided by R1, and the actual operating range of the circuit extends from more than 100 degrees Fahrenheit to less than 0 degrees Fahrenheit. It is therefore a very versatile circuit.

It is not essential for the thermistor to be built into the main unit, and there is no reason why it should not be remotely located from the rest of the unit. Quite a long connecting cable can be used between the thermistor sensor and the rest of the unit if necessary. The unit could thus be used as a fire alarm for an outbuilding, or in some similar application.

Under Temperature Version

The circuit of Figure 38 is easily modified to function as an under temperature indicator, and it is merely necessary to transpose the positions of R1 and TH1. The circuit could then be used, for example, as a frost alarm, and could be used by gardeners or in automotive applications. The operating temperature range is the same as for the original version of the unit.

By using all four gates of a 4001 or 4011 I.C. it would be possible to make both versions of the unit using a single device. The unit could then be adjusted so that it would indicate any temperature deviation outside two preset limits.

Over Temperature Alarm

This is basically the same circuit as the over temperature indicator, but the output of the Schmitt trigger is used to control an audible alarm circuit rather than an indicator light. The circuit diagram of this unit is shown in Figure 39.

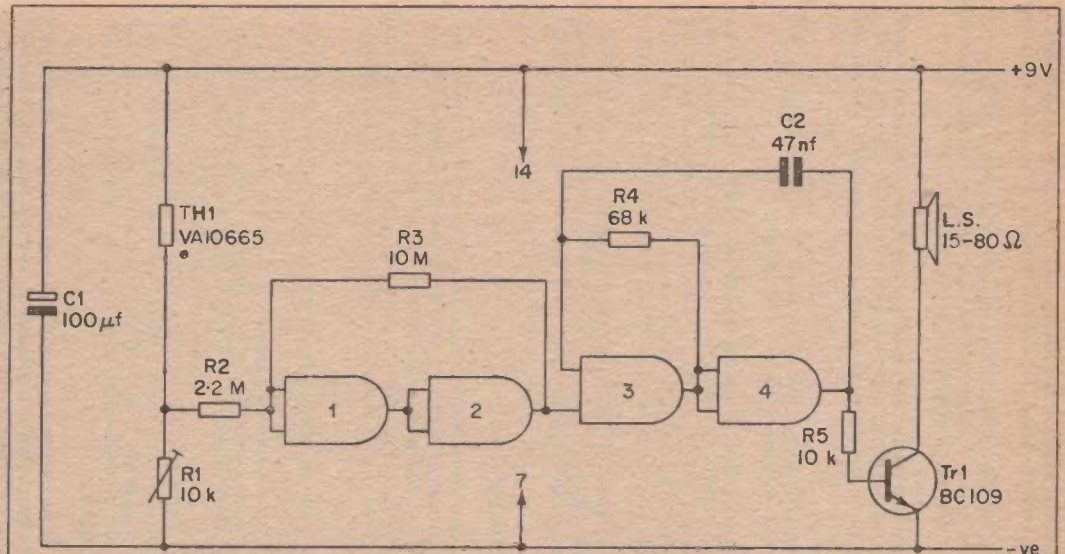

FIG. 39 Over temperature alarm circuit (use 4011 only)

Inverter 3 and inverter 4 are connected as an astable multvibrator which operates at a frequency of a few hundred Hz. This feeds a common emitter amplifier using Tr1, and this in turn operates a loudspeaker.

The multivibrator is blocked and cannot operate unless the output of the Schmitt trigger is high, and the alarm does not therefore sound until the circuit has been triggered.

The quiescent current and operating temperature range of this circuit are the same as for the over temperature indicator. The unit can be converted to an under temperature alarm by swopping over R1 and TH1.

It is important to note that this circuit will only ooperate using a 4011 I.C., and a 4001 is not suitable in this instance.

Providing R1 with the correct adjustment is quite simple and is the same for this circuit and for the over temperature indicator. The thermistor is heated or cooled to the required threshold temperature, and then R1 is adjusted for the lowest resistance which causes the indicator lamp to come on or the alarm to sound, as appropriate.

For the under temperature versions the procedure is much the same, the only difference being that R1 must be adjusted for the highest resistance which keeps the indicator lamp on or the alarm sounding.

Electronic Egg Timer

Two simple timers which provide an audible output at the end of a variable timing period have already been covered. These circuits were limited to a maximum timing interval of only about 10 seconds, because using a longer time constant would result in the tone generator being turned on only gradually, which would obviously not be satisfactory.

The timer circuit shown in Figure 40 is basically similar to the original one (see Figure 12) in that it uses an R–C timing network and an astable multivibrator tone generator. However, instead of the tone generated being fed to the output stage/speaker via an enabling gate, it is fed direct to this arrangement. The multivibrator itself is controlled on this occasion, via a control voltage which is fed to one input of gate 4. This terminal is normally low and the astable circuit is muted. The output of gate 5 is also normally low with Tr1 being cut off and passing no current. This is very important, as if it were normally high, Tr1 would be biased on and there would be a very high static current consumption.

Gates 2 and 3 are used as the Schmitt trigger, and this has its input fed from an inverter which in turn has its input fed from the R–C timing network. C1 is the capacitive part of the timing network and R1 – VR1 are the resistive part.

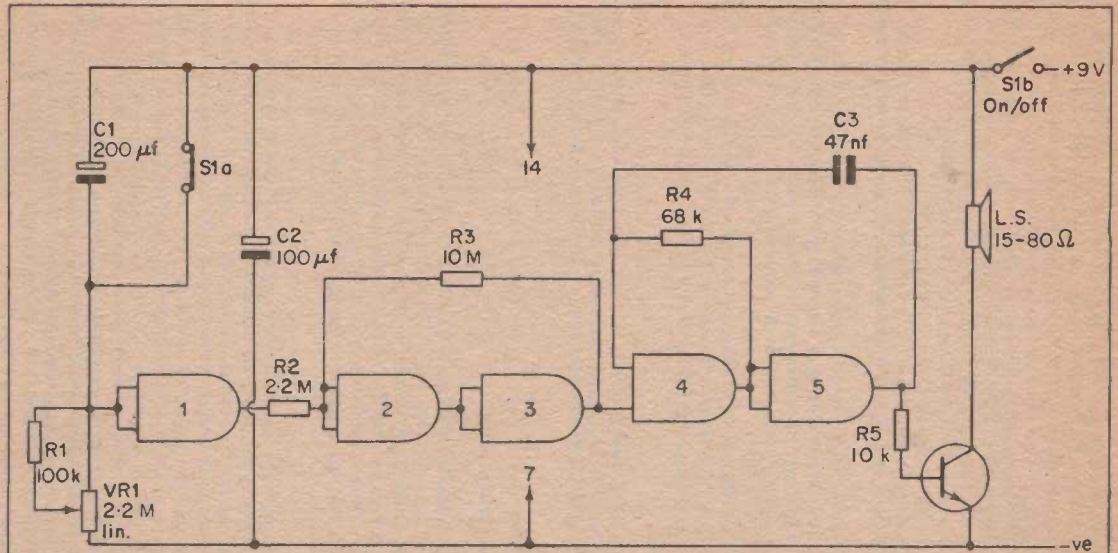

FIG. 40 Electronic egg timer circuit (use 4011 only)

S1a opens when the on/off switch (S1b) is closed, and this starts the timing interval. C1 begins to charge up through VR1 and R1 and eventually the voltage across R1 and VR1 will fall to the transfer voltage of gate 1. When this happens, the output voltage of gate 1 will gradually begin to rise. After a short while its output voltage will reach the trigger voltage of the Schmitt trigger circuit, and the output of inverter 3 will immediately go high. This turns on the multivibrator and the audible alarm tone is produced from the speaker.

When the unit is switched off, S1a discharges C1 and the unit is then ready to start another timing period when it is switched on once again.

VR1 enables the length of the timing interval to be varied from less than 30 seconds to more than 6 minutes, and the unit is thus suitable for use as an egg timer, or indeed for a multitude of uses in the house. A timer of this type can be much more useful than one might imagine.

A dial calibrated in minutes should be marked around the control knob of VR1, and there is unfortunately no quick way of doing this. It is a matter of finding all the calibration points using a process of trial and error.

Note that this circuit can only be built using a 4011 I.C., as gate 4 must be a NAND type. In actual fact it requires two I.C.s, since five gates are employed in the circuit and only four are contained in each 4011 I.C.

Under Voltage Indicator

Many pieces of 9 volt battery operated equipment, particularly in the field of test equipment, use a stabilised supply rail of between 5.6 and 7.5 V. Malfunction of the equipment can occur if this voltage should fall below its nominal level due to battery ageing, but many pieces of gear do not incorporate any form of battery check facility. This can be added to such equipment using the simple circuit shown in Figure 41.

The upper and lower threshold voltages of a CMOS Schmitt trigger are determined by the individual characteristics of the gates employed and by the supply rail potential. This circuit is therefore powered from a stabilised supply so that these voltages are not significantly affected by variations in the supply rail potential. This stabilised potential has been made lower than that of the monitored voltage for obvious reasons.

The two inverters are connected as a simple Schmitt trigger which has its input fed from the monitored voltage via a preset potentiometer (R1). R1 is adjusted so that the Schmitt trigger is normally in the high state, with the voltage at its slider being fractionally higher than the lower threshold voltage of the Schmitt trigger. An L.E.D. indicator (D1) and current limiting resistor (R4) are connected at the output of

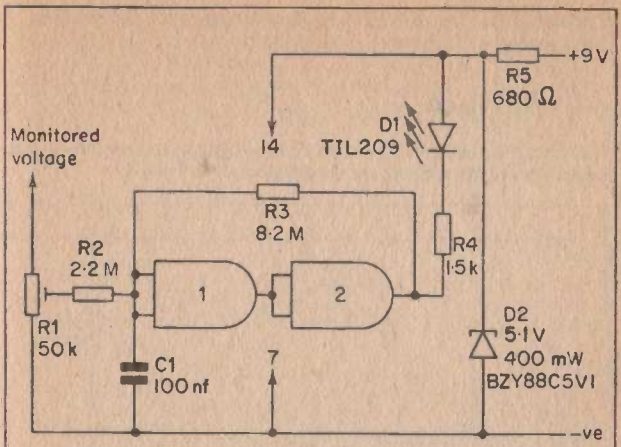

FIG. 41 Under voltage indicator circuit

the Schmitt trigger, and these are not supplied with power unless the output of the trigger circuit goes low.

This is precisely what will happen if the monitored voltage should fall significantly, as the input voltage to the Schmitt trigger will fall below the lower threshold voltage and will cause the circuit to change state. The circuit thus indicates any significant fall in the monitored voltage.

The circuit is very easy to set up, and it is merely necessary to adjust R1 for what is virtually the lowest slider voltage which does not cause D1 to come on. It is best not to take this voltage too close to the lower threshold voltage of the Schmitt trigger, as it must be remembered that voltage stabiliser circuits are all less than perfect. There is usually a certain decrease in a stabilised rail which is derived from a battery supply, even before the battery voltage drops below a suitable working level.

It is possible to have the monitor circuit permanently connected to the unstabilised supply, but the unit will consume a current of about 6 mA under quiescent conditions, this being the current used by the zener regulator circuit (R5 and D2). It could therefore significantly reduce the working life of the battery.

A more practical solution is to connect the unit to the positive supply by way of a push to make non-locking push button switch. This can then be periodically operated in order to check whether or not the battery needs replacing.

Capacitor C1 is needed in order to suppress transient voltages which could cause the circuit to operate eratically.

Over Voltage Version

The circuit of Figure 41 can easily be modified to act as an over voltage indicator, and the appropriate circuit appears in Figure 42.

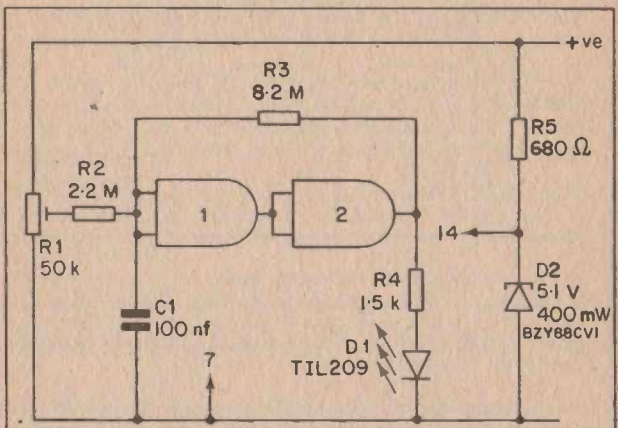

FIG 42 Over voltage indicator circuit

Here the Schmitt triggers output is normally in the low state, and the L.E.D. indicator circuit, which is now connected between the trigger output and the negative supply, does not receive any current. If the supply voltage goes above a predetermined level, the voltage at the input of the trigger circuit will exceed the upper threshold voltage, and the output of the circuit will go high. Current will then be supplied to D1 which will, in consequence, come on and indicate the excessive supply voltage.

The circuit can be adjusted to operate at any voltage from about 3 to 15 volts. In order to give R1 the correct setting it is necessary to connect the unit to a supply voltage which is equal to the required threshold voltage. R1 is then adjusted for the lowest slider voltage which causes D1 to come on.

Due to the fact that the circuit has a degree of hysteresis, it is necessary to start with R1 slider at minimum voltage, and then gradually increase this until D1 lights up. Starting with R1 slider at maximum voltage

and then turning it back until the L.E.D. goes out is not correct. If this is done, the lower theshold voltage of the Schmitt trigger will be reached when the input voltage reaches the overload point, whereas it should be the upper threshold voltage that is reached. The circuit would then fail to respond to a slightly excessive voltage.

Chapter 5

SPECIAL DEVICES

The previous chapters have been concerned with circuits based on simple inverters and gates, with all the projects being based on the 4001 and 4011 I.C.s. These are only two devices from a vast range of CMOS devices which are now available. It must be admitted that many of the I.C.s in this range are for highly specialised applications, and are of little use to the amateur enthusiast. On the other hand, there are several devices which can be usefully employed by the amateur, the frequency divider I.C.s being the most obvious examples.

In this chapter, details of some of the more specialised CMOS I.C.s will be given, together with some practical details of their use in simple projects.

Frequency Dividers

These are almost certainly the most useful of the specialised CMOS devices, and four types will be considered here. These are the 4013 type D flip flop, the 4027 J–K master slave flip flop, the 4017 decade counter, and the 4018 presettable divide by 'N' counter. The latter can be connected so that it will divide by any even number from two to ten (inclusive), and it will be discussed separately from the other three devices.

The most simple of the CMOS frequency dividers is the 4013, and this contains two D type flip flops. In order to get this type of circuit to divide by two it is merely necessary to connect the Q output to the data input, and earth the set and reset terminals. The input is then applied to the clock terminal and the output is obtained from the Q output.

Connection details for the 4013 are shown in Figure 43(a). If only a single divide by two circuit is required, the clock input of the unused device should be connected to the negative supply rail. It is possible to obtain a divide by four action by connecting the output of one flip flop to the output of the other one.

The 4027 I.C. contains two J–K flip flops, and the circuit diagram of Figure 43(b) shows how these are connected to provide a divide by two action. Again it is possible to obtain a divide by four action by using the two flip flops in series.

Connection details for the 4017 decade counter, or divide by ten circuit, is shown in Figure 43(c). This is very simple with the input being applied to the clock terminal and the output being obtained from the carry out terminal. The reset and clock enable terminals must be earthed.

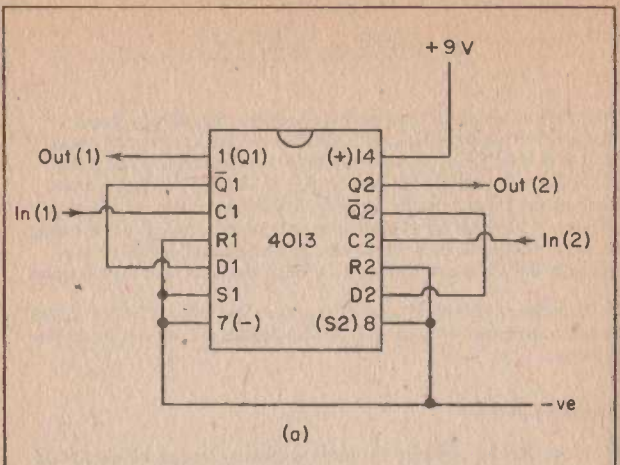

FIG. 43(a) A 4013 I.C. can be used to form two divide by two circuits

An interesting feature of this device is that it has ten outputs apart from the carry out one. These are marked '0' to '9' in Figure 43(c). These go high for one complete clock cycle in sequence. Thus during the first clock input cycle the '0' output goes high, then the '1' output goes high for the next cycle, and so on until the '9' output has gone high for one cycle. Then the whole sequence starts again from the beginning. This feature can be used to operate the 4017 as a preset-table divide by N counter, but additional active circuit elements are required, and in most instances it is easier and cheaper to use the 4018 I.C. However, there are other applications in which this series of output pulses can be utilised.

Crystal Calibrators

Probably the most obvious use for a frequency divider is in a crystal calibration oscillator, and a simple circuit using a 4017 in this role is shown in Figure 44.

Here a couple of inverters are used in a simple crystal oscillator of the type shown earlier in Figure 27. This operates at a frequency of 1 MHz and has its output fed to the clock input of the 4017. An output frequency of 100 kHz therefore appears at the output of the 4017, and this circuit thus provides outputs at both 1 MHz and 100 kHz. This could, of course, be achieved using two separate oscillators, one

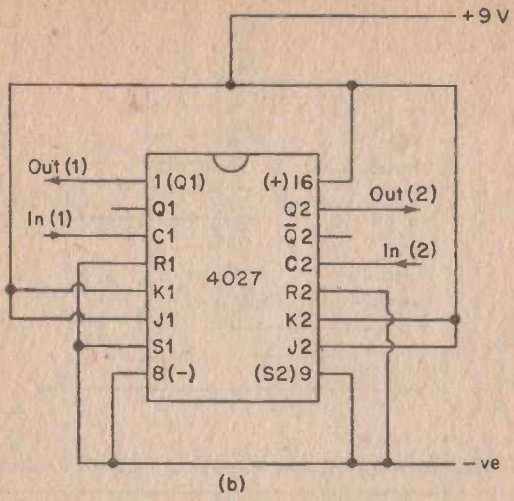

FIG. 43(b) A 4027 I.C. can be used to provide the same function

at each frequency, or by using two switched crystals. This method is preferable though, since crystals are far more expensive than the 4017 I.C.

The outputs of this circuit have fast rise and fall times, and the outputs are therefore rich in the required harmonics. It provides marker frequencies at 1 MHz intervals from 1 MHz to over 30 MHz, and at 100 kHz intervals from 100 kHz to over 30 MHz. The unit is thus suitable for calibrating general coverage M.W./S.W. receivers.

For optimum accuracy to be obtained it is necessary to trim the oscillator frequency to precisely 1 MHz. Probably the easiest way to do this is to connect a lead to the 100 kHz output of the unit, and place this near to an operating receiver which is tuned to Radio 2 on the L.W. band. B.B.C. Radio 2 operates at precisely 200 kHz on the L.W. band, and the first harmonic of the 100 kHz signal will react with the Radio 2 signal to produce a beat note. This note will be very low in pitch, and C2 is adjusted to produce the lowest possible beat note. With careful tuning of the oscillator it should be possible to obtain a beat note of less than 1 Hz.

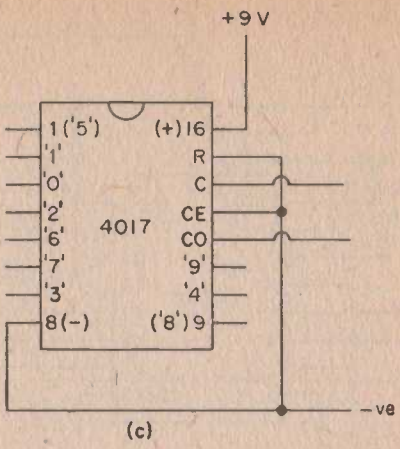

FIG. 43(c) A 4017 I.C. connected as a divide by 10 circuit

For most purposes such a high degree of accuracy is not required, and it is usually possible to obtain more than adequate accuracy by leaving out the trimmer capacitor (C2), and connecting the crystal in parallel with R2.

It is worth noting that most receivers have spurious responses and misleading results can be obtained if the calibration signal is picked up on one of these. For this reason it is advisable to use only a very loose coupling between the receiver and the calibrator, and it will probably not be necessary to use a direct coupling at all. Simply placing a lead connected to the appropriate output of the calibrator close to the receiver's aerial socket should suffice.

Triple Output Version

The crystal calibration of Figure 44 is excellent for calibrating general coverage receivers, but it leaves a lot to be desired when it comes to the calibration of an amateur bands only set. For instance, the 80 Metre band extends from 3.5 to 3.8 MHz, and so the calibrator would only provide calibration points at the band limits, plus two inside these limits.

For this reason it is quite common for calibrators intended for use with amateur bands receivers to have a very low output frequency in addition

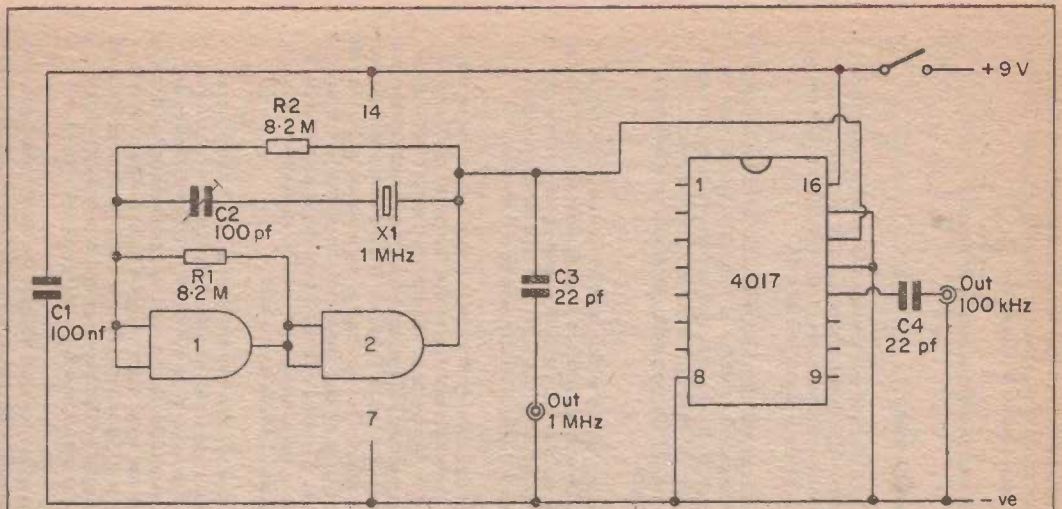

FIG. 44 A simple 1 MHz/100 kHz crystal calibration oscillator

to the normal ones. This can easily be achieved with the circuit of Figure 44 by simply adding an extra decade counter at the 100 kHz output. This then provides outputs at 1 MHz, 100 kHz, and 10 kHz. The modified circuit is shown in Figure 45.

This is set up and used in the same way as the original circuit.

Simple Calibration Oscillator

Although L–C oscillators do not provide such good accuracy and stability as crystal ones, it is nevertheless possible to make a perfectly satisfactory calibration oscillator using an L–C oscillator. The circuit diagram of such a device is shown in Figure 46.

Inverter 1 is used as an inductive feedback oscillator of the type used in the B.F.O./I.F. Alignment oscillator of Figure 29. In this case the tuned circuit is a Denco M.W. R.F. transformer, and the frequency of oscillation is tunable over the H.F. end of the M.W. band (about 1.7 to 0.8 MHz) by means of VC1. In practice the oscillator is tuned to a frequency of 1 MHz.

Inverter 2 is used as a sort of buffer amplifier, and the amplitude of the signal at its output is sufficient to properly drive the clock input of the 4017 decade counter. A 100 kHz output signal is, of course, obtained from the output of the 4017. The unit therefore provides calibration signals at 1 MHz, 100 kHz, and their harmonics.

The circuit is set up and used in much the same way as the crystal calibrators, but it must be remembered that the crystal oscillators have only a very restricted tuning range, whereas this circuit covers a fairly wide range of frequencies. VC1 will almost certainly need some adjustment before a beat note can be obtained. When a beat note has been obtained, VC1 is adjusted for zero beat in the same way as for a crystal oscillator, but it is unlikely that the unit can be adjusted as precisely as a crystal oscillator. The long term stability of this unit will not be as good as that of a crystal controlled unit, and it is advisable to set the unit up against Radio 2 whenever it is used.

It is not a good idea to solder direct to the pins of T1 as this has a polystyrene former which will melt with the heat of the soldering iron. The pins at the base of the coil will fit a B9A valveholder, and it is strongly recommended that the coil is mounted in one of these, and that the soldered connections are made to the holder. The core of the coil is screwed right down when the coil is received, and it must be unscrewed slightly so that about 10 mm of metal screwthread protrudes from the top of the coil.

The pin numbers shown in Figure 46 show the correct phasing for the coil, and it is essential that this is correct. There are actually three windings on the coil, but the one connected across pins 8 and 9 is

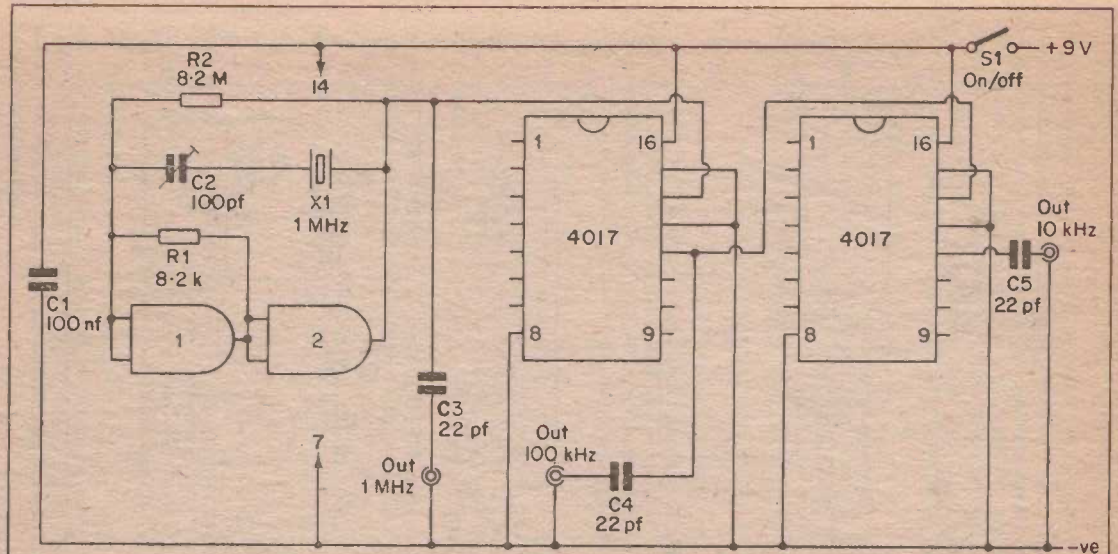

FIG. 45 A 1MHz/100 kHz/10 kHz crystal calibrator

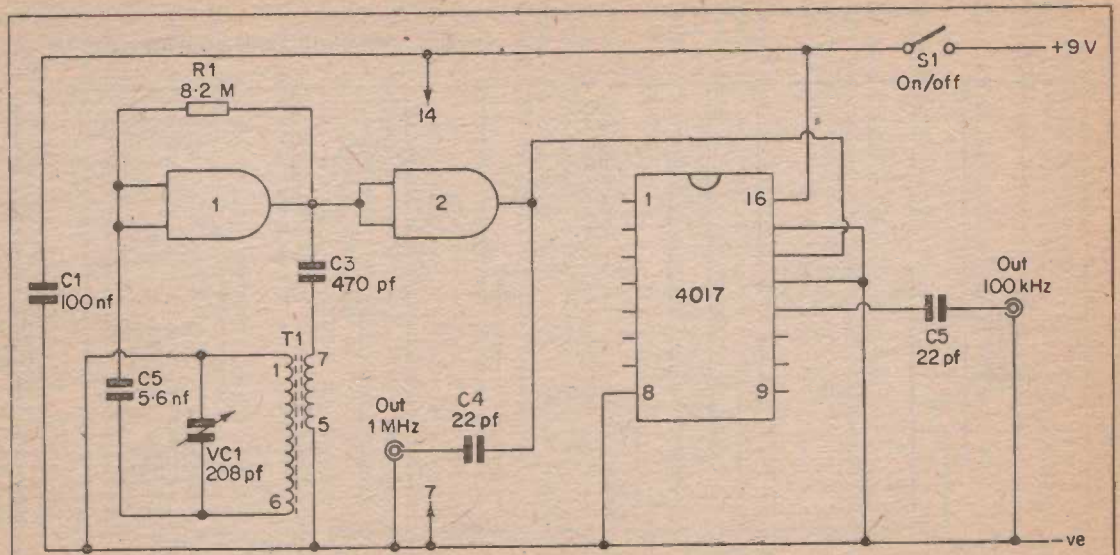

FIG. 46 An inexpensive 1 MHz/100 kHz calibration oscillator

ignored. The full description of the coil (which must be given when ordering it) is 'Yellow R.F. coil for transistor useage, Range 2T'.

All the calibrator circuits shown here have used the 4017 I.C., but the oscillators could just as easily be used to feed a 4013 or 4027 device. In this case the two halves of these I.C.s would be connected in series, and fundamental output frequencies of 1 MHz, 500 kHz, and 250 kHz would be obtained. It would not be possible to set these circuits up against Radio 2 on the L.W. band since there would be no output at 200 kHz, but the standard frequency transmission at 5 MHz could be used instead.

The circuit of Figure 45 is not restricted to use as a crystal oscillator, and circuits of this type are found in many digital electronic circuits. Frequency meters and electronic timers are typical examples. In such applications it will probably be necessary to add extra division stages, but this is very easily accomplished.

Risetime

One point that must be borne in mind when using CMOS frequency dividers is that for reliable operation they require an input signal having a fast risetime. The input waveform should have a risetime of less than 5 micro-seconds and should be more than 0.5 micro-seconds wide.

If a CMOS divider is to be used successfully use from a slow input waveform it must have some form of speed-up circuit added at the input. One way of achieving this is to add a Schmitt trigger at the input, as shown in Figure 47. The way in which the Schmitt trigger works will not be considered here as it was fully dealt with in the previous chapter.

The way in which it speeds up the input waveform is simple. As the input waveform rises it will have no effect on the output of the Schmitt trigger until it reaches the threshold voltage of the trigger. Then the output very rapidly swings positive and operates the divider. It is on the positive edge of the waveform that the divider is operated.

Electronic Game

It was mentioned earlier that the 4017 I.C. has ten outputs apart from the usual carry out one. Five of these outputs are utilised in the circuit of Figure 48 which shows how the device can be used as the basis of a simple electronic game. It also demonstrates the properties of the 4017 I.C.

The two inverters are used in an astable multivibrator, and the operating frequency of this can be varied from less than 1 Hz to over 100 Hz by means of VR1. The output of the multivibrator is used to drive the clock input of the 4017.

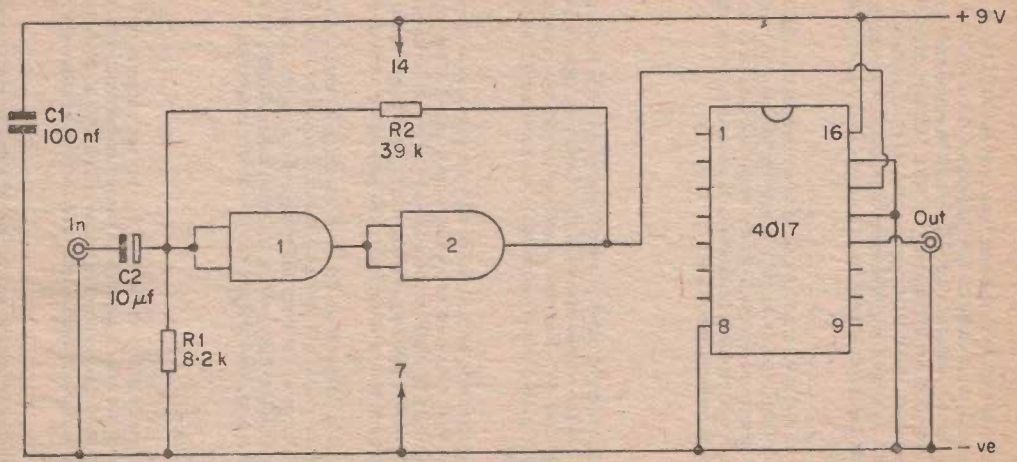

FIG. 47 A Schmitt trigger can be used to reliably operate a divider circuit from a slowly rising wave form

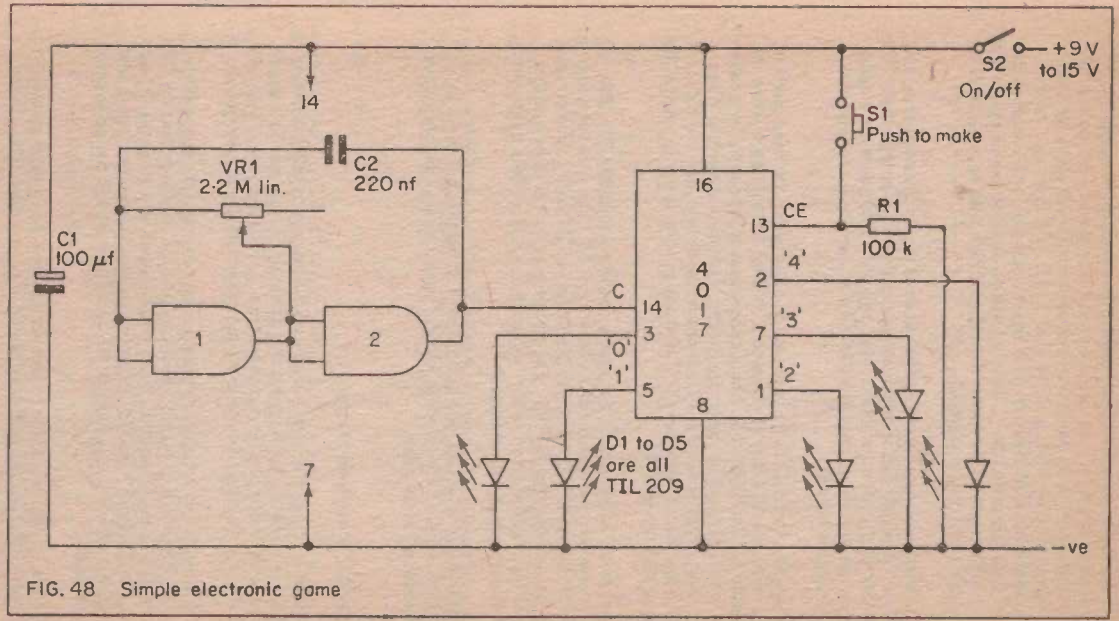

FIG. 48 Simple electronic game

The clock enable terminal of the 4017 is connected to earth through R1, and so when S2 is closed and power is applied to the circuit, the 4017 will start to operate. The first input cycle will cause pin 3 (the '0' output) to go high, and the first L.E.D. will light up. At the commencement of the next clock input cycle pin 3 will return to the low state and pin 5 (the '1' output) will go high for one complete input cycle. Then pin 5 goes low and pin 1 goes high, and so on until all the L.E.D.s have turned on in sequence.

There is then a pause during which none of the L.E.D.s come on, and this is the period during which the unconnected outputs go high. When all five of these outputs have gone high the cycle starts once again from the beginning, with the five L.E.D.s turning on in sequence followed by a break.

In practice the L.E.D.s are mounted in a row along the front panel of the unit, and the idea of thegame is to stop the sequence when the middle L.E.D. (D3) is on. The sequence is stopped simply by pressing S1 which is a push to make non-locking push button switch. When this is operated it takes the clock enable input high, and this blocks the clock signal and holds the 4017 in whatever state it was in when at the instant S1 was closed.

The circuit is reset ready for a new round by releasing S1. The sequence then continues from where it left off. The speed at which the circuit operates, and therefore the degree of difficulty, is controlled by the setting given to VR1. The circuit may appear to be one that tests the reaction speed of the competitor, but it is really more a test of co-ordination and anticipation.

It is possible to use the circuit from a 9 volt supply, but the L.E.D. display will not be very bright and it is better to use a supply voltage of about 12 to 15 volts.

The 4018 Presettable Divider

Almost certainly the most versatile of the inexpensive CMOS frequency divider I.C.s is the 4018 presettable divide by N counter. This can be used to divide by any even number from 2 to 10 inclusive. Figure 49 shows the necessary connections to obtain a divide by ten action.

The basic way in which the device operates is quite simple to understand. The clock signal is divided by 2 at the Q1 output, 4 at the Q2 output, 6 at the Q3 output, 8 at the Q4 output, and 10 at the Q5 output. In Figure 49 the Q5 output is coupled to the data input, and therefore after ten input cycles the circuit is reset and the pulse count starts again.

In order to obtain a divide by two action the Q1 output is connected to the data input instead of having the Q5 input coupled to it. Connect

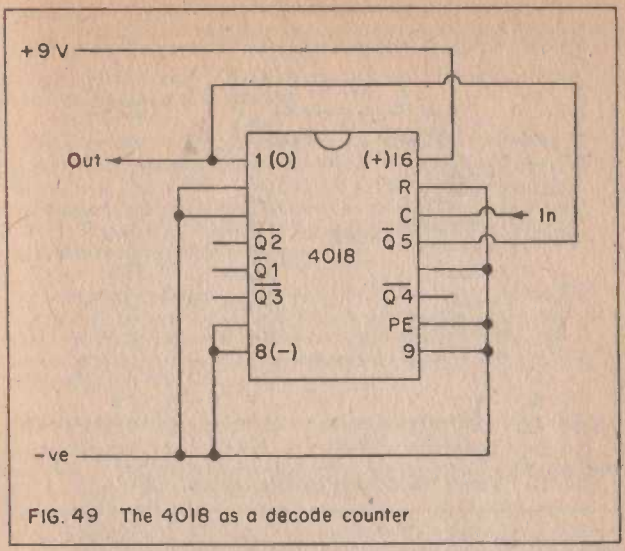

FIG. 49 The 4018 as a decode counter

the data input to Q2 for a divide by 4 action, to Q3 for a divide by six action, or to Q4 for a divide by 8 action.

In common with the other CMOS frequency dividers considered here, the 4018 will operate satisfactorily up to input frequencies of about 5 MHz when it is used with a 9 V supply line.

Display Driver

One of the most useful and interesting of the I.C.s in the CMOS range is the 4026 which is a decade counter and decoder. Conventionally a separate decade counter and decoder I.C. are used to provide a digital readout, but the 4026 performs both these functions and this considerably reduces the complexity of digital systems in which it is used.

Another advantage of this I.C. over most others is that it does not need to drive the output display via either switching transistors or current limiting resistors. It can be used to drive a low current seven segment display direct. The author has used this device successfully with a DL704E seven segment L.E.D. indicator, but it should work just as well with any similar device.

The circuit diagram shown in Figure 50 shows how the 4026 can be connected to operate as a simple pulse counter. The display will show

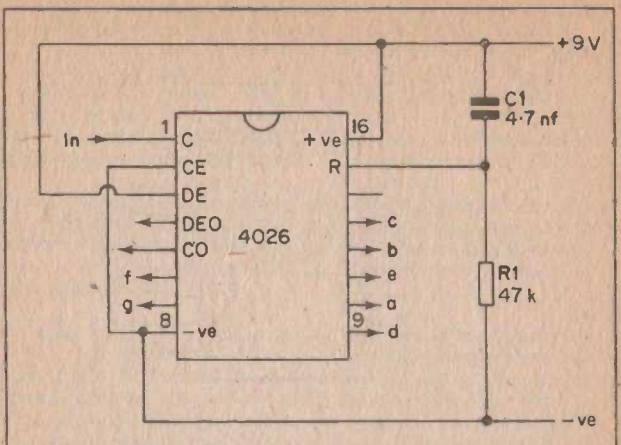

FIG. 50 The 4026 decode counter/readout I.C.

the number of output pulses received at the clock input up to a maximum of nine, after which the display goes back to zero and starts counting up to nine again. In virtually all practical applications a maximum count of more than nine will be required, and the circuit can be made to count as high as one wishes simply by connecting the carry out terminal of this circuit to the clock input of a second identical circuit. The carry out input divides the clock input by ten, and so the first circuit counts the units (and drives the left hand display) while the second one counts the tens (and drives the right hand digit).

Obviously, by adding further digits the circuit can be made to count thousands, tens of thousands, and so on. Note that the 4026 can only be used to directly drive common cathode displays, and is not suitable for direct interface with common anode ones (such as the DL707E).

Apart from the useful features already mentioned, the 4026 has a few others. Pin 2 is a clock enable input, and the circuit operates normally when this is low, and fails to respond to input pulses when it is high. In many applications the clock signal is fed to the counter circuit via an enabling gate. When the 4026 is used in such applications a separate control gate is not necessary, and this input can be fed with the control signal instead.

When pin 3 is high the circuit works normally, but when it is low the display is switched off. The I.C. is operative in all other respects. This is very useful since it means that the display is easily controlled, and

need only be switched on when a reading is to be taken. Economic battery operation is therefore possible where it might otherwise not be.

A display enable output is provided at pin 4, and this can be used to drive the decimal point of a display.

The reset input is usually connected to the negative supply via a resistor, and the counter can be reset to zero by a brief positive pulse to this input. In Figure 50 R1 ties the reset to earth and C1 provides a brief positive pulse at switch on which ensures that the counter starts at zero. If a push button switch is connected in place of C1 it is possible to reset the circuit manually.

There are many applications for which the 4026 is ideally suited, but most of these are too complicated to come within the scope of this book. One simple novelty application is as an electronic random number indicator unit, and a simple circuit for one of these is shown in Figure 51.

The two inverters operate as a 1 kHz astable multivibrator and are used to feed the clock input of I.C.1. The carry out terminal of I.C.1 is in turn used to feed the clock input of I.C.2. These two I.C.s plus the two readout devices thus form a two digit counter.

As the circuit stands, the display will be off and the clock signal will be muted. If S2 is pressed, the clock signal will operate the counter, and it will take the counter through a complete 00 to 99 count about ten times per second. When S2 is released, the counter will stop at whatever number it happened to be at at the instant S2 broke the clock enable circuit to earth.

What this number happens to be is quite unpredictable, and in this way the circuit operates as a random number indicator. The unit can be made to display the number by operating S1 which connects the display enable terminals to the positive supply.

S3 is the normal on/off switch.

Bilateral Switches

A bilateral switch is a type of enabling gate, except whereas most enabling gates are only suitable for use with pulsed signals, a bilateral switch can be used in linear applications. For low signal levels the typical distortion level through a bilateral switch is only about 0.4%.

There are two readily available CMOS bilateral switches, the 4016 and the 4066. These are both contained in a 14 pin DIL package and have the pinning arrangement shown in Figure 52. The main difference between these two devices is that the 4016 will operate at frequencies up to about 10 MHz while the 4066 will work up to 40 MHz.

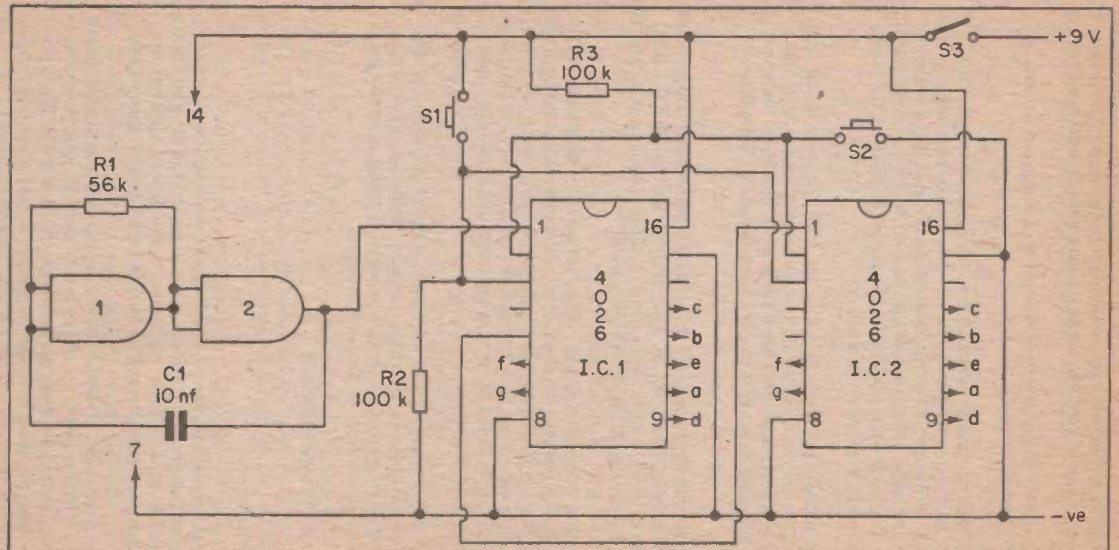

FIG. 51 The circuit diagram of a simple electronic random number indicator

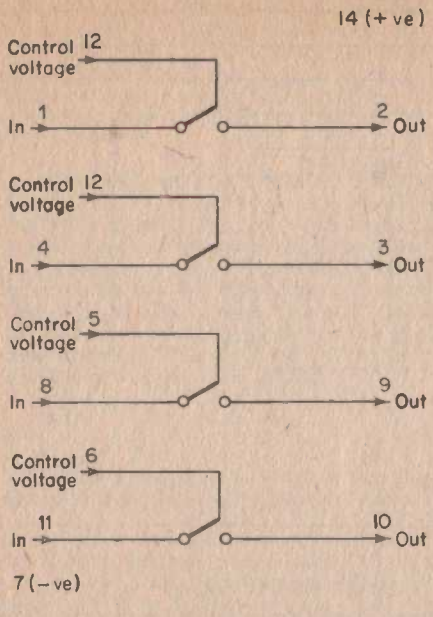

FIG. 52 The leadout diagram for the 4016 and 4066 I.C.s

The on resistance of the switches is approximately 300 ohms and the off resistance is about 1 million Megohms. The switches are off when the control voltage is low and on when it is high. Signal levels of about two volts peak to peak can be handled when these devices are operated from a single supply rail, but when operated from a dual balanced supply they can handle peak to peak signal voltages equal to the sum of the supply rail voltages.

As will be apparent from Figure 52, the 4016 and 4066 devices each contain four bilateral switches, and this makes these devices very versatile.

It is worth noting that although each switch has an input and output legend in Figure 52, this has only been done as it is more convenient to think in these terms when considering practical uses for these devices, than just simply using pin numbers for identification purposes. These switches are, as their name states, bilateral, and in practice it would seem to be possible to use them either way round.

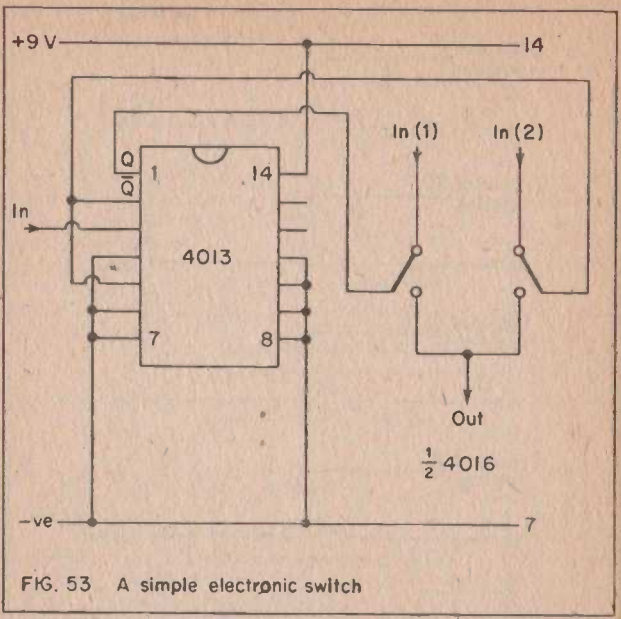

FIG. 53 A simple electronic switch

These switches are only single throw types, but it is possible to obtain a double throw action by using two switches with the outputs connected in parallel. The control terminals of the switches must be fed from a circuit which ensures that they are always in antiphase, with one switch in the on state and the other in the off condition.

This can be achieved by feeding the switches from the Q and $\bar{Q}$ outputs of a flip flop circuit, such as the 4013 type D flip flop. Such a circuit is shown in Figure 53.

The 4013 is connected as a divide by two circuit with one of the two flip flops it contains being unused. The two outputs of the 4013 are always in the opposite logic state and these states change with each successive input pulse. If, for instance, the Q output is high and the $\bar{Q}$ one is low when the power supply is initially connected to the circuit, then input 1 will be enabled and input 2 will be blocked. Applying a brief input pulse to the circuit will cause the flip flop to change state, and then input 1 will be blocked and input 2 will be enabled. The circuit thus provides a purely electronic S.P.D.T. switch.

Several variations on this basic circuit are possible. By paralleling the inputs instead of the outputs, the circuit will then channel the single input circuit to only one of two circuits connected at the output. By simply omitting one of the bilateral switches a purely electronic S.P.S.T. switch is produced. By connecting two further bilateral switches in the same configuration as the original two, and feeding one control input from each output of the 4013, a D.P.D.T. action is obtained.

When comtemplating using one of these switches always bear in mind the limitations on both the signal amplitude and impedance. For example, the D.P.D.T. version of this switch could not be used as the send/receive switch of an intercom, as although it could probably be made to handle the signal amplitudes by use of a dual balanced supply, the 300 ohm series resistance of each switch would limit the output to the speakers to an unsatisfactory level. The 4016 device is specified in the circuits described here since there are very few applications where the additional performance of the 4066 is required, and the 4016 is less expensive and more widely available.

Touch Switch

In simple applications a touch activated version of the circuit of Figure 53 is probably of more use. Such a circuit appears in Figure 54.

Here two inverters are used as a bistable multivibrator with high value cross coupling resistors. This makes the circuit sufficiently sensitive to be operated by touch contacts. We will assume for the sake of this circuit explanation that the circuit takes up the state of having inverter 1 output low and inverter 2 output high when the supply is initially connected (although it could in fact taken up the opposite state).

In order to trigger the circuit into the opposite state, and so reverse the states of the bilateral switches, it is merely necessary to touch the left hand set of touch contacts. This takes the input of inverter 1 low since it will be connected to earth through the skin resistance of the operator. This sends the output of inverter 1 high which in turn takes the input of inverter 2 high due to the coupling by way of R2. Inverter 2 output therefore goes low, and inverter 1 input will therefore stay in the low state even when the operator's finger is removed from the touch contacts, since it will be held low by being coupled to the low output of inverter 2 by way of R1.

The circuit can be reset to the original state by touching the right hand set of touch contacts. An identical circuit action then takes place, but the roles of the inverters are reversed this time.

It is possible to trigger the circuit from one state to the other indefinitely by operating each set of contacts in turn. There are, of course, no moving parts whatever to wear out

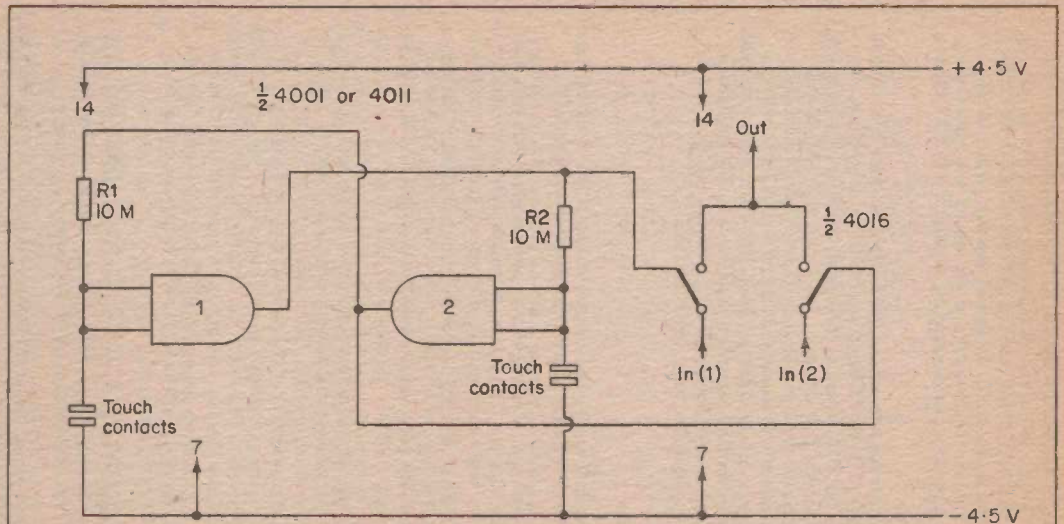

FIG. 54 An S.P.D.T electronic touch switch

As was the case with the circuit of Figure 53, several variations on this basic circuit are possible.

Audio Squelch

Squelch circuits are commonly employed in F.M. tuners and receivers, and in V.H.F. communications equipment. With this type of equipment there is a high level of background noise in the absence of a signal, and the purpose of the squelch circuit is to mute the receiver unless a signal is present. This eliminates the very loud and hence annoying background hiss that occurs when tuning an F.M. set between stations, or when no signal is present at the input of a V.H.F. communications set.

In the case of this type of equipment the squelch circuit is usually activated by the carrier wave signal of the received transmission, rather than by the audio signal. There are however, audio applications where a squelch circuit can be useful. One example would be in the case of a public address system which is being used in a noisy environment, with a fairly high background noise level being transmitted over the equipment.

In this case the squelch circuit would be adjusted so that it would not be activated by the normal background noise level (of human rather than an electrical origin), but so that it would only enable the equipment in the presence of a proper microphone signal.

There must be many other applications for such equipment apart from this one, and this is an application to which the 4016 is ideally suited. The circuit diagram of an audio squelch unit using one of the bilateral switches in the 4016 I.C. is shown in Figure 55.

Operation of this circuit is quite straightforward. Some of the input signal is fed to the input of the bilateral switch and the remainder is fed to a high gain common emitter amplifier via a gain control (VR1) and a D.C. blocking capacitor (C2). Tr1 is the basis of the amplifier and this has collector load resistor R1 and base bias resistor R2.

The output of this amplifier is fed to a rectifier and smoothing network using C3, D1, D2, C4 and R3. The output of this network is fed to the control input of the bilateral switch.

VR1 is adjusted so that the control voltage fed to the bilateral switch is insufficient to enable the switch with only a background signal being fed to the input, but it is adjusted so that this voltage is only just short of the trigger voltage of the switch. Therefore, when a proper input signal is present, the trigger voltage will be exceeded and theswitch will be enabled. The unit thus provides the required squelch action.

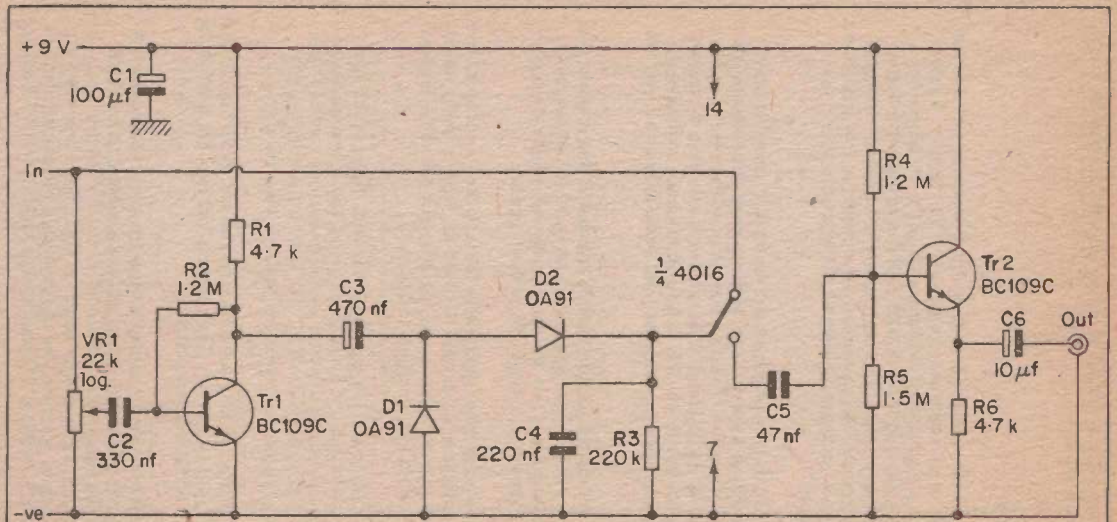

FIG. 55 An audio squelch unit

It is perhaps not entirely correct to call the voltage at which the bilateral switch changes state a trigger voltage, because this infers that the switch can only be fully on or fully off. This is not the case, and there is a range of control voltages over which it will be in an intermediate state. Fortunately however, this range of voltages is very restricted, and the 4016 has a fairly well defined changeover voltage. This circuit therefore works satisfactorily in practice without the need to incorporate any triggering.

The circuit has a fast attack and slow decay (hysteresis) which is necessary to ensure that the unit does not cut off during the brief pauses which occur during normal speech. The decay time can be altered to suit individual requirements by modifying the value of C4. The decay time is proportional to the value of this component, and it is something less than one second with the value shown in Figure 55.

Satisfactory operation of the device is possible with a nominal signal input level of less than 100 mV R.M.S. to a little more than 1 V R.M.S. (sinewave input). The input impedance is about 10 k. Tr2 and associated components form an emitter follower output stage which provide the unit with a low output impedance.

C3 must be a high quality component if it is an electrolytic type, and it would probably be best to use a tantalum bead or plastic foil component here. Some electrolytic types have relatively high leakage currents which would result in the decay time of the circuit being greatly prolonged.

Automatic Cutout

This circuit is intended for use with disco and home movie equipment where the facility to automatically cut out a secondary channel (playing background music for instance) by applying a signal to the main input (such as a commentary) is required. The circuit diagram of this unit is shown in Figure 56.

The controlled input is fed to a gain control, and then to a bilateral switch. From here it is fed to the output via mixing resistor, R1.

Some of the main input is fed to gain control VR3, and then to mixing resistor R5. VR1 and VR3 allow the two input signals to be balanced to the required levels at the output. Some of the input signal at the main input is fed to a high gain common emitter amplifier by way of gain control (VR2) and D.C. blocking capacitor (C4).

The output from this amplifier is fed to a rectification and smoothing network using C2, D2, D1, C1, and R2. The output of this network is fed to the control input of the bilateral switch.

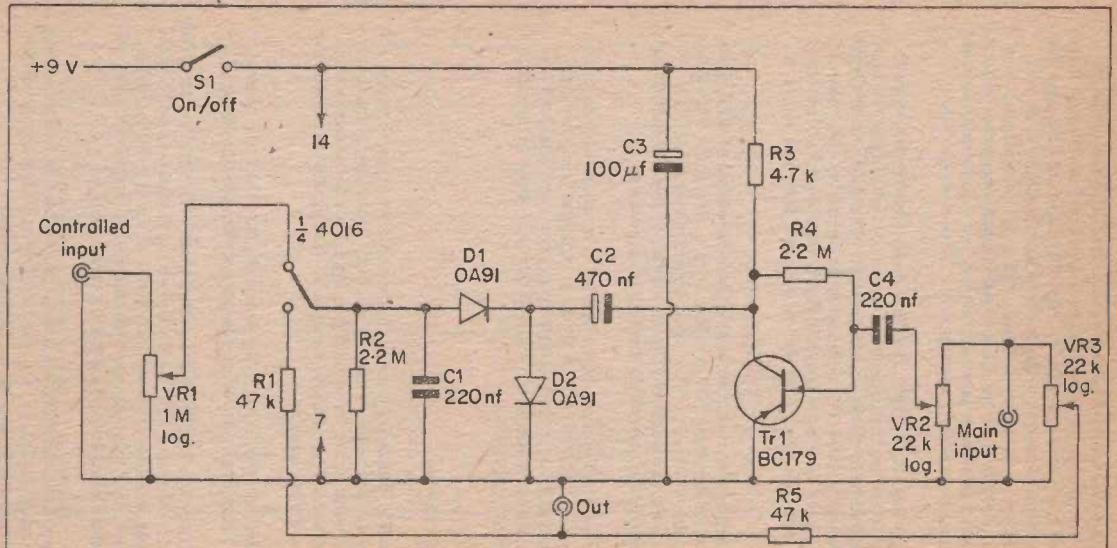

FIG. 56 An automatic cut out unit

When no input signal is fed to the main input, the control input of the bilateral switch will be at earth potential, but as this is a positive earth circuit the control input is in fact high, and so the switch is enabled. The controlled signal is therefore fed to the output.

If an input signal of sufficient level is applied to the main input, the negative D.C. bias produced across R2 and C1 will be virtually equal to the supply potential, and so the control input of the bilateral switch will be taken low, and the controlled input will be blocked. Thus the main input can be used to cut out the controlled one.

VR2 is given any setting which enables the main input to control the secondary one without spurious interruptions of the controlled input occurring. A minimum input amplitude of about 100 mV is required at the main input in order to cut off the secondary input.

As was the case with the previous circuit, the diode feed capacitor (C2) should be a high quality electrolytic type, or a plastic foil component.

Also in common with the previous circuit, this one has hysteresis, with the decay time of the circuit being variable by means of C1.

The type numbers under which the CMOS I.C.s employed in the circuits in this book are sold have already been discussed, and details of the leadout arrangements have been given. Details of the other semiconductors which have been specified for projects are given in Figure 57.

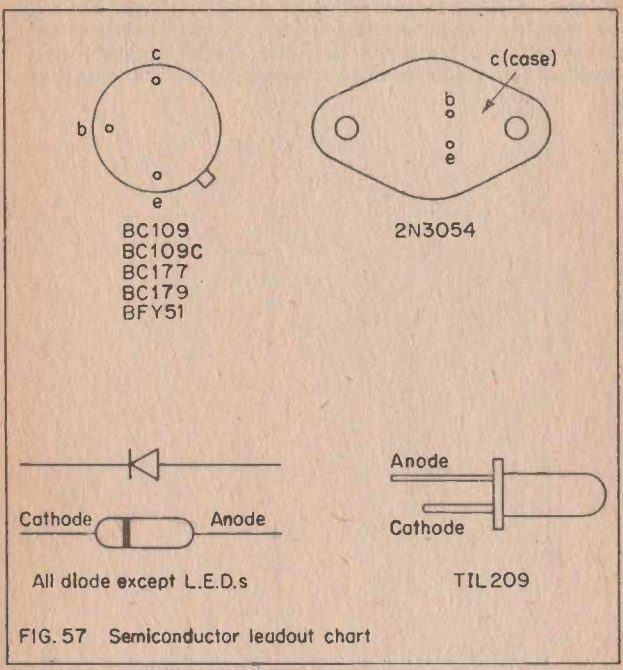

FIG. 57 Semiconductor leadout chart

There are many alternatives to the specified semiconductors, and suitable substitutes for the BC109 for instance, are BC169, BC184L, BC172, etc. However, as the specified types are probably the cheapest and most widely available types, there is little point in making a substitution unless a suitable alternative is already to hand.

All resistors are ordinary $\frac{1}{4}$, $\frac{1}{3}$, or half watt types of the usual tolerances (5% up to 1 Meg. and 10% above 1 Meg.) except where noted otherwise in the text. Potentiometers are all carbon types, and they are either logarithmic or linear (log. or lin.), the circuit diagram indicating which

is appropriate for each one. Presets can be virtually any type and are chosen to best suit the particular layout used.

Except where specified otherwise in the text, capacitors up to about 330 nF (0.33 mfd) can be any plastic foil or ceramic type having a tolerance of 20% or better. Some ceramic types have very wide tolerances and are best avoided by inexperienced constructors who are in doubt as to their suitability for a particular circuit.

Trimmer capacitors are used in some of the R.F. oscillators, and at the relatively low frequencies involved in these it is not necessary to use any special type. Any trimmer having the specified maximum capacitance and a reasonably low minimum capacitance should be satisfactory.

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