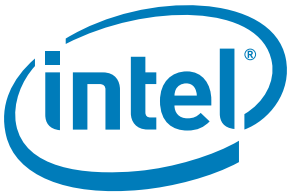

Intel® Atom™ Processor Z2760

Datasheet

October 2012

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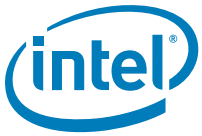

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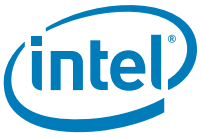

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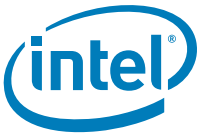
Tables



Revision History

Document Number	Revision Number	Description	Revision Date
328104	001	• Initial release	October 2012

§

1 Introduction

1.1 Platform Overview

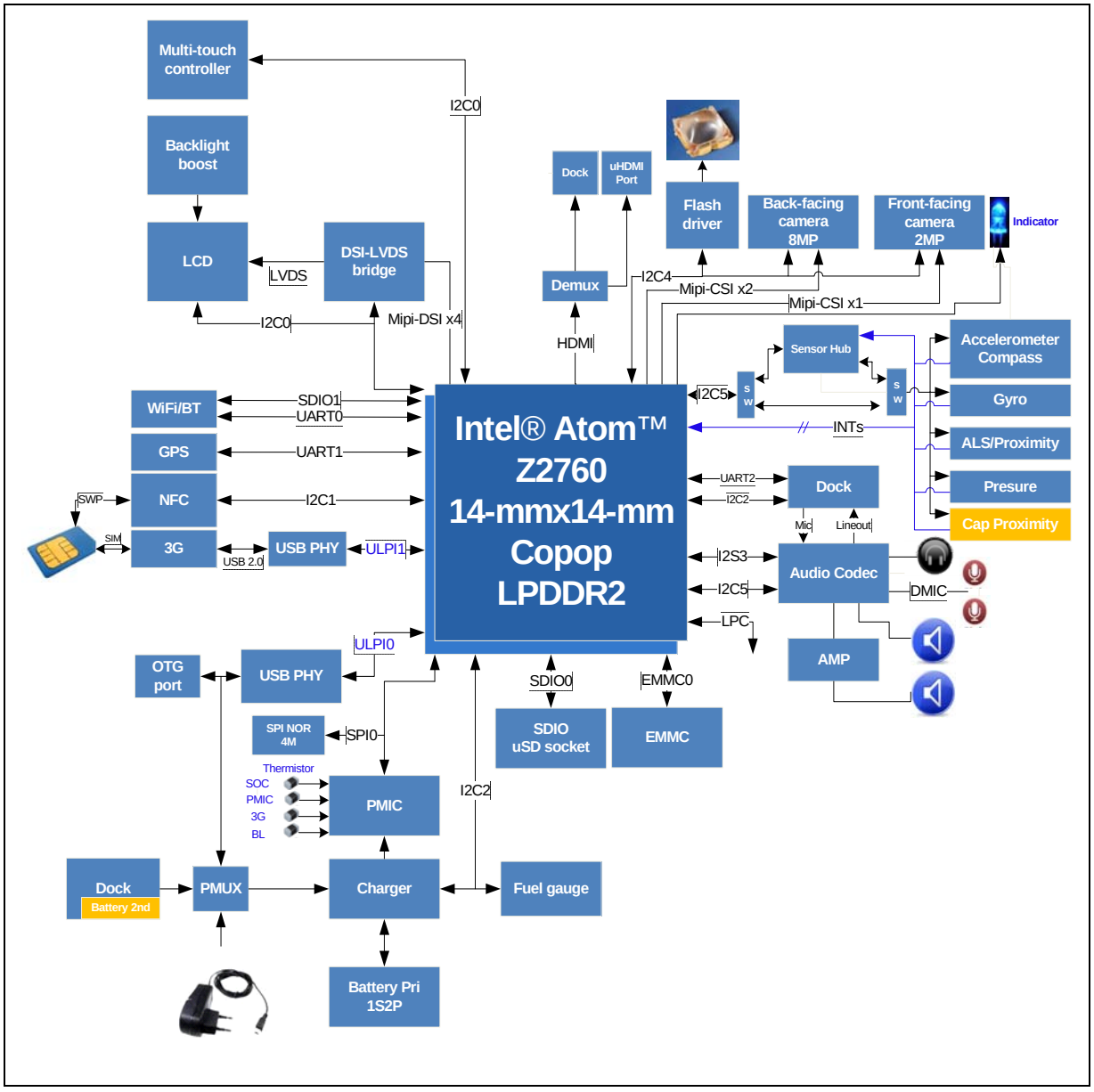
This Datasheet provides Direct Current (DC) and Alternate Current (AC) electrical specifications, signal integrity, differential signaling specifications, pinout and signal definitions, interface functional descriptions, and additional feature information pertinent to the implementation and operation of the processor on its respective platform.

Intel® Atom™ Processor Z2760 is the next generation 32 nm System on a Chip product targeted for tablet and tablet convertible platforms. Atom™ Processor Z2760 is implemented based on the second-generation high-k metal gate transistor.

Note: Throughout this document the Atom™ Processor Z2760 is referenced as Processor or SoC.

Figure 1.2 shows an example representation of the platform.

Figure 1-1. Platform Block Diagram



Note: An example system block diagram using the Intel® Atom™ Processor Z2760.

1.2 Atom™ Processor Z2760 Feature Summary

Table 1-1. Atom™ Processor Z2760 Key Feature Summary

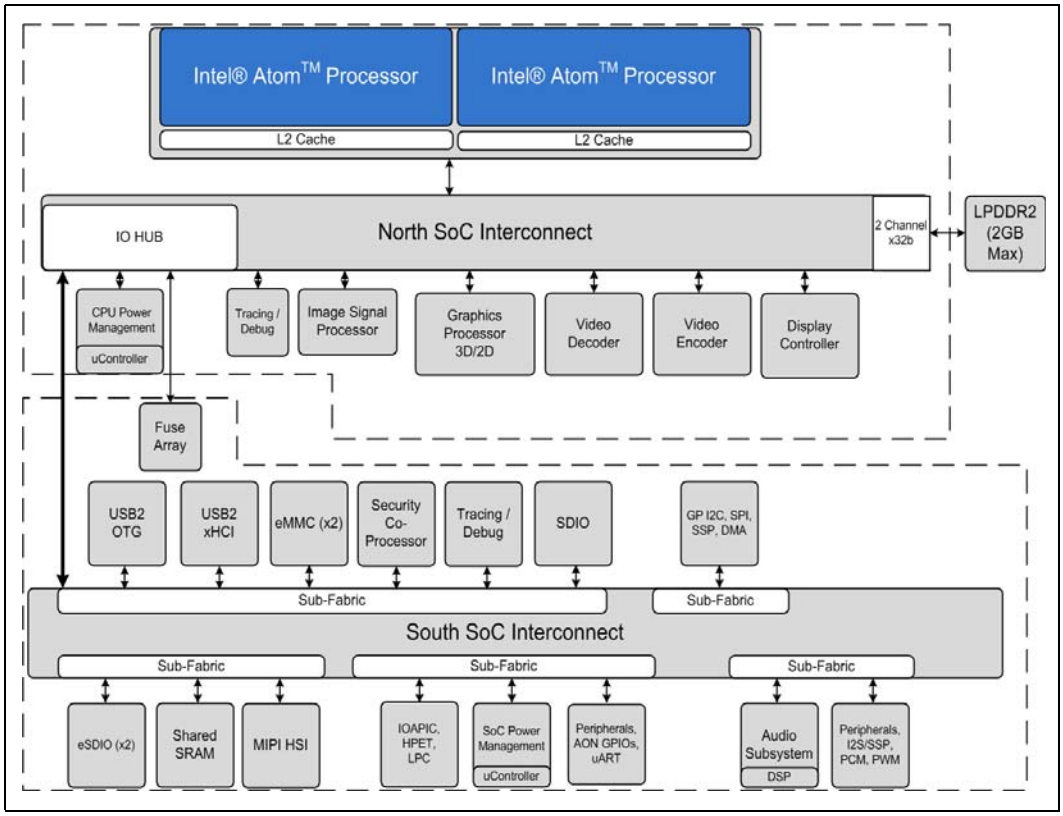
- Atom™ Processor Z2760 - System-On-Chip (SoC)
  - 32 nm high-k/metal gate transistor technology
- Compact Co-POP Package
  - 14 mm x 14 mm, 760 balls, 0.483 mm pitch
  - Support Dual Channel 32-bit LPDDR2-800 Co-POP memory technology
- Intel® Atom™ Microarchitecture
  - Intel Smart Cache, 1MB L2
  - Intel® Hyper-Threading Technology (Intel® HT Technology)
  - Enhanced data prefetcher and enhanced register access manager
  - Enhanced Intel® Smart Idle Technology-C6/S0i1/S0i3 power reduction features
  - Enhanced Intel SpeedStep® Technology
  - Digital Thermal Sensor (DTS)
  - Intel® Burst Technology
- 2D/3D Graphics Core
  - DirectX* 9.3, OpenVG* 1.1, OpenGL-ES*2.0, OpenGL* 2.1 support
- Hardware accelerated video encode and decode
  - 1080p video encode
  - 1080p video decode
- Display Controller
  - x4 Interface
  - MIPI-DSI port
  - HDMI 1.3a interface
- System Memory Interface
  - Dual Channel 32-bit LPDDR2 Interface
  - Supports 1GB, 2GB total capacity
  - Supports a rate of 800 MTS
- Programmable ISP
  - Glue-less interface to CMOS sensors with MIPI CSI-2 interface
  - High resolution still image 8 Mpixel
  - Video - 2 Mpixel
  - Supports Auto-Exposure, Auto-White Balance, and Auto-Focus
- Storage
  - eMMC 4.41
  - SD / SDHC (SD 2.0)
- 6 Master I^2C controllers
  - Supports fast , and standard speed modes
- SPI Controller
  - 1 PMIC interface
- USB 2.0 High Speed Interfaces
  - 2x USB Interfaces via ULPI
- UART
  - 3x 16550 compliant UART controllers
  - Up to 3.6864M baud rate
- Intel® Smart Sound Technology (Intel® SST)
  - Low power programmable codec to decode/encode popular audio formats
- Flexible GPIO configuration
  - Configurable mux with functional blocks
  - Always on GPIOs to enable wake events
  - Core power GPIOs shut down in sleep mode
- Test Interface
  - IEEE-1149.1 and IEEE1149.7 (JTAG) Boundary Scan
- Intel Smart and Secure Technology
  - Programmable engine
  - Low power
- Application Examples
  - Tablets
  - Tablet Convertible Devices

Note: *Other names and brands may be claimed as the property of others.

1.3 Atom™ Processor Z2760 Partitioning

Atom™ Processor Z2760 contains two main partitions—the North Complex (NC), that has functions that are roughly equivalent to (Processor + Graphics Memory Controller Hub (GMCH)), and the South Complex (SC).

Figure 1-2. Atom™ Processor Z2760 SoC Partition Diagram



The main components of the North Complex are:

- Dual Intel® Atom™ Processor cores (Each core supports two threads)
- Dual channel 32-bit LPDDR2 memory controller
- a3-D graphics core
- Video decode engine
- Video encode engine
- MIPI-DSI interface
- Dedicated pipe for HDMI
- Image signal processor for camera support

The main components of the South Complex are:

- Intel® Smart Sound Technology (Intel® SST)
- Intel® Smart and Secure Technology (Intel® S&ST)
- eMMC controller
- SD/SDIO controllers
- System Control Unit
- Two ULPI controllers to support two USB interfaces
- iLB (Intel Legacy Block) to support an LPC Interface

- Standard interfaces such as GPIO, I^2S, UART, I^2C

Atom™ Processor Z2760 will deliver Intel® Smart Idle Technology (Intel® SIT), (S0ix) power, lower scenario power, and higher performance Gfx/Video encoding/decoding. It has multiple logical and physical power partitions to selectively turn off/on power to functional components with OSPM architecture.

1.4 Processor Core

- Dual IA-32 CPU Cores
- Intel® Hyper-Threading Technology 2-threads per core
- On die, primary 32kB, 8-way L1 instructions cache and 24kB, 6-way L1 write-back data cache per core.
- 1MB, 8-way ECC protected L2 cache per core.
- Intel® Streaming SIMD Extensions 2 and 3 (SSE2 and SSE3) and Supplemental Streaming SIMD Extensions 3 (SSSE3) support
- Thermal management support via Intel® Thermal Monitor (TM1 & TM2)
- Supports C0-C4, C1E-C4E and Deep Power Down Technology (code named C6)
- Execute Disable Bit support for enhanced security
- Supports Intel® Burst Technology
- Supports Intel® SpeedStep™ Technology

1.5 System Memory Features

- There are two identical memory controllers used to support dual-channel architecture. Each controller supports a 32-bit channel data width.
- Integrated LPDDR2 Memory controller that supports dual x32 channels
- 800 MT/s data rates
- Maximum bandwidth, 3.2GB/s (single channel), 6.4GB/s (dual channel)
- Support for a total memory size of 1GB, and 2GB
- Support for 1Gb, 2Gb, and 4Gb memory technology
- Support for LPDDR2-S4B (1.2V) devices.
- Support 14 x 14 mm one channel or two channels PoP (Package on Package)

1.6 Graphics Processing Unit Features

- Support DirectX* 9.3 compliant Pixel Shader* v2.0 and OpenGL* 2.1
- 533 MHz render clock frequency

*Other names and brands may be claimed as the property of others.

1.7 Video and Display

- The Intel® Atom™ Processor supports full MPEG2(VLD/ iDCT/MC), WMV, Fast video Composing, HW decode/ acceleration for MPEG4 Part 10 (AVC/H.264) & VC-1; 720p60, 1080i60, 1080p@24 up to 20 Mbps
- MPEG4 part2 is supported on Atom™ Processor Z2760 SW, but it does not utilize Atom™ Processor Z2760 HW
- SW Video Encode (no HW support); No hardware assist for Flash Decode
- Video image Enhancement: Hue, Saturation, Brightness, Contrast (HSBC) adjust, Bob De-Interlacing

1.7.1 Hardware Accelerated Video Encode

- The video encode hardware accelerator improves video capture performance by providing dedicated hardware based acceleration.
- Permits 720p30 H.264 BP encode
- MPEG4 encode and H.263 video conferencing.
- Encode Support up to H.263 Level 70.
- Full hardware accelerated Elementary Stream Encode.
- Subpel motion estimation and Integer motion estimation.

1.7.2 Hardware Accelerated Video Decode

- Video Decode Hardware accelerator with full Elementary Stream Decode
- Support Dual stream fast context switch homogeneous elementary stream decode up to H.264 Level 4.1
- Decode Support up to MPEG-4 ASP Level 5, MPEG-2 Main Profile High level, WMV Main Profile High level, VC-1 High Profile level 4.2.

1.7.3 Display Controller

- 2-D Graphic controller
- Two display pipes, Pipe A and B support the dual independent displays
- MIPI-DSI interface (4 lanes total)
  - Up to 1.0 Gbps data rate per lane
  - Command mode panel with full frame buffer support
  - 1, 2, 3, or 4-lane support
  - Partial display mode support with type 1 and type 2 displays
- Atom™ Processor Z2760 supports standard features as listed in HDMI 1.3a specification, the following is the summary of key features:
  - Support maximum 1080p60 resolution
  - Auto Lipsync Correction
  - Compatible with DVI 1.0 compliant devices. (HDMI 1.3a Appendix C)
- Video Image Enhancement processing integrated into the display controller

- Support for dynamic contrast enhancement, skin tone correction, blue stretch, programmable gamma, color space conversion, hue, saturation, contrast, and brightness controls.
- Supports HDCP 1.3

1.7.4 Video Image Enhancement Features

- Adaptive dynamic black level/white level dynamic range expansion
- Skin color correction
- Blue stretch enhancement
- Demodulation angle correction
- Fully programmable 3 x 3 matrix color space correction
- Hue, saturation, contrast, and brightness adjustment
- 10-bit per pixel numerical precision
- Throughput (clock speed) for up to 1080p @ 60 fps display

1.8 Image Signal Processor Feature Set

- Two MIPI CSI-2 interfaces for external image sensors.
- Still image—8 MPixels, ISP is capable to process 15 fps
  —Burst Mode Capture—up to 15 fps
- Bad pixel detection and correction
- Enhanced color interpolation
- Lens shade correction
- Automatic white balancing
- Sensor bit depth: up to 12 bit
- Programmable gamma correction
- Flash light control
- Black level compensation
- Noise filter, sharpening/blurring filter
- Auto focus and auto exposure measurements
- Color correction matrix
- Luminance/chrominance swapping
- Color processing (contrast, saturation, brightness, and hue)
- YUV sensor support
- Digital zoom for video and preview resolutions
- Horizontal mirroring of self-picture frame
- Display ready RGB output in self picture and the ability to rotate in 90 degree steps
- Windowing and frame synchronization

- Frame skip support for video encoding

1.9 Intel® Smart Power Technology (Intel® SPT) and Intel® Smart Idle Technology (Intel® SIT)

- Supports (C0–C6) states
- Display Device controls D0–D3
- GFX Device states D0, D0i3, and D3
- ISP Device states D0, D0i3, and D3
- Video Decode/Encode engine states D0, D0i3, and D3
- Programmable thermal throttling
- Conditional Memory Self-refresh during C2–C6 states.
- Supports C2 popup for snoop and defer C3/C4 states based on snoop traffic.
- Active power management of display links.
- Programmable thermal management algorithms

1.10 South Complex Overview

The South Complex integrates accelerators and system control functions that are typically performed by the IA-32 processor or programmable external components. This significantly reduces the system power for many applications and lowers the system cost and component count.

The South Complex is built around industry standard interfaces and interconnects. This enables easy integration of common IP blocks from the embedded ecosystem to provide industry standard Input and Output interfaces.

The South Complex provides the following interfaces and functionality:

- Support boot from eMMC* devices
- Two eMMC* channels
- Two external ULPI interface to off-chip USB transceivers
- SD/SDHC card interface
- 4-bit SDIO interfaces for internal COMM devices
- I^2S interfaces for external analog audio codecs
- I^2C interfaces to allow the monitoring of in-box environmental sensors and to control in-box components
- SPI master interfaces to interface with simple external devices
- GPIO pins
- An integrated audio accelerator providing autonomous decoding of most common compressed audio and voice formats
- An integrated security engine providing high speed decryption of protected content, validation of signed software modules, and protected key management

- An integrated, System Controller Unit (SCU) to provide power management for the entire Atom™ Processor Z2760 chip
- A 256KB block of SRAM for system boot code and other functions when the system DRAM is unavailable
- An LPC interface

1.10.1 SD/SDIO/eMMC*

- Support for one SD v2.0 port with SDHC capability
  - — (Classes 2, 4, 6 and 10)
  - — up to 200Mb/s (50 MHz x 4 bits)
- Two SDIO v2.0 ports with wake-up sources to support communication devices
- eMMC*
  - — Support two eMMC* v4.41 Ports:
    - —x8 bus width, up to 800Mb/s

1.10.2 Intel® Smart & Secure Technology (Intel® S&ST)

Atom™ Processor Z2760 contains a Security Engine and additional hardware security features that enable a secure and robust platform.

Platform security critical elements (keys and licenses) are stored in Secure Storage.

Atom™ Processor Z2760 is also capable of providing fine grain memory protection by enforcing a memory access policy for each device. This feature is called IMR (Isolated Memory Region). IMR provides DMA protection. It also supports inline encrypt and decrypt engines.

The key security engine features are:

- Secure Boot
- Flexible Secure Execution Environment to run 3rd party Secure Services (with Security Engine 2.0 SDK)
- Secure Storage eMMC (in NAND & Intel Fuses)
- Hardware cryptographic acceleration for AES, DES, and 3DES algorithms
- PKI Engine supporting RSA and ECC acceleration
- Hashing Engines for SHA-1 and SHA-2
- FIPS compliant RNG
- Digital Rights Management
- Memory access control mechanism through Isolated Memory Regions (IMR)
- Inline encrypt and decrypt engines to provide robust and scalable DRM playback
- Additional Security Timers and Counters

1.10.3 Intel® Smart Sound Technology (Intel® SST)

- Based on standard 32-bit RISC architecture with integrated 24-bit audio processing instructions. Industry leading low-power consumption coupled with high-fidelity the 24-bit audio digital software provides support for:
  - MPEG2, MPEG3, MPEG2/4, MPEG-L2.5, AAC, AAC+, eAAC+, WMAv9, AV, RA, and AC3
- Supports VoIP
- Dual-issue, static super-scalar VLIW
- Mode less switching between 16-, 24-, and 64-bit dual-issue instructions
- Dual MACs that can operate as 32 x 16-bit and/or 24 x 24-bit
- Four Integrated I2S ports for discrete audio codec
- Supports two DMA engines

1.10.4 Low Speed Peripheral Features

1.10.4.1 General Purpose I/O (GPIO)

Atom™ Processor Z2760 provides highly-multiplexed general purpose I/O (GPIO) pins for use in generating and capturing application-specific input and output signals. Atom™ Processor Z2760 has two instances of the GPIO controller.

- GPIO_0 Controller locates in the AON power well, connects to the AON SC Fabric, and it can control up to 93 GPIO buffers.
- GPIO_1 Controller locates in the Core power well, connects to the GP Fabric and can control up to 76 GPIO buffers.
- Each GPIO pin can be programmed as an output, an input, or as bi-directional for certain alternate functions (that override the value programmed in the GPIO direction registers).
- When programmed as an input, a GPIO can also serve as an interrupt source. All GPIO pins are configured as inputs during the assertion of all resets, and they remain inputs until configured otherwise.
- In addition, select special-function GPIO pins serve as bi-directional pins where the I/O direction is driven from the respective unit (overriding the GPIO direction register).

A number of GPIO pins are designed to support wake functionality and currently wake capable GPIO pins need to be connected to the AON GPIO 0 controller. When a wake GPIO pin detects a rising/falling edge during standby, GPIO 0 sends an interrupt signal to the System Controller Unit (SCU) to initiate the wake sequence for the system.

1.10.4.2 Inter-Integrated Circuit (I^2C) Controller

Only 7-bit addressing mode is supported. These controllers operate in master mode only, no multi-master support.

Modes of operation:

- Standard speed mode (with data rates up to 100Kb/s)

- Fast mode (with data rates up to 400Kb/s)

1.10.4.3 Serial Peripheral Interface (SPI)

- Implements four SPI master controllers
- Each controller contains:
  - one 64-entry receive FIFO
  - one 64-entry transmit FIFO
- SPI_0—Support master mode
  - Dedicated for PMIC interface by SCU
  - Not accessible by IA core
- SPI_1 and SPI_2—support master mode
  - Contains multiple chip selects
  - Accessible by IA-32 processor
- SPI_3
  - Support Master and Slave modes
  - Supports data entries from 4 to 32 bits in length and FIFO depths of 16 entries.

1.10.4.4 UART

Atom™ Processor Z2760 supports three instances of a 16550 compliant UART controller.

1.10.5 USB 2.0

- Supports two ULPI ports for interface with off chip transceivers.
- An 8-bit data interface at 60 MHz ULPI clock.
- Refer to UTMI+ Low Pin Interface (ULPI) Subsystem.

1.10.6 System and Power Management Controller Features

The system controller subsystem consists of system controller core, which contains on-chip memories (ROM, RAM), peripherals and shim.

1.10.7 Shared SRAM

The SRAM used in Atom™ Processor Z2760 is essentially a single port, fully pipeline RAM with a throughput and latency of 1 cycle. The total capacity is 256KB. It is divided into nine chunks (7 physical 32KB instances and 2 physical 16KB instances). The SRAM is shared between multiple agents in Atom™ Processor Z2760, namely Audio, USB and the System Controller. The SRAM controller acts as the interface between the Atom™ Processor Z2760 Fabric and the SRAM. It provides secure access to the SRAM in addition to the protocol conversion between the Fabric and the SRAM.

1.10.8 System Controller Subsystem

The System Controller subsystem is one of the first subsystems to be functional after reset. It is ON all the time and very low power. It is responsible for the following functionality:

- System boot—including loading boot block code for IA-32 core, P-unit and System Controller Unit from eMMC*
- Platform Level Configuration Block
- Implements OSPM based on the Power Management policy of peripherals connected to the Atom™ Processor Z2760
- Implementing sequencer logic for power/clock gating
- Implementing Message Signaled Interrupts
- Handling interrupts and wake-up events
- Receiving messages from the IA-32 core
- Communication with Low Speed peripherals
- Implementing Virtual RTC (copy of PMIC RTC)

1.10.9 Intel Legacy Block

The Intel Legacy Block is a collection of blocks critical for implementing legacy PC platform features.

Supports:

- I/O APIC
- High Performance Event Timers (HPET)
- Low Pin Count (LPC) Interface

1.11 Reference Documents

1.11.1 Intel Reference Documents

Document	Document Number / Location
Intel® Atom™ Processor Z2760 Specification Update	Refer Note

Note: Contact your Intel representative for the latest revision and document number of this document.

1.12 External / Industry Standard Reference Documents

Table 1-2. External / Industry Standard Reference Documents

Reference	Location
LPDDR2 Draft Specification (as of 11/30/2008)	
MIPI DPHY revision 1.00 May 2009	
MIPI DSI revision 1.01.00 February 2008	
MIPI DCS revision 1.01.00 June 2006	
MIPI CSI-2 1.01 April 2009	
UTMI+ Low Pin Interface (ULPI) Specification, Revision 1.1	http://www.ulpi.org/ULPI_v1_1.zip
SD Specifications Part A2 SD Controller Simplified Specification - v2.00	http://www.sdcard.org/developers/tech/host_controller/simple_spec/Simplified_SD_Host_Controller_Spec.pdf
Secure Digital I/O (SDIO) Simplified v2.0	
Embedded MultiMedia Card - JESD84-A441 eMMC*/MMCA 4.41Specification	
Inter-IC Sound, or Integrated Interchip Sound (I^2S)	
Inter-Integrated Circuit (I^2C) v3.0	
Universal Asynchronous Receiver/Transmitter (UART 16550 compliant)	
High-bandwidth Digital Content Protection (HDCP) Revision 1.3	
Intel® Low Pin Count (LPC) Interface specification Revision 1.1	http://www.intel.com/design/chipsets/industry/lpc.htm

1.13 Acronyms and Terminology

The following is a list of important acronyms and terminology used in this document.

Acronym	Description
AOAC	Always On Always Connected
BL	Burst Length
CL	CAS Latency
Core	The silicon that contains one or more logical processors (with or without Intel® Hyper-Threading Technology (Intel® HT Technology).
Core Logic	Platform logic delivered by Intel, most notably the processor and I/O complexes, but may also include things like integrated wired or wireless networking devices, and so on. Each domain (for example, die, or package) includes one or more PMUs, where each of these PMUs communicate which one another to coordinate and align platform—level activity, state transitions, and so on.
CPU	Central Processing Unit
DDR	Double Data Rate
DFT	Design for Testability
DLL	Delay-Locked Loop
DM	Data Mask
DRAM	Dynamic Random Access Memory
DSR	Deep Self Refresh
External	Element residing outside of Atom™ Processor Z2760's core logic, for example the PMIC.
Fabric	An internal cross-bar or partial cross-bar which allows Masters or Initiators to communicate with Slave or Targets.
FIFO	First-In-First-Out
FSM	Finite State-Machine
Gb	Giga-bit
GB	Giga-Byte
GMCH	Graphics and Memory Controller Hub
GPIO	General Purpose Input Output
I^2S	Inter-Integrated Sound Protocol
Intel® Hyper-Threading Technology (Intel® HT Technology)	Intel® Hyper-Threading Technology (Intel® HT Technology) enables two logical processors for a single physical processor.
Intel® SIT	Intel® Smart Idle Technology (Intel® SIT): Enables the CPU core and the rest of the SoC to switch off while the operating system remains in the "ON" state (S0). The technique takes full advantage of clock and distributed power gating across many SoC power islands.
Intel® SPT	Intel® Smart Power Technology (Intel® SPT): Provides a complete hardware and software infrastructure that enables the next generation OS/software managed, usage model based policy driven power management architecture. The fine grained technique aggressively manages the idle and active power states on the platform by driving the CPU to optimal low power "C" and "P" states and the individual platform components to turn off based on the usage model.

Acronym	Description
Intel® Thermal Monitor	Intel® Thermal Monitor is a feature of the processor. The thermal monitor contains the Thermal Control Circuit (TCC). When the Intel® Thermal Monitor is enabled and active due to the die temperature reaching the pre-determined activation temperature, the TCC attempts to cool the processor by stopping the processor clocks for a period of time and then allowing them to run full speed for a period of time (duty cycle ~30–50%) until the processor temperature drops below the activation temperature.
Interconnect	A physical communication path between one or more internal and/or external elements, such as, USB, and so forth.
JTAG	Joint Test Action Group
Link	Interconnect between an internal subsystem and external device.
LPM	Link Power Management.
MIPI	Mobile Industry Processor Interface
MIPI-CSI	Camera Serial Interface. A serial interface between a digital camera module an application processor.
MIPI-DSI	Display Serial Interface. A serial interface between a display module and an application processor.
MIPI-HSI	High-Speed Synchronous Serial Interface. A serial interface between an communications modem and an application processor.
MT/s	Mega-Transfers per Second
ODT	On-Die Termination
OS	Operating System
OSPM	OS-{Directed, Guided} Power Management
PCM	Pulse Code Modulation
Platform PM	Platform Power Management Generally refers to mid-grain capabilities and policies that hierarchically reside below OSPM (coarse-grain) and above Subsystem or Device PM (fine-grain).
PLL	Phase-Locked Loop
PMIC	Power Management Integrated Circuit For the platform based around Atom™ Processor Z2760, Avondale Cove will be the PMIC of choice and will control the regulation of voltages to Atom™ Processor Z2760 and other platform parts.
PMU	Power Management Unit Generally refers to a functional unit within our core logic responsible for platform-level coordination and control as defined by this specification. May consist of a dedicated or shared microcontroller, multiple microcontrollers, or even discrete gates. Also known as the Power Manager.
Processor	The Intel® Atom™ Processor Z2760. Within this document the term is used interchangeably with “SoC”
Port	An independent point of connection between an external device and internal host controller.
PVT	Process, Voltage and Temperature
Secure Boot	Method by which boot module store in non-volatile memory, is measured and authenticated before it is allowed to execute.
SoC	System on a Chip. Within this document the term is used interchangeably with “processor”.

Acronym	Description
Socket	A standard internal interface used to communicate between a logic cluster and the fabric. Standard interfaces for Atom™ Processor Z2760 include OCP, AHB, AXI, and APB.
SODIMM	Small Outline Dual In-line Memory Module
SR	Self Refresh
SSR	Shallow Self Refresh
Subsystem	A cluster of logic within Atom™ Processor Z2760 that performs a particular architectural feature and is independently power-managed from the perspective of Platform PM.
SVID	Serial Voltage Identification (SVID) is a binary pattern output from the processor that tells the voltage regulator—the voltage required to operate the processor.
TCC	The Thermal Control Circuit (TCC) is a feature of the processor that is used to cool the processor should the processor temperature exceed a predetermined temperature.
ULPI	UTMI+ Low Pin Interface
USB	Universal Serial Bus
VID	Voltage Identification (VID) is a binary pattern output from the processor that tells the voltage regulator—the voltage required to operate the processor.

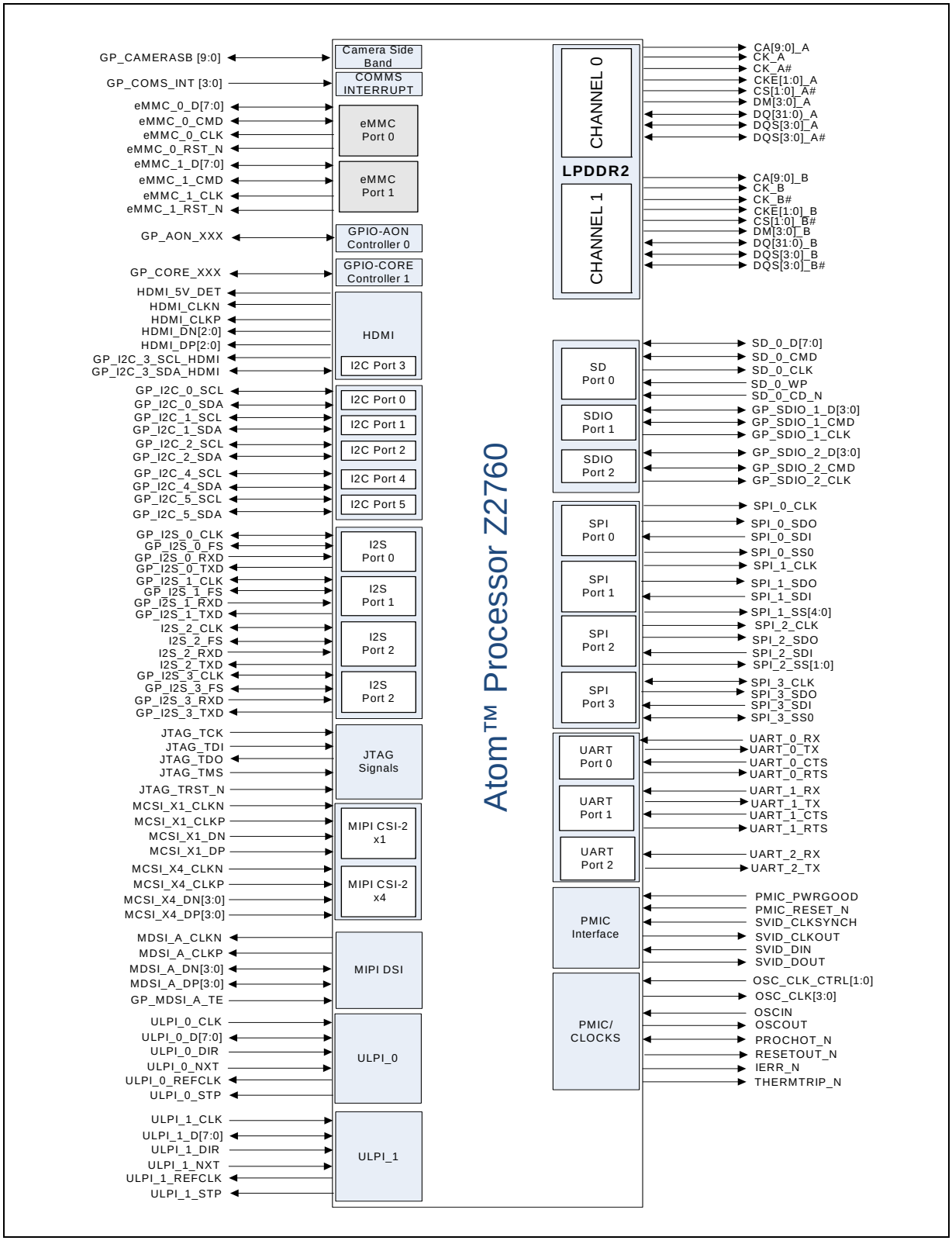
§

2 Signal Descriptions

2.1 Functional Signal Block Diagram

The signal block diagram for the SoC is shown in Figure 2-1.

Figure 2-1. Functional Signal Block Diagram



2.2 Buffer Types and Descriptions

Table 2-3. I/O Buffer Description

Buffer Type	Interface(s)	Description
ANALOG	ALL	Analog reference or output: This may be used as a threshold voltage or for buffer compensation.
LPDDR2	LPDDR2	CMOS Driver/Receiver for LPDDR2 signaling
VREF	LPDDR2	Vref to the DRAM
MIPI-DPHY	MIPI CSI-2 and MIPI DSI	Input/Output buffer compliant to MIPI DPHY Specification Revision 0.90, supporting HSTX, HSRX, LPTX, and LPRX modes.
HDMI	HDMI	TMDS differential output, compliant to HDMI specification, Revision 1.3a.
GPIOMV	GPIOs, COMS_INT, Camera SB, SDIO (Port 1 and 2), I^2C, I^2S, JTAG, Keyboard, SPI, UART, PTI, PMIC, HSI, and USB ULPI	1.2V and 1.8 V-tolerant General Purpose Input/Output buffer with programmable drive strength and pull-up resistors.
GPIOHV	SD (Port 0)	3.0V-tolerant General Purpose Input/Output buffer with programmable drive strength and integrated pull-up resistors.
MMC	eMMC*	CMOS driver/receiver for eMMC signaling
CLK	OSC_Clock Output	Oscillator output

2.3 Clock Interface

Table 2-4. Clock Interface Signals

Name	Dir.	Buffer Type	Nominal Voltage	System Rail Name	Signal Description
OSCIN	I	NA	1.08	VCC108AON	**Oscillator Input:** Provides input to Pierce oscillator from 38.4 MHz crystal.
OSCOUT	O	NA	1.08	VCC108AON	**Oscillator Output:** Output of Pierce oscillator.
OSC_CLK[3:0]	O	GPIOMV	1.80	VCC180AON	**OSC Clock Output**
OSC_CLK_CTRL[1:0]	I	GPIOMV	1.80	VCC180AON	**OSC Clock Output:** Control for OSC_CLK1 and OSC_CLK0 respectively

2.4 Memory Interfaces

2.4.1 LPDDR2 Interface (Pads on Top of Package)

Table 2-5. LPDDR2 Interface Signals on Top Side (Pads) (Sheet 1 of 2)

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
DQ[31:0]_A/ DQ[31:0]_B	I/O	LPDDR2	1.25V	VCC122AON	**Data lines:** DQ signal interface to the DRAM data bus.
DQS[3:0]_A/ DQS[3:0]_B	I/O	LPDDR2	1.25V	VCC122AON	**Data Strobes:** To latch data signals. During writes, these signals are driven by memory controller. Offset to be centered in the data phase. During reads, these signals are driven by memory devices, edge aligned with data. One bit per data byte lane -DQS0 corresponds to DQ[7:0] -DQS1 corresponds to DQ[15:8] -DQS2 corresponds to DQ[23:16] -DQS3 corresponds to DQ[31:24]
DQS[3:0]_A#/ DQS[3:0]_B#	I/O	LPDDR2	1.25V	VCC122AON	**Complimentary Data Strobe**
CA[9:0]_A / CA[9:0]_B	O	LPDDR2	1.25V	VCC122AON	**Command Address Bus:** These signals are used to define the command and address being accessed for the memory.
CKE[1:0]_A / CKE[1:0]_B	O	LPDDR2	1.25V	VCC122AON	**Clock Enable:** CKE is used for power control of the DRAM devices. There is one CKE per Rank.
CK_A/CK_B	O	LPDDR2	1.25V	VCC122AON	**Differential DDR Clock:** The crossing of CK and CK_N is used to sample the memory address and control signals.
CK_A#/ CK_B#	O	LPDDR2	1.25V	VCC122AON	**Complimentary Differential Clock**
CS[1:0]_A#/ CS[1:0]_B#	O	LPDDR2	1.25V	VCC122AON	**Chip Select:** These signals determine whether a command is valid in a given cycle for the devices connected to it. There is one chip select signal for each Rank.
DM[3:0]_A/ DM[3:0]_B	O	LPDDR2	1.25V	VCC122AON	**Data Mask:** One bit per byte indicating which bytes should be written.

Table 2-5. LPDDR2 Interface Signals on Top Side (Pads) (Sheet 2 of 2)

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
VREFDQ_A / VREFDQ_B	O	VREF	N/A	VCC122AON	**VREFDQ:** is reference for DQ input buffers.
VREFCA_A / VREFCA_B	O	VREF	N/A	VCC122AON	**VREFCA:** is reference for command/address input buffers.
ZQ_A /ZQ_B	I	ANALOG	N/A	N/A	**DRAM Driver Calibration:** This signal is used by DDR to calibrate its drivers output impedance.
VDD1	O	POWER	1.8 V	VCC180AON	**LPDDR2 core power 1:** nominal 1.8 V
VDD2	O	POWER	1.25/ 1.35 V	VCC122AON/ 1.35V Rail	**LPDDR2 core power 2:** nominal 1.35V or 1.25V
VSS	N/A	POWER	N/A	VSS	**Ground:** Shared between the DDR2 PoP pad, ground to board and SoC die.

NOTE: The pads for the signals in the above table are located on the top of the SoC package.

2.4.2 LPDDR2 Interface (Pins on Bottom of Package)

Table 2-6. LPDDR2 Interface Signals on Bottom Side (Pins)

Name	Dir.	Buffer Type	Nominal Voltage (V)	System Rail Name	Signal Description
M_RCOMP0	I	LPDDR2	NA	NA	**System Memory Impedance Compensation:** This signal requires a 49.9 Ω ±1% resistor to ground
M_RCOMP1	I	LPDDR2	NA	NA	**System Memory Impedance Compensation:** This signal requires a 1 KΩ ±5% resistor to VCC120AON rail
M_RCOMP2	I	LPDDR2	NA	NA	**System Memory Impedance Compensation:** This signal requires a 1 KΩ ±5% resistor to ground
ZQ_A	I	ANALOG	NA	NA	**DRAM Driver Calibration:** This signal requires a 240 Ω ±1% resistor to ground.
ZQ_B	I	ANALOG	NA	NA	**DRAM Driver Calibration:** This signal requires a 240 Ω ±1% resistor to ground.
VDD1	I	POWER	1.80	VCC180AON	**LPDDR2 core power 1:** nominal 1.8 V.
VDD2	I	POWER	1.25	VCC122AON	**LPDDR2 core power 2:** nominal 1.25V.

2.5 Display Interface

Intel® Atom™ Processor Z2760 supports 2 display interfaces, which include 1 HDMI port and 1 MIPI DSI port.

2.5.1 HDMI 1.3a Interface

Table 2-7. HDMI 1.3a Interface Signals

Name	Dir.	Buffer Type	Nominal Voltage (V)	Connects to System Rail	Signal Description
HDMI_DP[2:0] / HDMI_DN[2:0]	O	HDMI	3.30 V	VCC330	**HDMI_DP/DN:** TMDS data differential pairs
HDMI_CLKP/ HDMI_CLKN	O	HDMI	3.30 V	VCC330	**HDMI _CLKP/CLKN:** TMDS clk differential pair
HDMI_EXTR	I/O	ANALOG	3.30 V	NA	**Bias Resistor:** This signal generates bias current. An external precision resistor of 2.49 KΩ ±1% should be connected from this pin to ground.
RSVD	I/O	ANALOG	3.30 V	NA	**RSVD (Ball G3)**: An external precision resistor of 1 MΩ must be connected from this pin to VCC180AON.
HDMI_5V_DET	O	HDMI	1.25 V	VCC122AON	**HDMI 5V Detect: Processor asserts this pin when it detects voltage above 3.3V on any of the TMDS bus.**
GP_I2C_3_SCL_HDMI	I/O	GPIOMV	1.25 V	VCC122AON	**Display I^2C Serial Clock** to support DDC
GP_I2C_3_SDA_HDMI	I/O	GPIOMV	1.25 V	VCC122AON	**Display I^2C Serial Data** to support DDC

2.5.2 MIPI DSI Port A—4 Lanes

Table 2-8. MIPI DSI Port A—4 Lanes Interface Signals (Sheet 1 of 2)

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
MDSI_A_CLKP	O	DPHY	1.25 V	VCC122AON	**MDSI_CLKP:** MIPI DSI Clock out_p
MDSI_A_CLKN	O	DPHY	1.25 V	VCC122AON	**MDSI_CLKN:** MIPI DSI Clock out_n
MDSI_A_DP[3:0]	I/O	DPHY	1.25 V	VCC122AON	**MDSI_A_DP:** MIPI DataP Lanes

Table 2-8. MIPI DSI Port A—4 Lanes Interface Signals (Sheet 2 of 2)

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
MDSI_A_DN[3:0]	I/O	DPHY	1.25 V	VCC122AON	**MDSI_A_DN:** MIPI DataN Lanes
GP_MDSI_A_TE	I	GPIOMV	1.80 V	VCC180AON	**MDSI_A_TE:** Tearing Effect Signal from x4 PipeA display
MDSI_COMP	I/O	ANALOG	NA	NA	**MDSI_COMP:** This is for pre-driver slew rate compensation for the MIPI DSI Interface. An external precision resistor of 150 Ω ±1% should be connected from this pin to ground.

2.6 Camera Interface

There are two MIPI CSI-2 interfaces on processor for use with external image sensors.

2.6.1 MIPI CSI-2 Interface—Four (x4) Lanes

Table 2-9. MIPI CSI-2 Interface—Four (4) Lanes Interface Signals

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
MCSI_X4_CLKP	I	DPHY	1.25 V	VCC122AON	**MCSI_X4_CLKP:** MIPI CSI input clock positive
MCSI_X4_CLKN	I	DPHY	1.25 V	VCC122AON	**MCSI_X4_CLKN:** MIPI CSI input clock negative
MCSI_X4_DP[3:0]	I	DPHY	1.25 V	VCC122AON	**MCSI_X4_DP:** MIPI CSI DataP
MCSI_X4_DN[3:0]	I	DPHY	1.25 V	VCC122AON	**MCSI_X4_DN:** MIPI CSI DataN
MCSI_COMP	I/O	ANALOG	NA	NA	**MCSI_COMP:** An external precision resistor of 150 Ω ±1% should be connected from this pin to ground.

2.6.2 MIPI CSI-2 Interface—One (x1) Lane

Table 2-10. MIPI CSI-2 Interface—One (1) Lane Interface Signals

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
MCSI_X1_DP	I	DPHY	1.25 V	VCC122AON	**MCSI_X1_DP:** MIPI CSI DataP Lane 0

Table 2-10.MIPI CSI-2 Interface—One (1) Lane Interface Signals

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
MCSI_X1_DN	I	DPHY	1.25 V	VCC122AON	**MCSI_X1_DN:** MIPI CSI DataN Lane 0
MCSI_X1_CLKP	I	DPHY	1.25 V	VCC122AON	**MCSI_X1_CLKP:** MIPI Clock Input positive
MCSI_X1_CLKN	I	DPHY	1.25 V	VCC122AON	**MCSI_X1_CLKN:** MIPI clock Input negative

Table 2-11.Camera Side Band Signals

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description (As used on iCDK)
GP_CAMERA_SB0	I/O	GPIOMV	1.80 V	VCC180AON	Xenon Charge: Active high control signal to Xenon Flash to start charging the Capacitor.
GP_CAMERA_SB1	I/O	GPIOMV	1.80 V	VCC180AON	Xenon Ready: Active low output from Xenon Flash to indicate that the capacitor is fully charged and is ready to be triggered.
GP_CAMERA_SB2	I/O	GPIOMV	1.80 V	VCC180AON	Flash Trigger: Active high control signal to trigger Xenon flash or LED flash.
GP_CAMERA_SB3	I/O	GPIOMV	1.80 V	VCC180AON	Pre-light Trigger: Asserted to light up a pilot lamp prior to firing the flash bulb.
GP_CAMERA_SB4	I/O	GPIOMV	1.80 V	VCC180AON	Reserved for future camera enabling.
GP_CAMERA_SB5	I/O	GPIOMV	1.80 V	VCC180AON	Reserved for future camera enabling.
GP_CAMERA_SB6	I/O	GPIOMV	1.80 V	VCC180AON	Reset PMU: Use for COMM GPIO to reset modem's PMU.
GP_CAMERA_SB7	I/O	GPIOMV	1.80 V	VCC180AON	Sensor strobe: Asserted to indicate the start of a full frame (in a single shot mode) or a flash exposed frame for flash synchronization.
GP_CAMERA_SB8	I/O	GPIOMV	1.80 V	VCC180AON	Sensor trigger: To control Sensor 1 standby power state.
GP_CAMERA_SB9	I/O	GPIOMV	1.80 V	VCC180AON	**Sensor 1 reset**: Active low output signal to reset.

NOTE: Signal Description for CAMERASB signals reflect the usage of the signals on the platform. If

any Camera Side Band functionality is required, CAMERASB signals should be preferred as these pins are directly connected to ISP block within the processor when programmed for ALT FUNC 1.

2.7 I²C Interface

The processor has 6 I²C ports, labelled I2C_0 to I2C_5.

Table 2-12.I²C Interface

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
GP_I2C_[2:0]_SDA	I/O	GPIOMV	1.25 V/ 1.80 V	VCC122_180AON	**I²C Data:** For I²C Port 0, 1, 2
GP_I2C_[2:0]_SCL	I/O	GPIOMV	1.25 V/ 1.80 V	VCC122_180AON	**I²C Clock:** For I²C Port 0, 1, 2
GP_I2C_[5:4]_SDA	I/O	GPIOMV	1.80 V	VCC180AON	**I²C Data:** For I²C Port 4 and 5
GP_I2C_[5:4]_SCL	I/O	GPIOMV	1.80 V	VCC180AON	**I²C Clock:** For I²C Port 4 and 5

NOTE: I2C_3 is dedicated for HDMI interface, described in the HDMI signal table.

2.8 USB ULPI Interfaces

The processor includes two USB controllers.

Table 2-13.USB ULPI Interfaces Signals (Sheet 1 of 2)

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
ULPI0					
ULPI_0_CLK	I	GPIOMV	1.80 V	VCC180AON	**ULPI_0_CLK:** ULPI interface clock fromPHY(60 MHz)
ULPI_0_DIR	I	GPIOMV	1.80 V	VCC180AON	**ULPI_0_DIR**: Direction—Controls the direction of the data bus
ULPI_0_NXT	I	GPIOMV	1.80 V	VCC180AON	**ULPI_0_NXT:** Next signal for PHY
ULPI_0_STP	O	GPIOMV	1.80 V	VCC180AON	**ULPI_0_STP:** Stop signal for PHY
ULPI_0_D[7:0]	I/O	GPIOMV	1.80 V	VCC180AON	**ULPI_0_D:** Bi-directional data bus
ULPI_0_REFCLK	O	GPIOMV	1.80 V	VCC180AON	**ULPI_0_REFCLK:** ULPI interface reference clock to PHY based on osc clock out (19.2 MHz).
ULPI1					

Table 2-13.USB ULPI Interfaces Signals (Sheet 2 of 2)

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
ULPI_1_CLK	I	GPIOMV	1.80 V	VCC180AON	**ULPI_1_CLK:** ULPI interface clock from PHY (60 MHz)
ULPI_1_DIR	I	GPIOMV	1.80 V	VCC180AON	**ULPI_1_DIR**: Direction—Controls the direction of the data bus
ULPI_1_NXT	I	GPIOMV	1.80 V	VCC180AON	**ULPI_1_NXT:** Next signal for PHY
ULPI_1_STP	O	GPIOMV	1.80 V	VCC180AON	**ULPI_1_STP:** Stop signal for PHY
ULPI_1_D[7:0]	I/O	GPIOMV	1.80 V	VCC180AON	**ULPI_1_D:** Bi-directional data bus
ULPI_1_REFCLK	O	GPIOMV	1.80 V	VCC180AON	**ULPI_1_REFCLK:** ULPI interface reference clock to PHY based on osc clock out (19.2 MHz).

2.9 Audio Interfaces

The processor has 4 I2S ports, used for Modem, BT and discrete CODEC.

Table 2-14.I^{2}S Audio Interface Signals (Sheet 1 of 2)

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
GP_I2S_0_CLK	I/O	GPIOMV	1.80 V	VCC180AON	**I2S Clock:** Can be configured either as an input or an output.
GP_I2S_0_FS	I/O	GPIOMV	1.80 V	VCC180AON	**I2S Frame Sync:** Can be configured either as an input or an output.
GP_I2S_0_TXD	O	GPIOMV	1.80 V	VCC180AON	**I2S Transmit Data:** Output data line is actively driven or tri-state.
GP_I2S_0_RXD	I	GPIOMV	1.80 V	VCC180AON	**I2S Receive Data:** Input data line.
GP_I2S_1_CLK	I/O	GPIOMV	1.80 V	VCC180AON	**I2S Clock:** Can be configured either as an input or an output.
GP_I2S_1_FS	I/O	GPIOMV	1.80 V	VCC180AON	**I2S Frame Sync:** Can be configured either as an input or an output.
GP_I2S_1_TXD	O	GPIOMV	1.80 V	VCC180AON	**I2S Transmit Data:** Output data line is actively driven or tri-state.
GP_I2S_1_RXD	I	GPIOMV	1.80 V	VCC180AON	**I2S Receive Data:** Input data line.

Table 2-14.I²S Audio Interface Signals (Sheet 2 of 2)

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
I2S_2_CLK	I/O	GPIOMV	1.25 V	VCC122AON	**I2S Clock:** Can be configured either as an input or an output. **Note:** This interface should be left unused.
I2S_2_FS	I/O	GPIOMV	1.25 V	VCC122AON	**I2S Frame Sync:** Can be configured either as an input or an output. **Note:** This interface should be left unused.
I2S_2_TXD	O	GPIOMV	1.25	VCC122AON	**I2S Transmit Data:** Output data line is actively driven or tri-stated. **Note:** This interface should be left unused.
I2S_2_RXD	I	GPIOMV	1.25	VCC122AON	**I2S Receive Data:** Input data line. **Note:** This interface should be left unused.
GP_I2S_3_CLK	I/O	GPIOMV	1.80 V	VCC180AON	**I2S Clock:** Can be configured either as an input or an output.
GP_I2S_3_FS	I/O	GPIOMV	1.80 V	VCC180AON	**I2S Frame Sync:** Can be configured either as an input or an output.
GP_I2S_3_TXD	O	GPIOMV	1.80 V	VCC180AON	**I2S Transmit Data:** Output data line is actively driven or tri-state.
GP_I2S_3_RXD	I	GPIOMV	1.80 V	VCC180AON	**I2S Receive Data:** Input data line.

2.10 3G MODEM and Complimentary Wireless Solution (CWS) Interfaces

2.10.1 COMMs Interrupts

Table 2-15.COMMs Interrupts Signal

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
GP_COMS_INT[3:0]	I	GPIOMV	1.80 V	VCC180AON	**COMMs Interrupt Pins:** COMS_INT Pins when configured as ALT FUNC[1], directly connect to the SCU Interrupt Controller to reduce interrupt latency. COMS_INT in ALT FUNC[1] are **Active High Interrupts**. Edge Sensitive and Active low interrupt are not supported on COMS_INT[3..0] pins when configured as ALT FUNC[1] COMS_INT pins when configured as ALT_FUNC[0] act as regular GPIO_AON_XXX signals.

NOTE: CWS (Complimentary Wireless Solution) refers to wireless interface for Wi-Fi, BT (Bluetooth*), FM, GPS, NFC (Near Field Communication), Mobile-TV, and so forth. COMS_INT signals are directly connected to the wake logic therefore are lower latency then other GPIO_AON signals.

2.11 SDIO Interface

2.11.1 Signals on SDIO Ports 1 and 2

Table 2-16.SDIO Port 1 and 2 Signals

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
GP_SDIO_1_D[3:0]/ GP_SDIO_2_D[3:0]	I/O	GPIOMV	1.80 V	VCC180AON	**SDIO_D:** SDIO Port Data bus.
GP_SDIO_1_CMD/ GP_SDIO_2_CMD	I/O	GPIOMV	1.80 V	VCC180AON	**SDIO_CMD:** This signal is used for card initialization and transfer of commands.
GP_SDIO_1_CLK / GP_SDIO_2_CLK	O	GPIOMV	1.80 V	VCC180AON	**SDIO_CLK:** SDIO Port Clock
GP_SDIO_1_PWR GP_SDIO_2_PWR	O	GPIOMV	1.80 V	VCC180AON	**SDIO_PWR:** Control power on SDIO controller.

2.12 SPI Interface

The processor has 4 SPI ports with SPI0 accessible only to System Controller Unit. SPI0 supports master mode only.

SPI ports SPI_1, SPI_2, and SPI_3 are not intended for use as SPI ports, but can be used as GPIO.

2.12.1 SPI Ports 0/1/2/3

Table 2-17.SPI_0/1/2/3—SPI Port (Sheet 1 of 2)

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
GP_SPI_0_SS0	O	GPIOMV	1.25 V	VCC122AON	**SPI_0_SS:** SPI Slave Select for Port 0
GP_SPI_0_SDO	O	GPIOMV	1.25 V	VCC122AON	**SPI_0_SDO:** SPI Port 0 Serial Data Out
GP_SPI_0_SDI	I	GPIOMV	1.25 V	VCC122AON	**SPI_0_SDI:** SPI Port 0 Serial Data In
GP_SPI_0_CLK	O	GPIOMV	1.25 V	VCC122AON	**SPI_0_CLK:** SPI Port 0 Clock
GP_SPI_1_SS[4:0]	O	GPIOMV	1.25 V or 1.80 V	VCC122_180 AON	**SPI_1_SS:** SPI Slave Select for Port 1. **Note:** Interface should not be used as SPI.
GP_SPI_1_SDO	O	GPIOMV	1.25 V or 1.80 V	VCC122_180 AON	**SPI_1_SDO:** SPI Port 1 Serial Data Out. **Note:** Interface should not be used as SPI.
GP_SPI_1_SDI	I	GPIOMV	1.25 V or 1.80 V	VCC122_180 AON	**SPI_1_SDI:** SPI Port 1 Serial Data In. **Note:** Interface should not be used as SPI.
GP_SPI_1_CLK	O	GPIOMV	1.25 V or 1.80 V	VCC122_180 AON	**SPI_1_CLK:** SPI Port 1 Clock. **Note:** Interface should not be used as SPI.
GP_SPI_2_SS[1:0]	O	GPIOMV	1.80 V	VCC180AON	**SPI_2_SS:** SPI 2 Slave Select. **Note:** Interface should not be used as SPI.
GP_SPI_2_SDO	O	GPIOMV	1.80 V	VCC180AON	**SPI 2 SDO:** SPI Port 2 Serial Data Out. **Note:** Interface should not be used as SPI.
GP_SPI_2_SDI	I	GPIOMV	1.80 V	VCC180AON	**SPI 2 SDI:** SPI Port 2 Serial Data In. **Note:** Interface should not be used as SPI.

Table 2-17.SPI_0/1/2/3—SPI Port (Sheet 2 of 2)

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
GP_SPI_2_CLK	O	GPIOMV	1.80 V	VCC180AON	**SPI 2 CLK:** SPI Port 2 Clock. **Note:** Interface should not be used as SPI.
GP_SPI_3_SS0	O	GPIOMV	1.80 V	VCC180AON	**SPI_3_SS:** SPI 3 Slave Select. **Note:** Interface should not be used as SPI.
GP_SPI_3_SDO	O	GPIOMV	1.80 V	VCC180AON	**SPI 3 SDO:** SPI Port 3 Serial Data Out – defaults to output. **Note:** Interface should not be used as SPI.
GP_SPI_3_SDI	I	GPIOMV	1.80 V	VCC180AON	**SPI 3 SDI:** SPI Port 3 Serial Data In – defaults to input. **Note:** Interface should not be used as SPI.
GP_SPI_3_CLK	I/O	GPIOMV	1.80 V	VCC180AON	**SPI 3 Clock:** SPI Port 3 Clock. **Note:** Interface should not be used as SPI.

2.13 UART Interface

Table 2-18.UART COMMs Signals (Sheet 1 of 2)

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
UART Port 0					
GP_UART_0_RX	I	GPIOMV	1.80 V	VCC180AON	**UART_0_RX:** UART Port 0 Data Receive
GP_UART_0_TX	O	GPIOMV	1.80 V	VCC180AON	**UART_0_TX:** UART Port 0 Data Transmit
GP_UART_0_CTS	I	GPIOMV	1.80 V	VCC180AON	**UART_0_CTS:** UART port 0 Clear to Send
GP_UART_0_RTS	O	GPIOMV	1.80 V	VCC180AON	**UART_0_RTS:** UART port 0 Request to Send
UART Port 1					
GP_UART_1_RX	I	GPIOMV	1.80 V	VCC180AON	**UART_1_RX:** UART Port 1Data Receive
GP_UART_1_TX	O	GPIOMV	1.80 V	VCC180AON	**UART_1_TX**: UART Port 1 Data Transmit
GP_UART_1_CTS	I	GPIOMV	1.80 V	VCC180AON	**UART_1_CTS:** UART port 1 Clear to Send

Table 2-18.UART COMMs Signals (Sheet 2 of 2)

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
GP_UART_1_RTS	O	GPIOMV	1.80 V	VCC180AON	**UART_1_RTS:** UART port 1 Request to Send
UART Port 2					
GP_UART_2_RX	I	GPIOMV	1.80 V	VCC180AON	**UART_2_RX:** UART Port 2 Data Receive
GP_UART_2_TX	O	GPIOMV	1.80 V	VCC180AON	**UART_2_TX:** UART Port 2 Data Transmit

2.14 LPC Interface

Table 2-19.LPC Interface Signals

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
GP_LPC_AD[0:3]	I/O	GPIOMV	1.80 V	VCC180AON	**LPC_AD[0:3]:** LPC Multiplexed Command, Address, Data.
GP_LPC_CLKOUT	O	GPIOMV	1.80 V	VCC180AON	**LPC_CLKOUT:** Clocks driven by the CLV to LPC devices.
GP_LPC_CLKRUN	I/O	GPIOMV	1.80 V	VCC180AON	**LPC_CLKRUN:** interface for clock run protocol for disabling the clock
GP_LPC_FRAME#	O	GPIOMV	1.80 V	VCC180AON	**LPC_FRAME#:** Indicates start of LPC cycle, or an abort.
GP_LPC_RESET#	O	GPIOMV	1.80 V	VCC180AON	**LPC_RESET#:** LPC Bus Reset

2.15 GPIO Interfaces

Table 2-20.GPIO Interface Signals (Sheet 1 of 6)

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Ball	GPIO Function
AON GPIO Interface Signals						
GP_COMS_INT0	I	GPIOMV	1.80 V	VCC180AON	H36	GP_AON_000
GP_COMS_INT1	I	GPIOMV	1.80 V	VCC180AON	G31	GP_AON_001
GP_COMS_INT2	I	GPIOMV	1.80 V	VCC180AON	H32	GP_AON_002
GP_COMS_INT3	I	GPIOMV	1.80 V	VCC180AON	G33	GP_AON_003
GP_I2S_0_CLK	I/O	GPIOMV	1.80 V	VCC180AON	D32	GP_AON_004
GP_I2S_0_FS	I/O	GPIOMV	1.80 V	VCC180AON	D28	GP_AON_005
GP_I2S_0_TXD	O	GPIOMV	1.80 V	VCC180AON	C33	GP_AON_006
GP_I2S_0_RXD	I	GPIOMV	1.80 V	VCC180AON	B32	GP_AON_007
GP_I2S_1_CLK	I/O	GPIOMV	1.80 V	VCC180AON	E29	GP_AON_008

Table 2-20.GPIO Interface Signals (Sheet 2 of 6)

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Ball	GPIO Function
GP_I2S_1_FS	I/O	GPIOMV	1.80 V	VCC180AON	F30	GP_AON_009
GP_I2S_1_TXD	O	GPIOMV	1.80 V	VCC180AON	E31	GP_AON_010
GP_I2S_1_RXD	I	GPIOMV	1.80 V	VCC180AON	B28	GP_AON_011
GP_I2S_3_CLK	I/O	GPIOMV	1.8 V	VCC180AON	D30	GP_AON_012
GP_I2S_3_FS	I/O	GPIOMV	1.8 V	VCC180AON	B30	GP_AON_013
GP_SPI_1_SS0	O	GPIOMV	1.25 V or 1.8 V	VCC122_180AON	AN29	GP_AON_016
GP_SPI_1_SS1	O	GPIOMV	1.25 V or 1.8 V	VCC122_180AON	AT30	GP_AON_017
GP_SPI_1_SS2	O	GPIOMV	1.25 V or 1.8 V	VCC122_180AON	AP28	GP_AON_018
GP_SPI_1_SS3	O	GPIOMV	1.25 V or 1.8 V	VCC122_180AON	AV30	GP_AON_019
GP_SPI_1_SS4	O	GPIOMV	1.25 V or 1.8 V	VCC122A_180AON	AR29	GP_AON_020
GP_SPI_1_SDO	O	GPIOMV	1.25 V or 1.8 V	VCC122_180AON	AR27	GP_AON_021
GP_SPI_1_SDI	I	GPIOMV	1.25 V or 1.8 V	VCC122_180AON	AM28	GP_AON_022
GP_SPI_1_CLK	O	GPIOMV	1.25 V or 1.8 V	VCC122_180AON	AV28	GP_AON_023
GP_I2C_0_SDA	I/O	GPIOMV	1.25 V or 1.8 V	VCC122_180AON	AN27	GP_AON_024
GP_I2C_0_SCL	I/O	GPIOMV	1.25 V or 1.8 V	VCC122_180AON	AT28	GP_AON_025
GP_I2C_1_SDA	I/O	GPIOMV	1.25 V or 1.8 V	VCC122_180AON	AT26	GP_AON_026
GP_I2C_1_SCL	I/O	GPIOMV	1.25 V or 1.8 V	VCC122_180AON	AU27	GP_AON_027
GP_I2C_2_SDA	I/O	GPIOMV	1.25 V or 1.8 V	VCC122_180AON	AV26	GP_AON_028
GP_I2C_2_SCL	I/O	GPIOMV	1.25 V or 1.8 V	VCC122_180AON	AM26	GP_AON_029
GP_XDP_C0_BPM0#	I/O	GPIOMV	1.80 V	VCC180AON	AK32	GP_AON_030
GP_XDP_C0_BPM1#	I/O	GPIOMV	1.80 V	VCC180AON	AK34	GP_AON_031
GP_XDP_C0_BPM2#	I/O	GPIOMV	1.80 V	VCC180AON	AJ35	GP_AON_032
GP_XDP_C0_BPM3#	I/O	GPIOMV	1.80 V	VCC180AON	AJ33	GP_AON_033
GP_XDP_C1_BPM0#	I/O	GPIOMV	1.80 V	VCC180AON	AJ37	GP_AON_034
GP_XDP_C1_BPM1#	I/O	GPIOMV	1.80 V	VCC180AON	AG33	GP_AON_035
GP_XDP_C1_BPM2#	I/O	GPIOMV	1.80 V	VCC180AON	AH32	GP_AON_036
GP_XDP_C1_BPM3#	I/O	GPIOMV	1.80 V	VCC180AON	AH38	GP_AON_037

Table 2-20.GPIO Interface Signals (Sheet 3 of 6)

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Ball	GPIO Function
GP_XDP_PREQ#	I	GPIOMV	1.80 V	VCC180AON	AH36	GP_AON_038
GP_XDP_PRDY#	O	GPIOMV	1.80 V	VCC180AON	AG35	GP_AON_039
GP_XDP_BLK_DP	O	GPIOMV	1.80 V	VCC180AON	AF32	GP_AON_040
GP_XDP_BLK_DN	O	GPIOMV	1.80 V	VCC180AON	AE37	GP_AON_041
GP_AON_042	I/O	GPIOMV	1.80 V	VCC180AON	AF38	GP_AON_042
GP_AON_043	I/O	GPIOMV	1.80 V	VCC180AON	AF36	GP_AON_043
GP_AON_044	I/O	GPIOMV	1.80 V	VCC180AON	AB32	GP_AON_044
GP_AON_045	I/O	GPIOMV	1.80 V	VCC180AON	AA33	GP_AON_045
GP_XDP_PWRMODE0	O	GPIOMV	1.80 V	VCC180AON	AE33	GP_AON_046
GP_XDP_PWRMODE1	O	GPIOMV	1.80 V	VCC180AON	AD36	GP_AON_047
GP_XDP_PWRMODE2	O	GPIOMV	1.80 V	VCC180AON	AA37	GP_AON_048
GP_AON_049	I/O	GPIOMV	1.80 V	VCC180AON	AE35	GP_AON_049
GP_SPI_3_SS0	O	GPIOMV	1.80 V	VCC180AON	J35	GP_AON_050
GP_AON_051	I/O	GPIOMV	1.80 V	VCC180AON	K32	GP_AON_051
GP_SPI_3_SDO	O	GPIOMV	1.80 V	VCC180AON	L33	GP_AON_052
GP_SPI_3_SDI	I	GPIOMV	1.80 V	VCC180AON	K38	GP_AON_053
GP_SPI_3_CLK	O	GPIOMV	1.80 V	VCC180AON	L35	GP_AON_054
GP_SPI_2_SS0	O	GPIOMV	1.80 V	VCC180AON	M32	GP_AON_055
GP_SPI_2_SS1	O	GPIOMV	1.80 V	VCC180AON	M36	GP_AON_056
GP_SPI_2_SDO	O	GPIOMV	1.80 V	VCC180AON	M38	GP_AON_057
GP_SPI_2_SDI	I	GPIOMV	1.80 V	VCC180AON	M34	GP_AON_058
GP_SPI_2_CLK	O	GPIOMV	1.80 V	VCC180AON	K34	GP_AON_059
GP_AON_060	I/O	GPIOMV	1.80 V	VCC180AON	F38	GP_AON_060
GP_AON_061	I/O	GPIOMV	1.80 V	VCC180AON	F36	GP_AON_061
GP_AON_062	I/O	GPIOMV	1.80 V	VCC180AON	C37	GP_AON_062
GP_AON_063	I/O	GPIOMV	1.80 V	VCC180AON	F34	GP_AON_063
GP_UART_1_RX	I	GPIOMV	1.80 V	VCC180AON	D36	GP_AON_064
GP_UART_1_TX	O	GPIOMV	1.80 V	VCC180AON	E35	GP_AON_065
GP_UART_1_RTS	I	GPIOMV	1.80 V	VCC180AON	E37	GP_AON_066
GP_UART_2_RX	O	GPIOMV	1.80 V	VCC180AON	E33	GP_AON_067
GP_UART_1_CTS	I	GPIOMV	1.80 V	VCC180AON	C35	GP_AON_068
GP_SD_0_CD#	I	GPIOMV	1.80 V	VCC180AON	AL5	GP_AON_069
GP_SDIO_1_D1	I/O	GPIOMV	1.80 V	VCC180AON	AM4	GP_AON_070
GP_SDIO_2_D1	I/O	GPIOMV	1.80 V	VCC180AON	AR3	GP_AON_071
GP_AON_072	I/O	GPIOMV	1.80 V	VCC180AON	J37	GP_AON_072
GP_UART_2_TX	O	GPIOMV	1.80 V	VCC180AON	J33	GP_AON_073

Table 2-20.GPIO Interface Signals (Sheet 4 of 6)

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Ball	GPIO Function
GP_I2S_3_TXD	O	GPIOMV	1.80 V	VCC180AON	K36	GP_AON_074
GP_I2S_3_RXD	I	GPIOMV	1.80 V	VCC180AON	H38	GP_AON_075
GP_AON_076	I/O	GPIOMV	1.80 V	VCC180AON	AP16	GP_AON_076
GP_AON_077	I/O	GPIOMV	1.80 V	VCC180AON	AR15	GP_AON_077
GP_AON_078	I/O	GPIOMV	1.80 V	VCC180AON	AV16	GP_AON_078
GP_AON_079	I/O	GPIOMV	1.80 V	VCC180AON	AT14	GP_AON_079
GP_SPI_0_SS0	O	GPIOMV	1.80 V	VCC180AON	T32	GP_AON_080
GP_SPI_0_SDO	O	GPIOMV	1.80 V	VCC180AON	T34	GP_AON_081
GP_SPI_0_SDI	I	GPIOMV	1.80 V	VCC180AON	U35	GP_AON_082
GP_SPI_0_CLK	O	GPIOMV	1.80 V	VCC180AON	T36	GP_AON_083
GP_LPC_FRAME#	O	GPIOMV	1.80 V	VCC180AON	AP36	GP_AON_084
GP_LPC_AD0	I/O	GPIOMV	1.80 V	VCC180AON	AN35	GP_AON_085
GP_LPC_AD1	I/O	GPIOMV	1.80 V	VCC180AON	AL35	GP_AON_086
GP_LPC_AD2	I/O	GPIOMV	1.80 V	VCC180AON	AT38	GP_AON_087
GP_LPC_AD3	I/O	GPIOMV	1.80 V	VCC180AON	AN37	GP_AON_088
GP_AON_089	I/O	GPIOMV	1.80 V	VCC180AON	AM32	GP_AON_089
GP_LPC_CLKRUN	I	GPIOMV	1.80 V	VCC180AON	AK36	GP_AON_090
GP_LPC_CLKOUT	O	GPIOMV	1.80 V	VCC180AON	AN33	GP_AON_091
GP_LPC_RESET#	O	GPIOMV	1.80 V	VCC180AON	AL33	GP_AON_092
GP_AON_093	I/O	GPIOMV	1.80 V	VCC180AON	AM34	GP_AON_093
GP_AON_094	I/O	GPIOMV	1.80 V	VCC180AON	AP38	GP_AON_094
Core GPIO Interface Signals						
GP_MDSI_A_TE	I	GPIOMV	1.80 V	VCC180AON	AB4	GP_CORE_006
GP_CORE_007	I/O	GPIOMV	1.80 V	VCC180AON	AD4	GP_CORE_007
GP_CORE_012	I/O	GPIOMV	1.80 V	VCC180AON	AM16	GP_CORE_012
GP_SD_0_PWR	O	GPIOMV	1.80 V	VCC180AON	AN17	GP_CORE_013
GP_SDIO_1_PWR	O	GPIOMV	1.80 V	VCC180AON	AR13	GP_CORE_014
GP_CORE_015	I/O	GPIOMV	1.80 V	VCC180AON	AT16	GP_CORE_015
GP_CORE_016	I/O	GPIOMV	1.80 V	VCC180AON	AP12	GP_CORE_016
GP_CORE_017	I/O	GPIOMV	1.80 V	VCC180AON	AN15	GP_CORE_017
GP_CORE_018	I/O	GPIOMV	1.80 V	VCC180AON	AV14	GP_CORE_018
GP_SDIO_2_PWR	O	GPIOMV	1.80 V	VCC180AON	AR11	GP_CORE_019
GP_CORE_020	I/O	GPIOMV	1.80 V	VCC180AON	AU15	GP_CORE_020
GP_eMMC_0_RST#	O	GPIOMV	1.80 V	VCC180AON	AV12	GP_CORE_021
GP_eMMC_1_RST#	O	GPIOMV	1.80 V	VCC180AON	AN13	GP_CORE_022

Table 2-20.GPIO Interface Signals (Sheet 5 of 6)

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Ball	GPIO Function
GP_UART_0_RX	I	GPIOMV	1.80 V	VCC180AON	AM14	GP_CORE_026
GP_UART_0_TX	O	GPIOMV	1.80 V	VCC180AON	AV8	GP_CORE_027
GP_UART_0_CTS	I	GPIOMV	1.80 V	VCC180AON	AN11	GP_CORE_028
GP_UART_0_RTS	O	GPIOMV	1.80 V	VCC180AON	AR9	GP_CORE_029
GP_CORE_030	I/O	GPIOMV	1.80 V	VCC180AON	AM12	GP_CORE_030
GP_CORE_031	I/O	GPIOMV	1.80 V	VCC180AON	AM10	GP_CORE_031
GP_CORE_032	I/O	GPIOMV	1.80 V	VCC180AON	AU11	GP_CORE_032
GP_CORE_033	I/O	GPIOMV	1.80 V	VCC180AON	AN9	GP_CORE_033
GP_I2C_3_SCL_HDMI	I/O	GPIOMV	1.25 V	VCC122AON	F8	GP_CORE_035
GP_I2C_3_SDA_HDMI	I/O	GPIOMV	1.25 V	VCC122AON	H4	GP_CORE_036
GP_HDMI_HPD	I	GPIOMV	1.25 V	VCC122AON	J7	GP_CORE_037
GP_I2C_4_SDA	I/O	GPIOMV	1.80 V	VCC180AON	AF4	GP_CORE_038
GP_I2C_4_SCL	I/O	GPIOMV	1.80 V	VCC180AON	AE5	GP_CORE_039
GP_I2C_5_SDA	I/O	GPIOMV	1.80 V	VCC180AON	AD2	GP_CORE_040
GP_I2C_5_SCL	I/O	GPIOMV	1.80 V	VCC180AON	AF6	GP_CORE_041
GP_SD_0_D0	I/O	GPIOMV	1.80 V or 2.85V	VCCSDIO	AJ5	GP_CORE_042
GP_SD_0_D1	I/O	GPIOMV	1.80 V or 2.85V	VCCSDIO	AJ7	GP_CORE_043
GP_SD_0_D2	I/O	GPIOMV	1.80 V or 2.85V	VCCSDIO	AG5	GP_CORE_044
GP_SD_0_D3	I/O	GPIOMV	1.80 V or 2.85V	VCCSDIO	AJ9	GP_CORE_045
GP_SD_0_D4	I/O	GPIOMV	1.80 V or 2.85V	VCCSDIO	AH8	GP_CORE_046
GP_SD_0_D5	I/O	GPIOMV	1.80 V or 2.85V	VCCSDIO	AH4	GP_CORE_047
GP_SD_0_D6	I/O	GPIOMV	1.80 V or 2.85V	VCCSDIO	AG9	GP_CORE_048
GP_SD_0_D7	I/O	GPIOMV	1.80 V or 2.85V	VCCSDIO	AG3	GP_CORE_049
GP_SD_0_CMD	I/O	GPIOMV	1.80 V or 2.85V	VCCSDIO	AK6	GP_CORE_050
GP_SD_0_CLK	O	GPIOMV	1.80 V or 2.85V	VCCSDIO	AK8	GP_CORE_051
GP_SD_0_WP	I	GPIOMV	1.80 V or 2.85V	VCCSDIO	AK4	GP_CORE_052
GP_SDIO_1_D0	I/O	GPIOMV	1.80 V	VCC180AON	AN7	GP_CORE_053
GP_SDIO_1_D2	I/O	GPIOMV	1.80 V	VCC180AON	AN5	GP_CORE_054
GP_SDIO_1_D3	I/O	GPIOMV	1.80 V	VCC180AON	AM8	GP_CORE_055

Table 2-20.GPIO Interface Signals (Sheet 6 of 6)

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Ball	GPIO Function
GP_SDIO_2_D0	I/O	GPIOMV	1.80 V	VCC180AON	AR5	GP_CORE_056
GP_SDIO_2_D2	I/O	GPIOMV	1.80 V	VCC180AON	AU3	GP_CORE_057
GP_SDIO_2_D3	I/O	GPIOMV	1.80 V	VCC180AON	AT2	GP_CORE_058
GP_SDIO_1_CMD	I/O	GPIOMV	1.80 V	VCC180AON	AP2	GP_CORE_059
GP_SDIO_1_CLK	O	GPIOMV	1.80 V	VCC180AON	AM2	GP_CORE_060
GP_SDIO_2_CMD	I/O	GPIOMV	1.80 V	VCC180AON	AP4	GP_CORE_061
GP_SDIO_2_CLK	O	GPIOMV	1.80 V	VCC180AON	AM6	GP_CORE_062
GP_CAMERA_SB0	I/O	GPIOMV	1.80 V	VCC180AON	AV6	GP_CORE_063
GP_CAMERA_SB1	I/O	GPIOMV	1.80 V	VCC180AON	AT10	GP_CORE_064
GP_CAMERA_SB2	I/O	GPIOMV	1.80 V	VCC180AON	AU7	GP_CORE_066
GP_CAMERA_SB3	I/O	GPIOMV	1.80 V	VCC180AON	AV4	GP_CORE_066
GP_FW_STRAP0	I	GPIOMV	1.80 V	VCC180AON	G19	GP_CORE_067
GP_KSEL_STRAP2	I	GPIOMV	1.80 V	VCC180AON	D12	GP_CORE_068
GP_KSEL_STRAP0	I	GPIOMV	1.80 V	VCC180AON	B12	GP_CORE_069
GP_FW_STRAP1	I	GPIOMV	1.80 V	VCC180AON	H16	GP_CORE_070
GP_KSEL_STRAP1	I	GPIOMV	1.80 V	VCC180AON	D10	GP_CORE_071
GP_FW_STRAP2	I	GPIOMV	1.80 V	VCC180AON	C17	GP_CORE_072
GP_CORE_073	I/O	GPIOMV	1.80 V	VCC180AON	K6	GP_CORE_073
GP_CORE_074	I/O	GPIOMV	1.80 V	VCC180AON	J5	GP_CORE_074
GP_CORE_075	I/O	GPIOMV	1.80 V	VCC180AON	J9	GP_CORE_075
GP_CAMERA_SB4	I/O	GPIOMV	1.80 V	VCC180AON	AD8	GP_CORE_076
GP_CAMERA_SB5	I/O	GPIOMV	1.80 V	VCC180AON	AC5	GP_CORE_077
GP_CAMERA_SB6	I/O	GPIOMV	1.80 V	VCC180AON	AB8	GP_CORE_078
GP_CAMERA_SB7	I/O	GPIOMV	1.80 V	VCC180AON	AB2	GP_CORE_079
GP_CAMERA_SB8	I/O	GPIOMV	1.80 V	VCC180AON	AB6	GP_CORE_080
GP_CAMERA_SB9	I/O	GPIOMV	1.80 V	VCC180AON	AC3	GP_CORE_081
GP_CORE_082	I/O	GPIOMV	1.80 V	VCC180AON	AE7	GP_CORE_082

NOTE: Table 2-21 provides the state of Signals—GP_KSEL_STRAP[0:2] and GP_FW_STRAP[0:2] during the Rising Edge of PMIC_PWRGOOD. These signals are multiplexed as Strap Signals on the rising edge of PMIC_PWRGOOD and put the processor into debug functionality.

NOTE: Make sure the state of these pins does not change during the Rising Edge of PMIC_PWRGOOD.

Table 2-21.State of Signals GP_KSEL_STRAP[0:2] and GP_FW_STRAP[0:2]

Pin Number	Pin Name	Rising Edge of PMIC _PWRGOOD	Strap Function	Strap Description
G19	GP_FW_STRAP0	L	FW_STRAP[0]	**RSVD**
H16	GP_FW_STRAP1	L	FW_STRAP[1]	**RSVD**
C17	GP_FW_STRAP2	L	FW_STRAP[2]	**RSVD**
B12	GP_KSEL_STRAP0	H	KSEL[0]	**RSVD**
D10	GP_KSEL_STRAP1	H	KSEL[1]	**RSVD** Need external pull-up
D12	GP_KSEL_STRAP2	L	KSEL[2]	**RSVD**

2.16 PMIC Interfaces

Table 2-22.PMIC Interface Signals

Name	Dir.	Buffer Type	Nominal Voltage (V)	Connects to System Rail	Signal Description
PMIC_PWRGOOD	I	GPIOMV	1.25	VCC122AON	**POWER GOOD:** PMIC asserts this signal to indicate that all power rails to SoC are good.
PMIC_RESET#	I	GPIOMV	1.25	VCC122AON	**Hard Reset:** Active low When asserted, SoC returns to its initial default state.
GP_SPI_0_SS0	O	GPIOMV	1.25	VCC122AON	**SPI 0 Slave Select**
GP_SPI_0_SDO	O	GPIOMV	1.25	VCC122AON	**SPI_0_SDO:** SPI Port 0 Serial Data Out – defaults to output.
GP_SPI_0_SDI	I	GPIOMV	1.25	VCC122AON	**SPI_0_SDI:** SPI Port 0 Serial Data In – defaults to input.
GP_SPI_0_CLK	O	GPIOMV	1.25	VCC122AON	**SPI_0_CLK:** SPI Port 0 Clock – defaults to output.
SVID_DIN	I	GPIOMV	1.25	VCC122AON	SVID_DIN: Serial VID Data In
SVID_CLKSYNCH	I	GPIOMV	1.25	VCC122AON	SVID_CLKSYNCH: Serial VID Clock Synch
SVID_DOUT	O	GPIOMV	1.25	VCC122AON	SVID_DOUT: Serial VID Data Out
SVID_CLKOUT	O	GPIOMV	1.25	VCC122AON	SVID_CLKOUT: Serial VID Clock Output
VCCSENSE VNNSENSE VSSSENSE	O	ANALOG	-	VCC VNN VSS	Voltage Sense Signals: Connects from SoC to PMIC—used by the Voltage Regulator (VR) to monitor the voltage at the SoC (these are feedback pins to the VR). Voltage Regulator must connect feedback lines for VCC, VNN and VSS to these pins on the package.

2.17 Miscellaneous Interface

Table 2-23.Miscellaneous Interface Signals

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
RSVD	NA	NA	NA	NA	**Reserved:** Pin reserved for future use.
IERR#	O	GPIOMV	1.80 V	VCC180AON	**IERR#: Active Low Signal:** This signal is an internal Error indication. Asserted when processor has an internal error and may have unexpectedly stopped execution.
RESETOUT#	O	GPIOMV	1.80 V	VCC180AON	**SCU Controlled Platform Reset:** Open drain.

2.18 Test and Debug Interfaces

2.18.1 JTAG Interface

Table 2-24.JTAG Interface Signals (Sheet 1 of 2)

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
JTAG_TCK	I	GPIOMV	1.80 V	VCC180AON	**JTAG Test Clock:** TCLK is a clock input to drive the Test Access Port (TAP) state machine during test and debug. This signal can be used in 2-pin mode to support cJTAG 1149.7
JTAG_TDI	I	GPIOMV	1.80 V	VCC180AON	**JTAG Test Data Input:** This signal receives serial test instruction and data of Test logic.
JTAG_TDO	O	GPIOMV	1.80 V	VCC180AON	**JTAG Test Data Output:** Serial output for test instruction and data from the test logic.
JTAG_TMS	I	GPIOMV	1.80 V	VCC180AON	**JTAG Test Mode Select:** Decoded by the TAP controller to control test operations. This signal can be used in 2-pin mode to support cJTAG 1149.7.

Table 2-24.JTAG Interface Signals (Sheet 2 of 2)

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
JTAG_TRST#	I	GPIOMV	1.80 V	VCC180AON	**JTAG Test Reset:** Asynchronous initialization of the TAP controller.
GP_XDP_C0_BPM[0:3]# GP_XDP_C1_BPM[0:3]#	I/O	GPIOMV	1.80 V	VCC180AON	**Breakpoint and Performance Monitor Signals:** These signals are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.
GP_XDP_PREQ#	I	GPIOMV	1.80 V	VCC180AON	**PREQ#** is used by debug tools to request debug operation of the processor.
GP_XDP_PRDY#	O	GPIOMV	1.80 V	VCC180AON	**PRDY#** is a processor output used by debug tools to determine processor debug readiness.
GP_XDP_BLK_DP GP_XDP_BLK_DN	O	GPIOMV	1.80 V	VCC180AON	**ITP clock:**
GP_XDP_PWRMODE [0:3]	O	GPIOMV	1.80 V	VCC180AON	**Power mode**:

2.19 Thermal Management Signals

Table 2-25.Thermal Management Signals

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
PROCHOT#	I/O	GPIOMV	1.80	VCC180AON	**Processor Hot:** **As an output,** PROCHOT# goes active when the SoC temperature monitoring sensor detects that the SoC has reached its maximum safe operating temperature. This indicates that the SoC Thermal Control Circuit (TCC) has been activated, if enabled. **As an input,** assertion of PROCHOT# by the system activates the TCC. TCC remains active until the system de-asserts PROCHOT#. Once TCC is enabled this will cause the SoC to Throttle to lower frequency and lower core voltage thus to reduce system temperature.
THERMTRIP#	O	GPIOMV	1.80	VCC180AON	**Catastrophic Thermal Trip:** The SoC protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The SoC stops all execution when the junction temperature has reached a potentially catastrophic temperature. This condition is signaled to the system by the THERMTRIP# pin.

2.20 Storage Interfaces

2.20.1 Secure Digital (SD) Port 0

Table 2-26.Secure Digital (SD)—Port 0 Signals

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
GP_SD_0_D[7:0]	I/O	GPIOHV	2.85V	VCCSDIO	**SD Port Data:** Bi-directional Data Bus for transfer of data to and from the SD/MMC Card.
GP_SD_0_CMD	I/O	GPIOHV	2.85V	VCCSDIO	**SD Port Command:** This signal is used for card initialization and transfer of commands.
GP_SD_0_CLK	O	GPIOHV	2.85V	VCCSDIO	**SD Port Clock:** SD Port Clock.
GP_SD_0_WP	I	GPIOHV	2.85V	VCCSDIO	**SD Port Write Protect:** Active High pin. When high the card does not accept writes.
GP_SD_0_CD#	I	GPIOMV	1.80 V	VCC180AON	**SD Port Card Detect:** Active low when a card is present. Floating (pulled high with internal PU) when a card is not present. Attached to the SD card connector. Supports Card Detection (Insertion/Removal) with dedicated card detection signal only.
GP_SD_0_PWR	O	GPIOMV	1.80 V	VCC180AON	**SD_PWR:** Power control for the SD card connector.
GPIO_RCOMP30	I/O	ANALOG	NA	NA	**GPIO Rcomp30**: This signal requires a 34.8 Ω ±1% resistor to ground.
GPIO_RCOMP18	I/O	ANALOG	NA	NA	**GPIO Rcomp18**: This signal requires a 51 Ω ±5% resistor to ground.

2.20.2 eMMC* Interface

Table 2-27.eMMC* Port 0 and Port 1 Signals

Name	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
EMMC_0_D[7:0] EMMC_1_D[7:0]	I/O	NAND	1.80 V	VCC180AON	**eMMC Port Data:** Bi-directional port used to transfer data to and from eMMC* device.
EMMC_0_CMD EMMC_1_CMD	I/O	NAND	1.80 V	VCC180AON	**eMMC Port Command**: This signal is used for card initialization and transfer of commands. It has two modes—open-drain for initialization, and push-pull for fast command transfer.
EMMC_0_CLK EMMC_1_CLK	I/O	NAND	1.80 V	VCC180AON	**eMMC Port Clock:** Driven by the processor. This signal is used to latch the command or data being sent to the device.
GP_EMMC_0_RST# GP_EMMC_1_RST#	O	NAND	1.80 V	VCC180AON	**eMMC Reset Signals**
EMMC_RCOMP	I	ANALOG	n/a	VCC180AON	**eMMC RCOMP**: This signal requires a 22 Ω ±5% resistor to ground.

2.21 HSI Interface

The MIPI HSI interface is not used on this device.

Table 2-28.MIPI HSI Interface Signals (Sheet 1 of 2)

Name	Pin#	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
MHSI_CAWAKE	C21	I	HSI	1.8 V	VCC180AON	Wake Signal from Cellular modem
MHSI_CADATA	D18	I	HSI	1.8 V	VCC180AON	Data signal from Cellular modem
MHSI_CAFLAG	D20	I	HSI	1.8 V	VCC180AON	Flag signal from Cellular modem
MHSI_CAREADY	E19	I	HSI	1.8 V	VCC180AON	Ready signal from Cellular modem
MHSI_ACWAKE	C21	O	HSI	1.8 V	VCC180AON	Wake to Cellular modem
MHSI_ACDATA	B20	O	HSI	1.8 V	VCC180AON	Data signal to Cellular modem

Table 2-28.MIPI HSI Interface Signals (Sheet 2 of 2)

Name	Pin#	Dir.	Buffer Type	Nominal Voltage	Connects to System Rail	Signal Description
MHSI_ACFLAG	F16	O	HSI	1.8 V	VCC180AON	Flag signal to Cellular modem
MHSI_ACREADY	G21	O	HSI	1.8 V	VCC180AON	Ready signal to Cellular modem
MHSI_RCOMP	B20	IO	ANALOG	NA	NA	This is for pre-driver slew rate compensation for the HSI Port. This signal requires a 49.9 Ω ±1% resistor to ground.

§

3 Functional Description

3.1 Memory Interface

3.1.1 Overview

The Memory Interface is a dual channel LPDDR2 interface. Each channel uses a single channel LPDDR2 memory controller. The single channel memory controller is instantiated two times in order to support a dual-channel architecture.

The data bus of each channel is 32 bits wide and it supports data rates of 800 MT/s, which can provide a maximum throughput of 3.2GB/s per channel. With dual-channel the data throughput doubles per speed grade.

Table 3-29 summarizes the key features of the Memory controller.

Table 3-29.Memory Interface Feature Set

Feature	Device Support
DRAM Technology	LPDDR2
DRAM CMD Bus Rate	Double pumped
DRAM Data Rate	800 (MT/s)
DRAM Speed Grade	800: 6-6-6, 6-8-8, 6-10-10
DRAM Device Data Width	x32
DRAM Device Density	1Gb, 2Gb or 4Gb
DRAM Burst Length	4 or 8
Burst Type	Sequential or Interleaved
Memory Channels	1 or 2
Data Width per Channel	32-bit
Peak Bandwidth	3.2 GB/s @ 800 MT/s (1 chan), 6.4 GB/s @ 800 MT/s (2 chans)
Ranks per Channel	1 or 2
Total Memory Size	512 MB or 1GB per channel. 1GB, or 2 GB with 2 channels.
Partial Write w/ Data Mask	Yes
Refresh	All-bank refresh, and temperature-dependent refresh intervals
Auto Refresh duty cycle	3.9us
Power Saving Features	• Power Down (PD) • Shallow/Deep SR • PASR support
PVT Compensation	Rcomp, Scomp, ZQ Calibration
I/O Voltage	1.2 V
Memory Packaging	Package on Package (POP) 220 ball, 0.5 mm pitch, 14 x 14 mm

3.1.2 Features

- Memory Controller Features
  - — LPDDR2 memory controller
  - — 32-bit data bus per channel
  - — Supports 800 MT/s rates
  - — Supports 1 or 2 ranks (same for single or dual channels)
    - —Memory Controller A controls channel A
    - —Memory Controller B controls channel B
  - — Supports total memory size of 1GB per channel, maximum of 2GB with dual channels
  - — Supports only x32 DRAM device
  - — Supports DRAM burst length 8 or 4
  - — Supports DRAM mode register read
  - — Supports single or dual channels
  - — Supports 1Gb, 2Gb, and 4Gb DRAM device densities
  - — Supports only LPDDR2-S4B DRAM device type
    - —PMIC directly supports VDD2=1.2v only
  - — Supports Data Masks for partial data write to memory
  - — Aggressive power management to reduce power consumption
  - — Proactive page closing policies to close unused pages
  - — Programmable delay for self refresh entry
  - — Tri-state CK/CK# during powered down

3.1.3 Memory Configurations

3.1.3.1 Supported DRAM Configuration

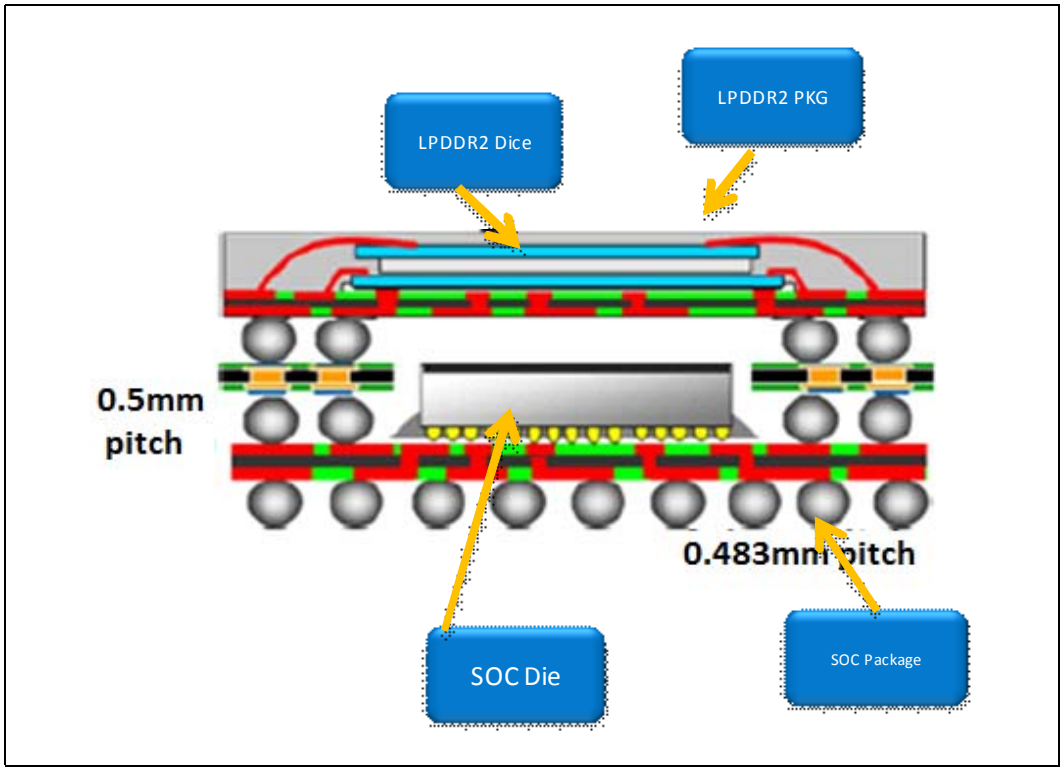
The Intel® Atom™ Processor Z2760 will only support PoP (Package on Package) memory devices.

The LPDDR2 memory device package will be attached directly on top of the processor package & hence this is called a package-on-package [POP] configuration between the memory controller & the LPDDR22 system memory.

To aid seamless connection between the memory controller and the LPDDR2 device; the memory controller package balls that communicate with LPDDR2 are brought out on all the 4 top sides of the package. The interconnect route from the memory controller to LPDDR2 is essentially the transmission line on the package. No board interconnect routing exists for the memory subsystem and hence the usual signal integrity distortion on the memory channels is substantially reduced.

Figure below shows different components in a POP topology. Intel will supply SOC with the PKG interposer on which LPDDR2 modules can be assembled.

Figure 3-3. Co-POP Overview Block Diagram



3.1.3.2 Supported DRAM Devices

To support the system memory sizes of 1 GB, and 2 GB the following DRAM devices are supported (see Table 3-30).

Table 3-30. Supported LPDDR2 DRAM Chips

Supported LPDDR2 DRAM Chips							
DRAM Density	Data Width	Banks	Bank Addr	Row Addr	Col Addr	Page Size	Standard
1Gb	x32	8	BA[2:0]	RA[12:0]	CA[8:0]	2KB	LPDDR2-S4
2Gb	x32	8	BA[2:0]	RA[13:0]	CA[8:0]	2KB	LPDDR2-S4
4Gb*	x32	8	BA[2:0]	RA[13:0]	CA[9:0]	4KB	LPDDR2-S4

3.1.3.3 Intel® Supported Channel/Rank Configuration

Table 3-31 shows the total memory size per rank and per channel with the supported DRAM chips used to make up the rank. All non-shaded rows in Table 3-31 are supported memory configurations.

Table 3-31.Supported LPDDR2—S4B System Memory Configurations

Total System Memory Size	Channel 0			Channel 1		
	Number of Ranks	Density / DRAM Chip (Rank)	Chip Data Width	Number of Ranks	Density / DRAM Chip (Rank)	Chip Data Width
1 GB	2	2 Gb	x32	2	2Gb	x32
1 GB	1	4 Gb	x32	1	4Gb	x32
2 GB	2	4 Gb	x32	2	4Gb	x32

NOTES:
1. Choosing a memory configuration that uses more dice increases z-height of the memory.

3.1.4 Memory Controller Functional Description

The Memory controller includes support for automatic refresh interval adjustment based on DRAM temperature, which is new for LPDDR2.

The Memory Controller Primary Function is to:

- Service memory access requests
- Translate system addresses into DRAM rank, bank, row, and column addresses
- Determine and track page state while servicing requests
- Track and enforce DRAM protocol timing to meet LPDDR2 specifications
- Perform any needed paging operations and complete the read or write request
- Transfer read/write data
- Handle periodic DRAM refresh events
- Provide timers to close unused opened pages

3.1.4.1 DRAM Burst Length

The memory controller supports DRAM burst lengths of 4 and 8, which are configurable through the DTR0 register.

- When the memory controller is configured for BL4, the memory controller performs two back-to-back 16-byte DRAM transactions for a 32-byte request.
- When the memory controller is configured for BL8 (default burst length):
  - For a 32-byte request, the memory controller performs one 32-byte DRAM transactions.
  - For a 64-byte read/write transaction:
    - Two memory channel—the memory controller performs on one 32-byte transaction on one channel, then another 32-byte transaction on the other channel.
    - One memory channel—the Memory controller performs two back-to-back 32-byte DRAM transaction.
  - This is the default burst length.

3.2 Graphics Subsystem

3.2.1 Overview

The graphics subsystem includes a 3-D graphics engine, video encode and decode engines, and a display controller which provides the 2-D graphics functionality for the display pipelines.

Key Features of Graphics Core:

1. 2D graphics, 3D graphics, vector graphics and video encode and decode supported on common hardware
2. Tile based architecture
3. Universal Scalable Shader Engine – multi-threaded engine incorporating Pixel and Vertex Shader functionality
4. Advanced Shader Feature Set – in excess of Microsoft VS3.0, PS3.0 & OGL2.0
5. Industry standard API support – OpenGL-ES 2.0, OpenVG 1.1
6. Fine grained task switching, load balancing and power management
7. Advanced geometry DMA driven operation for minimum CPU interaction
8. Fully virtualized memory addressing for OS operation in a unified memory architecture
9. Advanced & Standard 2D operations i.e. vector graphics, BLTs, ROPs etc

3.2.2 2D / 3D Graphics Features

- Deferred Pixel Shading
- On chip tile floating point depth buffer
- 8-bit Stencil with on chip tile stencil buffer
- 8 parallel depth/stencil tests per clock
- Scissor test
- Texture support
  - — Cube Map
  - — 3D Textures
  - — Projected Textures
  - — 2D Textures
  - — Non square Textures
- Texture Formats
  - — ARGB 8888,565,1555
  - — Mono chromatic 8, 16, 16f, 32f, 32int
  - — Dual channel, 8:8, 16:16, 16f:16f
  - — Compressed Textures PVR-TC1, PVR-TC2, ETC1.
  - — Programmable support for all YUV formats

- Resolution Support
  - Frame buffer max size = 8K x 8K
  - Texture max size = 8K x 8K
- Texture Filtering
  - Bilinear, Trilinear, Anisotropic, Convolution, PCF
  - Independent min and max control
- Gamma Correction
- YUV->RGB
- Normalization
- Indexed Primitive List support
  - Bus mastered
- Programmable vertex DMA
- Render to texture
  - Including twiddled formats
  - Auto MipMap generation

3.2.2.1 Universal Scalable Shader Engine Features

- Single programming model:
  - Multi-threaded with 16 simultaneous execution threads and up to 64 simultaneous data instances
  - Zero-cost swapping in, and out, of threads
  - Cached program execution model – max program size 262144 instructions
  - Dedicated pixel processing instructions
  - Dedicated vertex processing instructions
  - Dedicated video encode/decode instructions
  - 4096 32-bit registers 48 40-bit registers
  - 3-way 10 bit integer and 4-way 10 bit integer operations
- SIMD execution unit supporting operations in:
  - 32 Bit IEEE Float
  - 2-way 16 bit fixed point
  - 4-way 8 bit integer
  - 32 bit integer
  - 32bit bit-wise (logical only)
  - Dual Issue Instructions
- Static and Dynamic flow control
  - Subroutine calls
  - Loops

- Conditional branches
- Zero-cost instruction predication

- Procedural Geometry
  - Allows generation of primitives
  - Effective geometry compression
  - High order surface support
- External data access
  - Permits reads from main memory via cache
  - Permits writes to main memory via cache
  - Data fence facility
  - Dependent texture reads

3.2.2.2 Video Encode

3.2.2.2.1 Video Encode Features

The Intel® Atom™ Processor Z2760 supports full hardware accelerated video encode. The video encode hardware accelerator improves video capture performance by providing dedicated hardware based acceleration. Other benefits are low power consumption, low host processor load, and high picture quality.

The processor supports full hardware acceleration of the following video encode:

- Permits 720p30 H.264 BP encode
- MPEG4 encode and H.263 video conferencing
- Integer motion estimation
- Subpel motion estimation
- Transform and inverse transform
- Quantization and inverse quantization
- Encode Support up to H.263 Level 70
- Full hardware accelerated Elementary Stream Encode
- Internal Rate Control
- MMU support
- Deblocking

3.2.2.2.2 Encoding Pipeline

In general, the encoding process is pipelined into a number of stages. For MPEG-4/H.263/H.264 encoding, the data is processed in macroblocks, with a minimum of interaction from the embedded controller within each processing stage.

3.2.2.2.3 Encode Codec Support

The processor supports the following profiles and levels as shown in Table 3-32.

Table 3-32.The Profiles and Levels of Support

Standard	Profile	Maximum Bit Rate (BPS)	Typical Picture and Frame Rate
H.264	BP	128K	QCIF@15fps
H.264	BP	192K	QCIF@15fps
H.264	BP	384K	CIF@15fps or QVGA@20fps
H.264	BP	2M	CIF@15fps or QVGA@20fps
H.264	BP	10M	525SD@30fps, 625SD@25fps, VGA@30fps
H.264	BP	14M	720p@30fps, 525SD@60fps, 625SD@50fps
H.264	BP	20M	720p@60fps
H.264	BP	20M	1080p@30fps
H.264	BP	50M	1080p@30fps
H.264	BP	50M	1080p@30fps
H.263	BP	64K	QCIF@15fps
H.263	BP	128K	QCIF@30fps, CIF@15fps, QVGA@15fps
H.263	BP	384K	CIF@30fps, QVGA@30fps
H.263	BP	2M	CIF@30fps, QVGA@30fps
H.263	BP	128K	QCIF@15fps
MPEG4	SP	64K	QCIF@15fps
MPEG4	SP	128k	QCIF@30fps, CIF@15fps, QVGA@15fps
MPEG4	SP	384k	CIF@30fps or QVGA@30fps
MPEG4	SP	768K	CIF@30fps or QVGA@30fps
MPEG4	SP	8M	525SD@30fps, 625SD@25fps, VGA@30fps
M-JPEG	Baseline		VGA@30fps, 525SD@30fps, 625SD@25fps

Note: Video Decode

The general features for the Video decode hardware accelerator are:

- Decode Support up to H.264 (AVC) High Profile level 4.2
- Decode Support up to MPEG-2 Main Profile High level
- Decode Support up to MPEG-4 ASP Level 5.
- Does not support global motion compensation
- Decode Support up to WMV Main Profile High level
- Decode Support up to VC-1 High Profile level 4.2
- Decode Support up to H.263 Level 70
- Decode Support up to AVS JiZhun profile Level 6.0.
- Decode Support up to SorensenSparc @60hz
- Decode Support up to Realvideo9
- Support Dual stream fast context switch homogeneous elementary stream decode up to H.264 Level 4.1

- Full hardware accelerated Elementary Stream Decode
- Decode up to H.264 High Profile Level 4.1 at 2X rate for smooth fast forward
  - CABAD, CAVLD, VLD and Exp-Golomb decoding
  - Inverse scan; iDCT and integer inverse transform
  - Half, quarter and eighth-pel motion compensation
  - Full support for unrestricted motion vectors
  - Full bi-directional prediction
  - Inverse H.264 intra prediction
- H.264 de-blocking filter; VC-1 (WMV 9) de-blocking/overlap filter
- Support for trick modes and error concealment/recovery
- Support for Data Partitioning
- Support for Error Concealment and Correction
- Support for out of loop deblocking
  - Implemented as a separate memory surface to preserve the standard reference frames for proper decoding.
- Support for Rotation
  - Implemented as a separate memory surface in addition to the standard orientation reference frames
- MMU Support
- Support for External Cache
- The video decode accelerator improves video performance/power by providing hardware-based acceleration at the macroblock level (variable length decode stage entry point). The processor supports full hardware acceleration of the following video decode standards.

Table 3-33.Hardware Accelerated Video Decode Codec Support (Sheet 1 of 2)

Codec	Profile	Level	Notes
H.264	Baseline profile	L3	1
H.264	Main profile	L4.1	
H.264	High profile	L4.1	
MPEG2	Main profile	High	
DivX	Certified	High Def	2
MPEG4	Simple profile	L3	
MPEG4	Advanced simple profile	L5	3
VC1	Simple profile	Medium	4
VC1	Main Profile	High	4
VC1	Advanced profile	L3	4
WMV9	Simple profile	Medium	4
WMV9	Main profile	High	4
H.263	Profile0	L70	

Table 3-33.Hardware Accelerated Video Decode Codec Support (Sheet 2 of 2)

Codec	Profile	Level	Notes
Sorenson	Spark	SD@60Hz	
RealVideo9	RealPlayer11,RealPlayer10, RealPlayer9	HD	
RealVideo8	RealPlayer8	HD	4
JPEG	Baseline	1 Gpix	5,6

NOTES:
1. Higher levels are supported where the toolset used is those common to both Baseline and Main profile.
2. DivX is based on MPEG4 Advanced simple profile but ignores the levels defined by MPEG4. There are two variants of DivX. The "certified" version does not require GMC or quarter pixel motion compensation prediction. The "non-certified" does support these features. A DivX encoder can produce stream that are either certified or not certified but will warn the user when producing non-compliant streams.
3. There is a restriction that for GMC streams only one warp point is supported.
4. Video decoder performs all processing required to reconstruct pictures used to generate references. There is a requirement that these picture when being displayed require some out of loop post processing. This is expected to be done in the display pipeline to minimise bandwidth or in a compositing engine.
5. The size is limited to 32k*32k for three component data e.g. YCbCr 4:4:4, 4:2:2, 4:2:0 or RGB but reduced to 16k*16k for four component images e.g. CMYK. This performance is for 4:2:0.

3.3 Display Interfaces

The display controller provides the 2D graphics functionalities for the display pipelines. The display controller converts a set of source images or surfaces, merges them and delivers them at the proper timing to output interfaces that are connected to the display devices. Along the display pipe, the display data can be converted from one format to another, scale and image enhancement processing, gamma converted. The output of the display pipe is then formatted to a stream of pixels with necessary timing that is comfortable to a specific display port specification like MIPI DSI, HDMI, and sends out of the SoC through a physical layer interface.

3.3.1 Display Controller Partitioning and Interfaces

The display controller is organized into two display outputs - MIPI for internal LCD panels and HDMI for external panels.

T display controller supports the following features:

- Two display pipes, Pipe A, B
  - Display Pipe A: drive a MIPI DSI panel with maximum 4-lane in one internal panel configuration.
  - Display Pipe B: drive HDMI port including HDCP encryption and audio sample configuration and fetching.
- 6 display planes for input frame buffers
  - Display Plane A, B: For graphic frame buffer, maximum size 2048x 2048 active size. Surface size can be bigger and limited by tile stride in OS.
  - OverlayA: video overlay planes.
  - Cursor A, Cursor B: hardware cursor with up to 256x256 size
  - VGA: driverless-display for debug purpose only.
- Video overlay features:
  - Video overlay supported multi-taps filtering which buffers 2 or 3 full scan lines of buffers to up to 1920 pixels. The vertical filter is 3-tap for all components. The horizontal filter is 5-tap for Y and 3-tap for U/V components.
  - Video filtering employed in-line filtering (scaling) that is capable to downscale 3 times in both horizon and vertical direction without aliasing. Video can be downscaled past 3 times to approximately 16 times with some visible artifacts due to decimating.
  - Video overlay supported Image Enhancement Processor Lite IP that provide following functionalities:

    —Black/white level expansion

    —Blue stretch and skin color correction

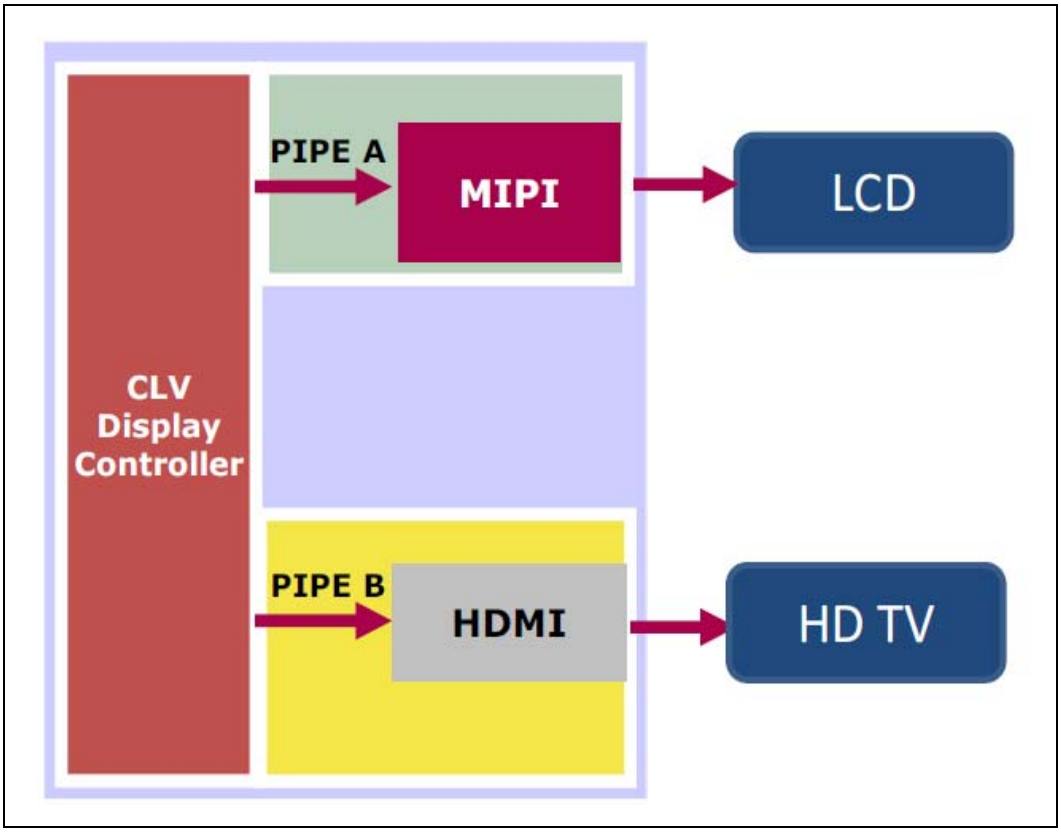
    —Demodulation angle, Hue, Saturation, Contrast, Brightness, and Color Space Conversion.
- MIPI interface:
  - Pipe A can support all types of MIPI DSI panels from type 1 to type 4.
  - Pipe A can support display with full frame buffer and partial frame buffer
  - Advanced bandwidth management will be implemented to prevent tearing effect.
  - DSI controllers and PHY clocks are generated by independent PLL to support a wide range of clocks.
- Power management features
  - When a pipe is not in use its power well can be power gated to save leakage.
  - When a pipe is active additional clock gating is implemented to save dynamic powers
  - Pipe A comprehended advantage of display self-refresh and fully clock gated until next plane buffer update from software.
- External monitor support will be HDMI only

— Digital TV will use the HDMI interface. The design is compliant to HDMI 1.3a spec. The HDMI interface also supports compressed and uncompressed audio streams. This interface can optionally supported HDCP (High Definition Content Protection) cipher streams.

— 3x3 Panel Fitter can be utilized by pipe B to scale to desired resolution and aspect ratio. It supports letterbox and pillar-box.

— A Display PLL is dedicated to support external monitor. It will be configured and powered on before an external monitor port is enabled.

Figure 3-4. Display Support



3.3.2 Dual Independent Display

Dual Independent Display is the display of different images, possibly at different resolutions, on two displays. This is supported by using display pipes, one pipe driving one of the displays, and the second pipe driving the other display.

Dual Independent Display is similar to Clone Mode, except that different images are being displayed, and different resolutions may be used.

3.3.3 MIPI-DSI

3.3.3.1 Overview

MIPI interface supports display resolution up to 1366 x 768p @ 60Hz and with a 24b per pixel panel only. 18b per pixel panel can be connected but not fully supported. That is, there is no dithering function for a MIPI command mode panel. The MIPI interface consists of 1 clock lane and 4 data lanes. Max throughput for interface is 4x1GT/s = 4.0GT/s

3.3.3.2 Power Management

3.3.3.2.1 Different Display Power Management Features

Table 3-34.Display Power Management Options

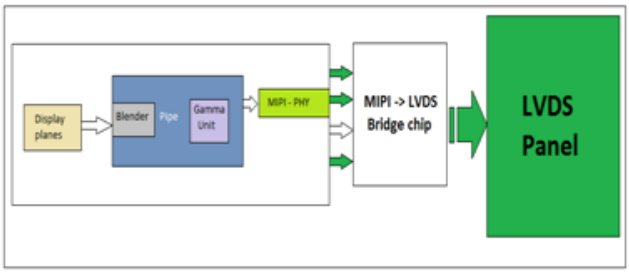
Power management	How it works	Requirements to implement
DSR (Display Self Refresh)	• If there is no update to host interface display planes, then driver • Sends CMD to MIPI display / MIPI bridge to refresh from local frame buffer. • For any display interrupt or Gfx activity, driver enables DC plane/ pipes/PLL if they are PG or ULPS. • Checks exit latency against the power state requirement before it can enter DSR.	• Requires appropriate amount of local frame buffer on the panel or bridge. • Requires MIPI panel or MIPI bridge to comply with DCS command sets of MIPI spec. • Panel or bridge should provide in-line TE trigger or TE pin so display will know when to send the next buffer and avoid tearing effect.
DPST 3.0 (Display Power Saving Technology)	• Host side Display controller has DPST 3.0 engine which can reduce up to 27% of panel backlight power. • It processes the frames, analyze the picture in one frame and decides/ updates to change image and backlight in future frames.	• DPST needs to be enabled by display driver. Currently DPST will not work in parallel with DSR. • If MIPI panel does not have local frame buffer, then DPST should be enabled and DSR can be disabled. • DPST should be enabled for additional power savings for bridge chips which does not have local frame buffer.
CABC (Content Adaptive Backlight control)	• CABC engine resides inside either display bridge or panel and it can process the current frames to update backlight for next frames. • This can work in parallel with DSR. Power savings due to CABC is bigger when playing higher fps video(30% of backlight).	• Needs CABC inside panel or bridge.
ALS (Ambient light sensor) based BKLT power savings	• Modulates backlight based on ambience light. • Power savings are more(30%) for darker ambience and less for brighter ambience [20%]	• Needs ALS inside panel or bridge.

3.3.4 LVDS Panel Support

A external MIPI DSI-to-LVDS bridge device is required to connect the display controller to an LVDS panel. Bridge Device is used for larger panels

Below is the Block Diagram to Drive LVDS panels.

Figure 3-5. Block Diagram of Bridge Device to Drive LVDS Panels



3.4 HDMI [High Definition Multimedia Interface]

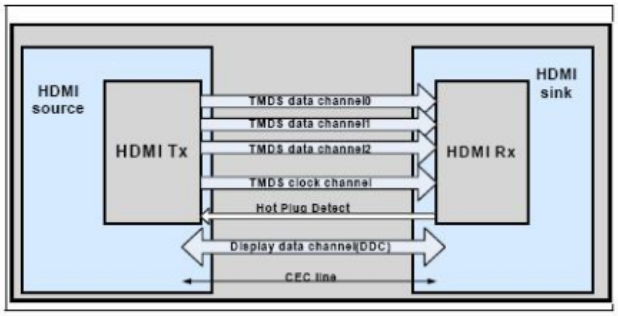
3.4.1 Overview

The High-Definition Multimedia Interface (HDMI) is provided for transmitting uncompressed digital audio and video signals. It can carry high quality multi-channel audio data and all standard and high-definition consumer electronics video formats.

As shown in Figure 3-6 the HDMI cable carries four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA Display data channel (DDC).

Audio, video and auxiliary (control/status) data is transmitted across the three TMDS data channels. The video pixel clock is transmitted on the TMDS clock channel and is used by the receiver for data recovery on the three data channels.

Figure 3-6. HDMI Overview



3.4.2 HDMI Features

HDMI rev1.3a is supported through x4 link with integrated audio and software lip synch. Transfer rate is 1.65GT/z. HDCP rev1.3 is supported. The controller is running at 165Mhz and support 1080p and PHY is using TMDS with total bandwidth of 4.95Gbps. HDMI PHY also has HPD (hot plus detect) interface.

Pixel depth of 24-bit only is supported. SMPTE 170M / ITU-R BT.601 and ITU-R BT.709-5 colorimeter is supported. The SoC supports Multi-channel Audio -up to 8 channels. HDCP is supporting both Ri and Pj checks.

Deep color mode is NOT supported which requires usage os 10/12/16bit per color. Only 8bit color is supported. IEC 61966-2-4 (xvYCC) and Gamut Metadata is NOT supported. One bit Audio and High Bit Rate Audio is not supported. HDCP with AV mute is not supported.

3.4.3 HDMI DDC

The Enhanced Display Data Channel (E-DDC) as required by HDMI allows the display (HDMI receiver) to inform the host (HDMI transmitter) about its identity and capabilities using an I2C bus. It is enhanced from DDC (the older standard) by enabling the communication channel to address a larger set of data. The communication channel, as used for this purpose, is uni-directional from display to host using the E-DDC operational modes except for the command to initiate an EDID data transfer which the host device sends to the display. The contents and formats of data are described in the VESA Enhanced Extended Display Identification Data Standard (EEDID) and a number of E-EDID extension block standards.

E-DDC is a protocol based on I2C and is used on a bi-directional data channel between the display and host. This protocol accesses devices at I2C address of A0h / A1h as well as the address 60h. The 60h address is used as a segment register to allow larger amounts of data to be retrieved than is possible using earlier DDC standards. I2C_3 is used for reading the EDID from the display devices through HDMI.

3.5 Imaging Subsystem / MIPI-CSI Interfaces

The Intel® Atom™ Processor Z2760 contains an internal ISP (Image Signal Processer) that supports 2 MIPI-CSI2 compliant sensors, up to 8MP. Typical use-case is a high-MP rear camera for still / video capture and a lower-res front camera for video conferencing.

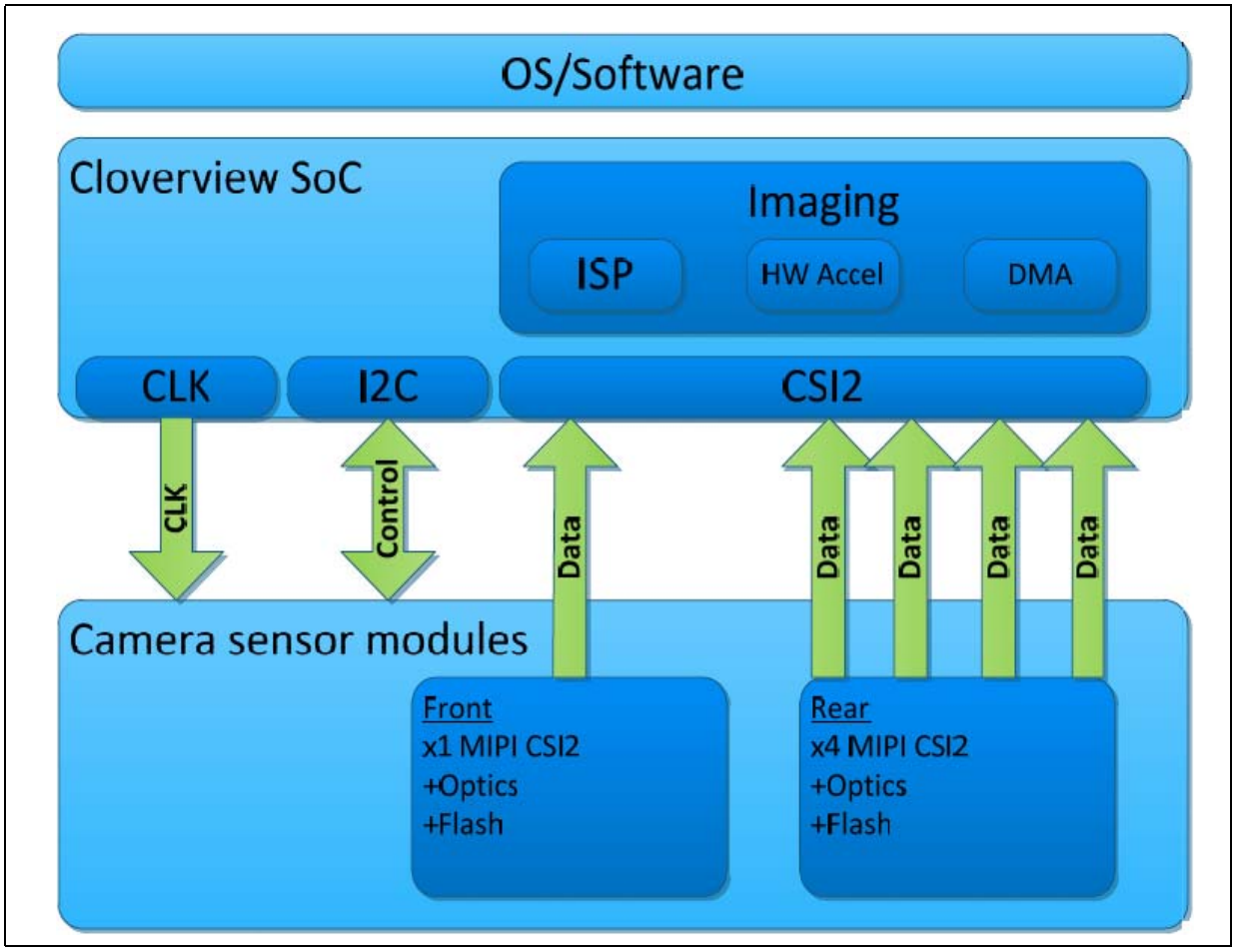
3.5.1 Overview

The processor supports one MIPI CSI x4 for the primary sensor and one MIPI CSI x1 for the secondary sensor.

The SoC platform camera solution may be divided into 3 levels as shown in Figure 3-7:

1. OS / SW.
2. Imaging core, based on the Image Signal Processor (ISP) and MIPI-CSI2 input.
3. Camera sensors & peripheries.

Figure 3-7. Camera Connectivity



3.5.1.1 Imaging Core

The imaging core includes the MIPI-CSI I/Os, the ISP 2300 processor, DMA and local SRAM. The imaging core receives the pixel stream sent over the MIPI-CSI interface and relays them to the ISP for processing. The ISP then performs demosaicing (converting the 1-color-per-pixel format to a standard RGB/YUV format), as well as additional image corrections, enhancements and processing (as required by the OS/SW). The resulting output is then placed in the system DRAM for consumption by the OS/SW.

3.5.1.2 Camera Sensors & Peripherals

Each sensor is connected using the MIPI-CSI lanes for data (pixels) and I2C for control (commands).

The SoC uses the underlying I2C interface to configure and control the sensor, where the sensor utilizes the data connectivity of the MIPI-CSI interface to send to the SoC a stream of pixels in BAYER format for each frame taken.

In addition, the SoC may choose to operate one or more of the sensor peripheries, such as a flash (LED or Xenon based), mechanical shutter (if present) and a focus motor (if present). The flash, auto-focus & mechanical shutter are controller through GPIOs or discrete I2C components.

3.5.1.3 OS/SW

The OS/SW includes drivers, OS modules & applications that work together to configure, activate and operate the imaging core & camera sensor together.

The image, as captured by the sensor and processed by the imaging core, is then either displayed to the viewfinder (screen), saved to storage or is processed in an application-dependant manner (e.g. video conferencing).

The SW drivers also play a role in the image processing, as it receives statistical information required for 3A processing (Auto-focus, auto-white balance and auto exposure), performs the required algorithms (which are not suitable for the ISP) and reconfigures the camera sensor & ISP accordingly.

3.5.2 Imaging Capabilities

The ISP performs all the basic image / video capture processing (as listed below), whereas the application will perform the format encoding (or anything else).

The following table summarizes the ISP capabilities:

Table 3-35. ISP Capabilities

Feature	capabilities
Sensor interfaces	primary sensor (MIPI CSI x4) Secondary sensor (MIPI CSI x1)
Image capture	8MP @ 15fps
Video capture	720p30 or 1080p30
Input formats	RAW 8,10,12 - ISP processing Other - pass through to SW
Special features	Image and video stabilization Low light noise reduction Burst mode capture Memory to memory processing 3A (AE, AWB, and AF)

The following list summarizes the ISP image processing capabilities:

Table 3-36. ISP Image Processing Capabilities (Sheet 1 of 2)

Fixed pattern noise reduction	Multi-axis color control
Black level compensation	Chroma enhancement
Lens shading correction	Extended dynamic range
White balance	Tone control
Bayer domain down scaling	Gamma

Table 3-36.ISP Image Processing Capabilities (Sheet 2 of 2)

Defect pixel detection and correction	Scaling for viewfinder
Bayer noise reduction	Temporal noise reduction
Color interpolation	Red Eye Removal
3A Statistics	Chromatic aberration correction
Digital video stabilization	XNR
False color correction	Digital zoom
YCC noise reduction	Skin tone detection
Sharpen/edge enhancement	Skin tone correction
Color space conversion/Image effects	Lens geometry distortion correction

3.5.3 Sensors

In order to integrate a sensor into the platform solution, the sensor has to be connected properly over the MIPI-CSI2 interface, receive the required power rails (may vary between sensors).

Also, for each sensor, new OS/SW support may be required. According to the specific OS, new sensor drivers may have to be developed.

After the sensor has been integrated into the system, it must undergo a process of tuning & calibration (as detailed below).

3.5.3.1 Sensor Tuning and Calibration

In order to receive the best image quality that can be provided by a given system, the ISP, sensor and sensor module must be calibrated and tuned to work best together.

The tuning and calibration compensate for variation between sensors, modules (optics), thermal considerations, platform placements and other factors that vary between system.

The tuning and calibration data may affect all components in the system (sensor configuration, ISP parameters or SW configuration).

3.6 Audio Subsystem / I2S Interfaces

3.6.1 Overview

The goal of the Low Power Audio subsystem is provide hardware acceleration for common audio and voice functions such as codec, Acoustic Echo Cancellation, noise cancellation, and so forth.

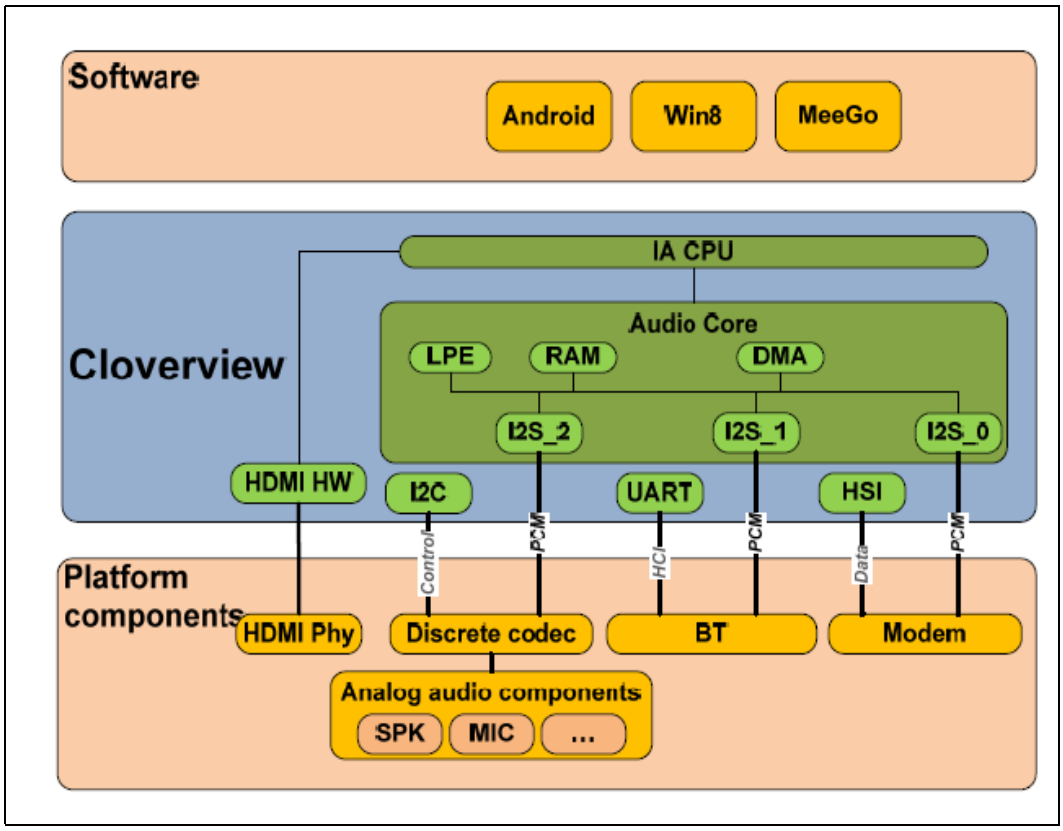
The platform is expected to provide to music playback times similar a commercial music player and VoIP and CSV call times similar to commercial available VoIP-enabled 3G based Smart phones.

3.6.2 Platform Components

As shown below, the SoC has 3 levels of audio support:

1. OS / SW.
2. Audio core, based on Low Power Engine (LPE) and I2S outputs.
3. Audio devices. Including the I2S audio codec and other devices.

Figure 3-8. Audio Components



3.6.3 OS/SW

The OS/SW includes drivers, OS modules & applications that work together to playback (or record) audio streams. These audio streams are then forwarded (or received from) to the LPE audio core for further processing and output (or input) in one of 2 ways:

1. Raw Data (PCM sample), where the OS/SW already decodes and processes the audio samples and outputs a decoded stream.
2. Encoded, where the OS/SW leaves the decoding and processing to the audio core (for more power efficient audio processing).

3.6.4 Audio Core

The audio core receives the set of streams (encoded & raw) and processes them.

The audio core uses the HiFi-2 programmable audio DSP engine (LPE). The audio core also includes a dedicated DMA, SRAM and instruction and data RAMs for DSP operation.

Using a specifically written DSP FW, the audio core:

1. Decodes the known samples from the encoded streams.
2. Performs audio processing.
3. Mixes the streams into a single stream.
4. Outputs on the relevant I2S port.

3.6.5 Audio Devices

The audio devices in the platform are the recipients (or originators) of the audio data.

1. The discrete audio codec receives (or sends) the audio data for local output (or input) devices, such as hands-free speakers, headset jack & local microphone.
2. The BT adapter receives (and sends) samples to be played back on the BT hands-free and headset devices.
3. The cellular modem receives (and sends) samples of an ongoing voice call.

3.6.6 I2S Mapping

As shown in the Figure 3-8, the platform supports 4 different I2S devices which are mapped as shown below.

Table 3-37.I2S Mapping

I2S interface	Device	Usage
I2S_0	Discrete Codec (secondary) OR WWAN Modem	Support for independent outputs OR Voice calls [Future support]
I2S_1	BT	Bluetooth audio
I2S_2	Not used	Not used
I2S_3	Discrete D2A codec	On-platform audio (speakers, microphone, headset, line-out, etc)

3.7 I^2C Interface

The SoC supports 6 instances of the I^2C controller inside the Low-Speed Peripheral Cluster. Only 7-bit addressing mode is supported. These controllers operate in master mode only. Max device is limited to 130 pF capacitive load.

3.7.1 I²C Protocol

The I²C bus is a two-wire serial interface, consisting of a serial data line (SDA) and a serial clock (SCL). These wires carry information between the devices connected to the bus. Each device is recognized by a unique address and can operate as either a "transmitter" or "receiver," depending on the function of the device. Devices are considered slaves when performing data transfers, as the SoC will always be a master. A master is a device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

- The SoC is always I²C master, it does not support multi-master mode
- The SoC can support clock stretching by slave devices
- The I²C is a synchronous serial interface.
- The SDA line is a bi-directional signal and changes only while the SCL line is low, except for STOP, START, and RESTART conditions.
- The output drivers are open-drain or open-collector to perform wire-AND functions on the bus.
- The maximum number of devices on the bus is limited by the maximum capacitance specification.
  - Refer to the *Electrical Specs Chapter for details.*
- Data is transmitted in byte packages.

3.7.2 I²C Modes of Operation

The I²C module can operate in the following modes:

- Standard mode (with data rates up to 100Kb/s),
- Fast mode (with data rates up to 400Kb/s),

The I²C can communicate with devices only using these modes as long as they are attached to the bus. Additionally, fast mode devices are downward compatible.

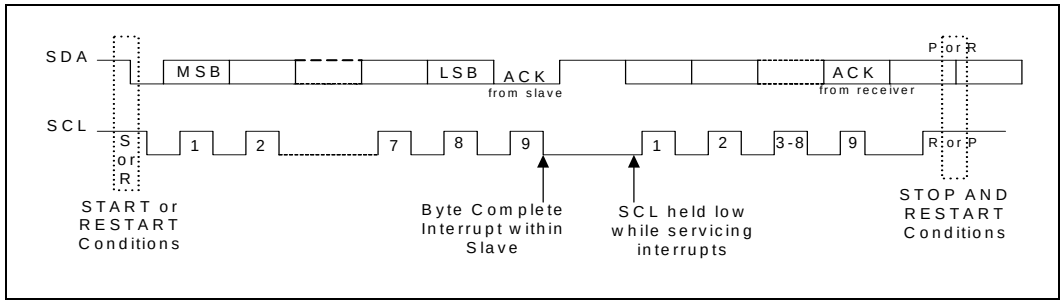
- Fast mode devices can communicate with standard mode devices in 0–100Kb/s I²C bus system.

However, according to the I²C specification, Standard mode devices are not upward compatible and should not be incorporated in a fast-mode I²C bus system as they cannot follow the higher transfer rate and unpredictable states would occur.

3.7.3 Functional Description

- The I^2C master is responsible for generating the clock and controlling the transfer of data.
- The slave is responsible for either transmitting or receiving data to/from the master.
- The acknowledgement of data is sent by the device that is receiving data, which can be either a master or a slave.
- Each slave has a unique address that is determined by the system designer
  - When a master wants to communicate with a slave, the master transmits a START/RESTART condition that is then followed by the slave's address and a control bit (R/W), to determine if the master wants to transmit data or receive data from the slave.
  - The slave then sends an acknowledge (ACK) pulse after the address.
- If the master(master-transmitter) is writing to the slave(slave-receiver)
  - The receiver gets one byte of data.
  - This transaction continues until the master terminates the transmission with a STOP condition.
- If the master is reading from a slave (master-receiver)
  - the slave transmits (slave-transmitter) a byte of data to the master, and the master then acknowledges the transaction with the ACK pulse.
  - This transaction continues until the master terminates the transmission by not acknowledging (NACK) the transaction after the last byte is received, and then the master issues a STOP condition or addresses another slave after issuing a RESTART condition. This behavior is illustrated in Figure 3-9.

Figure 3-9. Data Transfer on the I^2C Bus



3.7.3.1 Clock Stretching

All I2C controllers support clock stretching. The SoC is always the master and drives the serial clock at all time, except for the acknowledge pulse. Only during the acknowledge pulse, the slave can optionally hold the clock at logic 0 longer than the expected low time. The I2C controller waits for the device to release the clock line before proceeding to the next bit of the transfer. A slave device might stretch the clock if it is not ready to accept the next bit from the master.

3.7.3.2 I2C Sensors

Multiple sensors are expected to be used in Intel® Atom™ Processor Z2760 based tablets.

The SoC provides multiple low speed peripheral buses that can be used to connect the sensor devices to the platform. The preferred interface for the sensors connection is I2C. The expectation is the I2C host controller will be the master and the sensor devices will be slaves.

3.8 Serial Peripheral Interface (SPI) Interface

The SoC implements three instances of SPI controller and one instance of SSP controller in SPI mode.

Table 3-38. Summary of SPI Interfaces

Bus	Host	Usage	Freq	Comment
SPI_0	SCU	PMIC, NOR, UART	25Mhz	IA32 access is blocked, Master Mode only
SPI_1	IA32	Unused	25Mhz	Not recommended for use
SPI_2	IA32	Unused	25Mhz	Not recommended for use.
SPI_3	IA32	Unused	25Mhz	Not recommended for use.

SPI_0 can be accessed exclusively by the SCU and communicates to PMIC, UART, and NOR devices. IA X86 host accesses to SPI0 are blocked by hardware. SPI_1, SPI_2, and SPI_3 are controlled by the IA X86 host.

SPI_1, SPI_2, and SPI_3 interfaces are not supported. Customers intending to use SPI_1, SPI_2, or SPI_3 interfaces in their design should obtain prior approval.

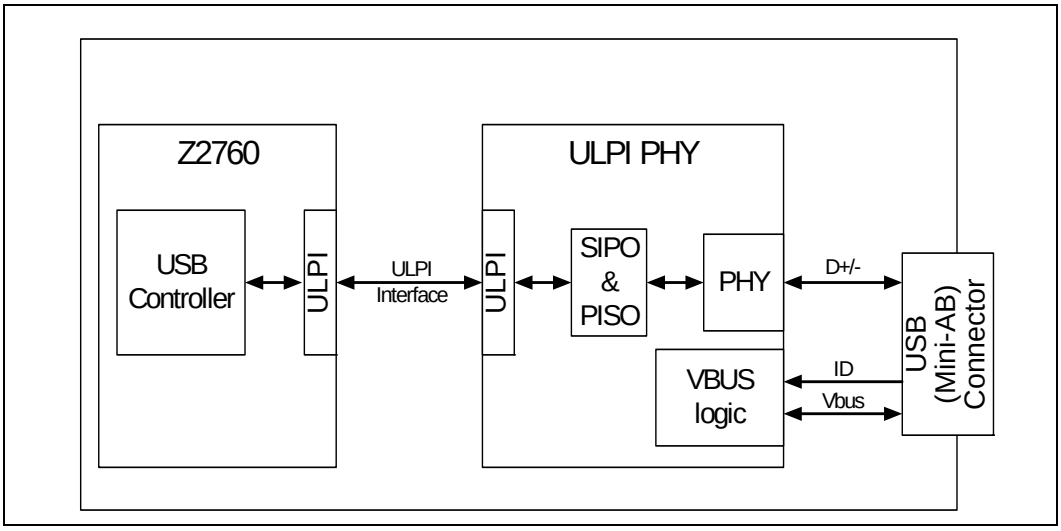
3.9 USB Controller and ULPI Interface

3.9.1 Overview

SoC features two USB controllers.

The controllers are primarily intended to be used as EHCI compliant hosts connected to an external PHY. The same IP core provides the controller functionality for both controllers. However, the configuration of the controller IP core will differ.

Figure 3-10.ULPI0 Implementation



3.9.2 Feature Set

3.9.2.1 Host Controllers

All USB device peripherals are compliant with the USB 2.0 specification:

- Intel EHCI Host controller. The USB Host Controller registers and data structures are compliant to Intel EHCI specification. Device controller registers and data structures are implemented as extensions to the EHCI programmers interface.
- Supports Link Power Management (LPM)
- An 8-bit data interface transmitted SDR at 60 MHz ULPI clock
- Through the USB PHY:
  - Directly connected USB legacy (USB 1.1) full and low speed devices without a companion USB 1.1 Host Controller or Host Controller driver software using EHCI standard data structures.

3.9.3 Link Power Management

3.9.3.1 Introduction

USB 2.0 released a Link Power Management ECN support to save additional power during idle periods across links and devices. The following table lists the various Link Power Management states

Table 3-39.USB Link States

LPM State	Description	Notes
L0 (On)	Port is enabled for propagation of transaction signaling traffic.	
L1 (Sleep)	New low power sleep state similar to L2 (suspend) but with a faster exit latency	Latencies Entry: ~10 µs Exit: ~70 µs – 1 ms (host-specific)
L2 (Suspend)	Entry to L2 is triggered using a command to a hub or host port, at which point the port ceases signaling down the port. The device discovers suspend after 3ms or inactivity on the port	Latencies Entry: ~3 ms Exit: >30 ms (OS-dependent)
L3 (Off)	Port is not capable of any data signaling. Disabled, inactive state.	

The host directs the link to enter a L1 state by issuing a LPM token. The device replies by acknowledged the LPM transition (ACK), or indicates that it is not ready to make the low power transition (NYET) or indicates that it does not support the L1 state (STALL).

The decision to enter the L1 state has to be made by the host after taking after examining the progress made by currently scheduled transactions (if any) and possibly by looking ahead at the transactions that are scheduled to be executed.

3.9.3.2 LPM Support

The USB 2.0 LPM Controller provides support for generating and receiving LPM transactions and also provides additional registers to support LPM and the EHCI addendum specification.

Though the USB controller provides support at the link-level to enter and exit LPM states, it does not do so autonomously and must be directed to the enter or exit LPM state by another platform component. This functionality is performed by the software (Host Controller Driver) or alternatively by the Firmware.

3.9.3.3 Software-Directed LPM

LPM capabilities will be detected automatically by the EHCI Host Controller Driver (HCD) during host controller initialization and device connection.

Selective Suspend of the port into LPM state is enabled by the HCD using the sysfs interface.

The HCD will also support auto suspend of the port into the LPM L1 state.

3.10 MIPI-HSI Interface

The MIPI HSI interface is not used.

3.11 PMIC Interfaces

Communication between the processor and the PMIC is done through a primary SPI interface and a secondary SVID interface.

3.11.1 SPI 0

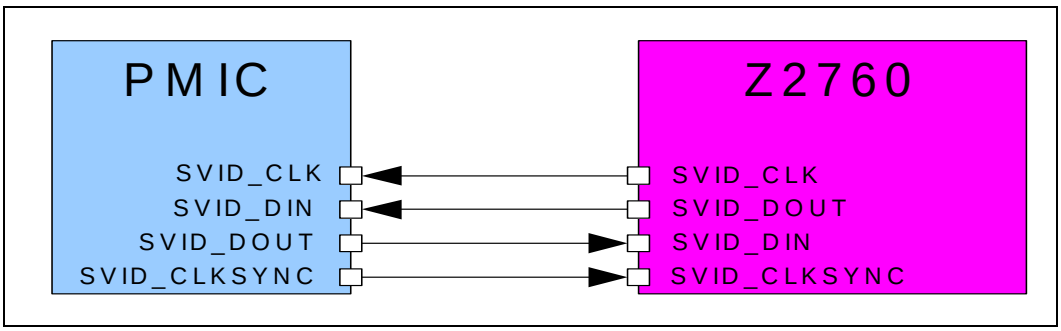
- PMIC is a slave device controlled by the SoC.
- The SoC SPI_0 interface is dedicated exclusive for SCU access to control the PMIC.
- SPI_0
  - One slave select signals
  - Supports master mode only
  - Supports up to serial rate of 12.5 MHz

3.11.2 SVID

3.11.2.1 Serial VID

The Serial Voltage ID (SVID) is a 4-pin interface between the processor and the PMIC. It sends 7-bit VID values from the SoC to the PMIC to set the core VCC and VNN supply voltages. Dynamic voltage switching is supported. The SVID interface may also pass additional indicator status.

Figure 3-11.SVID Interface



3.12 Storage Interfaces

3.12.1 Overview

Atom™ Processor Z2760 supports mass storage devices with a stack of drivers that manage the physical connection of the device to the bus and the translation of the commands from the system to the device.

The primary bootable and embedded storage in the platform is based on eMMC based storage.

Intel® Atom™ Processor Z2760 Supports:

1. 2 ports of eMMC 4.41 controller

2. 1 port of an SD 2.0 Controller.

Figure 3-12.Storage Controllers

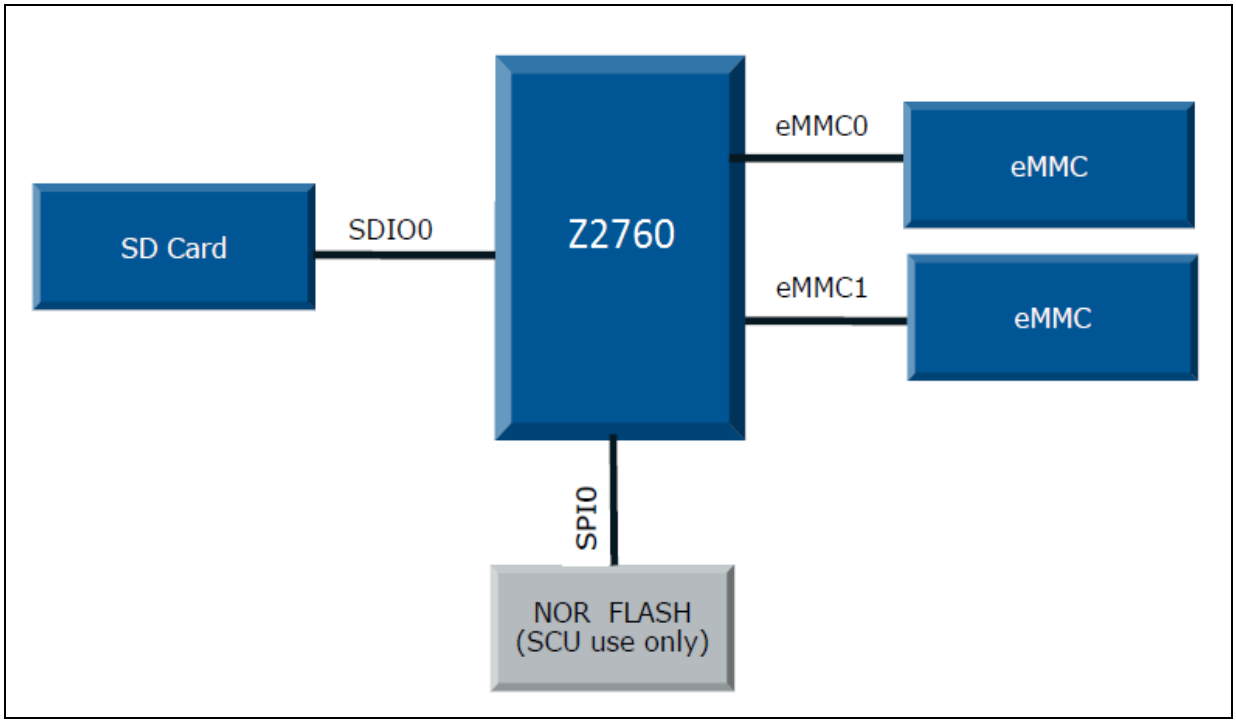


Table 3-40.Storage Controller Instances

Port	Protocol	Data Pins	IO	Primary usage
eMMC0	eMMC	8	1.8 V	eMMC boot
eMMC1	eMMC	8	1.8 V	Optional
SD0	SD	8	2.85 V	SD card

3.12.2 eMMC

3.12.2.1 eMMC NAND Flash

eMMC 4.41 allows for different partitions for boot as well as user partition area for generic data storage in addition it also supports a replay protected memory block partition to manage data in an authenticated and replay protected manner.

This allows for BIOS and OS based boot as well as partitions in the eMMC NAND for user data.

3.12.2.2 eMMC Host Controller Feature Set

- Meets eMMC Specification version 4.41 (JEDEC Standard JESD84-A441)
- Host clock rate variable between 0 and 50 MHz

3.12.3 SD / SDHC Card Interface

3.12.3.1 SD Card Host Controller Overview

The Secure Digital (SD) Host controller is configured to control:

- Secure Digital Host Controller Standard Specifications (SD host – version 2.0)
- Secure Digital memory (SD memory – version 2.0)
- Secure Digital Part 1 Physical Layer Specification – (SD PHY - version 2.0)
- Secure Digital Part1 eSD (Embedded SD) Addendum – (eSD - version 2.1)
- Support for SD and SDHC cards up to 32GB.
- Card Detection (Insertion / Removal)
  - Supports Card Detection (Insertion/Removal) with dedicated card detection signal only.
- Host clock rate variable between 0 and 50 MHz
- Designed to work with I/O cards, Read-only cards and Read/Write cards.

Table 3-41.SD Usage

Port	Protocols	Data Pins	Voltage	Card Detect	Usage
SD0	SD/SDHC	8	2.85v	yes	SD card

3.13 Communications Interfaces

The Intel® Atom™ Processor Z2760 supports two Secure Digital IO (SDIO) v2.0 interfaces for connections to embedded communications devices.

- Meets SD Host Controller Standard Specification Version 2.0
- Up to 25Mbytes per second read and write rates using 4 parallel data lines
- Support 1.8V IO only for communications

Table 3-42.SDIO Usage

Port	Protocols	Data Pins	Voltage	Card Detect	Usage
SDIO1	SDIO	4	1.8 V	no	Wifi
SDIO2	SDIO	4	1.8 V	no	Unused

3.14 Intel® Smart and Secure Technology (Intel® S&ST)

3.14.1 Overview

This section describes the security components and capabilities. The security system contains a Security Engine and additional hardware security features that enable a secure and robust platform.

3.14.2 Detailed Feature Set

3.14.2.1 Hardware Security features

- Hardware based cryptography accelerations
- Flexible Secure Execution Environment to run Secure Services
- D0i2 support for the Intel® S&ST engine.
- Memory access control mechanism through Isolated Memory Regions (IMR or Next generation RAR)
- In line encrypt and decrypt engines to provide robust and scalable DRM playback
- 3 always on-chip Security Timers and counters & secure RTC (counter)
- Protected eMMC partition used exclusively by SCU

3.14.2.2 Platform Software Security features

- Secure BIOS, FW and OS boot with OS integrity protection
- Content Protection capabilities such as EPID-CP, WMDRM 10 and PlayReady 1.2
- Hardened OMA-DM lock capability
- Extended Firmware Development environment for Intel® S&ST programming
- Hardened OMA-DM device Remote device lock
- OS Integrity protection for Android/MeeGo Windows
- Intel Anti-Theft support
- PlayReady and WMDRAM 10 support
- Application Sandboxing and access control

3.15 GPIO Interface

The SoC provides highly-multiplexed general-purpose I/O (GPIO) pins for use in generating and capturing application-specific input and output signals. There are 2 instances of the GPIO Controllers, GPIO_Controller_[0..1].

The characteristic of the GPIO Controller are:

- GPIO_Controller_0 is located on the AON power well and connected to the AON SC Fabric.

- GPIO_Controller_1 is located in the Core power well and connected to the GP Fabric.

The characteristic of the GPIO pins are:

- Most GPIO pin can be programmed as an output, an input, or as bi-directional for certain alternate functions (that override the value programmed in the GPIO direction registers). When programmed as an input, a GPIO can also serve as an interrupt source.
  - GP_CORE_[067..072] are GPI only
  - GP_AON_[014] is multiplexed with SD_0_CMD ball.
- All GPIO pins are configured as inputs during the assertion of all resets, and they remain inputs until configured otherwise.
  - In addition, select special-function GPIO pins serve as bi-directional pins where the I/O direction is driven from the respective unit (overriding the GPIO direction register).
- A number of GPIO pins are designed to support wake functionality and currently wake capable GPIO pins need to be connected to the AON GPIO 0 controller. When a wake GPIO pin detects a rising/falling edge during standby, GPIO 0 sends an interrupt signal to the system controller unit to initiate the wake sequence for the system.

GPIO pins may have alternate input and output functions. A pin may serve either as GPIO or as an alternate function, but not as both at the same time, as described in Section 3.15.3.3, “GPIO Operation as an Alternate Function” .

3.15.1 GPIO Features

Most of the peripheral pins double as GPIO pins. This section lists the general features of the GPIO.

- As inputs, the GPIOs can be sampled or programmed to generate interrupts from either rising or falling edges.
- As outputs, the GPIOs can be individually cleared or set. They can be pre programmed to either state when entering standby.
- Each GPIO can be programmed to alternate functions, providing system flexibility.

3.15.2 GPIO Topology

For functional interfaces which use GPIO buffers, there will be connections between the functional controller, eg. I2S controller, and the GPIO controller (either 0 or 1, depending on the location of the functional interface). Inside GPIO controller, there‘s a mux on both the input and output path called Alternate Function mux, where a platform can select between different functional connections, in addition to regular GPIO functionality.

Note that this Alternate Function mux does not include Debug muxing. The control for this Alternate Function Mux is retained inside the GPIO alternate function registers which is programmed by F/W. F/W will make sure that the pins are programmed appropriately (either coming out of reset or standby) before the controllers become active.

The output signal from GPIO controller is latched inside the FLIS, and use the latch value to maintain the state of the GPIO pins even when the GPIO controller or Functional controller is powered down.

The FLIS is the logic block that contains controls for the particular I/O interface at the family level. It contains both functional and DFx logic. The main architecture of the FLIS is comprised of a functional and a DFx communication method, shared registers, and DFx logic.

Inside the GPIO controller, the output enable signal that comes from the functional controller is muxed with the GPDR (output enable when the pins are used as GPIO).

Interfaces which require several individual signals, such as I2S, require that all of the interface signals to be configured to the interface or as GPIOs. Configuration of only a subset of the signals can result in the interface working improperly.

3.15.3 Operation

The GPIO signals operate as either general-purpose I/O or as one of their alternate functions. This section describes the operation in both modes.

3.15.3.1 Wake Event Handling/Propagation

When an edge is detected on one of the wake pins, a register bit will be set in the and an interrupt will be asserted to the SCU. SCU F/W will use the platform configuration information (embedded in some header) to determine which logical subsystem the interrupt came from. SCU F/W will then look up the Wake Config Table to determine whether that subsystem is configured to be wakeable in that particular standby mode and update the Wake Status register accordingly. In most cases, SCU F/W will also propagate the event to the OSPM.

OSPM will then determine to which S0ix state the subsystem needs to go, and convey that information back to SCU F/W. SCU F/W will then proceed to reconfigure the GPIO controller's Alternate Function and wake the corresponding controller.

3.15.3.2 GPIO Glitch Filter

When in general purpose mode, input GPIO signals enter a glitch filter by default, before reaching the edge detection registers.

- The glitch filter will filter out any pulses that do not remain for three rising edges of the GPIO clock.
  - To ensure that a pulse is detected by the edge detection register, the pulse should be three clock cycles long (that is, 60 ns for a 50 MHz clock)

When an edge is detected on one of those Wake pins, a register bit will be set in the and an interrupt will be asserted to the SCU. SCU F/W will use the platform configuration information (embedded in some header) to determine which logical subsystem the interrupt came from. It will then look up the Wake Config Table to determine whether the subsystem is configured to be wakeable in that particular standby mode and updates the Wake Status register. In most cases, SCU F/W will also propagate the event to the OSPM.

OSPM will then determine which S0ix state the subsystem needs to go and conveys that information back to SCU F/W, which will then proceed to reconfigure the GPIO controller's Alternate Function and wake the corresponding controller.

3.15.3.3 GPIO Operation as an Alternate Function

GPIO pins can have as many as three alternate input and three alternate output functions. If a GPIO is used for an alternate function, then it cannot be used as a GPIO at the same time. When using an alternate function of a GPIO signal, first configure the alternate function and then enable the corresponding unit. Also, disable the unit prior to changing the alternate function signals in the GPIO control registers.

3.16 Clock Distribution

3.16.1 Clock Overview

The Intel® Atom™ Processor Z2760 contains a variable frequency, multiple clock domain, multiple power plane clocking system. Crossing between various frequency is deterministic and synchronized. The clock architecture achieves low power clocking solution and yet support various IP clocking requirement on the SOC. The architecture include clock synchronization scheme, multiple clock domain crossing. In addition, it also supports Intel® Burst Technology, which enhances processor performance. The Intel® Atom™ Processor Z2760 platform eliminates need for external clock generator.

3.16.2 Clocking Requirements Summary

The Intel® Atom™ Processor Z2760 platform makes use of 2 crystals on board as follows:

XTAL frequency	Connected to	Usage
32.768KHz	PMIC	RTC Clock Slow clock supply to external components
38.4Mhz	SOC	Generating soc internal clock sources Generating reference clock to external devices in the platform

The 32.768KHz clock is used as a sleep clock for external devices and as an RTC clock when the platform is Off.

The 38.4MHz reference clock is used by the soc to generate the various internal clock sources as well as external reference clock supply to external devices.

3.16.3 Clock Generation

There are 6 PLLs on the processor:

- The Core PLL provides the clock for the CPU.
- The HFH PLL creates clocks fo.graphics, image signal processing and memory.
- The LFH PLL filters the output of the pierce oscillator and provides a clock source mainly for the south complex logic.
- The USB PLL creates clocks for the USB HSIC and OTG interface.
- The DPLL creates clocks for the HDMI display interface and pipr2DB controller.
- DSIPLL is used to generate clocks for DSI MIPI interface.

3.16.4 Reference Clock Interface

The processor accepts a 38.4 MHz external reference clock by the crystal oscillator. At parallel resonance, the crystal behaves inductively and resonates with capacitance shunting the crystal terminals.

The processor uses the crystal in parallel resonance mode. It is important to use a crystal which has been calibrated in this mode during its manufacture. Using a crystal calibrated for series resonance will still function but will also violate the device ppm specification.

3.16.5 Features of Platform Integrated Clock Architecture

- Since the function controllers are inside the SOC, the requests and enables are also inside the SOC, coordinated by the SCU. Integrated clock control reduces clock control pin count and reduces control latency.
- Digital interfaces are less sensitive to noise, frequency and duty cycle variations facilitating higher levels of SOC integration and less power dissipated in the reduction of noise in clocks. Digital interfaces also facilitate signaling levels compatible with the SOC silicon geometry. The initial strategy for radio and audio low noise and precise analog clock requirements have been to solve locally, where interference and crosstalk can be minimized.
- Integrated clock generation saves power normally lost in maintaining clock transmission line dissipation when a central, discrete clock generator is used. Depending on waveform and voltage, propagating each clock from one chip to another across an FR-4 circuit board can cost between 7-10mW.
- New, revolutionary low power PLLs were created and incorporated into this design, consuming less than a tenth of the power of previous generation PLLs.

3.16.6 Clock Supply to Platform Components

The clocking scheme was design to support driving reference clock and sleep clock into external devices within the platform and this is in order to save non-required crystals (price, space, power).

It is strongly recommended to use the existing infrastructure and avoid usage of additional crystals.

One legitimate reason to use an additional crystal would be if a device is not satisfied with 19.2MHz (or its division). Nevertheless component selection needs to take this into consideration.

3.16.6.1 Reference Clock Supply

As said the SOC is able to generate a reference clock to external devices in the platform.

It shall be able to provide 19.2MHz and its divisions (2, 4).

Following are the clock output signals and their usage:

Table 3-43.Clock Output Signals and their Usage

Clock Output	Platform Component	Frequency	Clock request Line
OSC_CLK_OUT_0	Camera_CLK_1	19.2MHz	OSC_CLK_OUT_0
OSC_CLK_OUT_1	Camera_CLK_2	19.2MHz	OSC_CLK_OUT_1
OSC_CLK_OUT_2	Audio Codec	19.2MHz	Only SW control
OSC_CLK_OUT_3	MIPI2LVDS bridge	19.2MHz	Only SW control
USB_ULPI_REF_CLK	USB PHY	19.2MHz	Only SW control
USB_ULPI_1_REF_CLK	Optional second USB PHY / HSIC PHY	19.2MHz	Only SW control

Note: All clock outputs that have SW control and additionally OSC_CLK_OUT_0/1 are accompanied by dedicated clock request lines (OSC_CLK_CTL_0/1) that allow an external device to control them directly. This is used for devices that wake up spontaneously like the WLAN and cellular modems. Cellular Modems will use their own clocks as they don't rely on platform clocks.

The SW enables control of the clock request line and also can override and enable the clock output directly.

3.16.7 Sleep/Slow Clock Supply

The PMIC supports two sleep clock outputs, each capable of driving up to four loads. Sleep clock 1 will begin to toggle after VCC180AON is up. The sleep clocks can be disabled / enabled independently by FW.

Following are the sleep clock output signals and their usage:

Table 3-44.Sleep Clock Output Signals and their Usage

Clock Output	Platform Components	Frequency
SLPCLK1	• WLAN/BT combo • Cellular modem • GPS • USB PHY	32.768 KHz
SLPCLK2	For additional devices	32.768 KHz

3.17 Intel Legacy Block (iLB)

3.17.1 Overview

The Intel Legacy Block (iLB) is a collection of HW blocks that are critical for implementing the legacy PC platform features.

3.17.2 IOAPIC

The Intel® Atom™ Processor Z2760 supports IOAPIC interrupt controllers but not the legacy 8259. It has a virtual IOAPIC which is emulated by the SCU and the real IOAPIC on CLV iLB BLOCK. The majority of the south cluster interrupts are routed through the emulated IOAPIC. SOC devices that have much less interrupt latency requirements are recommended to use the iLB IOAPIC. The SCU firmware shall enable the provision to program the SOC device routing either via the virtual IOAPIC or via the HW IOAPCI. The processor can support HW IOAPIC utilization for only a limited number of SOC SC devices.

3.17.3 LPC Support

The Intel® Atom™ Processor Z2760 supports a limited function LPC bus which is a 1.8 V interface and requires a platform level shifter to communicate with 3.3V LPC devices.

3.17.3.1 Key Changes in LPC

- No SERIRQ support
  - Traditional keyboard controller can not be used. Need to use GPIOs to raise an interrupt
- 1.8 V operation only
- 1 Clock output (can support 2 loads)
- No DMA support (i.e. no legacy devices like Floppy, printer etc)
- No LDRQ# support
- No LPCPD# support
- Legacy like A20M#, SMI/SCI not supported

3.17.3.2 LPC Usages

LPC bus is intended for use with:

- Trusted Platform Module
- Optional Embedded Controller (However limited functionality as no SERIRQ# support) for slider keyboard and battery charging

3.17.4 High Precision Event Timer (HPET)

This function provides a set of timers that to be used by the operating system for timing events. One timer block is implemented, containing one counter and 3 timers.

The legacy HPET itself is optional, there is a duplicate standalone HPET in the SCU block if HPET is the only legacy feature needed.

3.18 System Controller Unit (SCU) Subsystem

3.18.1 SCU Subsystem Overview

The System Controller subsystem is one of the first subsystems to be functional after reset. It is expected to be ON all the time; hence, it is designed to use very low power. The System Controller subsystem is responsible for the following functionality:

- System boot including loading boot block code for the IA-32 CPU core, P-unit, and System Controller Unit code from eMMC
- System Control and Configuration Block
- Implements the OSPM based Power Management policy of peripherals connected to the SoC
- Implements Sequencer logic for power and clock gating
- Implements Message Signaled Interrupts
- Handles interrupts and wakeup events
- Receives messages from the IA-32 CPU core
- Communication with Low-Speed peripherals
- Implements Virtual RTC (copy of PMIC RTC)

3.18.1.1 External Timers

The SCU contains eight timers. These timers are external to the System Controller Core; hence, can be accessed by the IA-32 CPU processor, and also by the System Controller Core. All eight timers are completely identical, but separately programmable.

The timer module contains system level registers followed by a set of programmable registers for each timer. Each timer generates an interrupt. All eight interrupts are ORed together and sent to the System Controller core as one single external timer interrupt.

Timers count down from a programmed value and generate an interrupt when the count reaches zero. Each timer has an independent clock. Only two events can cause the timer to load its initial value:

- Timer is enabled after being reset or disabled
- Timers count to zero.

All interrupt status registers and end of interrupt registers can be accessed at any time.

Each of the timers can be in free-running mode, if needed by firmware.

3.18.1.2 Always-On Timer (AOT) Support

The SoC provides Always-On TimeStamp Counter (TSC) as well as Local APIC Timers (LAPIC). This is accomplished by providing an Always On 64-bit timer that is running off the base system clock. The SCU supports AOT by providing system wake capability upon timer expiration from the AOT block.

The AOT can trigger a request to the SCU interrupt controller. This will cause the SCU to bring the system out of any standby state (S0i1–3).

3.18.1.3 Security Engine Timers

The SCU provides three separate timers (watchdog, periodic timer, and up-time clock) for the security engine. The timers are directly accessible and controlled by the Security Engine. The SCU forwards all interrupts associated with the three timers with a single interrupt request signal to the Security Engine. The SE interrupt status register is read by the security engine in order to determine the source of the interrupt.

3.18.1.4 HPET Timer

This function provides a set of timers that to be used by the operating system for timing events. One timer block is implemented, containing one counter and 3 timers. Clock source for the HPET is the 19.2 MHz OSC clock.

3.18.2 Virtual RTC

The Virtual Real Time Clock (vRTC) module provides a date and time keeping device. The actual battery backed up date and time RTC registers are implemented in the RTC well in PMIC. This module maintains copies of the registers in the RTC well. It implements actual RTC registers as well as the RTC indexed registers. All the registers are implemented in the hardware. This set of registers can be read by any unit.

3.18.2.1 vRTC Hardware Registers

The processor will implement one set of mirror images of standard register bank for RTC. The 14 bytes of the standard bank contains the RTC time and date information along with four registers, A–D, that are used for configuration of the RTC.

All vRTC registers are accessible from both the SCU core and the IA-32 CPU processor. The registers are updated automatically every second. The update pulse is generated using a timer based on a 25 MHz clock source.

The vRTC supports both 12- and 24-hour modes.

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4 Pin States

Table 4-45.Power Plane and States for I/O Signals (Sheet 1 of 3)

Signal Name	Power Plane	During Reset	Immediately After Reset	S0iX
HDMI				
HDMI_DP[2:0], HDMI_DN[2:0], HDMI_CLKP, HDMI_CLKN	VCC330	H(20K)	H(20K)	OFF
I2C				
GP_I2C_0_SCL, GP_I2C_0_SDA, GP_I2C_2_SCL, GP_I2C_2_SDA	VCC122_180AON	H(2K)	H(2K)	H(2K)
GP_I2C_1_SCL, GP_I2C_1_SDA	VCC122_!80AON	H(910)	H(910)	H(910)
GP_I2C_3_SCL_HDMI, GP_I2C_3_SDA_HDMI	VCC122AON	H(2K)	H(2K)	H(2K)
GP_I2C_[5:4]_SCL, GP_I2C_[5:4]_SDA	VCC180AON	H(2K)	H(2K)	H(2K)
MIPI-CSI				
MCSI_X4_CLKP, MCSI_X4_CLKN, MCSI_X4_DP[3:0], MCSI_X4_DN[3:0]	VCC122AON	Input	Input	Input
MCSI_X1_CLKP, MCSI_X1_CLKN, MCSI_X1_DP, MCSI_X1_DN	VCC122AON	Input	Input	Input
MIPI-DSI				
MDSI_A_CLKP, MDSI_A_CLKN, MDSI_A_DP[3:0], MDSI_A_DN[3:0]	VCC122AON	0	0	0
Camera Side-Band				
GP_CAMERA_SB[4]	VCC180AON	H(2K)	H(2K)	Input
USB ULPI				
ULPI_0_STP, ULPI_0_CLK, ULPI_1_STP, ULPI_1_CLK, ULPI_0_REFCLK, ULPI_1_REFCLK	VCC180AON	0	0	0
ULPI_0_D[7:0], ULPI_1_D[7:0], ULPI_0_DIR, ULPI_0_NXT, ULPI_1_DIR, ULPI_1_NXT	VCC180AON	L(20K)	L(20K)	L(20K)
SD				
GP_SD_0_CD#	VCC180AON	H(20K)	H(20K)	Input
SDIO				
GP_SDIO_1_D[3:0], GP_SDIO_1_CMD, GP_SDIO_1_CLK, GP_SDIO_1_PWR	VCC180AON	H(20K)	H(20K)	H(20K)
GP_SD_0_WP	VCCSDIO	L(20K)	L(20K)	L(20K)

Table 4-45.Power Plane and States for I/O Signals (Sheet 2 of 3)

Signal Name	Power Plane	During Reset	Immediately After Reset	S0iX
eMMC				
EMMC_0_CLK, EMMC_1_CLK	VCC180AON	0	0	0
EMMC_0_D[7:0], EMMC_1_D[7:0], EMMC_0_CMD, EMMC_1_CMD	VCC180AON	H(75K)	H(75K)	H(75K)
I^2S				
I2S_2_CLK, I2S_2_FS, I2S_2_RXD	VCC122AON	H(20K)	H(20K)	H(20K)
I2S_2_TXD	VCC122AON	0	0	0
MIPI-HSI				
MHSI_CAWAKE, MHSI_CADATA, MHSI_CAFLAG, MHSI_CAREADY	VCC180AON	Input	Input	Input
MHSI_ACWAKE, MHSI_ACWAKE, MHSI_ACDATA, MHSI_ACFLAG, MHSI_ACREADY	VCC180AON	L(20K)	L(20K)	L(20K)
XDP/JTAG				
JTAG_TDO	VCC180AON	Output H (2K)	Output H (2K)	Output H (2K)
JTAG_TDI, JTAG_TMS, JTAG_TCK, JTAG_TRST#	VCC180AON	Input H (2K)	Input H (2K)	Input H (2K)
UART				
GP_UART_0_RX, GP_UART_0_CTS, GP_UART_2_TX	VCC180AON	H(20K)	H(20K)	Input
GP_UART_0_TX, GP_UART_0_RTS	VCC180AON	H(20K)	H(20K)	1
GP_UART_1_CTS, GP_UART_1_TX	VCC180AON	H(20K)	H(20K)	1
GP_UART_1_RTS	VCC180AON	H(20K)	H(20K)	0
GP_UART_1_RX, GP_UART_2_RX	VCC180AON	H(20K)	H(20K)	Input
GPIO				
GP_XDP_C0_BPM0#, GP_XDP_C0_BPM1, GP_XDP_PWRMODE1, GP_XDP_PWRMODE2, GP_AON_049#	VCC180AON	H(20K)	H(20K)	H(20K)
Clocks				
OSC_CLK, CTRL[1:0]	VCC180AON	Input	Input	Input
OSC_CLK[3:1]	VCC180AON	L(20K)	L(20K)	No Change
OSC_CLK0	VCC180AON	Output	L(20K)	No Change
PMIC Interface				
PMIC_PWRGOOD, PMIC_RESET#, SVID_CLKSYNCH, SVID_DIN	VCC122AON	Input	Input	Input
SVID_CLKOUT, SVID_DOUT	VCC122AON	0	0	0

Table 4-45.Power Plane and States for I/O Signals (Sheet 3 of 3)

Signal Name	Power Plane	During Reset	Immediately After Reset	S0iX
Thermal Management				
PROCHOT#, THERMTRIP#	VCC180AON	H(20K), OD	H(20K), OD	H(20K), OD
MISC				
IERR#	VCC180AON	L(20K)	L(20K)	0
RESETOUT#	VCC180AON	0, OD	0, OD	1, OD

NOTE: The information in this table is representative of the default configuration. The configuration settings can be modified by system firmware.

Key:

- 'H' - Buffer is Hi-Z with weak pull-up.
- 'L' - Buffer is Hi-Z with weak pull-down.
- '1' - Buffer drives V_{OH}.
- '0' - Buffer drives V_{OL}.
- 'OFF' - Buffer powered off.
- 'OD' - Open Drain.

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5 Power Management

5.1 Overview

This chapter describes overall platform power management architecture and some details on the internal control for power management transitions within the Intel® Atom™ Processor Z2760 in various modes of operation.

The various modes of operation are described and nomenclature clarified. The transitions between modes and states are also documented, including specifics on power gate configurations.

5.2 Power Management (PM) Feature Set

The Key elements of this PM architecture are:

- Well defined Operating Modes such as Internet Browsing, MP3 Playback, and Voice Call.
- OS-transparent subsystem control using Firmware/Hardware.
- Definition of multiple stand-by states within the active system state
  - — New Idle System States - S0i1 and S0i3;
  - — Device States: D0i1 and D0i3
- Fine-grain Power Management
  - — Supports Power Islands for optimum power-down of subsystems
  - — Aggressive Power and Clock gating and integrated Clocks and VR power down by means of the PMIC.

5.2.1 North Complex Features

- Display Device controls D0–D3
- GFX Device states D0, D0i3, and D3
- Video Decode/Encode states D0, D0i3, and D3
- Dynamic I/O power reductions (disabling sense amps on input buffers and tri-stating output buffers)
- Conditional Memory Self-refresh during C2–C6.
- Support for C2 popup for snoop and deferred C3/C4 based on snoop traffic.
- Separate voltage islands controlled by power switches for North Cluster, GFX, Video Decode, Video Encode, External Display, Internal Display—Power off islands in D3 and possibly in D0i3.

5.2.2 South Complex Features

- Multiple individually controllable voltage rails
  - Shutdown for platform voltage rails by means of communication with the PMIC
- Extensive clock-gating on a subsystem basis
  - Manual register level clock gating for sub client functions within a client core.
  - Auto hardware clock gating for some clients and sub clients to reduce C0 dynamic power.
  - Register-based, coarse-grain clock-gating for entire core subsystem.
- Wake event support
- Device State support
- OSPM software layer to guide power transitions per subsystem
  - Optional OSPM transparent transition from D0i1 to D0i0.
- Support for various I/O power management features
  - Support for USB Link Power Management (LPM)
  - Platform selectable I/O termination for low-speed interfaces—allows flexibility to reduce power based on peripherals of choice
- Micro-controller based Power Management Units (PMUs) to provide autonomous PM events control

5.2.3 Acronyms and Terminology

5.2.4 Nomenclature

Table 5-46.Nomenclature and Definitions (Sheet 1 of 2)

Name	Definitions
PM (Power Management) States	Power Management states typically have an alphanumeric nomenclature, where the letter and number imply specific behavior *in* hardware. Transitions between states are highly controlled sequences, generally requested by software or firmware, though exceptions do exist where hardware makes the request (that is, D0i1 or L0s on PCI-express). Examples: Core States (C-States): C0 through C6 System States: S0, S0i1 and S0i3 Device States: D0, D0i1, D0i3, and D3 Link States: L0s A given hardware state may support several types of modes under one state
Mode (Also known as “operating mode”)	A mode has a much more flexible definition, dictated by the OS and a Policy Manager, in order to perform a specific task in a power-optimized manner. Alternately, “mode” may also be an abstracted term that can actually comprise multiple states, such as various “system idle” states. Examples: “AOAC Stand-by” mode may map to S0i1 depending on OS decision, or “Sleep” may map to S0i3 depending on OS decision.

Table 5-46.Nomenclature and Definitions (Sheet 2 of 2)

Name	Definitions
Usage (Also known as "usage model")	Typically, a usage involves a real-world description of a production device operated by an end-user. This involves a mixture of modes and states at the low level, with a higher level description, such as: • Keep browser active during Cellular or VOIP call • Allow GPS during browsing • Maintain last browser context, but do not allow browsing during Voice call • Usage models are not explicitly validated pre-silicon, although their fundamental states and modes may receive coverage. Validation must be done post-silicon with a real operating system and policy manager. • Usage powers are typically estimated using residencies in various modes, plus energy cost of mode transitions.
Profiles	Profiles are a usage or scenario, but with an accompanying time line that describes the dwell times and transition ramps between the various modes. These are useful for power delivery analysis to ensure we can support all mode switches. The usages involved in profiling are often theoretical or hypothetical, and don't have to be attached to a specific end-user model. Example: System is in a fairly idle state, with graphics disabled, and needs to switch to 3-D graphics mode. The system takes X nanoseconds to un-powergate the graphics engine to its leakage power, Y nanoseconds to enable clocks for idle power, and Z nanoseconds to fill the graphics pipeline for fully active power.

5.3 System Power Management Overview

5.3.1 System States

While S0 refers to the fully active system state—subsets of S0, called S0iX exist to extend the active state into "Idle" states called "Active Stand-by", "Stand-by", or "Sleep". The following table describes these states. A detailed description is available in the OSPM section.

Table 5-47.Standby States

State	Definition
S0	System Active The processor may be transitioning freely in and out of C-states.
S0i1	"Stand-by", "AOAC Stand-by", "Active Stand-by" Used during periods of audio playback while the user is not actively using the device.
S0i3	"Sleep", "Deep Sleep" Used when the user is not actively using the device. The processor in C6 (retained in shared SRAM). Sleep mode, always connected Able to wake from user or platform

Note: The processor does not support ACPI System Sleep states S1 or S3 in favor of the above lower wake latency S0iX states.

5.3.2 Device States

ACPI standards defined the concept of Device States using "Dx":

- D0 is active, and allows for active power management of the device.
- D3 is per the ACPI industry specification. The device is effectively powered off, however in D3_HOT some logic is powered so as to support detection and generation of wake events.

Device D-States are managed through the PCI configuration space. As only the devices located in the North Complex are PCI compliant—only those devices support Device D-States.

5.3.2.1 D0ix States

The subset states of D0 are defined only within the context of the processor and are not part of the ACPI standard.

Table 5-48 describes Device Idle States within D0.

Table 5-48.Device States—D0ix

State	Description
D0i0	Dynamic power not managed by system Individual device(s) can do transparent local clock and power gating.
D0i1	Transparent Dynamic clock gating
D0i2	Transparent and dynamic power gating Local state retention
D0i3	Driver managed clock and power gating – OS transparent Exit latency is managed by the driver.
D1/D2	OS aware low power states
D3	Fully off

5.3.2.2 Supported States by Subsystem

Table 5-49.Supported States by Subsystem (North Complex)

SubSystem	Supported States
Processor Cores	C0 – C6
Memory	D0, Active Power Down, Idle Power Down, Deep Power Down, Self Refresh
Graphics	D0 – D0i3
Video Encode	D0 – D0i3
Video Decode	D0 – D0i3

Table 5-49. Supported States by Subsystem (North Complex)

Display/MIPI	D0 – D3
External Display	D0, D3
ISP	D0, D0i0, and D3

Table 5-50. Supported States by Subsystem (South Complex)

Subsystem	Supported States
SD Controller (SD port 0)	D0, D0i0, D0i1, D0i2, D0i3 and D3
SDIO Controller—SDIO port 1 and port 2 (SDIO1/2)	D0, D0i0, D0i1, D0i2, D0i3 and D3
Security Engine	D0, D0i0, D0i1, D0i2, D0i3 and D3
USB[1]	D0, D0i0, D0i1, D0i2, D0i3 and D3
Audio Engine	D0, D0i0, D0i1, D0i2, D0i3 and D3
GPIO Core	D0, D0i0, D0i1, D0i2, D0i3 and D3
Shared SRAM	D0, D0i0, D0i1, D0i2, D0i3 and D3

1. Hardware automated LPM is not supported for USB.

5.3.3 Processor State Control (C-States)

The following is a high-level overview of the C-States that are supported:

- C1 is transparent to the North Complex
- C2 is entered when the core processor reads the P_BLK LVL2 register or receives MWAIT instruction hint to C2.
  - — or from C3/C4 if bus masters require snoops
- C4 is entered when the core processor reads the P_BLK LVL4 register or receives MWAIT instruction hint to C4.
  - — or after a return to C2 from a prior C4 state
- C6 is entered when the core processor reads the P_BLK LVL6 register or receives MWAIT instruction hint to C6.

The C-State ends when a break event occurs. Based on the break event, the processor returns the system to C0. The following are examples of such break events:

- Any unmasked interrupt goes active
- Any internal event that will cause an NMI
- Processor Pending Break Event (PBE#)

When in a C-State the processor may optionally gather interrupts and ACPI timer ticks to keep the core processor in the C-State for longer periods of time.

Table 5-51.Subsystem to C-State Mapping

Subsystem	C0/C1	C2	C4/C6
Graphics	On (Optionally Disabled)	Off/Power Gated	
Video Encode	On (Optionally Disabled)	Off/Power Gated	
Video Decode	On (Optionally Disabled)	Off/Power Gated	
Display	On (Optionally Disabled)	Off/Power Gated	
Memory	On (with power saving features)	Dynamic Self Refresh	

5.3.3.1 C0 State—Full On

This is the only state that runs software. All clocks are running and the core processor is active. The core processor services snoops and maintains cache coherency in this state. All power management for interfaces, clock gating, and so on are controlled at the unit level.

5.3.3.2 C1 State—Auto-Halt

The first level of power reduction occurs when the core processor executes an Auto-Halt instruction. This stops the execution of the instruction stream and greatly reduces the core processors power consumption. The core processor can service snoops and maintain cache coherency in this state. The North Complex logic does not distinguish C1 from C0 explicitly.

5.3.3.3 C4 State—Deeper Sleep

In this state, the core processor shuts down its PLL and cannot handle snoop requests. The core processor voltage regulator is also told to reduce the processor's voltage. During the C4 state, the North Complex will continue to handle traffic to memory so long as this traffic does not require a snoop (that is, no coherent traffic requests serviced).

C4 is entered by receiving a C4 request from the core processor/OS. The exit from C4 occurs when the North Complex detects a snoopable event or a break event, which would cause it to wake up the core processor and initiate the C0 sequence.

5.3.3.4 C4E State

The C4E state is essentially the same as C4 except that the core processor will transition to the Low Frequency Mode (LFM) frequency and voltage at entry and exit of this state.

5.3.3.5 C6 State

Prior to entering C6, the core processor will flush its cache and save its core context to a special on-die SRAM on a different power plane. Once the C6 entry sequence has completed, the core processor's voltage can be completely shut off.

The key difference for the North Complex logic between C4 and C6 is that since the core processor's cache is empty, there is no need to perform snoops on the internal FSB. This means that bus master events (which would cause popup from C4 to C2) can be allowed to flow unimpeded during C6. However, the core processor must still be returned to C0 in order to service interrupts.

A residency counter is read by the core processor to enable an intelligent promotion/demotion based on energy awareness of transitions and history of residencies/transitions.

Table 5-52.C-states

C-state	CPU core status	Cache status
C0 (HFM)	Normal operation	Normal operation
C0 (LFM)	Normal operation	Normal operation
C1	Both threads HALTed; Most clocks OFF	No cache flushed; Snoops wake up core
C1E	C1 + Freq, VID @ LFM	No cache flushed; Snoops wake up core @ MIN
C2	Similar to C1; North Complex blocks interrupts	No cache flushed; Snoops wake up core
C2E	Similar to C1E; North Complex blocks interrupts	No cache flushed; Snoops wake up core @ MIN
C4	C2 + PLLs OFF + VID = cache retention Vcc	Core’s D optionally flushed Some L2 ways flushed (L2 shrink)
C6	C2 + PLL OFF + VID = C6 powerdown Vcc (or Powergate)	Core D and L2 flushed + Cache power down

5.4 Power Rails and Domains

5.4.1 Overview

The SoC has many power rails to support high integration of high and low speed logic, and voltages required for industry standard peripherals. All voltage rails are provided by the accompanying PMIC chip. Some voltages have multiple versions that can be switched on or off at different times to support power management.

Additionally, the SoC supports much finer granularity of electrically isolated power rails that will be shorted in a production system board. These are isolated either for independent electrical analysis/observation, or independent power measurement.

5.4.2 Power Rails

5.4.2.1 Power Rail Type

This section defines the power state and power level options.

Type	Description
F	**Fixed:** Voltage level is fixed to be a certain value.
S	**Selectable:** Voltage can be selected at the platform level, but are static during normal operation.
V	**Variable:** Variable supplies are negotiable supply levels and can change during operation.

5.4.2.2 Power Rail Descriptions

This section describes the power signals and power states of each power signal.

Table 5-53.Power Rails

System Rail Name	Type	Voltage	Power for:
VCC	V	0.3–1.2 V	Core processor
VCC108AON	F	1.08 V	SRAM in AON domain
VCC108AS	F	1.08 V	power SRAM - for MP3 playback
VCC108	F	1.08 V	L2 and SRAMs for entire chip
VNNAON	V	0.75–1.1 V	SCU Block
VNN	V	0.75–1.1 V	Non-processor logic
VCCA100	F	1.05 V	CPU PLL, HF PLL, Display PLL, DSI PLL, USB PLL, CPU DTS, SoC DTS
VCCA100AS	F	1.05 V	LF PLL, HDMI Vref
VCC122AON	F	1.25 V	LPDDR2 I/O (Memory and SoC), PMIC Control; SPI (Port0, PMIC); SVID, I2S_2; Thermal control, HDMI DDC (I2C-3); MIPI DSI and CSI
VDD1	S	1.8 V	LPDDR2
VDD2	S	1.25 V	LPDDR2 core
VCC122_180AON (Selectable Voltage GPIOs)	S	1.25 or 1.8 V	I^2C Ports (0:2); SPI (1)
VCC180AON	F	1.8 V	USB ULPI, SPI (2/3); COMMs Interrupts; HS UART x3; Keyboard/GPIO; I^2S (0:1); JTAG; eMMC_CMD; Camera SB; I^2C (4:5); SDIO (1:2); GPIO/PTI; Dedicated GPIOs; eMMC
VCC330	F	3.3 V	HDMI 1.3a Data Interface
VCCSDIO	V	2.85	SDIO/MMC External Port

5.4.3 Internal Power Rails and Domains

The Intel® Atom™ Processor Z2760 supports independent external and derived or switched internal power domains:

- Power islands - in order to minimize leakage when functional cores are not required.
- These power islands allow the OSPM to shut off power to unused functions to reduce leakage for these gates to virtually nothing for internal switched power domains by putting a particular subsystem into a D0i3 state.
- Two primary internal rails run all of its core logic. The VNN family (VNN, and VNNAON).
- The VCC108, VCC108AS, VCC108AON are the 1.08 V supply used by the SRAM arrays.
- All subsystem supports clock gating.I/O domains are not power gated

5.4.3.1 S0i1

In S0i1, the processor core is powered down, and state is retained locally on CPU core SRAM. Additionally, the VNN rail is left powered.

5.4.3.2 S0i3

In S0i3, the VNN, VCC108 for SRAM and VCC108AS rail is shut down, CPU core SRAM contents are saved in system shared SRAM. The P-unit and North Complex state is restored from shared SRAM. In S0i3, SCU is looking for edge or level detection for wake events. Upon receiving a wake, SCU communicates with the PMIC to bring up voltage rails, and restore code from shared SRAM.

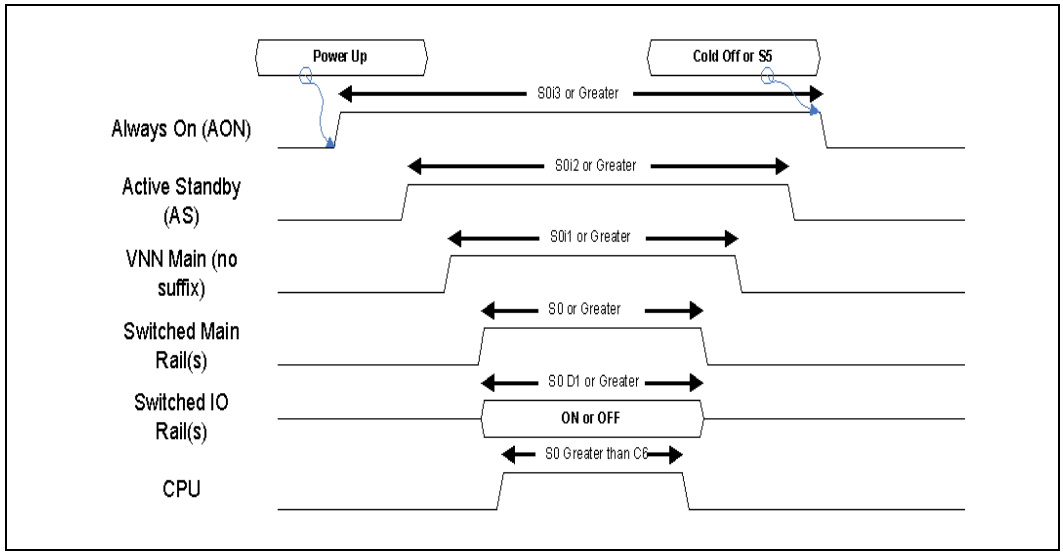
5.5 Domain Sequencing Requirements

There are two levels of sequencing: by domain, and by voltage. Generally, a whole domain is switched or remain on/off for a given system power state. Within a domain, a specific voltage ordering is honored in the same manner as in the initial default sequence. The order of initial power-up by domain is:

1. Always-On Domain (AON suffix)
2. Active Standby Domain (AS suffix)
3. VNN Main
4. Switched Main Domain
5. Switched I/O and Platform Rails
6. CPU VCC

The active period of a higher priority domain must always fully envelop all lower priority domains. That means that a lower priority domain on while a higher priority is off is NOT allowed.

Figure 5-13.Voltage Domain Waveform

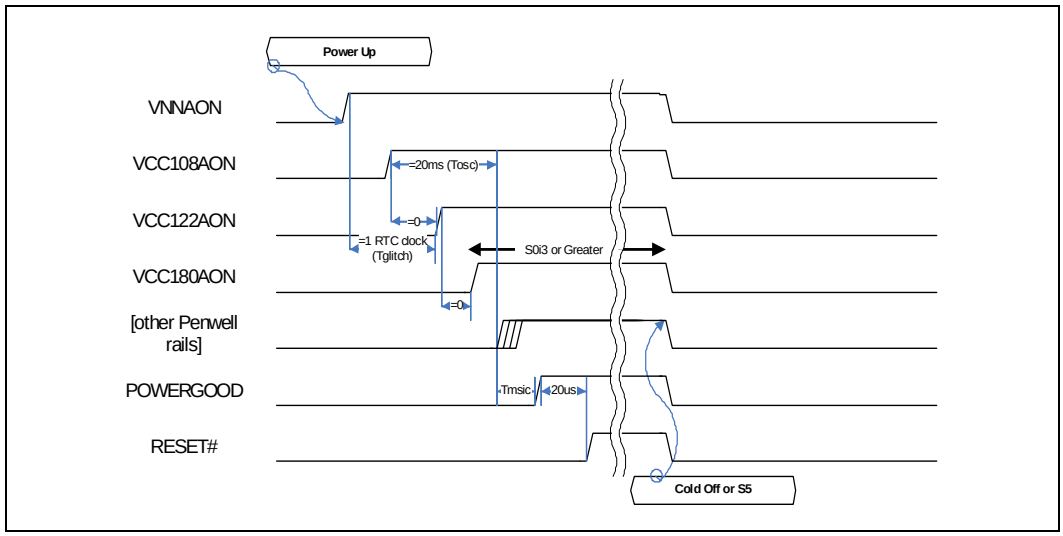


Note: Within a given domain with multiple supplies, they should come up in the same order every time.

5.5.1 Always-On (AON) Domain Sequencing

Within the SoC, it must receive its rails in an order to prevent glitching and indeterminism on all I/Os. Since core logic powers up deterministically and is isolated from exposure outside the silicon—then bringing it up first will ensure that as I/O voltages ramp, the buffers are programmed in the reset defaults driven by the core. Additionally, in staged buffers, such as 1.8 V I/Os, the pre-driver rail must be alive before the outermost driver to allow the core signals to propagate to the driver. Figure 5-14 illustrates the SoC view of the Always-On rail.

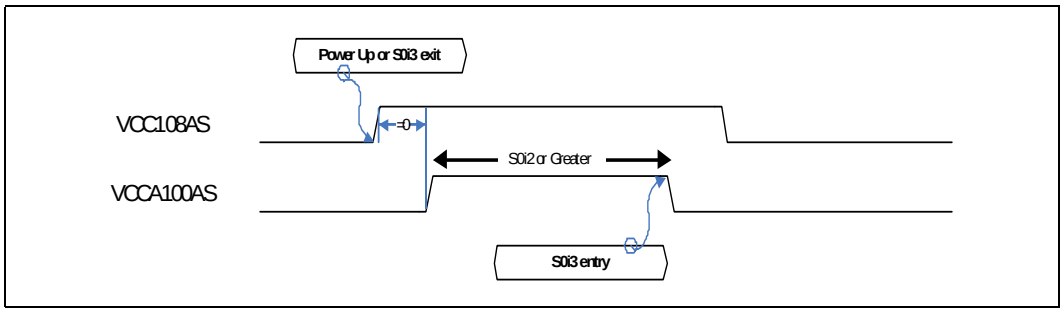
Figure 5-14.Always-On Voltage Sequencing



5.5.2 Active Standby (AS) Domain Sequencing

The Active Standby domain does not include any I/Os, so there is no determinism dependency. However, not all Active-Standby modes require the PLL, so VCC108AS must be a super set of VCCA100AS in order to support the PLL remaining off. Therefore, the low-to-high ordering is not necessarily followed here.

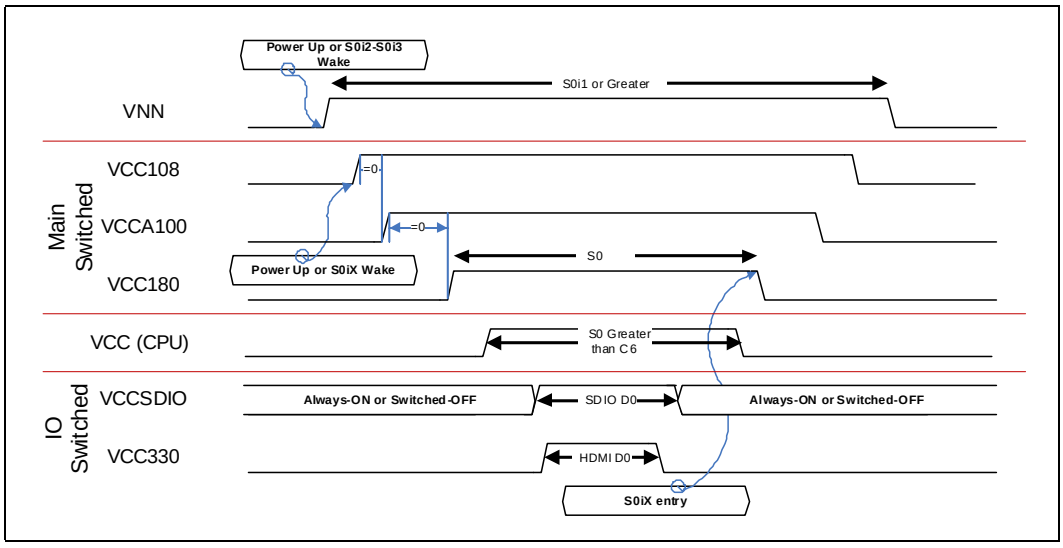
Figure 5-15.Active-Standby Voltage Sequencing



5.5.3 Main Domain Sequencing

There are a few categories within the main group. The VNN rail remains on in S0i1, although highly power gated, in order to retain processor and North Complex context in registers. The "main switched" group is needed for all S0 time. The CPU VCC is managed dynamically within S0. The "I/O switched" group includes VCCSDIO and VCC330 only when those devices specifically need to be brought to their functional state (D0). Additionally, other platform rails may be needed for external devices.

Figure 5-16.Main Voltage Sequencing



5.6 Operating System Power Management (OSPM)

The primary function of the Operating System Power Management (OSPM) is to efficiently manage power by controlling platform and subsystem power states.

- OSPM uses the concept of modes in order to determine the most power efficient state for the platform at any given point in time.
- A mode represents a comprehensive power model of the platform which provides access to all the resources required to support a specific usage model.
- Subsystems which are not explicitly required for a given usage model and the associated mode are placed in a low power mode.
- The System Controller Unit (SCU or PMU) which resides in the hardware, and has inherent knowledge of the subsystem PM capabilities, constraints, and implementation, will direct subsystem specific actions to implement a specific state.

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6 Thermal Management

The SoC contains many techniques to help better manage thermal attributes of the device. Similar to the Intel Core processor, it implements Intel® Thermal Monitor (thermal based clock throttling) and Intel Thermal Monitor 2 (thermal-based Enhanced Intel SpeedStep® Technology transitions).

6.1 On-Die Digital Thermal Sensor (DTS)

The processor contains three on-die Digital Thermal Sensors (DTS) that can be read by means of an MSR (no I/O interface). One Digital Thermal Sensor is located within each processor core and one is located on the die outside the processor cores. The digital sensors are the preferred method of reading the processor die temperature since they can be located much closer to the hottest portions of the die and can thus more accurately track the die temperature and potential activation of processor throttling by means of the Intel® Thermal Monitor.

6.1.1 Reading the Digital Thermal Sensor

Unlike traditional thermal devices, the Digital Thermal Sensor will output a temperature **relative** to the maximum supported operating temperature of the processor (Tjmax).

- It is the responsibility of software, most likely system BIOS, to convert the relative temperature to an absolute temperature, then return the absolute temperature to the operating system.
- The temperature returned by the Digital Thermal Sensor will always be at or below Tjmax; over temperature conditions are detectable by means of an Out Of Specification Status Bit. When this bit is set, the processor is operating out of specification and immediate shutdown of the system should occur if thermal throttling does not help.
- System BIOS should detect that this bit is set and inform the operating system that a critical shutdown is warranted. The processor operation and code execution is not assured once the activation of the Out of Specification Status Bit is set.

Changes to the temperature can be detected by means of two thresholds, one set above and another below the current temperature. These thresholds have the capability of generating interrupts by means of the thread’s local APIC which software must then service. It is important to note that the local APIC entries used by these interrupts are the same ones used by the Intel® Thermal Monitor and it is up to software to determine the cause of the interrupt, whether it be the Digital Sensor or Thermal Monitor.

6.2 Intel® Thermal Monitor

Intel® Thermal Monitor helps in controlling the processor temperature by activating the thermal control circuit (TCC) or PROCHOT# when the processor reaches its maximum operating temperature. There are two modes of operation for TCC: automatic and on-demand. There are two Automatic modes called Intel® Thermal Monitor 1 (TM1) and Intel® Thermal Monitor 2 (TM2). These are selected by writing into MSR registers. TCC will be activated only when the internal die temperature reaches maximum allowed value of operation. Its recommended to enable TM1/TM2and Enhanced Intel Speed step technology in the platform BIOS.

6.2.1 PROCHOT# Functionality

PROCHOT# will be asserted when the SoC temperature monitoring sensor detects that the SoC has reached its maximum safe operating temperature (approximately 90°C).

Once PROCHOT# is asserted. the SoC will start to throttle to lower frequency and lower core voltage in order to reduce the SoC's temperature. This can also be asserted externally (on-demand) to throttle the two CPU cores and/or the GFX core(s) in the SoC. By default, when PROCHOT# is asserted on the IA cores or the North Complex, IA cores are always throttled down to LFM (TM2 action). Also, TM2 throttling can be disabled in the BIOS.

6.2.2 Bi-Directional PROCHOT# Functionality

Bi-directional PROCHOT# is a feature that needs to be enabled by software. When PROCHOT# is driven by an external agent, it enables activation of either the TCC (Thermal Control Circuitry) or Enhanced TCC.

System State	Core State	PROCHOT# (Bidirectional)			THERMTRIP# (Output)
		Input		Output	
		Core	N Complex		
S0	C0	Supported	Optional	Active	Active
	C1/C1E	Supported	Optional	Active	Active
	C2/C2E	Supported[1]	Optional	Active	Active
	C4/C4E	Ignored	Optional	Active (NC only)	Active (NC only)
	C6	Ignored	Optional	Active (NC only)	Active (NC only)
S0i1	C6	Ignored	Ignored	Inactive	Inactive
S0i3	C6	Ignored	Ignored	Inactive	Inactive

1 PROCHOT# assertion is recognized during C2, but the CPU Core does not react to it until it has entered C0 due to a different interrupt/event.

6.2.3 On Demand Mode

In addition to the Intel® Thermal Monitor and the Bi-directional PROCHOT#, the thermal control circuitry that enables processor clock modulation can be enabled in software by writing to the IA32_CLOCK_MODULATION Model Specific Register, which is replicated per thread and the hardware resolves different programmed duty cycles by picking the one with highest performance.

6.2.4 THERMTRIP# Functionality

Logic in the SoC asserts the THERMTRIP# output pin when any of the DTS reach critical temperatures. It is expected that when the PMIC observes THERMTRIP# asserted, it will immediately turn off all internal voltage regulators and power switches, and disable all PMIC-attached/controlled discrete voltage regulators and power switches.

6.3 External Thermal Sensors

In addition to the thermal sensors located on the die itself, the SoC could have access to system thermal sensors external to the SoC. These additional thermal sensors could be located on external system components and accessed through the I^2C sensor network to provide additional thermal data in the system.

6.3.1 DRAM Thermal Sensor

The Intel® Atom™ Processor Z2760 is connected (via the DRAM bus) to a temperature-sensing capability located in each DRAM die in the DRAM memory chip stack(s) mounted on the device package. The MR4 register on each DRAM die defines the refresh rate timing required by that die to maintain information in memory, based on an on-die temperature sensor. Consequently, the DRAM's MR4 register "refresh rate request" content provides a rough indication of the DRAM die temperature.

6.3.2 PMIC Thermal Sensors

The SCU FW has access to thermal sensors accessible through the PMIC.

- PMIC internal temperature.
- System Battery temperature.
- PMIC-attached thermistors for system/skin temperatures.

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7 Absolute Maximums and Operating Conditions

7.1 SoC Storage Specifications

Table 7-54, includes a list of the specification for device storage in terms of maximum and minimum temperatures and relative humidity. These conditions should not be exceeded in storage or transportation.

Table 7-54.Storage Conditions

Parameter	Description	Minimum	Maximum	Notes
$T_{ABSOLUTE\ STORAGE}$	The non-operating device storage temperature. Damage (latent or otherwise) may occur when subjected to for any length of time.	-55 °C	125 °C	1, 2, 3
$T_{SUSTAINED\ STORAGE}$	The ambient storage temperature limit (in shipping media) for a sustained period of time.	-5 °C	40 °C	4, 5
$RH_{SUSTAINED\ STORAGE}$	The maximum device storage relative humidity for a sustained period of time.	60% @ 24 °C		5, 6
$TIME_{SUSTAINED\ STORAGE}$	A prolonged or extended period of time; typically associated with customer shelf life.	0 Months	6 Months	6

NOTES:

1. Refers to a component device that is not assembled in a board or socket that is not to be electrically connected to a voltage reference or I/O signal.
2. Specified temperatures are based on the data collected. Exceptions for surface mount reflow are specified in the applicable JEDEC standard and MAS documents. Non-adherence may affect processor reliability.
3. $T_{ABSOLUTE\ STORAGE}$ applies to the unassembled component only and does not apply to the shipping media, moisture barrier bags, or desiccant.
4. Intel® branded board products are certified to meet the following temperature and humidity limits that are given as an example only (Non-Operating Temperature Limit: -40 °C to 70 °C, Humidity: 50–90% non-condensing with a maximum wet bulb of 28 °C). Post board attach storage temperature limits are not specified for non-Intel branded boards.
5. The JDEC, J-JSTD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.
6. Nominal temperature and humidity conditions and durations are given and tested within the constraints imposed by $T_{SUSTAINED}$ and customer shelf life in applicable Intel boxes and bags.

Table 7-55.Thermal Characteristics

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
$T_{Junction}$	Die Junction Operating Temperature	0		90	ºC	1, 2
Θ_{JB}	Thermal resistance from junction to Board (JB)		8.6		°C/W	
$\Psi_{J\text{-}DBF}$	Thermal resistance from junction to die back side film (DBF)		1.1		°C/W	

NOTES:
1. PROCHOT# will be asserted when the SoC temperature monitoring sensor detects that the SoC has reached its maximum safe operating temperature. Once PROCHOT# is asserted SoC will start to throttle to lower frequency and lower core voltage thus to reduce system temperature.
2. THERMTRIP# (Catastrophic Thermal Trip) will be asserted to protect the SoC from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The SoC stops all execution when THERMTRIP# is asserted, this would happen when the junction temperature reaches a potentially catastrophic temperature.

7.2 Absolute Minimum and Maximum for each Power Rail

Table 7-56.Absolute Minimum and Maximum Voltage

System Rail Name	Type	Nominal Voltage (V)	Absolute Minimum Voltage	Absolute Maximum Voltage
VCC	V	0.3–1.2	-0.3	1.3
VCC108AON	F	1.08	-0.3	1.13
VCC108AS	F	1.08	-0.3	1.13
VCC108	F	1.08	-0.3	1.13
VNNAON	V	0.75–1.1	-0.3	1.3
VNN	V	0.75–1.1	-0.3	1.3
VCCA100	F	1.05	-0.3	1.076
VCCA100AS	F	1.05	-0.3	1.076
VCC122AON	F	1.25	-0.3	1.3
VDD1	S	1.8	-0.3	2.4
VDD2	S	1.2	NA	NA
VCC122_180AON (Selectable Voltage GPIOs)	S	1.2 or 1.8	-0.3	1.3/2.4
VCC180AON	F	1.8	-0.3	2.4
VCC330	F	3.3	-0.3	4
VCCSDIO	V	2.85	-0.3	4

NOTE: At conditions outside nominal operation limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to

conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits. If the component is exposed to conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function, or its reliability will be severely degraded. Although the device contains protective circuitry to resist damage from electro-static discharge, precautions should always be taken to avoid high static voltages or electric fields.

7.3 Electrostatic Discharge (ESD) Specification

Table 7-57.ESD Performance

Models	Passing Voltages
Human Body Model (HBM)	+/- 2 KV
Charged Device Model (CDM)	+/- 500 V

NOTE: Passing voltage applies to all signal and power pins.

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8 Electrical Specifications

8.1 Input/Output Clock Timing

8.1.1 38.4 MHz Input Crystal Clock

The SoC requires an external 38.4 MHz crystal in parallel resonance mode.

Table 8-58.38.4 MHz Crystal Input (OSCIN/OSCOUT)

Symbol	Parameter	Min.	Max.	Units	Notes
$OSC_{Accuracy}$	Parts-per-million of the crystal frequency	–	30	ppm	
OSC_IN C_{IN}	Input Pin Capacitance	1.5	5	pF	
C_{XTAL}	Crystal Pin Capacitance	3	5	pF	
OSC_OUTC_{OUT}	Output Pin Capacitance	–	6	pF	
L_{PIN}	Pin Inductance	–	7	nH	

8.1.2 Crystal Recommendation

Table 8-59.38.4 MHz Crystal Recommendation

Parameter	Min.	Typ.	Max.	Units	Notes
Frequency	–	38.4	–	MHz	
Cut	–	AT	–	n/a	
Loading	–	Parallel	–	n/a	
Load capacitance (CL)	–	–	12	pF	2
Drive Maximum	–	–	100	µW	
Shunt Capacitance (C0)	–	0.5	1.0	pf	
Series Resistance	–	–	80	Ω	1
Cut Accuracy Maximum	–	±35	–	ppm	
Temperature Stability Maximum (0–50 °C)	–	±30	–	ppm	
Aging Maximum	–	±3	–	ppm 1st year	
Q (Quality Factor)	130K	–	–	–	1

NOTES:.
1. ESR value can be ignored if Q factor specification is met
2. Max Circuit capacitance of 7 pF from crystal to OSCIN/OSCOUT pins of SoC, based on max trace length of 9mm and board impedance of 40 - 70 Ohm. If wider trace is considered the total length should be reduced.

8.2 19.2 MHz OSC Clock Output Specification

Table 8-60.19.2 MHz OSC_Clock Output

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes	Figure
	Frequency		19.2		MHz	2, 4	
T_{RISE} / T_{FALL}	Rise and Fall Time	5	–	20	ns	1,3	
Duty Cycle	Duty Cycle	45	–	55	%	2	
C2C-J	Cycle to cycle Jitter (Peak)	–	–	±300	ps	2,5	8.2
PJ	Period Jitter (peak to peak)	–	–	550	ps	2,6	8.2,8.3
TIE	Time period Interval (peak to peak)	–	–	400	ps	7	8.3
	Long Term Accuracy	–	–	±100	ppm		

NOTES:

1. Edge Rate is measured from 10%–90% of 1.8 V supply
2. Frequency, Duty Cycle and clock jitter are measured with respect to 50% of the 1.8 V supply.Duty cycle, Jitter(C2C-J and PJ) are measured across 100K cycles.
3. Based on trace length of 25–200 mm, Far End Load of 2–5 pF, ESD of 10 pF, and board impedance of 30–75 Ω.
4. Divide by 2 (to achieve frequency of 9.6 MHz) and Divide by 4 (to achieve frequency of 4.8 MHz) options available. these will be captured in future revision of Platform Firmware Architecture Specification (FAS) for more details.
5. Cycle to Cycle jitter represents how much the clock period changes between any two adjacent cycles. It can be found by applying a first-order difference operation to the period jitter, as shown by C2 and C3 in Figure.The peak cycle-to-cycle jitter is the maximum of the absolute values of these samples, taken over 100K cycles.
6. Period jitter value is measured by adjusting an oscilloscope to display a little more than one complete clock cycle with the display set to infinite persistence. Scope trigger is set on the first edge, and the period jitter is captured by measuring spread/peak-peak value of the second edge.
7. The TIE is estimated by measuring how far each active edge of the clock varies from its ideal position and is measured across for 100K cycles.

Figure 8-17.Clock Jitter Definitions

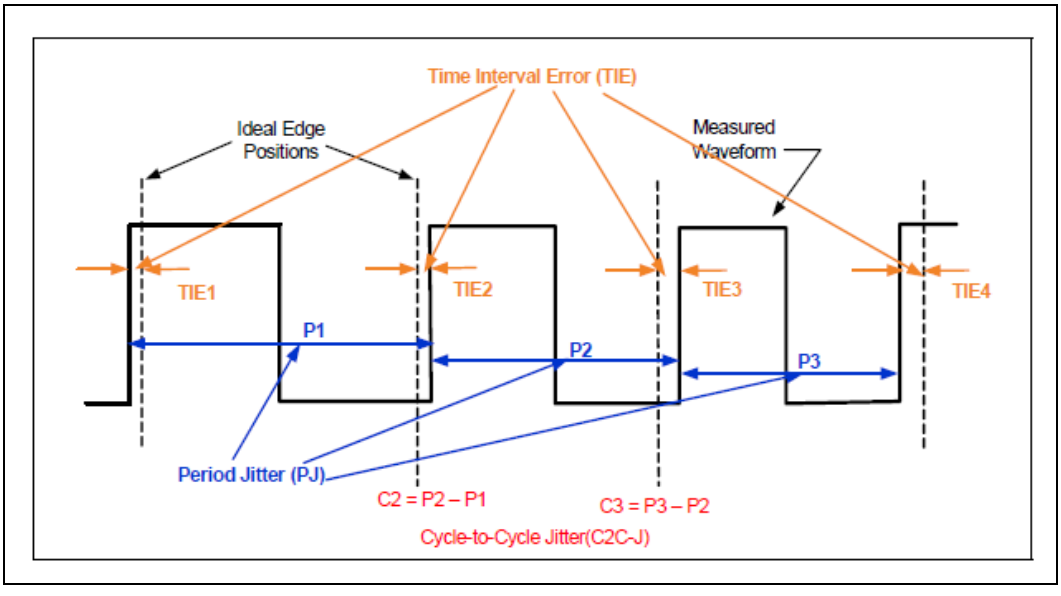
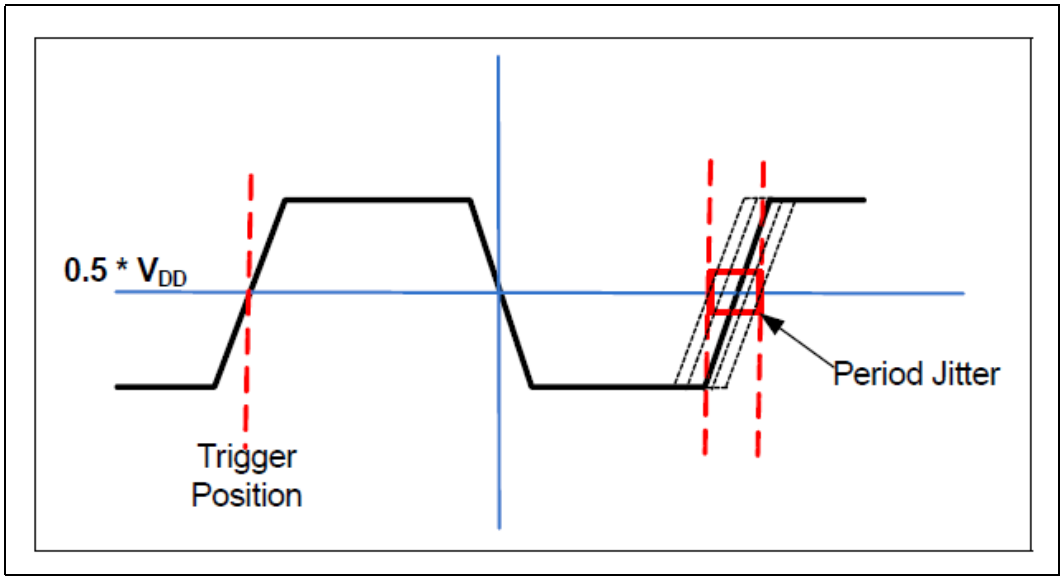


Figure 8-18.Period Jitter Measurement Methodology



8.2.1 ULPI REFCLK (19.2 MHz) Output Specification

Table 8-61.ULPI REFCLK (19.2 MHz) Output Specification

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
	Frequency		19.2		MHz	2
T_{RISE} / T_{FALL}	Rise and Fall time	2	–	10	ns	1,3
Duty Cycle	Duty Cycle	45	–	55	%	2
	Long Term Accuracy	–	–	±100	ppm	

NOTES:
1. Edge Rate is measured from 10%–90% of 1.8 V supply
2. Frequency and duty cycle are measured with respect to 50% of the 1.8 V supply.
3. Based on trace length of 25–200 mm, Far End Load of 2–5 pF, and board impedance of 30–75 Ω.

Table 8-62.ULPI REFCLK (19.2 MHz) Output Jitter Specification (Sheet 1 of 2)

Offset Frequency Band	Maximum Phase Jitter in Frequency Offset Band as Measured With Averaging and 1% Smoothing	Maximum Phase Jitter in Frequency Offset Band as Measured With Averaging And No Smoothing	Units
1–10 Hz	330	–	ps rms
10–100 Hz	90	–	ps rms
0.1–1 KHz	30	–	ps rms
1–10 KHz	8	–	ps rms
10–100 KHz	7	–	ps rms

Table 8-62.ULPI REFCLK (19.2 MHz) Output Jitter Specification (Sheet 2 of 2)

Offset Frequency Band	Maximum Phase Jitter in Frequency Offset Band as Measured With Averaging and 1% Smoothing	Maximum Phase Jitter in Frequency Offset Band as Measured With Averaging And No Smoothing	Units
0.1–0.5 MHz	40	400	ps rms
0.5–1 MHz	500	400	ps rms
Total Integrated Jitter	600	–	ps rms

8.3 LPDDR2 Electrical Characteristics

Table 8-63.Recommended LPDDR2-S4 AC/DC Operating Conditions

Symbol	LPDDR2-S4B [1]			LPDDR2 Usage	Unit	Notes
	Min.	Typ.	Max.			
VDD1	1.7	1.8	1.95	Core Power1	V	
VDD2	1.14	1.25	1.3	Core Power2	V	1,2
VDDCA	1.14	1.25	1.3	Input Buffer Power	V	1,2
VDDQ	1.14	1.25	1.3	I/O Buffer Power	V	1,2

NOTES:
1. VDDCA and VDDQ are derived from VCC122AON Rail. VCC122AON Rail from the PMIC is supposed to have tolerance of +3% -5% of typical voltage
2. Typical voltage for VDD2 (for S4B device), VDDCA and VDDO deviates from LPDDR2 JEDEC specification which is specified at 1.2V, though the min and max align with the LPDDR2 JEDEC specification.

Table 8-64.Single Ended AC and DC Input Levels for CA and CS_n Inputs

Symbol	Parameter	Minimum	Maximum	Unit	Notes
VIHCA(AC)	AC input logic high	Vref + 0.220	See Note 2	V	1, 2
VILCA(AC)	AC input logic low	Note 2	Vref - 0.220	V	1, 2
VIHCA(DC)	DC input logic high	Vref + 0.130	1.33	V	1,5
VILCA(DC)	DC input logic low	-0.0085	Vref - 0.130	V	1,6
VRefCA(DC)	Reference Voltage for CA and CS_n inputs	0.49 * VDDCA	0.51 * VDDCA	V	3, 4

NOTES:
1. For CA and CS_n input only pins. Vref = VrefCA(DC).
2. See Table 8-72, "AC Overshoot/Undershoot Specification" on page 118.
3. The AC peak noise on VRefCA may not allow VRefCA to deviate from VRefCA(DC) by more than +/-1% VDDCA (for reference: approximately +/- 12mV).
4. For reference: approximately. VDDCA/2 +/- 12mV
5. Deviates from LPDDR2 JEDEC specification, which has maximum VIHCA(DC) =VDDCA =1.3V. Intel has obtained waivers from majority of LPDDR2 Memory Vendors for this violation. To get more information about this waiver please contact your Intel Representative.
6. Deviates from LPDDR2 JEDEC specification, which has minimum VILCA(DC) =VSSCA =0V. Intel has obtained waivers from majority of LPDDR2 Memory Vendors for this violation. To get more information about this waiver please contact your Intel Representative.

Table 8-65.Single-Ended AC and DC Input Levels for CKE

Symbol	Parameter	Minimum	Maximum	Unit	Notes
VIHCKE	CKE Input High Level	0.8 * VDDCA	See Note 1	V	1
VILCKE	CKE Input Low Level	Note 1	0.2 * VDDCA	V	1

NOTE:
1. Refer to Table 8-72, "AC Overshoot/Undershoot Specification" on page 118.

Table 8-66.Single Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	Minimum	Maximum	Unit	Notes
VIHDQ(AC)	AC input logic high	Vref + 0.220	Note 2	V	1, 2
VILDQ(AC)	AC input logic low	Note 2	Vref - 0.220	V	1, 2
VIHDQ(DC)	DC input logic high	Vref + 0.130	VDDQ	V	1
VILDQ(DC)	DC input logic low	-0.0138	Vref - 0.130	V	5
VRefDQ(DC)	Reference Voltage for DQ, DM inputs	0.49 * VDDQ	0.51 * VDDQ	V	3, 4

NOTES:
1. For DQ input only pins. Vref = VrefDQ(DC).
2. See Table 8-72, "AC Overshoot/Undershoot Specification" on page 118.
3. The AC peak noise on VRefDQ may not allow VRefDQ to deviate from VRefDQ(DC) by more than +/-1% VDDQ (for reference: approximately +/- 12mV).
4. For reference: approximately VDDQ/2 +/- 12mV.
5. Deviates from LPDDR2 JEDEC specification, which has minimum VILDQ(DC) =VSSCA =0V. Intel has obtained waivers from majority of LPDDR2 Memory Vendors for this violation. To get more information about this waiver please contact your Intel Representative.

Table 8-67.Differential Swing Requirements for Clock (CK_t - CK_c) and Strobe (DQS_t - DQS_c): Differential AC and DC Input Levels

Symbol	Parameter	Minimum	Maximum	Unit	Notes
VIHdiff(dc)	Differential input high	2 x (VIH(dc) - Vref)	Note 3	V	1,4
VILdiff(dc)	Differential input low	Note 3	2 x (VIL(dc) - Vref)	V	1,4
VIHdiff(ac)	Differential input high ac	2 x (VIH(ac) - Vref)	Note 3	V	2,4
VILdiff(ac)	Differential input low ac	Note 3	2 x (VIL(ac) - Vref)	V	2,4

NOTES:
1. Used to define a differential signal slew-rate.
2. For CK_t - CK_c use VIH/VIL(ac) of CA and VREFCA; for DQS_t - DQS_c, use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK_t, CK_c, DQS_t, and DQS_c need to be within the respective limits (VIH(dc) max, VIL(dc) min) for single-ended signals as well as the limitations for overshoot.
4. For CK_t and CK_c, Vref = VrefCA(DC). For DQS_t and DQS_c, Vref = VrefDQ(DC).

Table 8-68.Single Ended Levels for CK_t, DQS_t, CK_c, DQS_c

Symbol	Parameter	Minimum	Maximum	Unit	Notes
VSEH(AC)	Single-ended high-level for strobes	(VDDQ / 2) + 0.220	Note 3	V	1, 2
	Single-ended high-level for CK_t, CK_c	(VDDCA / 2) + 0.220	Note 3	V	1, 2
VSEL(AC)	Single-ended low-level for strobes	Note 3	(VDDDQ / 2) - 0.220	V	1, 2
	Single-ended low-level for CK_t, CK_c	Note 3	(VDDCA / 2) - 0.220	V	1, 2

NOTES:
1. For CK_t, CK_c use VSEH/VSEL(ac) of CA; for strobes (DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c) use VIH/VIL(ac) of DQs.
2. VIH(ac)/VIL(ac) for DQs is based on VREFDQ; VSEH(ac)/VSEL(ac) for CA is based on VREFCA; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK_t, CK_c, DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c need to be within the respective limits (VIH(dc) maximum, VIL(dc) minimum for single-ended signals as well as the limitations for overshoot and undershoot. Refer to Table 8-72, "AC Overshoot/Undershoot Specification" on page 118.

Table 8-69.Cross Point Voltage for Differential Input Signals (CK, DQS)

Symbol	Parameter	Min.	Max.	Unit	Notes
VIXCA	Differential Input Cross Point Voltage relative to VDDCA/2 for CK_t, CK_c	-120	120	mV	1, 2
VIXDQ	Differential Input Cross Point Voltage relative to VDDQ/2 for DQS_t, DQS_c	-120	120	mV	1, 2

NOTES:
1. The typical value of VIX(AC) is expected to be about 0.5 × VDD of the transmitting device, and VIX(AC) is expected to track variations in VDD. VIX(AC) indicates the voltage at which differential input signals must cross.
2. For CK_t and CK_c, Vref = VrefCA(DC). For DQS_t and DQS_c, Vref = VrefDQ(DC).

Table 8-70.Single Ended AC and DC Output Levels (Sheet 1 of 2)

Symbol	Parameter		Value	Unit	Notes
VOH(DC)	DC output high measurement level (for IV curve linearity)		0.9 x VDDQ	V	1
VOL(DC)	DC output low measurement level (for IV curve linearity)		0.1 x VDDQ	V	2
VOH(AC)	AC output high measurement level (for output slew rate)		VREFDQ + 0.12	V	
VOL(AC)	AC output low measurement level (for output slew rate)		VREFDQ - 0.12	V	

Table 8-70.Single Ended AC and DC Output Levels (Sheet 2 of 2)

Symbol	Parameter		Value	Unit	Notes
I_{OZ}	Output Leakage current (DQ, DM, DQS_t, DQS_c) (DQ, DQS_t, DQS_c are disabled; 0V ≤ VOUT ≤ VDDQ	Min.	-5	µA	
		Max.	5	µA	
MM_{PUPD}	Delta RON between pull-up and pull-down for DQ/DM	Min.	-15	%	
		Max.	+15	%	

NOTES:
1. IOH = -0.1 mA
2. IOL = 0.1 mA

Table 8-71.Differential AC and DC Output Levels

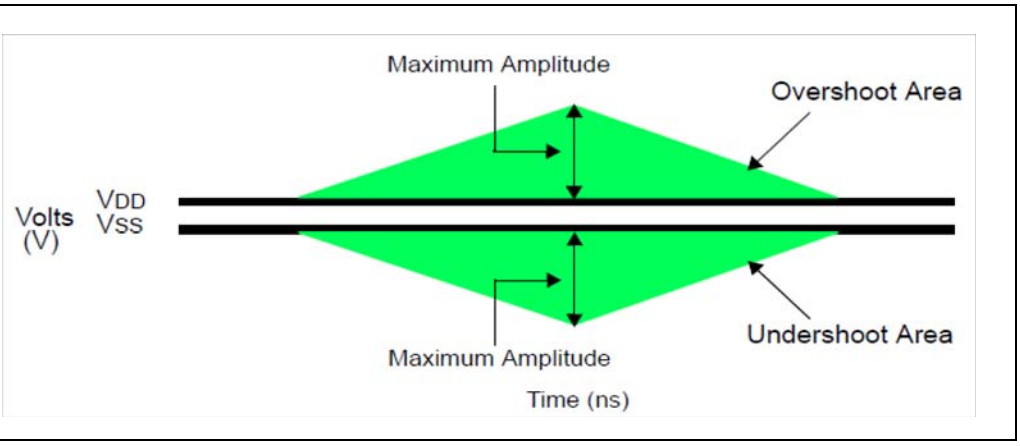
Symbol	Parameter	Value	Unit	Notes
VOHdiff(AC)	AC differential output high measurement level (for output SR)	+ 0.2 x VDDQ	V	
VOLdiff(AC)	AC differential output low measurement level (for output SR)	- 0.2 x VDDQ	V	

Table 8-72.AC Overshoot/Undershoot Specification

Parameter		800 MTS	Units	Notes
Maximum peak amplitude allowed for overshoot area. (See Figure)	Max.	0.35	V	
Maximum peak amplitude allowed for undershoot area. (See Figure)	Max.	0.35	V	
Maximum area above VDD. (See Figure)	Max.	0.2	V-ns	1, 3
Maximum area below VSS. (See Figure)	Max.	0.2	V-ns	2, 3
(CA0-9, CS_n, CKE, CK_t, CK_c, DQ, DQS_t, DQS_c, DM/DNV)				

NOTES:
1. For CA0-9, CK_t, CK_c, CS_n, and CKE, VDD stands for VDDCA. For DQ, DM/DNV, DQS_t, and DQS_c, VDD stands for VDDQ.
2. For CA0-9, CK_t, CK_c, CS_n, and CKE, VSS stands for VSSCA. For DQ, DM/DNV, DQS_t, and DQS_c, VSS stands forVSSQ.
3. Values are referenced from actual VDDQ, VDDCA, VSSQ, and VSSCA levels.

Figure 8-19.Overshoot and Undershoot Definition



8.4 MIPI DSI Electrical Characteristics

8.4.1 MIPI DSI DC Specification

Table 8-73.MIPI DSI DC Specification

Symbol	Parameter	Min.	Nom.	Max.	Unit	Notes
ILEAK	Pin Leakage current	-10	–	10	µA	
MIPI DSI HS-TX Mode						
V_{CMTX}	HS transmit static common-mode voltage	150	200	250	mV	
$\|V_{CMTX(1,0)}\|$	V_{CMTX} mismatch when output is differential-1 or differential-0	–	–	5	mV	
$\|V_{OD}\|$	HS transmit differential voltage	140	200	270	mV	
$\|\Delta V_{OD}\|$	V_{OD} mismatch when output is Differential-1 or Differential-0	–	–	10	mV	
V_{OHHS}	HS output high voltage	–	–	360	mV	
Z_{OS}	Single-ended output impedance	40	50	62.5	Ω	
ΔZ_{OS}	Single-ended output impedance mismatch	–	–	10	%	
MIPI DSI LP-TX Mode						
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	
V_{OL}	Thevenin output low level	-50	–	50	mV	
Z_{OLP}	Output impedance of LP transmitter	50	–	–	Ω	1
MIPI DSI LP-RX Mode						
V_{IH}	Logic 1 input voltage	880	–	–	mV	
V_{IL}	Logic 0 input voltage, not in ULP state	–	–	550	mV	
V_{HYST}	Input hysteresis	25	–	–	mV	
V_{IHCD}	Logic 1 Contention threshold	450	–	–	mV	
V_{ILCD}	Logic 0 Contention threshold	–	–	200	mV	

NOTE: 1. Deviates from MIPI D-PHY specification Rev 1.0, which has minimum ZOLP of 110 Ω.

8.5 HDMI Electrical Characteristics

8.5.1 HDMI 1.3a DC Specification

Table 8-74.HDMI 1.3a DC Specification

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
AV_{CC}	Link Reference Voltage	3.3–5%	3.3	3.3 +5%		
V_{OFF}	Single-ended standby (off) output voltage	AVcc -10	–	AVcc +10	mV	
Vswing	Single-ended output swing voltage	400	–	600	mV	
V_H	Single-ended high level output voltage (if attached Sink supports only <=165 MHz)	AVcc -10	–	AVcc +10	mV	
V_L	Single-ended low level output voltage (if attached Sink supports only <=165 MHz)	AVcc – 600	–	AVcc – 400	mV	

8.6 MIPI CSI-2 Electrical Characteristics

8.6.1 MIPI CSI-2 DC Specification

Table 8-75.MIPI HS-RX/MIPI LP-RX Minimum, Nominal, and Maximum Voltage Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
I_{LEAK}	Pin Leakage current	-10	–	10	µA	
MIPI CSI-2 HS-RX Mode						
$V_{CMRX(DC)}$	Common-mode voltage HS receive mode	70	–	330	mV	
V_{IDTH}	Differential input high threshold	–	–	70	mV	
V_{IDTL}	Differential input low threshold	-70	–	–	mV	
V_{IHHS}	Single-ended input high voltage	–	–	460	mV	
V_{ILHS}	Single-ended input low voltage	-40	–	–	mV	
$V_{TERM-EN}$	Single-ended threshold for HS termination enable	–	–	450	mV	
Z_{ID}	Differential input impedance	80	100	125	Ω	
MIPI CSI-2 LP-RX Mode						
V_{IH}	Logic 1 input voltage	880	–	–	mV	

Table 8-75.MIPI HS-RX/MIPI LP-RX Minimum, Nominal, and Maximum Voltage Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{IL}	Logic 0 input voltage, not in ULP state	–	–	550	mV	
$V_{IL-ULPS}$	Logic 0 input voltage, ULP state	–	–	300	mV	
V_{HYST}	Input hysteresis	25	–	–	mV	

8.7 SD/SDIO Electrical Characteristics

Table 8-76.SD/SDIO Ports Overview

Port #	Referred As	Usage	Nominal Voltage (V)	Notes
0	SD_0	External: To be used with external SD/MMC cards	2.85	Uses GPIO HV 2.85V Buffer
1	SDIO_1	Internal Only	1.8	Uses GPIO MV 1.8 V Buffer
2	SDIO_2	Internal Only	1.8	Uses GPIO MV 1.8 V Buffer

8.7.1 SD_0 Electrical Characteristics

Following specification is for Port SD_0 which is used for external purpose for use with external SD/SDHC cards.

8.7.1.1 SD_0 DC Specification

Table 8-77.SD DC Specification (Sheet 1 of 2)

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{OH}	Output High Voltage	0.75*VCCSDIO	–	–	V	I_{OH}=–100 µA VDD minimum
V_{OL}	Output Low Voltage	–	–	0.125*VCCSDIO	V	I_{OL}= 100 µA VDD minimum
V_{IH}	Input High Voltage	0.625*VCCSDIO	–	–	V	
V_{IL}	Input Low Voltage	–	–	0.58	V	
	Peak voltage on all lines	-0.3	–	VCCSDIO + 0.3V	V	
I_{LI}	Input Leakage Current	-10	–	10	µA	

Table 8-77.SD DC Specification (Sheet 2 of 2)

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
I_{L0}	Output Leakage Current	-10	–	10	µA	
Vhysteresis	Input Hysteresis	100	–	–	mV	
Cload	Input Load Capacitance	2	5	8	pF	

8.7.2 SDIO Electrical Characteristics

Following specification is for Ports SDIO_1 and SDIO_2 which are used only for connections to components internal to the tablet and use the GPIO MV 1.8 V Buffer.

8.7.2.1 SDIO DC Specification

For SDIO DC Specification please refer to GPIO MV (1.8 V) DC Specification mentioned in Table 8-84, "MV Buffer DC Specification (1.8 V and 1.2 V)" on page 126.

8.8 eMMC* Electrical Characteristics

8.8.1 eMMC* DC Specification

Table 8-78.eMMC* DC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{IL}	Input Low Voltage	Vss - 0.3	–	VCC180AON_eMMC*0.35	V	
V_{IH}	Input High Voltage	VCC180AON_eMMC* 0.65		VCC180AON_eMMC + 0.3	V	
V_{OL}	Output Low Voltage	–	–	0.45	V	1
V_{OH}	Output High Voltage	VCC180AON_eMMC- 0.45	–	–	V	1
Cpad	Pad Capacitance	–	–	5	pF	
I_{LI}	Input Leakage Current	-10	–	10	µA	
I_{L0}	Output Leakage Current	-10	–	10	µA	

Note: 1. Assuming a I_{OH}/I_{OL} of 2mA.

8.9 I²S Electrical Characteristics

Table 8-79.I²S Ports Overview

Port #	Mode Supported	Nominal Voltage (V)	Maximum Operational Frequency	Notes
0	Slave Only	1.8	4.8 MHz	Used to interface with 3G Modem. IFX Modem uses PCM Short Frame Mode.
1	Slave Only	1.8	9.6 MHz	Used to interface with Bluetooth*/FM Module. This port also connects to the PMIC and used for active noise cancellation (ANC).
2	Slave Only	1.25	9.6 MHz	Interface not used.
3	Slave Only / Master Mode	1.8	9.6 MHz	

NOTE: Master Mode is only supported on I²S Port3.

8.9.1 I²S DC Specifications

For the I²S DC Specification please refer to GPIO MV DC Specifications mentioned in Table 8-84, “MV Buffer DC Specification (1.8 V and 1.2 V)” on page 126.

8.10 SPI Electrical Characteristics

Table 8-80.SPI Ports Overview

Port #	Mode	Nominal Voltage (V)	Max. Frequency	Notes
0	Master Only	1.25	12.5 MHz	Dedicated to be used with PMIC.
1	Master Only	1.8 or 1.25	25 MHz	Interface not used.
2	Master Only	1.8	25 MHz	Interface not used.
3	Master and Slave	1.8	25 MHz (Master Mode) 13 MHz (Slave Mode)	Interface not used.

Table 8-81.SPI Modes

Mode	SCPOL	SCPH
0	0	0
1	0	1
2	1	0
3	1	1

NOTE: SCPOL and SCPH can be configured by SPI Register CTRL0. Refer to SPI registers for more information.

8.10.1 SPI DC Specification

For SPI Master and Slave DC Specification please refer to GPIO MV (1.8 V) DC Specification mentioned in Table 8-84, "MV Buffer DC Specification (1.8 V and 1.2 V)" on page 126.

8.11 I²C Electrical Characteristics

Table 8-82. I²C Ports Overview

I²C Port	Usage	Standard 100kb/s	Fast 400kb/s	Nominal Voltage	Notes
0	General	Yes	Yes	1.8 V or 1.25V	1,2,3,4
1	General	Yes	Yes	1.8 V or 1.25V	1,2,3,4
2	General	Yes	Yes	1.8 V or 1.25V	1,2,3,4
3	HDMI	Yes	n/a	1.25V	1
4	Camera Interface	Yes	Yes	1.8 V	1
5	General	Yes	Yes	1.8 V	1

NOTES:
1. The SoC is always I²C Master; Multi-Master mode is not supported.
2. Voltage applied to Ball# AW33 (VCC122_180AON_I2C) will decide the operating voltages for I²C Ports 0, 1, and
3. Standard, and Fast Modes are supported at 1.8V.
4. Standard and Fast modes are supported at 1.25V.

8.11.1 I²C Fast/Standard Mode Electrical Characteristics

8.11.1.1 I²C Fast/Standard Mode DC Specification

Table 8-83. I²C—SDA and SCL I/O Stages for F/S-Mode Devices

Symbol	Parameter	Standard-Mode 100 K			Fast-Mode 400 K			Unit	Notes [1]
		Min.	Typ.	Max.	Min.	Typ.	Max.		
T_{SP}	Pulse width of the spikes which are suppressed by the input filter	NA	NA	NA	0	–	10	ns	3
V_{OL}	Output Low Voltage	–	–	V_{DD} * 0.2	–	–	V_{DD} * 0.2	V	2
V_{IL}	Input Low Voltage	–	–	0.560	NA	NA	NA	V	4

NOTES:
1. For all other DC Specifications, refer to the GPIO MV DC Specification mentioned in Table 8-84, "MV Buffer DC Specification (1.8 V and 1.2 V)" on page 126.
2. V_{DD}=1.25V if Operating Voltage is configured to 1.25V/V_{DD}=1.8 V if the Operating Voltage is configured to 1.8 V.
3. Deviates from the I²C Specification, which states maximum, TSP of 50 ns for Fast Mode.

4. This applies to I^2C Port 3 only which is being used for HDMI. For V_{IL} for other ports refer to Table 8-84, "MV Buffer DC Specification (1.8 V and 1.2 V)" on page 126

8.12 GPIO MV Electrical Characteristics

GPIO MV Buffer is used across various interfaces on the SoC such as GPIOs, I^2C, I2S, MPTI, SPI, SDIO, SVID, UART, JTAG, LPC, and ULPI.

8.12.1 GPIO MV DC Specification

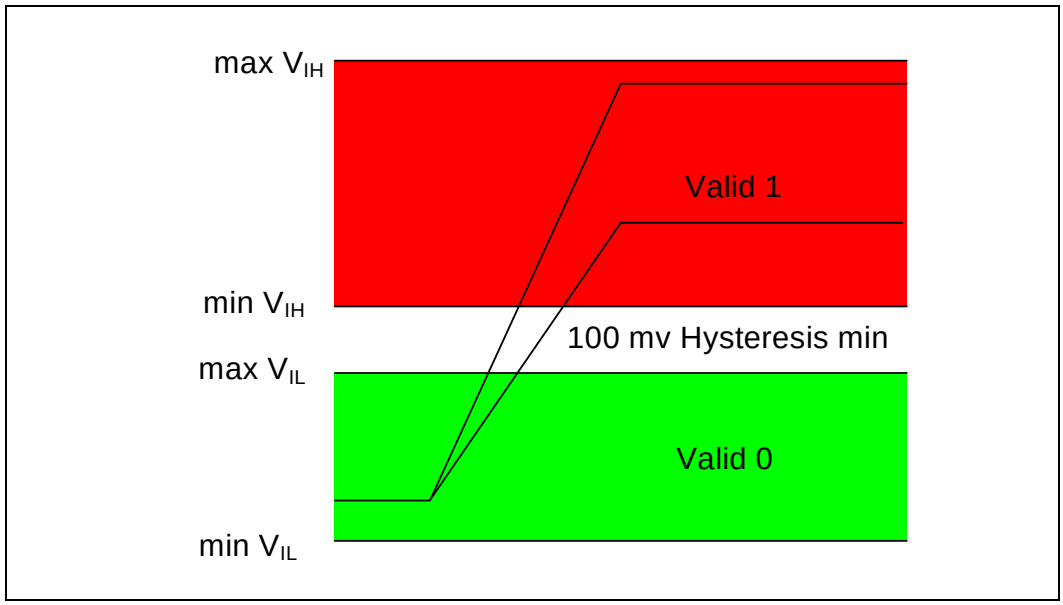
Table 8-84.MV Buffer DC Specification (1.8 V and 1.2 V) (Sheet 1 of 2)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{SUPPLY} (DC)	Vcc_12	1.175	1.25	1.260	V	
	Vcc_18	1.71	1.8	1.89		
$V_{IH(1.2)}$	Input High Voltage	860	–	–	mV	- 1.2V mode is designed to work with 1.8 V input level - 1.8 V mode is designed to work with a 1.2V input level - V_{IH} is the same for both 1.2V and 1.8 V MV buffers.
$V_{IH(1.8)}$	Input High Voltage	860	–	–	mV	- 1.2V mode is designed to work with 1.8 V input level - 1.8 V mode is designed to work with a 1.2 V input level - V_{IH} is the same for both 1.2V and 1.8 V MV buffers.
$V_{IL(1.2)}$	Input Low Voltage	–	–	400	mV	- V_{IL} is the same for both 1.2V and 1.8 V MV buffers.
$V_{IL(1.8)}$	Input Low Voltage	–	–	400	mV	- V_{IL} is the same for both 1.2V and 1.8 V MV buffers.
$V_{OH\ (1.2V)}$	Output High Voltage	Vcc_12*0.75	–	–	V	Measured at I_{OH} maximum.
$V_{OH\ (1.8\ V)}$	Output High Voltage	Vcc_18*0.75	–	–	V	Measured at I_{OH} maximum.
$V_{OL(1.2V)}$	Output Low Voltage	–	–	Vcc_12 *0.125	V	Measured at I_{OL} maximum.
$V_{OL(1.8\ V)}$	Output Low Voltage	–	–	Vcc_18 *0.125	V	Measured at I_{OL} maximum.
Vhysteresis	Input Hysteresis	100	–	–	mv	
I_{OH}/I_{OL}	Current at VoL/Voh	-3	–	3	mA	

Table 8-84.MV Buffer DC Specification (1.8 V and 1.2 V) (Sheet 2 of 2)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
I_{LI}	Input Leakage Current	-10	–	10	µA	
I_{LO}	Output Leakage Current	-10	–	10	µA	
Cload	Input Load Capacitance	2	5	8	pF	

Figure 8-20.GPIO Buffer Input Range



8.13 USB ULPI Electrical Characteristic

8.13.1 ULPI DC Specification

Please refer to GPIO MV (1.8 V) DC Specification, mentioned in Table 8-84, "MV Buffer DC Specification (1.8 V and 1.2 V)" on page 126.

8.14 UART Electrical Characteristics

The SoC supports three instances of a 16550 compliant UART controller.

Each of the UART interfaces support the following baud rates (T_{BAUD}):

- 3.6864M, 921.6k, 460.8K, 307.2K, 230.4K, 184.32K, 153.6K, 115.2K, 57.6K, 38.4K, 19.2K, 9.6K, 7.2K, 4.8K, 3.6K, 2.4K, 1.8K, 1.2K, 600, and 300.

8.14.1 UART DC Specification

Please refer to GPIO MV (1.8 V) DC Specification, mentioned in Table 8-84, "MV Buffer DC Specification (1.8 V and 1.2 V)" on page 126.

8.15 SVID Electrical Characteristics

The following section contains Electrical Characteristics about the Serial VID (SVID) Interface.

8.15.1 SVID DC Specification

Please refer to GPIO MV (1.2V) DC Specification, mentioned in Table 8-84, "MV Buffer DC Specification (1.8 V and 1.2 V)" on page 126.

8.16 JTAG Interface Electrical Characteristics

The following section contains Electrical Characteristics about the JTAG Interface.

8.16.1 JTAG DC Specification

Table 8-85.JTAG DC Specification

Symbol	Parameter	Min.	Max.	Unit
$V_{IL(1.2)}$	Input Low Voltage	–	350	mV

NOTE: For all other DC Specifications refer to GPIO MV (1.8 V) DC Specifications, mentioned in Table 8-84, "MV Buffer DC Specification (1.8 V and 1.2 V)" on page 126.

8.17 LPC Electrical Characteristics

This section contains the LPC Electrical specification. The SoC implements a 25 MHz instantiation though the LPC spec is 33 MHz. It also implements it using 1.8 V with an external level shifter to achieve 3.3V rather than being natively 3.3V.

8.17.1 LPC—DC Specification

For LPC DC Specification please refer to GPIO MV (1.8 V) DC Specification mentioned in "MV Buffer DC Specification (1.8 V and 1.2 V)" on page 126.

8.18 Power Rails

8.18.1 Power Rail Type

This section defines the power state and power level options.

Table 8-86.Power Rails—Type

Type	Description
F	**Fixed:** Voltage level is fixed to be a certain value.
S	**Selectable:** Voltage can be selected at the platform level, but are static during normal operation.
V	**Variable:** Variable supplies are negotiable supply levels and can change during operation.

8.18.2 Power Rail Description

This section describes the power signals and power states of each power signal.

Note: The numbers provided below are early silicon estimates based on simulations and are platform power delivery requirements, not component requirements. Measured at bulk capacitors of the PMIC.

Table 8-87.Power Rails (Sheet 1 of 2)

System Rail Name	Rail Type	Voltage (V)	Purpose	Tolerance	Active[5] Power States	Typical Current (mA)[5]	Peak Current[1] (mA)[5]	Note
VCC	V	0.3–1.2	Core CPU power	±5%	S0	600–1300	3800	2
VCC108AON	F	1.08	SRAM in AON domain	±25mV	AON	1.125	11.125	
VCC108AS	F	1.08	SRAM needed for Audio playback	±30mV	S0–S0i1	6	25	
VCC108	F	1.08	L2 and SRAMs for entire chip	±50mV	S0	10–30	315	
VNNAON	V	0.75–1.1	SCU Block	±5%	AON	1–10	200	
VNN	V	0.75–1.1	Non-CPU logic	±5%	S0–S0i1	308-1160	3500	2
VCCA100	F	1.05	CPU PLL, HF PLL, Display PLL, DSI PLL, CPU DTS, SoC DTS	±2.5%	S0	37	120	
VCCA100AS	F	1.05	LF PLL, HDMI Vref	± 2.5%	S0–S0i1	12	20	
VCC122AON	F	1.25	LPDDR2 I/O (DDR and SoC), PMIC Control; SPI (Port0, PMIC); SVID, I2S_2; Thermal control, HDMI DDC; MIPI DSI and CSI	+40mV to -45mV	AON	10–150	243	3
VDD2	S	1.25/ 1.35	LPDDR2 core	±5%	AON	250	680	

Table 8-87.Power Rails (Sheet 2 of 2)

System Rail Name	Rail Type	Voltage (V)	Purpose	Tolerance	Active[5] Power States	Typical Current (mA)[5]	Peak Current[1] (mA)[5]	Note
Selectable Voltage GPIOs	S	1.25 or 1.8	I^2C Ports (0:2); SPI (1)	Supply dependent	AON	–	Included in VCC122AON and VCC18AON	
V180AON	F	1.8	LPDDR2 Pre-driver Logic—Not used by the SoC	±5%	AON	16	125	
VCC180AON	F	1.8	ULPI, SPI (2/3); COMS_INT HS UART; GPIO; I^2S (0:1); JTAG; CAMERASB; I^2C (4:5); SDIO (1:2); GPIO; eMMC*	±5%	AON	20–50	201	4
VCC330	F	3.3	HDMI 1.3 Data I/F	± 5%	S0	6	20	
VCCSDIO	V	2.85	SDIO External Port	± 5%	S0	4	55	

NOTES:
1. "Peak current" defined as a sustained peak, lasting for at least 0.5 µs. The intent is to provide the peak current that is needed to be supplied by the voltage regulator. Peak currents represent only I_{CC} drawn by the processor, not other system components.
2. The peak current numbers are included for the purpose of VR design and external component specifications (such as, the inductor's saturation, and so forth) and cover all worse case scenarios (such as, power virus at maximum temperature). The maximum I_{CC} will last for short durations but long enough to be seen at the VR.
3. VCC122AON does not take into account the DRAM I/O current requirement of ~ 95 mA sustained over 0.5 µs.
   a. The dedicated GPIOs constitute a significant portion of the VCC180AON I_{CC}. Each dedicated GPIO can support up to 150 pF total load (T-line + trace) at 50 MHz. However it's not practical for all GPIOs to drive maximum load at maximum frequency so the I_{CC} is de-rated as: (10 GPIOs x 150 pF load x 200 KHz) + (24 GPIOs x 75 pF load x 10 MHz). The maximum load for the GPIOs are also restricted due to electrical droop.
4. Typical and Peak current values represent expected values based on pre-Si simulations.

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9 Mechanical and Package Specifications

9.1 Pin List

Table 9-88.Pin List (Bottom View)—Arranged by Pin Name (Sheet 1 of 7)

Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number
GP_CAMERA_SB0	AV6	PMIC_PWRGOOD	R35	VNN	AH24
GP_CAMERA_SB1	AT10	PMIC_RESET#	T38	VNN	AH26
GP_CAMERA_SB2	AU7	IERR#	B16	VNN	AJ13
GP_CAMERA_SB3	AV4	GP_UART_0_RX	AM14	VNN	AJ15
GP_CAMERA_SB4	AD8	GP_UART_0_TX	AV8	VNN	AJ17
GP_CAMERA_SB5	AC5	GP_UART_0_CTS	AN11	VNN	AJ19
GP_CAMERA_SB6	AB8	GP_UART_0_RTS	AR9	VNN	AJ21
GP_CAMERA_SB7	AB2	GP_UART_1_RX	D36	VNN	AJ23
GP_CAMERA_SB8	AB6	GP_UART_1_RTS	E37	VNN	AJ25
GP_CAMERA_SB9	AC3	GP_UART_1_TX	E35	VNN	AJ27
GP_COMS_INT0	H36	GP_UART_1_CTS	C35	VNN	AW19
GP_COMS_INT1	G31	GP_UART_2_RX	E33	VNN	AW21
GP_COMS_INT2	H32	GP_UART_2_TX	J33	VNN	L11
GP_COMS_INT3	G33	ULPI_1_CLK	AV36	VNN	L13
GP_AON_042	AF38	ULPI_1_D0	AT32	VNN	L15
GP_AON_043	AF36	ULPI_1_D1	AR31	VNN	L17
GP_AON_044	AB32	ULPI_1_D2	AU33	VNN	N13
GP_AON_045	AA33	ULPI_1_D3	AU31	VNN	N15
GP_AON_049	AE35	ULPI_1_D4	AU35	VNN	P12
GP_AON_051	K32	ULPI_1_D5	AN31	VNN	P14
GP_AON_062	C37	ULPI_1_D6	AR35	VNN	P16
GP_AON_063	F34	ULPI_1_D7	AT34	VNN	P4
GP_AON_060	F38	ULPI_1_DIR	AU37	VNN	P8
GP_AON_061	F36	ULPI_1_NXT	AP32	VNN	R1
GP_AON_072	J37	ULPI_1_REFCLK	AT36	VNN	R11
GP_AON_076	AP16	ULPI_1_STP	AR33	VNN	R13
GP_AON_077	AR15	ULPI_0_CLK	W35	VNN	R15
GP_AON_078	AV16	ULPI_0_D0	Y36	VNN	R17
GP_AON_079	AT14	ULPI_0_D1	AD34	VNN	R3
GP_AON_089	AM32	ULPI_0_D2	Y32	VNN	R5
GP_AON_093	AM34	ULPI_0_D3	AC33	VNN	R7

Table 9-88.Pin List (Bottom View)—Arranged by Pin Name (Sheet 2 of 7)

Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number
GP_AON_094	AP38	ULPI_0_D4	W33	VNN	R9
GP_CORE_012	AM16	ULPI_0_D5	AC35	VNN	T10
GP_CORE_015	AT16	ULPI_0_D6	AA35	VNN	T12
GP_CORE_016	AP12	ULPI_0_D7	AB36	VNN	T14
GP_CORE_017	AN15	ULPI_0_DIR	V32	VNN	T16
GP_CORE_018	AV14	ULPI_0_NXT	Y38	VNN	T2
GP_CORE_020	AU15	ULPI_0_REFCLK	U33	VNN	T4
GP_CORE_030	AM12	ULPI_0_STP	V36	VNN	T6
GP_CORE_031	AM10	RSVD	AW37	VNN	T8
GP_CORE_032	AU11	RSVD	H12	VNN	U1
GP_CORE_033	AN9	RSVD	D4	VNN	U11
GP_CORE_037	J7	RSVD	F4	VNN	U13
GP_CORE_067	G19	RSVD	G3	VNN	U15
GP_CORE_068	D12	RSVD	B10	VNN	U17
GP_CORE_069	B12	RSVD	U37	VNN	U3
GP_CORE_070	H16	RSVD	AC7	VNN	U5
GP_CORE_071	D10	RSVD	E27	VNN	U7
GP_CORE_072	C17	RSVD	F28	VNN	U9
GP_CORE_073	K6	RSVD	G13	VNN	V16
GP_CORE_074	J5	RSVD	F10	VNN	W15
GP_CORE_075	J9	RSVD	V26	VNN	W17
GP_CORE_082	AE7	RSVD	V20	VNN	Y16
GPIO_RCOMP18	AL3	RSVD	U25	VCCA100	T26
GPIO_RCOMP30	AL7	RSVD	U21	VCCA100	V14
GP_EMMC_0_RST#	AV12	VCC_VSSSENSE	R25	VDD1	AV18
EMMC_0_CLK	AT18	VCC	AA19	VDD1	AE1
EMMC_0_CMD	AP24	VCC	AA27	VDD1	C1
EMMC_0_D0	AR21	VCC	AC19	VDD1	C3
EMMC_0_D1	AM20	VCC	AC27	VDD1	A29
EMMC_0_D2	AP20	VCC	B22	VDD1	AN39
EMMC_0_D3	AT20	VCC	B24	VDD2	AW25
EMMC_0_D4	AU19	VCC	B26	VDD2	AW17
EMMC_0_D5	AL19	VCC	C23	VDD2	AW5
EMMC_0_D6	AM18	VCC	C25	VDD2	AW7
EMMC_0_D7	AR17	VCC	D22	VDD2	AG1
GP_EMMC_1_RST#	AN13	VCC	D24	VDD2	AH2
EMMC_1_CLK	AN19	VCC	D26	VDD2	A3
EMMC_1_CMD	AM24	VCC	E23	VDD2	B4

Table 9-88.Pin List (Bottom View)—Arranged by Pin Name (Sheet 3 of 7)

Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number
EMMC_1_D0	AR23	VCC	E25	VDD2	A35
EMMC_1_D1	AU23	VCC	F22	VDD2	B36
EMMC_1_D2	AN23	VCC	F24	VDD2	V38
EMMC_1_D3	AT22	VCC	G23	VDD2	AK38
EMMC_1_D4	AL21	VCC	H22	VDD2	AV34
EMMC_1_D5	AM22	VCC	H24	VDD2	AW35
EMMC_1_D6	AN21	VCC	J21	VNN_VSSSENSE	AA13
EMMC_1_D7	AL23	VCC	J23	VNNSENSE	Y14
EMMC_RCOMP	AR19	VCC	K22	VCCA100AS	F6
HDMI_5V_DET	E5	VCC	K24	VSS	A1
HDMI_EXTR	H6	VCC	L21	VSS	A5
HDMI_CLKN	E3	VCC	L23	VSS	AA11
HDMI_CLKP	D2	VCC	L25	VSS	AA31
HDMI_DN0	D8	VCC	L27	VSS	AB10
HDMI_DN1	A7	VCC	M20	VSS	AB14
HDMI_DN2	C5	VCC	M22	VSS	AB18
HDMI_DP0	B8	VCC	M24	VSS	AB20
HDMI_DP1	C7	VCC	M26	VSS	AB26
HDMI_DP2	B6	VCC	N19	VSS	AB28
GP_I2C_3_SCL_HDMI	F8	VCC	N21	VSS	AB34
GP_I2C_3_SDA_HDMI	H4	VCC	N23	VSS	AB38
GP_I2C_0_SCL	AT28	VCC	N25	VSS	AC13
GP_I2C_0_SDA	AN27	VCC	N27	VSS	AC31
GP_I2C_1_SCL	AU27	VCC	P20	VSS	AC37
GP_I2C_1_SDA	AT26	VCC	P22	VSS	AC9
GP_I2C_2_SCL	AM26	VCC	P26	VSS	AD10
GP_I2C_2_SDA	AV26	VCC	R19	VSS	AD14
GP_I2C_4_SCL	AE5	VCC	R21	VSS	AD20
GP_I2C_4_SDA	AF4	VCC	R23	VSS	AD22
GP_I2C_5_SCL	AF6	VCC	R27	VSS	AD24
GP_I2C_5_SDA	AD2	VCC	T22	VSS	AD26
GP_I2S_0_CLK	D32	VCC	T24	VSS	AD28
GP_I2S_0_FS	D28	VCC	U19	VSS	AD30
GP_I2S_0_RXD	B32	VCC	U23	VSS	AD32
GP_I2S_0_TXD	C33	VCC	U27	VSS	AD38
GP_I2S_1_CLK	E29	VCC	V22	VSS	AD6
GP_I2S_1_FS	F30	VCC	V24	VSS	AE13

Table 9-88.Pin List (Bottom View)—Arranged by Pin Name (Sheet 4 of 7)

Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number
GP_I2S_1_RXD	B28	VCC	W19	VSS	AE29
GP_I2S_1_TXD	E31	VCC	W27	VSS	AE3
I2S_2_CLK	N33	VCC	A23	VSS	AE31
I2S_2_FS	N31	VCC	A25	VSS	AE9
I2S_2_RXD	N37	VCC108	W23	VSS	AF10
I2S_2_TXD	P36	VCC108	W21	VSS	AF12
GP_I2S_3_CLK	D30	VCC108	AK28	VSS	AF34
GP_I2S_3_FS	B30	VCC108	AL27	VSS	AF8
GP_I2S_3_TXD	K36	VCC108AON_OSC	J15	VSS	AG11
GP_I2S_3_RXD	H38	VCC180AON	AV22	VSS	AG17
JTAG_TCK	B14	VCC180AON	AV24	VSS	AG21
JTAG_TDI	D14	VCC180AON	AW23	VSS	AG25
JTAG_TDO	J17	VCC180AON	A9	VSS	AG29
JTAG_TMS	E13	VCC330	A11	VSS	AG31
JTAG_TRST#	E17	VCC122_180AON_I2C	AW33	VSS	AG37
GP_XDP_C0_BPM0#	AK32	VCC122AON_MCLK	AL25	VSS	AG7
GP_XDP_C0_BPM1#	AK34	VCC122AON_MCLK	AK30	VSS	AH10
GP_XDP_C0_BPM2#	AJ35	VCC122AON_MEM	A13	VSS	AH12
GP_XDP_C0_BPM3#	AJ33	VCC122AON_MEM	A17	VSS	AH28
GP_XDP_C1_BPM0#	AJ37	VCC122AON_MEM	A31	VSS	AH34
GP_XDP_C1_BPM1#	AG33	VCC122AON_MEM	A37	VSS	AH6
GP_XDP_C1_BPM2#	AH32	VCC122AON_MEM	A39	VSS	AJ29
GP_XDP_C1_BPM3#	AH38	VCC122AON_MEM	AC1	VSS	AJ3
GP_XDP_PREQ#	AH36	VCC122AON_MEM	AE39	VSS	AJ31
GP_XDP_PRDY#	AG35	VCC122AON_MEM	AJ39	VSS	AK12
GP_XDP_BLK_DP	AF32	VCC122AON_MEM	AN1	VSS	AK14
GP_XDP_BLK_DN	AE37	VCC122AON_MEM	AR1	VSS	AK16
GP_XDP_PWRMODE0	AE33	VCC122AON_MEM	AU1	VSS	AK18
GP_XDP_PWRMODE1	AD36	VCC122AON_MEM	AV10	VSS	AK20
GP_XDP_PWRMODE2	AA37	VCC122AON_MEM	AW1	VSS	AK22
GP_LPC_AD0	AN35	VCC122AON_MEM	AW27	VSS	AK24
GP_LPC_AD1	AL35	VCC122AON_MEM	AW3	VSS	AK26
GP_LPC_AD2	AT38	VCC122AON_MEM	AW31	VSS	AL11
GP_LPC_AD3	AN37	VCC122AON_MEM	AW9	VSS	AL13
GP_LPC_CLKOUT	AN33	VCC122AON_MEM	B34	VSS	AL15
GP_LPC_CLKRUN	AK36	VCC122AON_MEM	C39	VSS	AL31

Table 9-88.Pin List (Bottom View)—Arranged by Pin Name (Sheet 5 of 7)

Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number
GP_LPC_FRAME#	AP36	VCC122AON_MEM	D38	VSS	AL37
GP_LPC_RESET#	AL33	VCC122AON_MEM	E39	VSS	AL9
M_RCOMP0	AT24	VCC122AON_MEM	G1	VSS	AM36
M_RCOMP1	AR25	VCC122AON_MEM	J1	VSS	AN3
M_RCOMP2	AN25	VCC122AON_MEM	R39	VSS	AP10
MCSI_X1_CLKN	V8	VCC122AON_MEM	U39	VSS	AP14
MCSI_X1_CLKP	V10	VCC122AON_MEM	W1	VSS	AP18
MCSI_X1_DN	W7	VCC122AON_MEM	AL29	VSS	AP22
MCSI_X1_DP	W9	VCC122AON_MEM	AW29	VSS	AP26
MCSI_X4_CLKN	W3	VCC122AON_MEM	AK10	VSS	AP30
MCSI_X4_CLKP	W5	VCC122AON_MEM	AL1	VSS	AP34
MCSI_X4_DN0	AA3	VCC122AON_MEM	AA1	VSS	AP6
MCSI_X4_DN1	Y2	VCC122AON_MEM	Y10	VSS	AR37
MCSI_X4_DN2	AA9	VCC122AON_MEM	A15	VSS	AR39
MCSI_X4_DN3	V4	VCC122AON_MEM	J13	VSS	AT12
MCSI_X4_DP0	AA5	VCC122AON_MEM	A33	VSS	AT4
MCSI_X4_DP1	Y4	VCC122AON_MEM	H28	VSS	AU13
MCSI_X4_DP2	AA7	VCC122AON_MEM	AG39	VSS	AU17
MCSI_X4_DP3	V6	VCC122AON_MEM	AH30	VSS	AU21
MDSI_A_CLKN	M8	VCCSDIO	AK2	VSS	AU25
MDSI_A_CLKP	M10	VCC122_180AON_I2S	G39	VSS	AU29
MDSI_A_DP0	N9	VCC122_180AON_I2S	AL39	VSS	AU39
MDSI_A_DP1	N5	VCC122AON	AW11	VSS	AU9
MDSI_A_DP2	L5	VCC122AON	AF2	VSS	AV2
MDSI_A_DP3	K4	VCC122AON	L1	VSS	AV32
MDSI_A_DN0	N7	VCC122AON	N1	VSS	AV38
MDSI_A_DN1	N3	VCC122AON	G9	VSS	AW39
MDSI_A_DN2	L7	VCC122AON	H18	VSS	B2
MDSI_A_DN3	K2	VCC122AON	J39	VSS	B38
MCSI_COMP	Y8	VCC122AON	L39	VSS	C11
GP_MDSI_A_TE	AB4	VCC122AON	AM30	VSS	C15
RSVD	M2	VCC180AON	AW13	VSS	C19
RSVD	M4	VCC180AON	AW15	VSS	C27
MDSI_COMP	L9	VCC180AON	AJ1	VSS	C29
GP_CORE_007	AD4	VCC180AON	E1	VSS	C31
MHSI_ACDATA	E21	VCC180AON	F2	VSS	D34
MHSI_ACFLAG	F16	VCC180AON	A21	VSS	D6
MHSI_ACREADY	G21	VCC180AON	AA39	VSS	E7

Table 9-88.Pin List (Bottom View)—Arranged by Pin Name (Sheet 6 of 7)

Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number
MHSI_ACWAKE	E15	VCC180AON	AC39	VSS	F12
MHSI_CADATA	D18	VCC180AON	N39	VSS	F14
MHSI_CAFLAG	D20	VCC180AON	W39	VSS	F18
MHSI_CAREADY	E19	VCCA100_CPUPLL	A27	VSS	F20
MHSI_CAWAKE	C21	VCCA100_CPUPLL	A19	VSS	F26
MHSI_RCOMP	B20	VCCA100_DPHYPLL	L19	VSS	G11
MPTI_CLK	AR7	VCCA100_DSIPLL	K18	VSS	G25
MPTI_D0	AU5	VCCA100_HFHPLL	G27	VSS	G29
MPTI_D1	AT8	VCCA100AS_LFHPLL	J27	VSS	G37
MPTI_D2	AT6	VCCA100AS_USBPLL	H26	VSS	G5
MPTI_D3	AP8	VCC108AON_SRAM	AA29	VSS	G7
OSC_CLK_CTRL0	C13	VCC108AS	AB30	VSS	H10
OSC_CLK_CTRL1	E9	VCC108AS	F32	VSS	H2
OSC_CLK0	G15	VCC108	AA21	VSS	H30
OSC_CLK1	D16	VCC108	AA23	VSS	H34
OSC_CLK2	G17	VCC108	AA25	VSS	H8
OSC_CLK3	H14	VCC108	AB12	VSS	J19
OSCIN	C9	VCC108	AB22	VSS	J25
OSCOUT	E11	VCC108	AB24	VSS	J29
GP_SPI_0_CLK	T36	VCC108	AC11	VSS	J3
GP_SPI_0_SDI	U35	VCC108	AC21	VSS	J31
GP_SPI_0_SDO	T34	VCC108	AC23	VSS	K12
GP_SPI_0_SS0	T32	VCC108	AC25	VSS	K14
GP_SPI_1_CLK	AV28	VCC108	AD12	VSS	K16
GP_SPI_1_SDI	AM28	VCC108	AE11	VSS	K20
GP_SPI_1_SDO	AR27	VCC108	N11	VSS	K26
GP_SPI_1_SS0	AN29	VCC108	N17	VSS	K8
GP_SPI_1_SS1	AT30	VCC108	K28	VSS	L3
GP_SPI_1_SS2	AP28	VCC108	L29	VSS	L31
GP_SPI_1_SS3	AV30	VCCSENSE	P24	VSS	L37
GP_SPI_1_SS4	AR29	VNNAON	AC29	VSS	M14
GP_SPI_2_CLK	K34	VNNAON	AF28	VSS	M16
GP_SPI_2_SDI	M34	VNNAON	AF30	VSS	M18
GP_SPI_2_SDO	M38	VNNAON	AJ11	VSS	M28
GP_SPI_2_SS0	M32	VNNAON	AL17	VSS	M30
GP_SPI_2_SS1	M36	VNNAON	J11	VSS	M6
GP_SPI_3_CLK	L35	VNNAON	K10	VSS	P10
GP_SPI_3_SDI	K38	VNNAON	K30	VSS	P18

Table 9-88.Pin List (Bottom View)—Arranged by Pin Name (Sheet 7 of 7)

Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number
GP_SPI_3_SDO	L33	VNNAON	N29	VSS	P2
GP_SPI_3_SS0	J35	VNNAON	R29	VSS	P28
GP_SD_0_CD#	AL5	VNNAON	U29	VSS	P30
GP_SD_0_CLK	AK8	VNNAON	W11	VSS	P34
GP_SD_0_CMD	AK6	VNNAON	W29	VSS	P6
GP_SD_0_D0	AJ5	VNN	AA15	VSS	R31
GP_SD_0_D1	AJ7	VNN	AA17	VSS	R37
GP_SD_0_D2	AG5	VNN	AB16	VSS	T18
GP_SD_0_D3	AJ9	VNN	AC15	VSS	T20
GP_SD_0_D4	AH8	VNN	AC17	VSS	T28
GP_SD_0_D5	AH4	VNN	AD16	VSS	T30
GP_SD_0_D6	AG9	VNN	AD18	VSS	U31
GP_SD_0_D7	AG3	VNN	AE15	VSS	V12
GP_SD_0_WP	AK4	VNN	AE17	VSS	V18
GP_SD_0_PWR	AN17	VNN	AE19	VSS	V2
GP_SDIO_1_CLK	AM2	VNN	AE21	VSS	V28
GP_SDIO_1_CMD	AP2	VNN	AE23	VSS	V30
GP_SDIO_1_D0	AN7	VNN	AE25	VSS	V34
GP_SDIO_1_D1	AM4	VNN	AE27	VSS	W13
GP_SDIO_1_D2	AN5	VNN	AF14	VSS	W25
GP_SDIO_1_D3	AM8	VNN	AF16	VSS	W31
GP_SDIO_1_PWR	AR13	VNN	AF18	VSS	W37
GP_SDIO_2_CLK	AM6	VNN	AF20	VSS	Y12
GP_SDIO_2_CMD	AP4	VNN	AF22	VSS	Y18
GP_SDIO_2_D0	AR5	VNN	AF24	VSS	Y20
GP_SDIO_2_D1	AR3	VNN	AF26	VSS	Y22
GP_SDIO_2_D2	AU3	VNN	AG13	VSS	Y24
GP_SDIO_2_D3	AT2	VNN	AG15	VSS	Y26
GP_SDIO_2_PWR	AR11	VNN	AG19	VSS	Y28
SVID_CLKOUT	N35	VNN	AG23	VSS	Y30
SVID_CLKSYNCH	R33	VNN	AG27	VSS	Y34
SVID_DIN	P38	VNN	AH14	VSS	Y6
SVID_DOUT	P32	VNN	AH16	ZQ_A	AV20
THERMTRIP#	B18	VNN	AH18	ZQ_B	AM38
PROCHOT#	H20	VNN	AH20		
RESETOUT#	G35	VNN	AH22		

Table 9-89.Pad List (Top View)—Arranged by Pad Name (Sheet 1 of 2)

Pad Name	Pad Number	Pad Name	Pad Number	Pad Name	Pad Number
CA0_B	S_AF25	CK_t_a	S_W26	VDDCA_A	S_P26
CA1_B	S_AG24	CK_c_a	S_W25	VDDQ_a/b	S_T2
CA2_B	S_AF24	CKE0_A	S_V26	VDDCA_A	S_Y26
CA3_B	S_AG23	CKE1_A	S_V27	VDDQ_a/b	S_AB2
CA4_B	S_AF22	CSB0_a	S_U25	VDDCA_A	S_AD26
CA5_B	S_AG16	CSB1_a	S_U26	VDDQ_a/b	S_AF2
CA6_B	S_AG15	DM0_A	S_T1	VDDQ_a/b	S_AF8
CA7_B	S_AF15	DM1_A	S_W3	VDDCA_B	S_AF13
CA8_B	S_AG14	DM2_A	S_J2	VDDCA_B	S_AF18
CA9_B	S_AF14	DM3_A	S_AF3	VDDCA_B	S_AF23
Vref(CA)_b	S_AF17	DQ0_A	S_J3	VDDQ_a/b	S_AG4
CK_t_b	S_AF19	DQ1_A	S_K1	VDD1_A/B	S_B1
CK_c_b	S_AG19	DQ10_A	S_AA3	VDD1_A/B	S_B21
CKE0_B	S_AG20	DQ11_A	S_AC2	VDD1_A/B	S_V2
CKE1_B	S_AF20	DQ12_A	S_AC3	VDD1_A/B	S_AE26
CSB0_b	S_AF21	DQ13_A	S_AD1	VDD1_A/B	S_AF12
CSB1_b	S_AG21	DQ14_A	S_AD2	VDD1_A/B	S_AG26
DM0_B	S_B22	DQ15_A	S_AE2	VDD2_A/B	S_A3
DM1_B	S_A19	DQ16_A	S_C1	VDD2_A/B	S_A22
DM2_B	S_G25	DQ17_A	S_C2	VDD2_A/B	S_B27
DM3_B	S_A11	DQ18_A	S_D1	VDD2_A/B	S_M26
DQ0_B	S_F27	DQ19_A	S_E3	VDD2_A/B	S_V1
DQ1_B	S_E26	DQ2_A	S_L2	VDD2_A/B	S_W2
DQ10_B	S_B16	DQ20_A	S_E2	VDD2_A/B	S_AA27
DQ11_B	S_A15	DQ21_A	S_F1	VDD2_A/B	S_AD27
DQ12_B	S_B14	DQ22_A	S_G2	VDD2_A/B	S_AF11
DQ13_B	S_A14	DQ23_A	S_G3	VDD2_A/B	S_AF16
DQ14_B	S_B13	DQ24_A	S_AG5	VDD2_A/B	S_AF26
DQ15_B	S_A12	DQ25_A	S_AF6	VDD2_A/B	S_AG2
DQ16_B	S_N25	DQ26_A	S_AG6	VSS_A/B	S_A2
DQ17_B	S_M27	DQ27_A	S_AF7	VSSQ_b	S_A4
DQ18_B	S_L26	DQ28_A	S_AG8	VSSQ_b	S_A7
DQ19_B	S_L25	DQ29_A	S_AF9	VSSQ_b	S_A13
DQ2_B	S_E25	DQ3_A	S_L3	VSSQ_b	S_A16
DQ20_B	S_K27	DQ30_A	S_AG9	VSSQ_b	S_A20
DQ21_B	S_J25	DQ31_A	S_AF10	VSS_A/B	S_A21
DQ22_B	S_J26	DQ4_A	S_M1	VSSQ_b	S_A25
DQ23_B	S_H27	DQ5_A	S_N2	VSS_A/B	S_A26

Table 9-89.Pad List (Top View)—Arranged by Pad Name (Sheet 2 of 2)

Pad Name	Pad Number	Pad Name	Pad Number	Pad Name	Pad Number
DQ24_B	S_A9	DQ6_A	S_N3	VSSQ_b	S_B11
DQ25_B	S_A8	DQ7_A	S_P1	VSSQ_b	S_E1
DQ26_B	S_B8	DQ8_A	S_AB1	VSSQ_b	S_E27
DQ27_B	S_B7	DQ9_A	S_AA2	VSSQ_a	S_G1
DQ28_B	S_A6	DQS0_t_a	S_R3	VSSQ_b	S_G27
DQ29_B	S_A5	DQS1_t_a	S_Y2	VSSQ_a	S_J1
DQ3_B	S_D27	DQS2_t_a	S_H1	VSSQ_b	S_J27
DQ30_B	S_B5	DQS3_t_a	S_AF4	VSSQ_a	S_L1
DQ31_B	S_B4	DQS0_c_a	S_R2	VSSQ_b	S_L27
DQ4_B	S_C27	DQS1_c_a	S_Y1	VSSQ_a	S_N1
DQ5_B	S_C26	DQS2_c_a	S_H2	VSS_A/B	S_N27
DQ6_B	S_B25	DQS3_c_a	S_AF5	VSSQ_a	S_R1
DQ7_B	S_A24	Vref(DQ)_a	S_U3	VSSCA_a	S_R27
DQ8_B	S_B17	DNU	S_A1	VSS_A/B	S_U1
DQ9_B	S_A17	DNU	S_A27	VSSQ_a	S_U2
DQS0_t_b	S_B23	VACC	S_B2	VSS_A/B	S_U27
DQS1_t_b	S_B18	VACC	S_B26	VSS_A/B	S_W1
DQS2_t_b	S_G26	DNU	S_AG1	VSSCA_a	S_W27
DQS3_t_b	S_B10	DNU	S_AG27	VSSQ_a	S_AA1
DQS0_c_b	S_A23	VDDQ_a/b	S_B3	VSS_A/B	S_AB27
DQS1_c_b	S_A18	VDDQ_a/b	S_B6	VSSQ_a	S_AC1
DQS2_c_b	S_H26	VDDQ_a/b	S_B9	VSSCA_a	S_AC27
DQS3_c_b	S_A10	VDDQ_a/b	S_B12	VSSQ_a	S_AE1
Vref(DQ)_b	S_B20	VDDQ_a/b	S_B15	VSS_A/B	S_AF1
CA0_A	S_P27	VDDQ_a/b	S_B19	VSS_A/B	S_AF27
CA1_A	S_R25	VDDQ_a/b	S_B24	VSSQ_a	S_AG3
CA2_A	S_R26	VDDQ_a/b	S_D2	VSSQ_a	S_AG7
CA3_A	S_T26	VDDQ_a/b	S_D26	VSSQ_a	S_AG10
CA4_A	S_T27	VDDQ_a/b	S_F2	VSS_A/B	S_AG11
CA5_A	S_Y27	VDDQ_a/b	S_F26	VSSCA_b	S_AG13
CA6_A	S_AA26	VDDQ_a/b	S_K2	VSS_A/B	S_AG17
CA7_A	S_AB26	VDDQ_a/b	S_K26	VSSCA_b	S_AG18
CA8_A	S_AC25	VDDQ_a/b	S_M2	VSSCA_b	S_AG22
CA9_A	S_AC26	VDDQ_a/b	S_N26	VSS_A/B	S_AG25
Vref(CA)_a	S_AA25	VDDQ_a/b	S_P2	ZQ_B	S_AG12
				ZQ_A	S_AE27

Table 9-90.Pin Location (Top View, Left Side) (Sheet 1 of 2)

	39	38	37	36	35	34	33	32	31	30	29	28	27	
AW	VSS		RSVD		VDD2		VCC122_180AON_I2C		VCC122AON_MEM		VCC122AON_MEM		VCC122AON_MEM	AW
AV		VSS		ULPI_1_CLK		VDD2		VSS		GP_SPI_1_SS3		GP_SPI_1_CLK		AV
AU	VSS		ULPI_1_DIR		ULPI_1_D4		ULPI_1_D2		ULPI_1_D3		VSS		GP_I2C_1_SCL	AU
AT		GP_LPC_AD2		ULPI_1_REFCLK		ULPI_1_D7		ULPI_1_D0		GP_SPI_1_SS1		GP_I2C_0_SCL		AT
AR	VSS		VSS		ULPI_1_D6		ULPI_1_STP		ULPI_1_D1		GP_SPI_1_SS4		GP_SPI_1_SDO	AR
AP		GP_AON_094		GP_LPC_FRAME#		VSS		ULPI_1_NXT		VSS		GP_SPI_1_SS2		AP
AN	VDD1		GP_LPC_AD3		GP_LPC_AD0		GP_LPC_CLKOUT		ULPI_1_D5		GP_SPI_1_SS0		GP_I2C_0_SDA	AN
AM		ZQ_B		VSS		GP_AON_093		GP_AON_089		VCC122AON		GP_SPI_1_SDI		AM
AL	VCC122_180AON_I2S		VSS		GP_LPC_AD1		GP_LPC_RESET#		VSS		VCC122AON_MEM		VCC108	AL
AK		VDD2		GP_LPC_CLKRUN		GP_XDP_C0_BPM1#		GP_XDP_C0_BPM0#		VCC122AON_MCLK		VCC108		AK
AJ	VCC122AON_MEM		GP_XDP_C1_BPM0#		GP_XDP_C0_BPM2#		GP_XDP_C0_BPM3#		VSS		VSS		VNN	AJ
AH		GP_XDP_C1_BPM3#		GP_XDP_PREQ#		VSS		GP_XDP_C1_BPM2#		VCC122AON_MEM		VSS		AH
AG	VCC122AON_MEM		VSS		GP_XDP_PRDY#		GP_XDP_C1_BPM1#		VSS		VSS		VNN	AG
AF		GP_AON_042		GP_AON_043		VSS		GP_XDP_BLK_DP		VNNAON		VNNAON		AF
AE	VCC122AON_MEM		GP_XDP_BLK_DN		GP_AON_049		GP_XDP_PWRMODE0		VSS		VSS		VNN	AE
AD		VSS		GP_XDP_PWRMODE1		ULPI_0_D1		VSS		VSS		VSS		AD
AC	VCC180AON		VSS		ULPI_0_D5		ULPI_0_D3		VSS		VNNAON		VCC	AC
AB		VSS		ULPI_0_D7		VSS		GP_AON_044		VCC108AS		VSS		AB
AA	VCC180AON		GP_XDP_PWRMODE2		ULPI_0_D6		GP_AON_045		VSS		VCC108AON_SRAM		VCC	AA
Y		ULPI_0_NXT		ULPI_0_D0		VSS		ULPI_0_D2		VSS		VSS		Y
W	VCC180AON		VSS		ULPI_0_CLK		ULPI_0_D4		VSS		VNNAON		VCC	W

Table 9-90.Pin Location (Top View, Left Side) (Sheet 2 of 2)

	39	38	37	36	35	34	33	32	31	30	29	28	27	
V		VDD2		ULPI_0_STP		VSS		ULPI_0_CIR		VSS		VSS		V
U	VCC122AON_MEM		RSVD		GP_SPI_0_SDI		ULPI_0_REFCLK		VSS		VNNAON		VCC	U
T		PMIC_RESET#		GP_SPI_0_CLK		GP_SPI_0_SDO		GP_SPI_0_SS0		VSS		VSS		T
R	VCC122AON_MEM		VSS		PMIC_PWRGOOD		SVID_CLKSYNCH		VSS		VNNAON		VCC	R
P		SVID_DIN		I2S_2_TXD		VSS		SVID_DOUT		VSS		VSS		P
N	VCC180AON		I2S_2_RXD		SVID_CLKOUT		I2S_2_CLK		I2S_2_FS		VNNAON		VCC	N
M		GP_SPI_2_SDO		GP_SPI_2_SS1		GP_SPI_2_SDI		GP_SPI_2_SS0		VSS		VSS		M
L	VCC122AON		VSS		GP_SPI_3_CLK		GP_SPI_3_SDO		VSS		VCC108		VCC	L
K		GP_SPI_3_SDI		GP_I2S_3_TXD		GP_SPI_2_CLK		GP_AON_051		VNNAON		VCC108		K
J	VCC122AON		GP_AON_072		GP_SPI_3_SS0		GP_UART_2_TX		VSS		VSS		VCCA100AS_LFHPLL	J
H		GP_I2S_3_RXD		GP_COMS_INT0		VSS		GP_COMS_INT2		VSS		VCC122AON_MEM		H
G	VCC122_180AON_I2S		VSS		RESETOUT#		GP_COMS_INT3		GP_COMS_INT1		VSS		VCCA100_HFHPLL	G
F		GP_AON_060		GP_AON_061		GP_AON_063		VCC108AS		GP_I2S_1_FS		RSVD		F
E	VCC122AON_MEM		GP_UART_1_RTS		GP_UART_1_TX		GP_UART_2_RX		GP_I2S_1_TXD		GP_I2S_1_CLK		RSVD	E
D		VCC122AON_MEM		GP_UART_1_RX		VSS		GP_I2S_0_CLK		GP_I2S_3_CLK		GP_I2S_0_FS		D
C	VCC122AON_MEM		GP_AON_062		GP_UART_1_CTS		GP_I2S_0_TXD		VSS		VSS		VSS	C
B		VSS		VDD2		VCC122AON_MEM		GP_I2S_0_RXD		GP_I2S_3_FS		GP_I2S_1_RXD		B
A	VCC122AON_MEM		VCC122AON_MEM		VDD2		VCC122AON_MEM		VCC122AON_MEM		VDD1		VCCA100_CPUPLL	A
	39	38	37	36	35	34	33	32	31	30	29	28	27	

Table 9-91.Pin Location (Top View, Center) (Sheet 1 of 2)

	26	25	24	23	22	21	20	19	18	17	16	15	14	
AW		VDD2		VCC180 AON		VNN		VNN		VDD2		VCC180 AON		AW
AV	GP_I2C_2_SDA		VCC180 AON		VCC180 AON		ZQ_A		VDD1		GP_AON_078		GP_CORE_018	AV
AU		VSS		EMMC_1_D1		VSS		EMMC_0_D4		VSS		GP_CORE_020		AU
AT	GP_I2C_1_SDA		M_RCOMP0		EMMC_1_D3		EMMC_0_D3		EMMC_0_CLK		GP_CORE_015		GP_AON_079	AT
AR		M_RCOMP1		EMMC_1_D0		EMMC_0_D0		EMMC_RCOMP		EMMC_0_D7		GP_AON_077		AR
AP	VSS		EMMC_0_CMD		VSS		EMMC_0_D2		VSS		GP_AON_076		VSS	AP
AN		M_RCOMP2		EMMC_1_D2		EMMC_1_D6		EMMC_1_CLK		GP_SD_0_PWR		GP_CORE_017		AN
AM	GP_I2C_2_SCL		EMMC_1_CMD		EMMC_1_D5		EMMC_0_D1		EMMC_0_D6		GP_CORE_012		GP_UART_0_RX	AM
AL		VCC122AON_MCLK		EMMC_1_D7		EMMC_1_D4		EMMC_0_D5		VNNAON		VSS		AL
AK	VSS		VSS		VSS		VSS		VSS		VSS		VSS	AK
AJ		VNN		VNN		VNN		VNN		VNN		VNN		AJ
AH	VNN		VNN		VNN		VNN		VNN		VNN		VNN	AH
AG		VSS		VNN		VSS		VNN		VSS		VNN		AG
AF	VNN		VNN		VNN		VNN		VNN		VNN		VNN	AF
AE		VNN		VNN		VNN		VNN		VNN		VNN		AE
AD	VSS		VSS		VSS		VSS		VNN		VNN		VSS	AD
AC		VCC108		VCC108		VCC108		VCC		VNN		VNN		AC
AB	VSS		VCC108		VCC108		VSS		VSS		VNN		VSS	AB
AA		VCC108		VCC108		VCC108		VCC		VNN		VNN		AA
Y	VSS		VSS		VSS		VSS		VSS		VNN		VNNSENSE	Y
W		VSS		VCC108		VCC108		VCC		VNN		VNN		W
V	RSVD		VCC		VCC		RSVD		VSS		VNN		VCCA100	V
U		RSVD		VCC		RSVD		VCC		VNN		VNN		U

Table 9-91.Pin Location (Top View, Center) (Sheet 2 of 2)

	26	25	24	23	22	21	20	19	18	17	16	15	14	
T	VCCA100		VCC		VCC		VSS		VSS		VNN		VNN	T
R		VCC_VSSENSE		VCC		VCC		VCC		VNN		VNN		R
P	VCC		VCCSENSE		VCC		VCC		VSS		VNN		VNN	P
N		VCC		VCC		VCC		VCC		VCC108		VNN		N
M	VCC		VCC		VCC		VCC		VSS		VSS		VSS	M
L		VCC		VCC		VCC		VCCA100_DPHYPLL		VNN		VNN		L
K	VSS		VCC		VCC		VSS		VCCA100_DSIPLL		VSS		VSS	K
J		VSS		VCC		VCC		VSS		JTAG_TDO		VCC108AON_OSC		J
H	VCCA100AS_USBPLL		VCC		VCC		PROCHOT#		VCC122AON		GP_CORE_070		OSC_CLK3	H
G		VSS		VCC		MHSI_ACREADY		GP_CORE_067		OSC_CLK2		OSC_CLK0		G
F	VSS		VCC		VCC		VSS		VSS		MHSI_ACFLAG		VSS	F
E		VCC		VCC		MHSI_ACDATA		MHSI_CAREADY		JTAG_TRST#		MHSI_ACWAKE		E
D	VCC		VCC		VCC		MHSI_CAFLAG		MHSI_CADATA		OSC_CLK1		JTAG_TDI	D
C		VCC		VCC		MHSI_CAWAKE		VSS		GP_CORE_072		VSS		C
B	VCC		VCC		VCC		MHSI_RCOMP		THERMTRIP#		IERR#		JTAG_TCK	B
A		VCC		VCC		VCC180AON		VCCA100_CPUPLL		VCC122AON_MEM		VCC122AON_MEM		A
	26	25	24	23	22	21	20	19	18	17	16	15	14	

Table 9-92.Pin Location (Top View, Right Side) (Sheet 1 of 3)

	13	12	11	10	9	8	7	6	5	4	3	2	1	
AW	VCC180AON		VCC122AON		VCC122AON_MEM		VDD2		VDD2		VCC122AON_MEM		VCC122AON_MEM	AW
AV		GP_EMMC_0_RST#		VCC122AON_MEM		GP_UART_0_TX		GP_CAMERA_SB0		GP_CAMERA_SB3		VSS		AV
AU	VSS		GP_CORE_032		VSS		GP_CAMERA_SB2		MPTI_D0		GP_SDIO_2_D2		VCC122AON_MEM	AU
AT		VSS		GP_CAMERA_SB1		MPTI_D1		MPTI_D2		VSS		GP_SDIO_2_D3		AT
AR	GP_SDIO_1_PWR		GP_SDIO_2_PWR		GP_UART_0_RTS		MPTI_CLK		GP_SDIO_2_D0		GP_SDIO_2_D1		VCC122AON_MEM	AR
AP		GP_CORE_016		VSS		MPTI_D3		VSS		GP_SDIO_2_CMD		GP_SDIO_1_CMD		AP
AN	GP_EMMC_1_RST#		GP_UART_0_CTS		GP_CORE_033		GP_SDIO_1_D0		GP_SDIO_1_D2		VSS		VCC122AON_MEM	AN
AM		GP_CORE_030		GP_CORE_031		GP_SDIO_1_D3		GP_SDIO_2_CLK		GP_SDIO_1_D1		GP_SDIO_1_CLK		AM
AL	VSS		VSS		VSS		GPIO_RCOMP30		GP_SD_0_CD#		GPIO_RCOMP18		VCC122AON_MEM	AL
AK		VSS		VCC122AON_MEM		GP_SD_0_CLK		GP_SD_0_CMD		GP_SD_0_WP		VCCSDIO		AK
AJ	VNN		VNNAON		GP_SD_0_D3		GP_SD_0_D1		GP_SD_0_D0		VSS		VCC180AON	AJ
AH		VSS		VSS		GP_SD_0_D4		VSS		GP_SD_0_D5		VDD2		AH
AG	VNN		VSS		GP_SD_0_D6		VSS		GP_SD_0_D2		GP_SD_0_D7		VDD2	AG
AF		VSS		VSS		VSS		GP_I2C_5_SCL		GP_I2C_4_SDA		VCC122AON		AF
AE	VSS		VCC108		VSS		GP_CORE_082		GP_I2C_4_SCL		VSS		VDD1	AE
AD		VCC108		VSS		GP_CAMERA_SB4		VSS		GP_CORE_007		GP_I2C_5_SDA		AD
AC	VSS		VCC108		VSS		RSVD		GP_CAMERA_SB5		GP_CAMERA_SB9		VCC122AON_MEM	AC
AB		VCC108		VSS		GP_CAMERA_SB6		GP_CAMERA_SB8		GP_MDSI_A_TE		GP_CAMERA_SB7		AB

Table 9-92.Pin Location (Top View, Right Side) (Sheet 2 of 3)

	13	12	11	10	9	8	7	6	5	4	3	2	1	
AA	VNN_VSSSENSE		VSS		MCSI_X4_DN2		MCSI_X4_DP2		MCSI_X4_DP0		MCSI_X4_DN0		VCC122AON_MEM	AA
Y		VSS		VCC122AON_MEM		MCSI_COMP		VSS		MCSI_X4_DP1		MCSI_X4_DN1		Y
W	VSS		VNNAON		MCSI_X1_DP		MCSI_X1_DN		MCSI_X4_CLKP		MCSI_X4_CLKN		VCC122AON_MEM	W
V		VSS		MCSI_X1_CLKP		MCSI_X1_CLKN		MCSI_X4_DP3		MCSI_X4_DN3		VSS		V
U	VNN		VNN		VNN		VNN		VNN		VNN		VNN	U
T		VNN		VNN		VNN		VNN		VNN		VNN		T
R	VNN		VNN		VNN		VNN		VNN		VNN		VNN	R
P		VNN		VSS		VNN		VSS		VNN		VSS		P
N	VNN		VCC108		MDSI_A_DP0		MDSI_A_DN0		MDSI_A_DP1		MDSI_A_DN1		VCC122AON	N
M				MDSI_A_CLKP		MDSI_A_CLKN		VSS		RSVD		RSVD		M
L	VNN		VNN		MDSI_COMP		MDSI_A_DN2		MDSI_A_DP2		VSS		VCC122AON	L
K		VSS		VNNAON		VSS		GP_CORE_073		MDSI_A_DP3		MDSI_A_DN3		K
J	VCC122AON_MEM		VNNAON		GP_CORE_075		GP_CORE_037		GP_CORE_074		VSS		VCC122AON_MEM	J
H		RSVD		VSS		VSS		HDMI_EXTR		GP_I2C_3_SDA_HDMI		VSS		H
G	RSVD		VSS		VCC122AON		VSS		VSS		RSVD		VCC122AON_MEM	G
F		VSS		RSVD		GP_I2C_3_SCL_HDMI		VCCA100AS		RSVD		VCC180AON		F
E	JTAG_TMS		OSCOUT		OSC_CLK_CTRL1		VSS		HDMI_5V_DET		HDMI_CLKN		VCC180AON	E
D		GP_CORE_068		GP_CORE_071		HDMI_DN0		VSS		RSVD		HDMI_CLKP		D

Table 9-92.Pin Location (Top View, Right Side) (Sheet 3 of 3)

	13	12	11	10	9	8	7	6	5	4	3	2	1	
C	OSC_CLK_CTRL0		VSS		OSCIN		HDMI_DP1		HDMI_DN2		VDD1		VDD1	C
B		GP_CORE_069		RSVD		HDMI_DP0		HDMI_DP2		VDD2		VSS		B
A	VCC122AON_MEM		VCC330		VCC180AON		HDMI_DN1		VSS		VDD2		VSS	A
	13	12	11	10	9	8	7	6	5	4	3	2	1	

Table 9-93.Topside Pinmap (Left-Side)

	27	26	25	24	23	22	21	20	19	18	17	16	15	14	
S_AG	NC	VDD1_A/B	VSS_A/B	CA1_B	CA3_B	VSS_A/B	CSB1_b	CKE0_B	CK_c_b	VSS_A/B	VSS_A/B	CA5_B	CA6_B	CA8_B	S_AG
S_AF	VSS_A/B	VDD2_A/B	CA0_B	CA2_B	VDDQ_a/b	CA4_B	CSB0_b	CKE1_B	CK_t_b	VDDQ_a/b	Vref(CA)_b	VDD2_A/B	CA7_B	CA9_B	S_AF
S_AE	ZQ_A	VDD1_A/B													S_AE
S_AD	VDD2_A/B	VDDQ_a/b													S_AD
S_AC	VSS_A/B	CA9_A	CA8_A												S_AC
S_AB	VSS_A/B	CA7_A													S_AB
S_AA	VDD2_A/B	CA6_A	Vref(CA)_a												S_AA
S_Y	CA5_A	VDDQ_a/b													S_Y
S_W	VSS_A/B	CK_t_a	CK_c_a												S_W
S_V	CKE1_A	CKE0_A													S_V
S_U	VSS_A/B	CSB1_a	CSB0_a												S_U
S_T	CA4_A	CA3_A													S_T
S_R	VSS_A/B	CA2_A	CA1_A												S_R
S_P	CA0_A	VDDQ_a/b													S_P
S_N	VSS_A/B	VDDQ_a/b	DQ16_B												S_N
S_M	DQ17_B	VDD2_A/B													S_M
S_L	VSS_A/B	DQ18_B	DQ19_B												S_L
S_K	DQ20_B	VDDQ_a/b													S_K
S_J	VSS_A/B	DQ22_B	DQ21_B												S_J
S_H	DQ23_B	DQS2_c_b													S_H
S_G	VSS_A/B	DQS2_t_b	DM2_B												S_G
S_F	DQ0_B	VDDQ_a/b													S_F
S_E	VSS_A/B	DQ1_B	DQ2_B												S_E
S_D	DQ3_B	VDDQ_a/b													S_D
S_C	DQ4_B	DQ5_B													S_C
S_B	VDD2_A/B	NC	DQ6_B	VDDQ_a/b	DQS0_t_b	DM0_B	VDD1_A/B	Vref(DQ)_b	VDDQ_a/b	DQS1_t_b	DQ8_B	DQ10_B	VDDQ_a/b	DQ12_B	S_B
S_A	NC	VSS_A/B	VSS_A/B	DQ7_B	DQS0_c_b	VDD2_A/B	VSS_A/B	VSS_A/B	DM1_B	DQS1_c_b	DQ9_B	VSS_A/B	DQ11_B	DQ13_B	S_A
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	

Table 9-94.TopSide Pinmap (Right-Side)

	13	12	11	10	9	8	7	6	5	4	3	2	1	
S_AG	VSS_A/B	ZQ_B	VSS_A/B	VSS_A/B	DQ30_A	DQ28_A	VSS_A/B	DQ26_A	DQ24_A	VDDQ_a/b	VSS_A/B	VDD2_A/B	NC	S_AG
S_AF	VDDQ_a/b	VDD1_A/B	VDD2_A/B	DQ31_A	DQ29_A	VDDQ_a/b	DQ27_A	DQ25_A	DQS3_c_a	DQS3_t_a	DM3_A	VDDQ_a/b	VSS_A/B	S_AF
S_AE												DQ15_A	VSS_A/B	S_AE
S_AD												DQ14_A	DQ13_A	S_AD
S_AC											DQ12_A	DQ11_A	VSS_A/B	S_AC
S_AB												VDDQ_a/b	DQ8_A	S_AB
S_AA											DQ10_A	DQ9_A	VSS_A/B	S_AA
S_Y												DQS1_t_a	DQS1_c_a	S_Y
S_W											DM1_A	VDD2_A/B	VSS_A/B	S_W
S_V												VDD1_A/B	VDD2_A/B	S_V
S_U											Vref(DQ)_a	VSS_A/B	VSS_A/B	S_U
S_T												VDDQ_a/b	DM0_A	S_T
S_R											DQS0_t_a	DQS0_c_a	VSS_A/B	S_R
S_P												VDDQ_a/b	DQ7_A	S_P
S_N											DQ6_A	DQ5_A	VSS_A/B	S_N
S_M												VDDQ_a/b	DQ4_A	S_M
S_L											DQ3_A	DQ2_A	VSS_A/B	S_L
S_K												VDDQ_a/b	DQ1_A	S_K
S_J											DQ0_A	DM2_A	VSS_A/B	S_J
S_H												DQS2_c_a	DQS2_t_a	S_H
S_G											DQ23_A	DQ22_A	VSS_A/B	S_G
S_F												VDDQ_a/b	DQ21_A	S_F
S_E											DQ19_A	DQ20_A	VSS_A/B	S_E
S_D												VDDQ_a/b	DQ18_A	S_D
S_C												DQ17_A	DQ16_A	S_C
S_B	DQ14_B	VDDQ_a/b	VSS_A/B	DQS3_t_b	VDDQ_a/b	DQ26_B	DQ27_B	VDDQ_a/b	DQ30_B	DQ31_B	VDDQ_a/b	NC	VDD1_A/B	S_B
S_A	VSS_A/B	DQ15_B	DM3_B	DQS3_c_b	DQ24_B	DQ25_B	VSS_A/B	DQ28_B	DQ29_B	VSS_A/B	VDD2_A/B	VSS_A/B	NC	S_A
	13	12	11	10	9	8	7	6	5	4	3	2	1	

9.2 Mechanical and Package Acronyms

Table 9-95.Mechanical and Package Acronyms

Acronym	Description
BO	Ball Out
DO	Die Outline
PL	Pin List

9.3 Package Specifications

The Intel® Atom™ Processor Z2760 is HF (Halogen Free)[1] and EU RoHS Compliant [2].

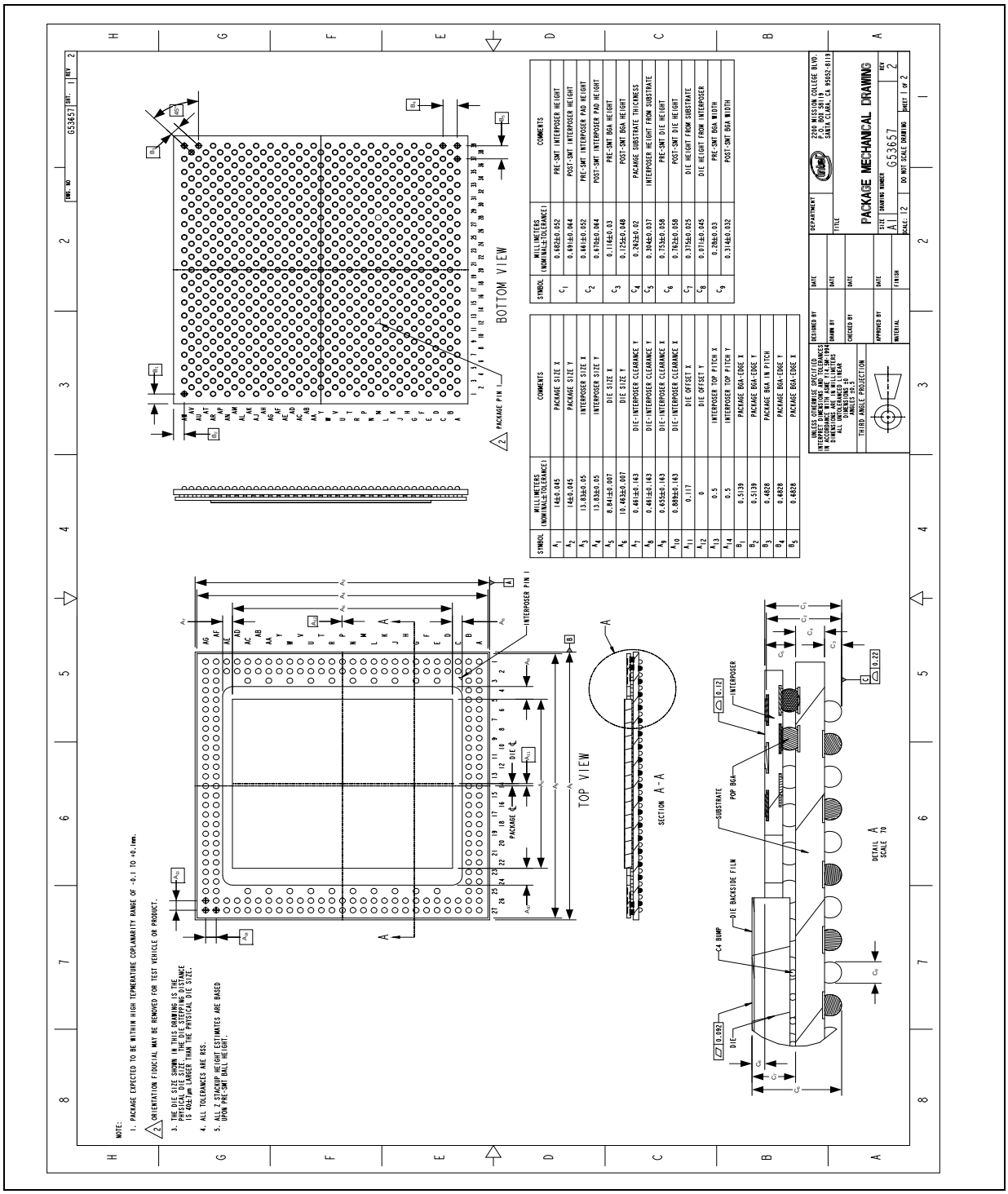
1. Halogen Free: Applies only to halogenated flame retardants and PVC in components. Halogens are below 900 PPM bromine and 900 PPM chlorine.
2. Compliant with EU RoHS Directive 2002/95/EC, 27 January 2003. Some EU RoHS exemptions may apply.
   a. Intel Material Declaration Data Sheets are available at http://intel.pcnalert.com/
   b. Select 'Search MDDS Database'.
   c. Information about theIntel® Atom™ Processor Z2760 will be available in the future on this web site.

Dimensions:

- Package parameters: 14 mm x 14 mm
- Ball Count bottom of package: 760
- Pad count top of package (LPDDR-2 interface): 220

9.4 Package Diagrams

Figure 9-21.Package Mechanical Drawing



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