

# **Intel® Xeon® Processor E5-1600/2600/4600 v1 and v2 Product Families**

**Thermal / Mechanical Design Guide**

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*September 2013*



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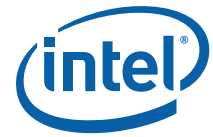
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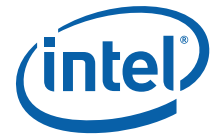
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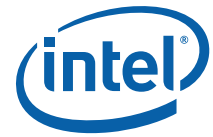
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## Revision History

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Revision Number	Description	Revision Date
-001	<ul style="list-style-type: none"><li>Initial Release</li></ul>	March 2012
-002	<ul style="list-style-type: none"><li>Added section 5.3.6 Short Duration TCC Activation and Catastrophic Thermal Management</li></ul>	September 2012
-003	<ul style="list-style-type: none"><li>Added E-5 v2 Product Family information</li></ul>	September 2013

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# 1 Introduction

This document provides guidelines for the design of thermal and mechanical solutions for the:

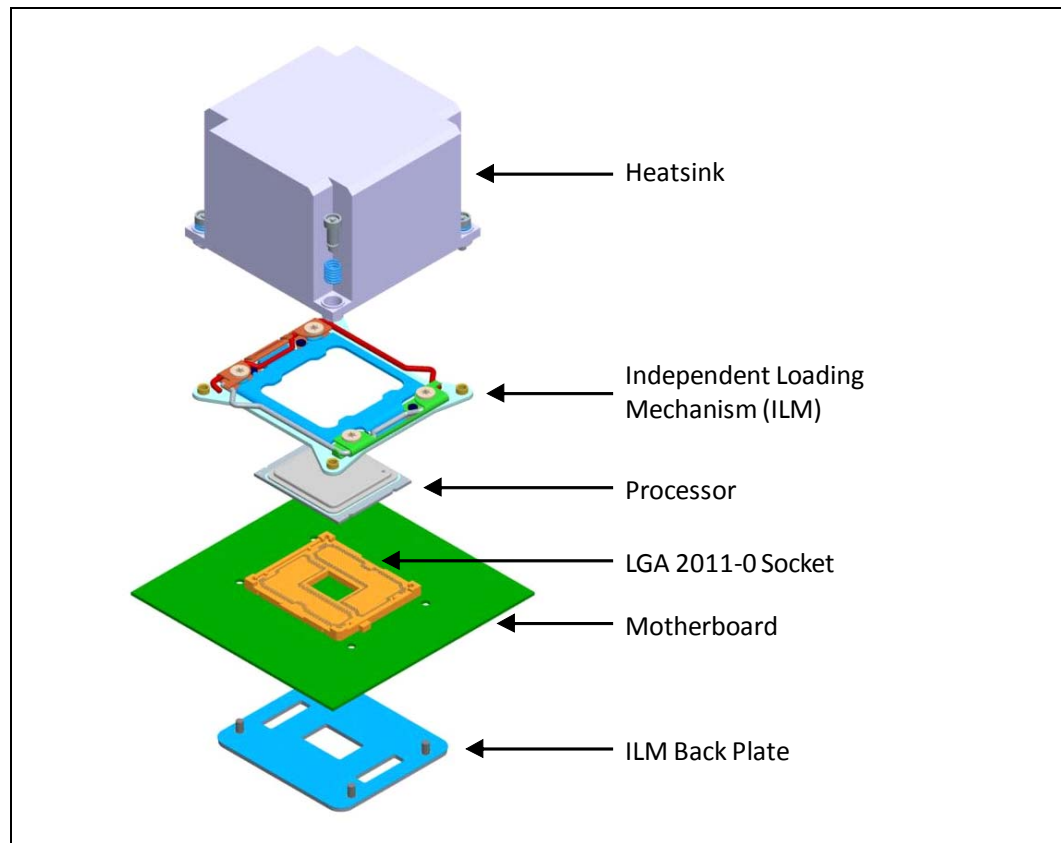
- Intel® Xeon® Processor E5-1600/2600/4600 v1 and v2 Product Families

processors in 2 and 4-socket servers, and 2-socket workstations. The processors covered are listed in the processor family datasheets listed in [Table 1-1](#).

The components described in this document include:

- The processor thermal solution (heatsink) and associated retention hardware.
- The LGA2011-0 socket, the Independent Loading Mechanism (ILM) and back plate.

**Figure 1-1. Platform Socket Stack**



The goals of this document are:

- To assist board and system thermal mechanical designers.
- To assist designers and suppliers of processor heatsinks.

Thermal profiles and other processor specifications are provided in the appropriate processor Datasheet.



## 1.1 References

Material and concepts available in the following documents may be beneficial when reading this document.

**Table 1-1. Reference Documents**

Document	Notes
<i>European Blue Angel Recycling Standards</i>	1
<i>Platform Environment Control Interface (PECI) Specification</i>	4
<i>Platform Digital Thermal Sensor (DTS) Based Thermal Specifications and Overview</i>	4
<i>Manufacturing With Intel Components Using Lead-Free Technology</i>	3
<i>Entry-level Electronics Bay Specification</i>	2
<i>Intel® Xeon® Processor E5-1600/2600/4600 v1 Product Families Datasheet - Volume One (326508)</i>	3
<i>Intel® Xeon® Processor E5-1600/2600/4600 v1 Product Families Datasheet - Volume Two (326509)</i>	3
<i>Intel® Xeon® Processor E5-1600 and E5-2600 v2 Product Families Datasheet - Volume One (329187)</i>	3
<i>Intel® Xeon® Processor E5-1600 and E5-2600 v2 Product Families Datasheet - Volume Two (329188)</i>	3
<i>Intel® Xeon® Processor E5-1600/2600/4600 v1 Product Families Specification Update (326510)</i>	3
<i>Intel® Xeon® Processor E5-1600 and E5-2600 v2 Product Families Specification Update (329189)</i>	3
<i>Intel® Xeon® Processor E5-1600/2600/4600 v1 and v2 Product Families – Thermal Model (326608)</i>	3
<i>Intel® Xeon® Processor E5-1600/2600/4600 v1 Product Families – Mechanical Model (326609)</i>	3
<i>Intel® Xeon® Processor E5-1600 and E5-2600 v2 Product Families – Mechanical Model (329299)</i>	3

**Notes:**

1. Available at <http://www.blauer-engel.de>
2. Available at <http://ssiforum.oaktree.com/>
3. Available at <https://learn.intel.com/portal/scripts/general/logon.aspx> (Code: ME709). Available electronically.
4. Contact your Intel representative for the latest version.

## 1.2 Definition of Terms

**Table 1-2. Terms and Descriptions (Sheet 1 of 2)**

Term	Description
Bypass	Bypass is the area between a passive heatsink and any object that can act to form a duct. For this example, it can be expressed as a dimension away from the outside dimension of the fins to the nearest surface.
DTS	Digital Thermal Sensor reports a relative die temperature as an offset from TCC activation temperature.
FSC	Fan Speed Control
IHS	Integrated Heat Spreader: a component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
Square ILM	Independent Loading Mechanism provides the force needed to seat the 2011-LGA package onto the socket contacts and has 80 × 80mm heatsink mounting hole pattern.



Table 1-2. Terms and Descriptions (Sheet 2 of 2)

Term	Description
Narrow ILM	Independent Loading Mechanism provides the force needed to seat the 2011-LGA package onto the socket contacts and has 56 × 94mm heatsink mounting hole pattern
LGA2011-0 socket	The processor mates with the system board through this surface mount, 2011-contact socket for Intel® Xeon® Processor 5-1600/E5-2600/E5-4600 Product Families-based platform.
PECI	The Platform Environment Control Interface (PECI) is a one-wire interface that provides a communication channel between Intel processor and chipset components to external monitoring devices.
$\Psi_{CA}$	Case-to-ambient thermal characterization parameter (psi). A measure of thermal solution performance using total package power. Defined as $(T_{CASE} - T_{LA}) / \text{Total Package Power}$ . Heat source should always be specified for $\Psi$ measurements.
$\Psi_{CS}$	Case-to-sink thermal characterization parameter. A measure of thermal interface material performance using total package power. Defined as $(T_{CASE} - T_S) / \text{Total Package Power}$ .
$\Psi_{SA}$	Sink-to-ambient thermal characterization parameter. A measure of heatsink thermal performance using total package power. Defined as $(T_S - T_{LA}) / \text{Total Package Power}$ .
$T_{CASE}$	The case temperature of the processor measured at the geometric center of the topside of the IHS.
$T_{CASE-MAX}$	The maximum case temperature as specified in a component specification.
TCC	Thermal Control Circuit: Thermal monitor uses the TCC to reduce the die temperature by using clock modulation and/or operating frequency and input voltage adjustment when the die temperature is very near its operating limits.
$T_{CONTROL}$	$T_{CONTROL}$ is a static value below TCC activation used as a trigger point for fan speed control. When $DTS > T_{CONTROL}$ , the processor must comply to the thermal profile.
TDP	Thermal Design Power: Thermal solution should be designed to dissipate this target power level. TDP is not the maximum power that the processor can dissipate.
Thermal Monitor	A power reduction feature designed to decrease temperature after the processor has reached its maximum operating temperature.
Thermal Profile	Line that defines case temperature specification of a processor at a given power level.
TIM	Thermal Interface Material: The thermally conductive compound between the heatsink and the processor case. This material fills the air gaps and voids, and enhances the transfer of the heat from the processor case to the heatsink.
$T_{LA}$	The measured ambient temperature locally surrounding the processor. The ambient temperature should be measured just upstream of a passive heatsink or at the fan inlet for an active heatsink.
$T_{SA}$	The system ambient air temperature external to a system chassis. This temperature is usually measured at the chassis air inlets.
U	A unit of measure used to define server rack spacing height. 1U is equal to 1.75 in, 2U equals 3.50 in, and so forth.





## 2 LGA2011-0 Socket

This section describes a surface mount, LGA (Land Grid Array) socket intended for the processors in the Intel® Xeon® Processor E5-1600/2600/4600 v1 and v2 Product Families-based platform. The socket provides I/O, power and ground contacts. The socket contains 2011 contacts arrayed about a cavity in the center of the socket with lead-free solder balls for surface mounting on the motherboard.

The socket has 2011 contacts. The LGA2011-0 socket is introducing a hexagonal area array ball-out which provides many benefits:

- Socket contact density increased by 12% while maintaining 40 mil minimum via pitch requirements.
- Corresponding square pitch array's would require a 38 mil via pitch for the same package size.

LGA2011-0 has 1.016 mm (40 mil) hexagonal pitch in a 58x43 grid array with 24x16 grid depopulation in the center of the array and selective depopulation elsewhere.

Figure 2-1. Hexagonal Array in LGA2011-0

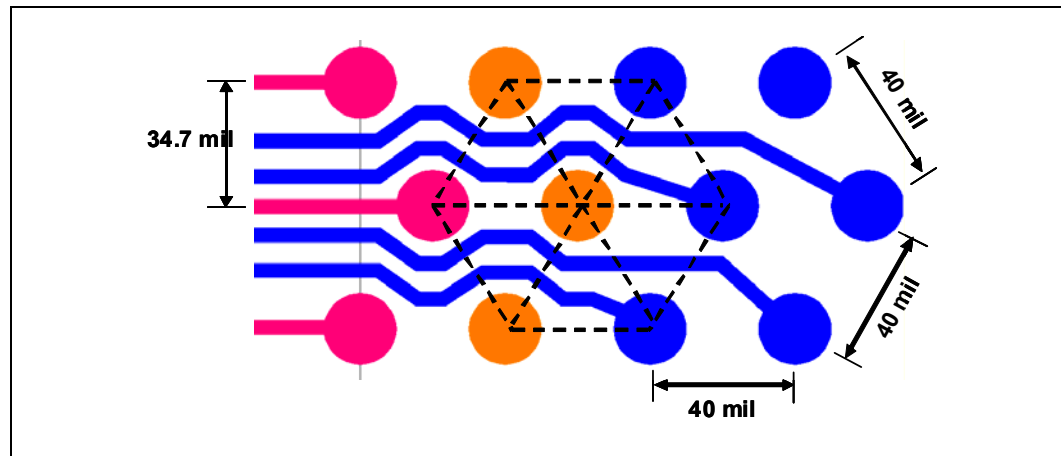
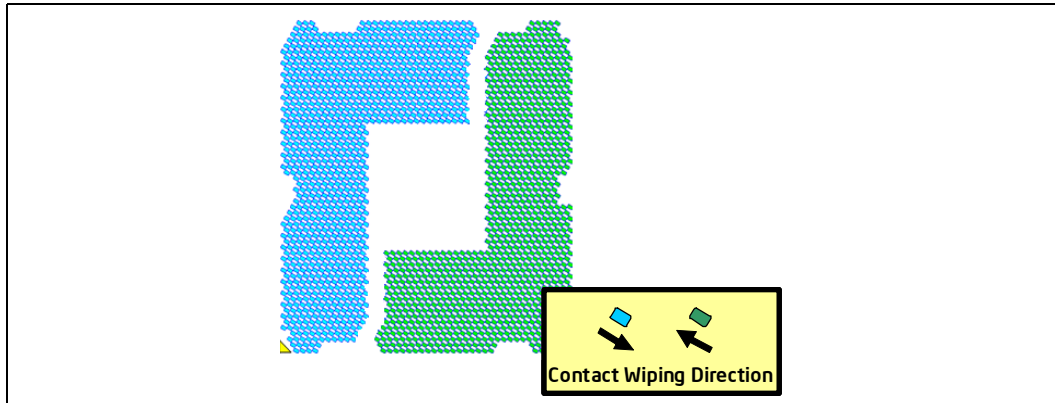


Table 2-1. LGA2011-0 Socket Attributes

LGA2011-0 Socket	Attributes
Component Size	58.5 mm(L)X51 mm (W)
Pitch	1.016 mm (Hex Array)
Ball Count	2011

Contact wiping direction is 180 degrees as shown in Figure 2-2.

Figure 2-2. Contact Wiping Direction



The socket must be compatible with the package (processor) and the Independent Loading Mechanism (ILM). The design includes a back plate which is integral to having a uniform load on the socket solder joints and the contacts. Socket loading specifications are listed in [Chapter 4](#). Schematic for LGA2011-0 socket is shown in [Figure 2-3](#). The seating plane is shown on the outer periphery of the socket.

Figure 2-3. Schematic of LGA2011-0 Socket with Pick and Place Cover Removed

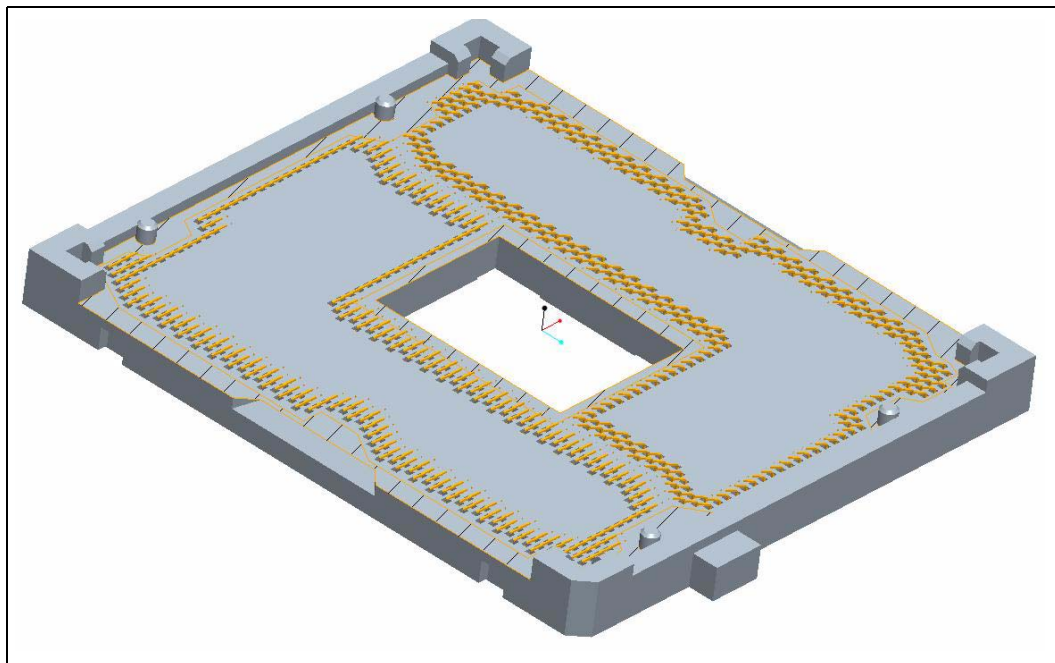
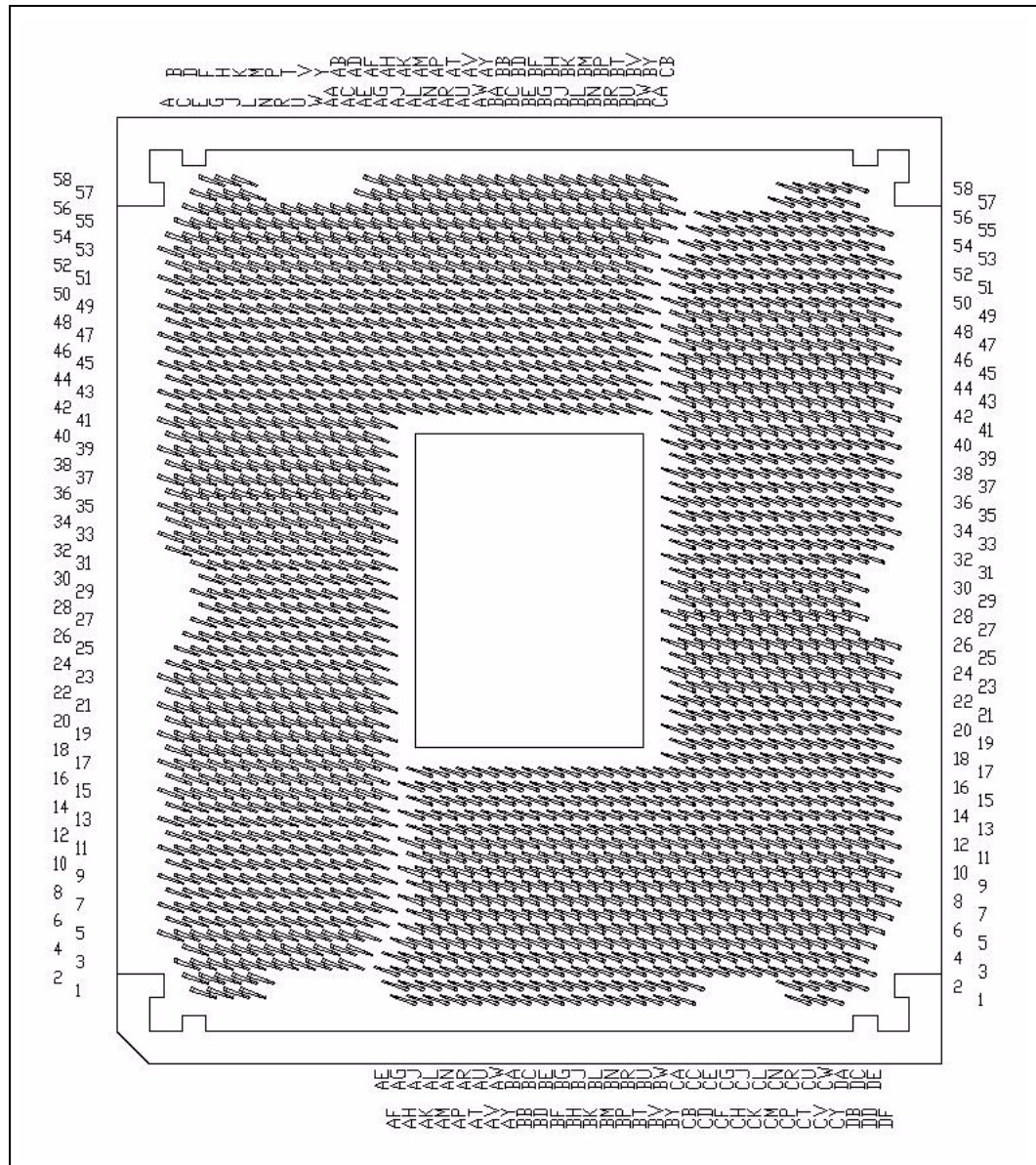




Figure 2-4. LGA2011-0 Socket Contact Numbering (Top View of Socket)

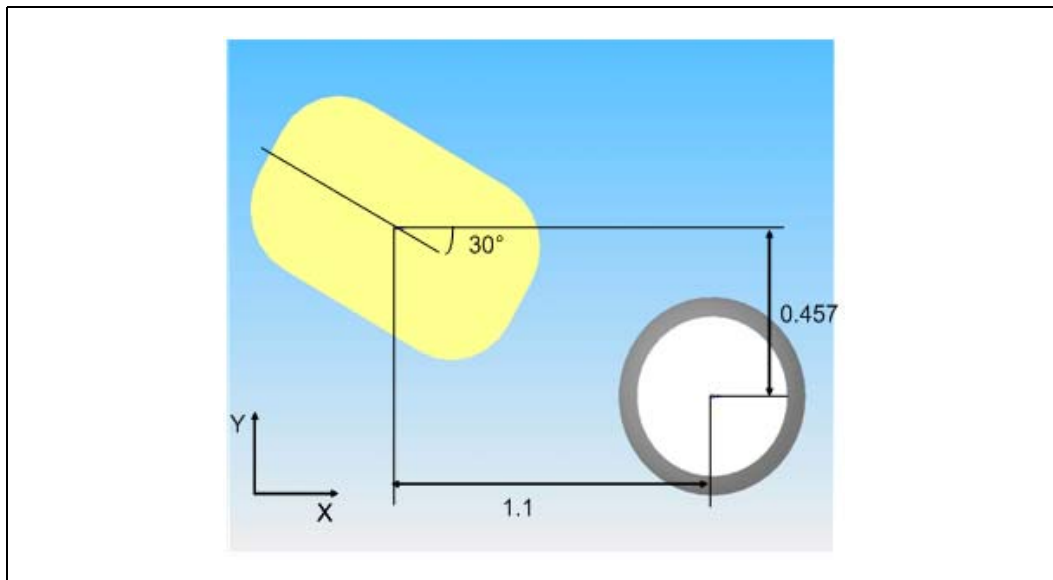




## 2.1 Contact/Land Mating Location

All socket contacts are designed such that the contact tip lands within the substrate pad boundary before any actuation load is applied and remain within the pad boundary at final installation, after actuation load is applied. The offset between LGA land center and solder ball center is defined in [Figure 2-5](#).

**Figure 2-5. Offset between LGA Land Center and Solder Ball Center**



**Note:** All dimensions are in mm.

## 2.2 Board Layout

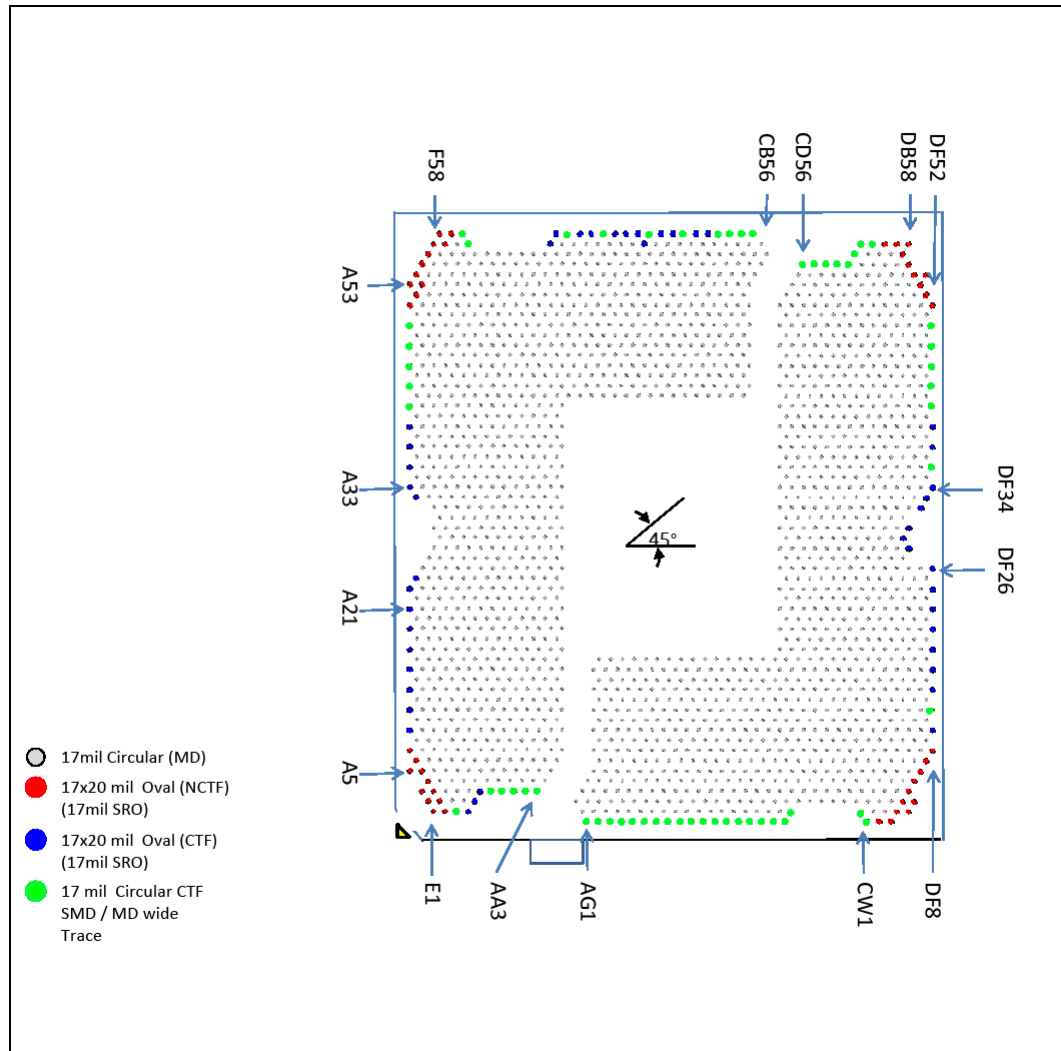
The land pattern for the LGA2011-0 socket is 40 mils hexagonal array. For CTF (Critical to Function) joints, the pad size will primarily be a circular Metal Defined (MD) pad and these pads should be designated as a Critical Dimension to the PCB vendors with a 17 mil  $\pm$  1 mil tolerance. Some CTF pads will have a SMD Pad (20 x 17 mil). For additional pad configurations details including the NCTF (Non-Critical to Function) joints, see [Section 2.3](#).

**Note:** There is no round-off (conversion) error between socket pitch (1.016 mm) and board pitch (40 mil) as these values are equivalent.





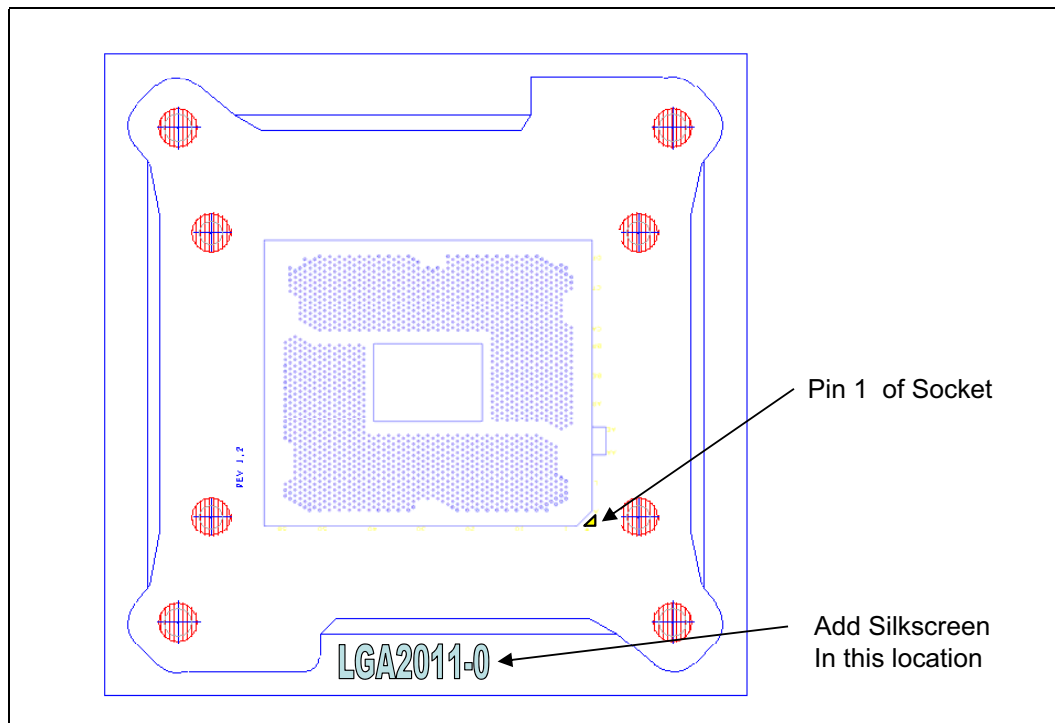
Figure 2-6. LGA2011-0 Socket Land Pattern (Top View of Board)



### 2.2.1 Suggested Silkscreen Marking for Socket Identification

Intel is recommending that customers mark the socket name approximately where shown in Figure 3-7. The final silkscreen location may vary with different motherboard designs, but should always be visible after ILM and component assembly.

Figure 2-7. Suggested Board Marking



## 2.3 Attachment to Motherboard

The socket is attached to the motherboard by 2011 solder balls. There are no additional external methods (that is, screw, extra solder, adhesive, and so forth) to attach the socket.

As indicated in [Figure 2-9](#), the Independent Loading Mechanism (ILM) is not present during the attach (reflow) process.

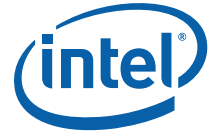
## 2.4 Socket Components

The socket has two main components, the socket body and Pick and Place (PnP) cover, and is delivered as a single integral assembly. Refer to [Appendix B](#) for detailed drawings.

### 2.4.1 Socket Body Housing

The housing material is thermoplastic or equivalent with UL 94 V-0 flame rating capable of withstanding 260°C for 40 seconds (typical reflow/rework). The socket coefficient of thermal expansion (in the XY plane), and creep properties, must be such that the integrity of the socket is maintained for the conditions listed in [Chapter 6](#).

The color of the housing will be dark as compared to the solder balls to provide the contrast needed for pick and place vision systems.



## 2.4.2 Solder Balls

A total of 2011 solder balls corresponding to the contacts are on the bottom of the socket for surface mounting with the motherboard.

The socket has the following solder ball material:

- Lead free SAC305 (SnAgCu) solder alloy with a silver (Ag) content 3%, copper (Cu) 0.5%, tin (Sn) 96.5% and a melting temperature of approximately 217°C. The immersion silver (ImAg) motherboard surface finish and solder paste alloy must be compatible with the SAC alloy solder paste.

The co-planarity (profile) and true position requirements are defined in [Appendix B](#).

## 2.4.3 Contacts

The base material for the contacts is high strength copper alloy.

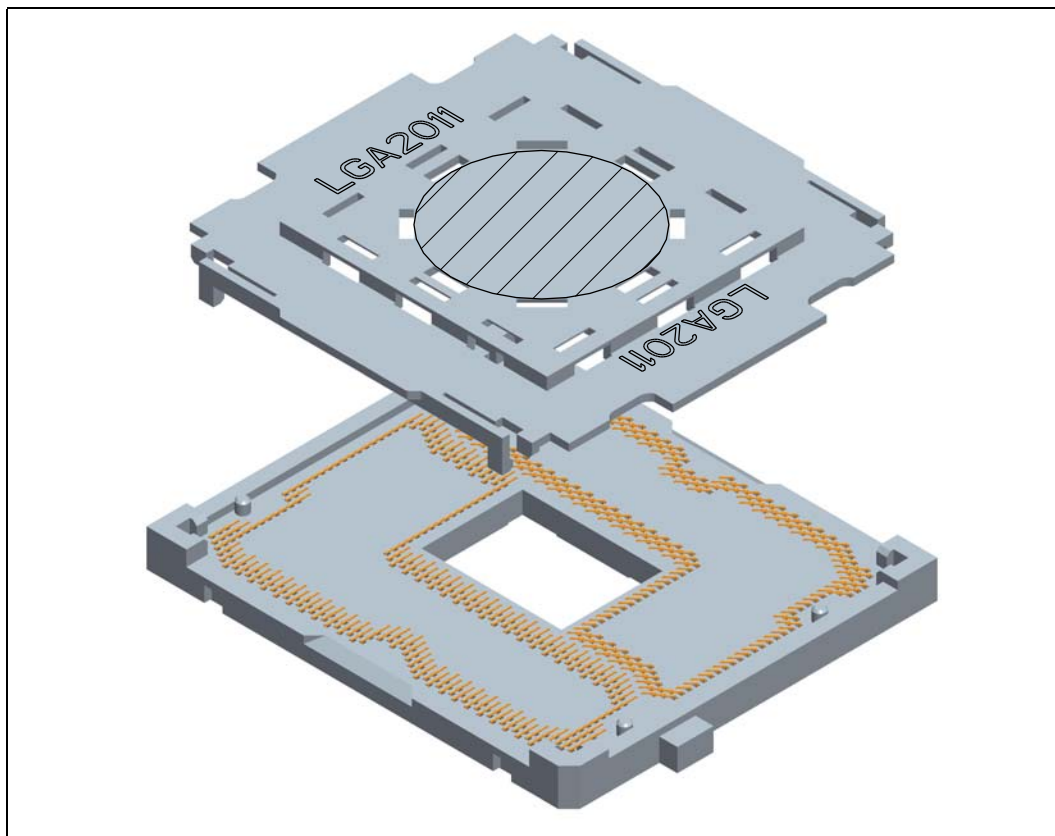
For the area on socket contacts where processor lands will mate, there is a 0.381  $\mu\text{m}$  [15  $\mu\text{inches}$ ] minimum gold plating over 1.27  $\mu\text{m}$  [50  $\mu\text{inches}$ ] minimum nickel underplate.

No contamination by solder in the contact area is allowed during solder reflow.

## 2.4.4 Pick and Place Cover

The cover provides a planar surface for vacuum pick up used to place components in the Surface Mount Technology (SMT) manufacturing line. The cover remains on the socket during reflow to help prevent contamination during reflow. The cover can withstand 260°C for 40 seconds (typical reflow/rework profile) and the conditions listed in [Chapter 6](#) without degrading.

Figure 2-8. LGA2011-0 Pick and Place Cover

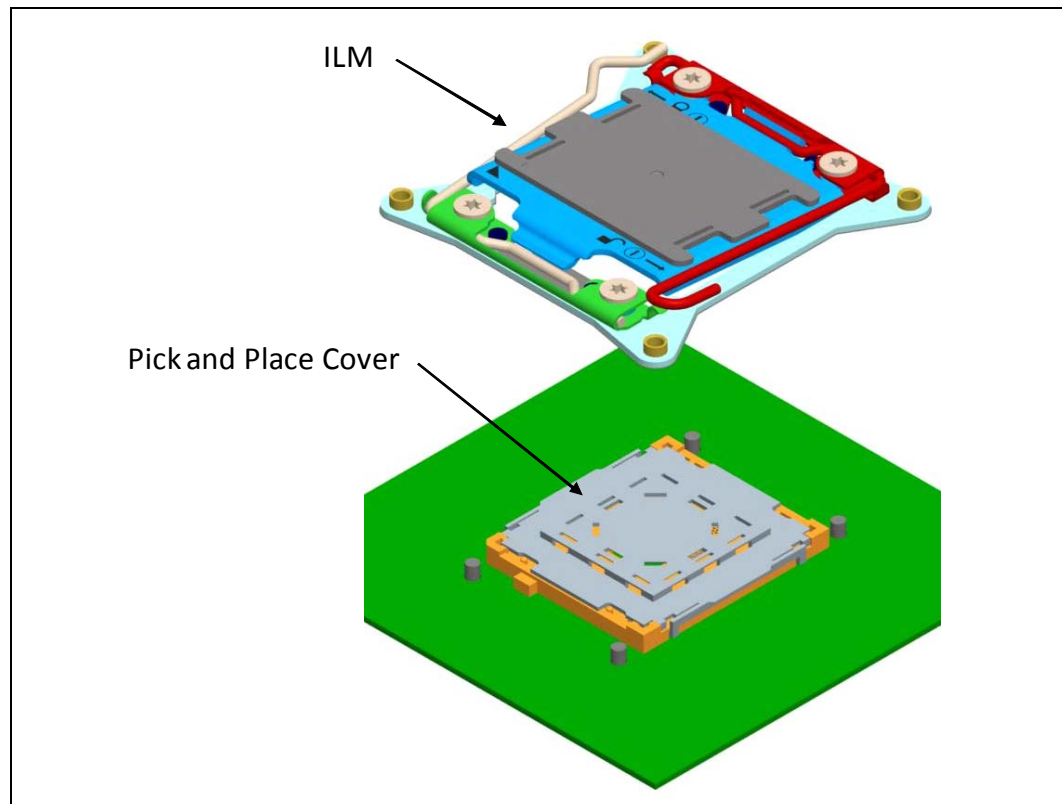


As indicated in [Figure 2-9](#), the pick and place (PnP) cover remains on the socket during ILM installation. Once the ILM with its cover is installed, Intel is recommending the PnP cover be removed to help prevent damage to the socket contacts. To reduce the risk of bent contacts the PnP Cover and ILM Cover were designed to not be compatible. See [Section 3.3](#) for additional information on ILM assembly to the board.

Cover retention must be sufficient to support the socket weight during lifting, translation, and placement (board manufacturing), and during board and system shipping and handling. Covers can be removed without tools.

The pick and place covers are designed to be interchangeable between socket suppliers.

**Figure 2-9. Pick and Place Cover**



**Note:** *Figure is representative and may not show the most current revision of parts.*

### 2.4.5 Socket Standoffs and Package Seating Plane

Standoffs on the bottom of the socket base establish the minimum socket height after solder reflow and are specified in [Appendix B](#).

Similarly, a seating plane on the topside of the socket establishes the minimum package height. See [Section 4.2](#) for the calculated IHS height above the motherboard.

## 2.5 Durability

The socket must withstand 30 cycles of processor insertion and removal. The maximum part average and single pin resistances from [Table 4-4](#) must be met when mated in the 1st and 30th cycles.

The socket Pick and Place cover must withstand 15 cycles of insertion and removal.

## 2.6 Markings

There are three markings on the socket:

- LGA2011-0: Font type is Helvetica Bold - minimum 6 point (2.125 mm).
- Manufacturer's insignia (font size at supplier's discretion).
- Lot identification code (allows traceability of manufacturing date and location).



All markings must withstand 260°C for 40 seconds (typical reflow/rework profile) without degrading, and must be visible after the socket is mounted on the motherboard.

LGA2011-0 and the manufacturer's insignia are molded or laser marked on the side wall.

## 2.7 Component Insertion Forces

Any actuation must meet or exceed SEMI S8-95 Safety Guidelines for Ergonomics/Human Factors Engineering of Semiconductor Manufacturing Equipment, example Table R2-7 (Maximum Grip Forces). The socket must be designed so that it requires no force to insert the package into the socket.

## 2.8 Socket Size

Socket information needed for motherboard design is given in [Appendix B](#).

This information should be used in conjunction with the reference motherboard keep-out drawings provided in [Appendix A](#) to ensure compatibility with the reference thermal mechanical components.

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### 3 Independent Loading Mechanism (ILM)

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The Independent Loading Mechanism (ILM) provides the force needed to seat the 2011-land LGA package onto the socket contacts. The ILM is physically separate from the socket body. The assembly of the ILM is expected to occur after attaching the socket to the board. The exact assembly location is dependent on manufacturing preference and test flow. See the Manufacturing Advantage Service (MAS) document for this platform for additional guidance.

The mechanical design of the ILM is a key contributor to the overall functionality of the LGA2011-0 socket. Intel performs detailed studies on integration of processor package, socket and ILM as a system. These studies directly impact the design of the ILM. The Intel reference ILM will be “built to print” from Intel controlled drawings. Intel recommends using the Intel Reference ILM. Custom non-Intel ILM designs do not benefit from Intel's detailed studies and may not incorporate critical design parameters.

There are two types of ILMs for socket LGA2011-0:

1. Square ILM - This ILM has 80x80 mm heatsink mounting hole pattern. Please refer to [Section 3.1](#) for more details
2. Narrow ILM - This ILM has 56x94 mm heatsink mounting hole pattern. Please refer to [Section 3.1](#) and [Section 3.5](#) for common features with square ILM and specific features of narrow ILM.

**Note:** The ILM has two critical functions: deliver the force to seat the processor onto the socket contacts and distribute the resulting load evenly through the socket solder joints. Another purpose of ILM is to ensure electrical integrity/performance of the socket and package.

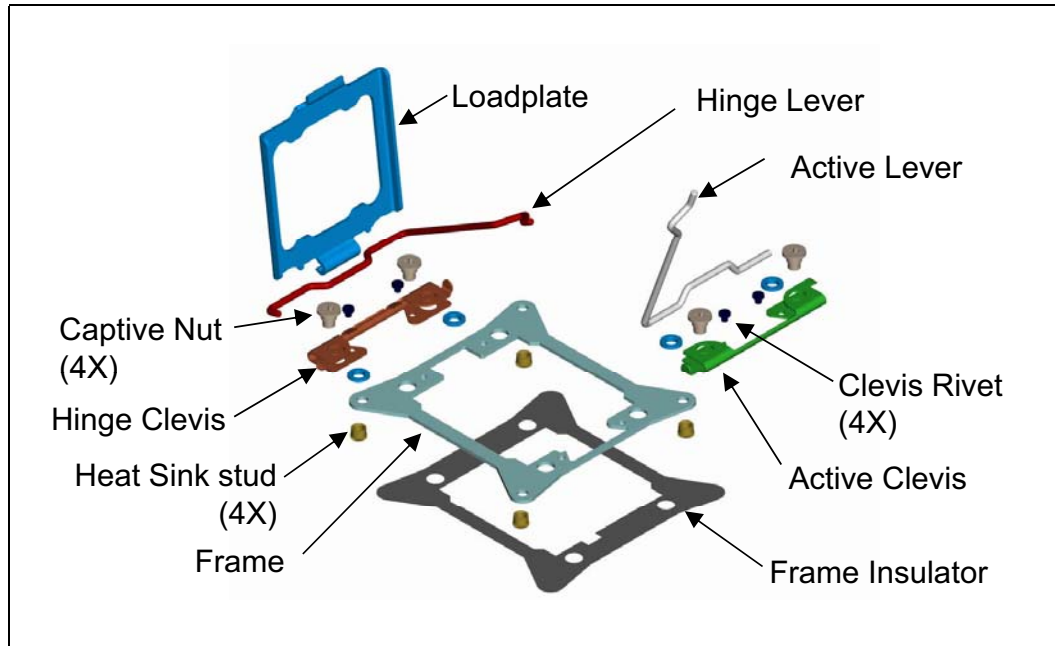
**Note:** This design will be “built to print” from Intel controlled drawings.

### 3.1 Square ILM Design Concept

The square ILM consists of two assemblies that will be procured as a set from the enabled vendors. These two components are the ILM assembly and back plate.

#### 3.1.1 Square ILM Assembly Design Overview

Figure 3-1. Square ILM Part Terminology



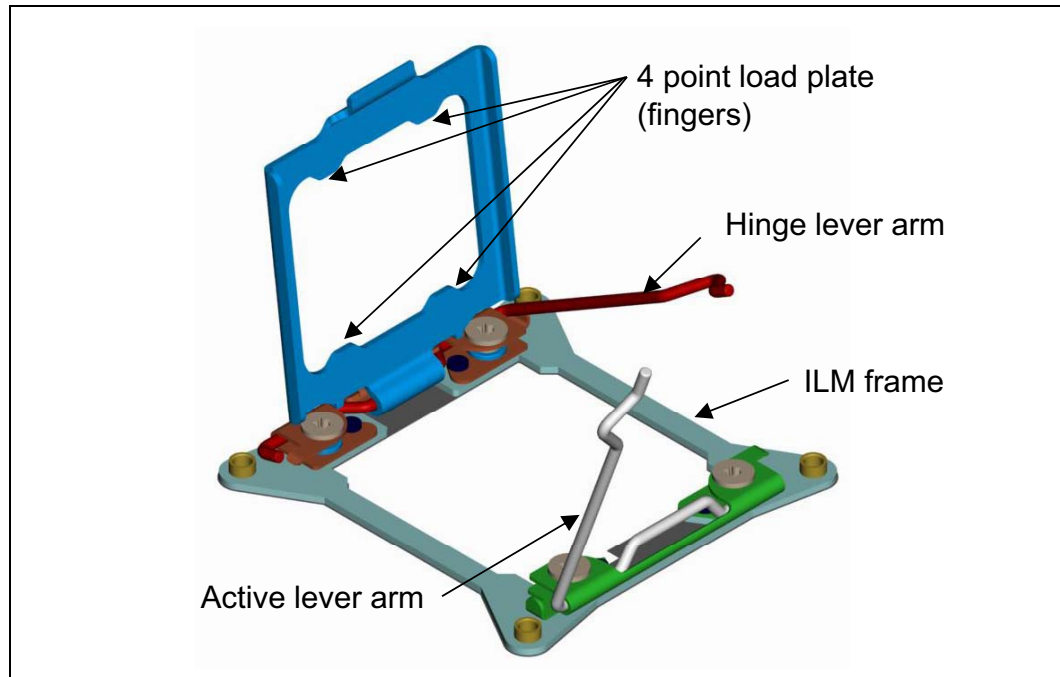
The square ILM assembly consists of five major pieces as shown in [Figure 3-1](#) and [Figure 3-2](#), hinge lever, active lever, load plate, load frame, ILM cover and the captive fasteners. For clarity the ILM cover is not shown in this view.

**Note:** The ILM assembly also contains an ILM cover as described in [Section 3.6](#).





**Figure 3-2. Square ILM Assembly**



**Note:** For clarity, the ILM cover is not shown in [Figure 3-2](#).

The hinge lever and active lever are designed to place equal force on both ends of the ILM load plate. The frame provides the hinge locations for the levers. The hinge lever connects the load plate to the frame. When closed, the load plate applies four point loads onto the IHS at the “finger” features shown in [Figure 3-2](#). Four point loading contributes to minimizing package and socket warpage as compared to two point loading. The reaction force from closing the load plate is transmitted to the frame and through the captive fasteners to the back plate. Some of the load is passed through the socket body to the board inducing a slight compression on the solder joints.

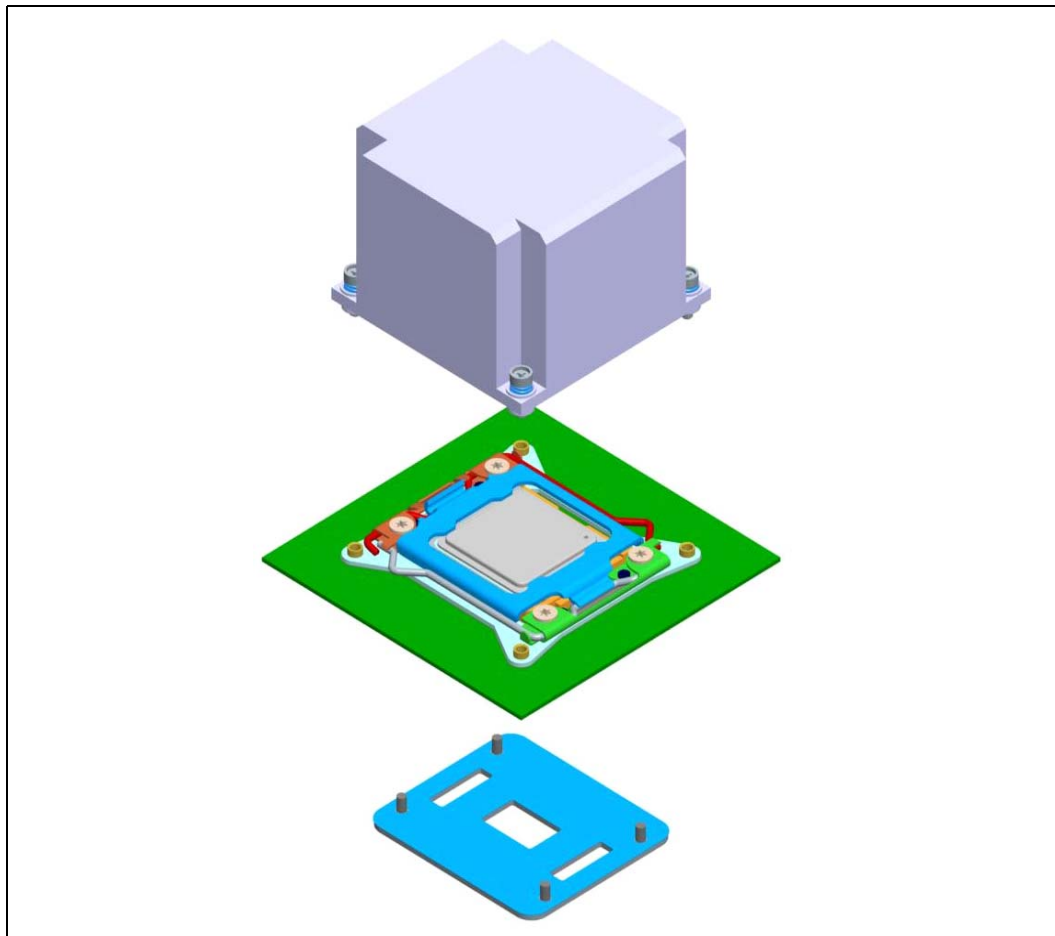
**Table 3-1. Square ILM Assembly Component Thickness and Material**

Component	Thickness (mm)	Material
ILM Frame	1.5	301 Stainless Steel
ILM Loadplate	1.5	301 Stainless Steel
ILM Backplate	2.2	S50C Low Carbon Steel

[Figure 3-3](#) shows the attachment points of the thermal solution to the ILM frame and the ILM to the back plate. This attachment method requires four holes in the motherboard for the ILM and no additional holes for the thermal solution. Orientation of the ILM is controlled with a key on the socket body. Orientation of the thermal solution is an option with a key to the ILM.

**Note:** Some customer reference boards (CRB) have four additional outer holes in the board. These holes are legacy and are not required for the current ILM reference design.

Figure 3-3. Square ILM as a Universal Retention Mechanism



## 3.2 ILM Features

These features are common to the square and narrow ILM:

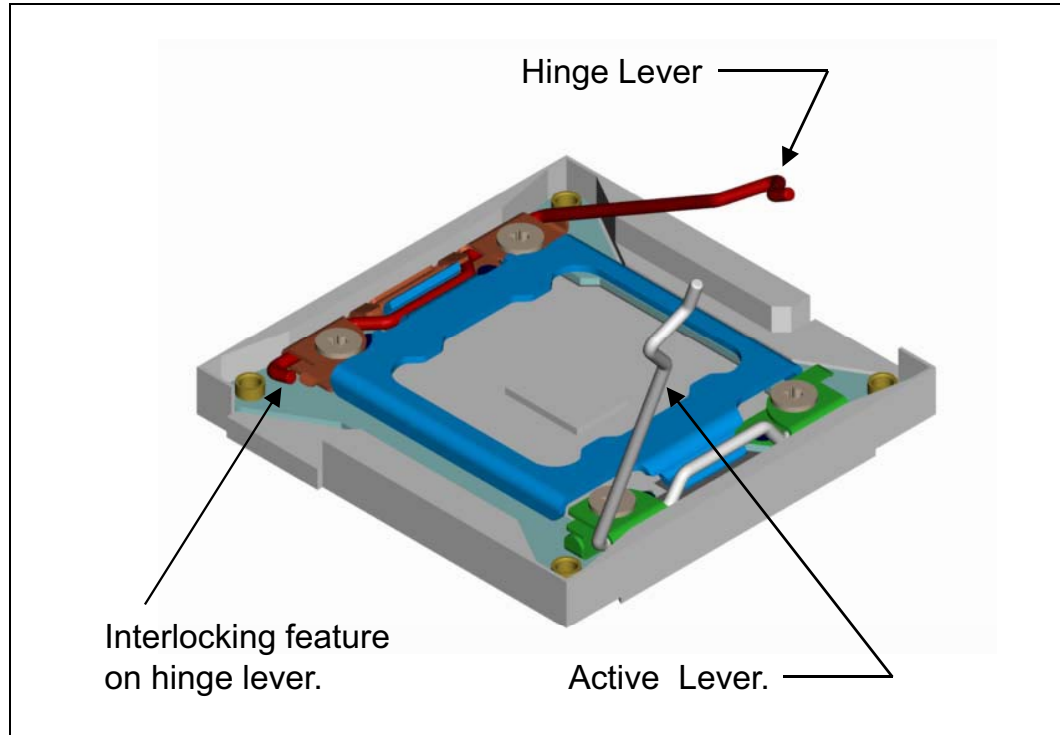
- Allows for topside thermal solution attach to a rigid structure. This eliminates the motherboard thickness dependency from the mechanical stackup.
- Captive nuts clamp the ILM frame to the board, providing good clamping and hence reduced board bending leading to higher solder joint reliability.
- ILM levers provide an interlocking mechanism to ensure proper opening or closing sequence for the operator. This has been implemented in both square and narrow ILM.

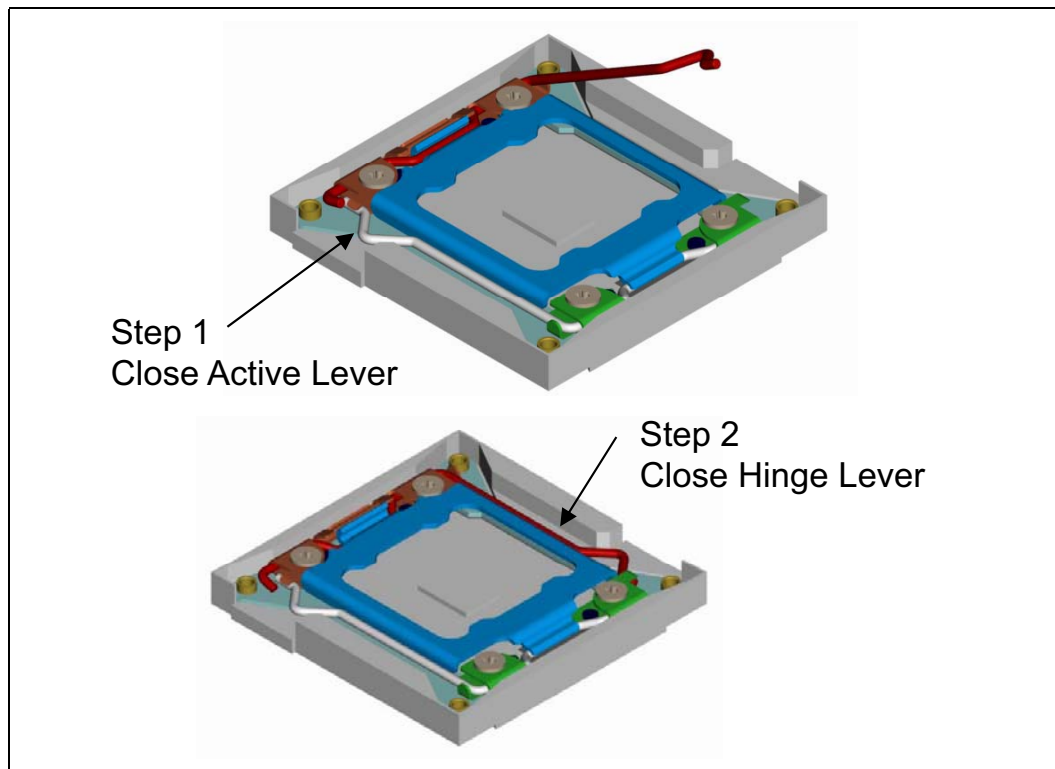
### 3.2.1 ILM Closing sequence

When closing the ILM, the interlocking features are intended to prevent the hinge lever from being latched first. If an attempt is made to close the hinge lever first, the hinge lever end stop will prevent the user from latching the active lever, indicating something is done wrong. Text on the ILM cover indicates the proper order of operation. Please refer to [Figure 3-4](#).

If hinge lever is pressed down first, it raises the load plate up at an angle higher than the active lever can make contact with, forcing a user to push it down. Also the hinge lever end stop will block the active lever from being able to be latched.

**Figure 3-4. ILM Interlocking Feature**



**Figure 3-5. ILM Lever Closing Sequence**

ILM lever closing sequence is shown in [Figure 3-5](#).

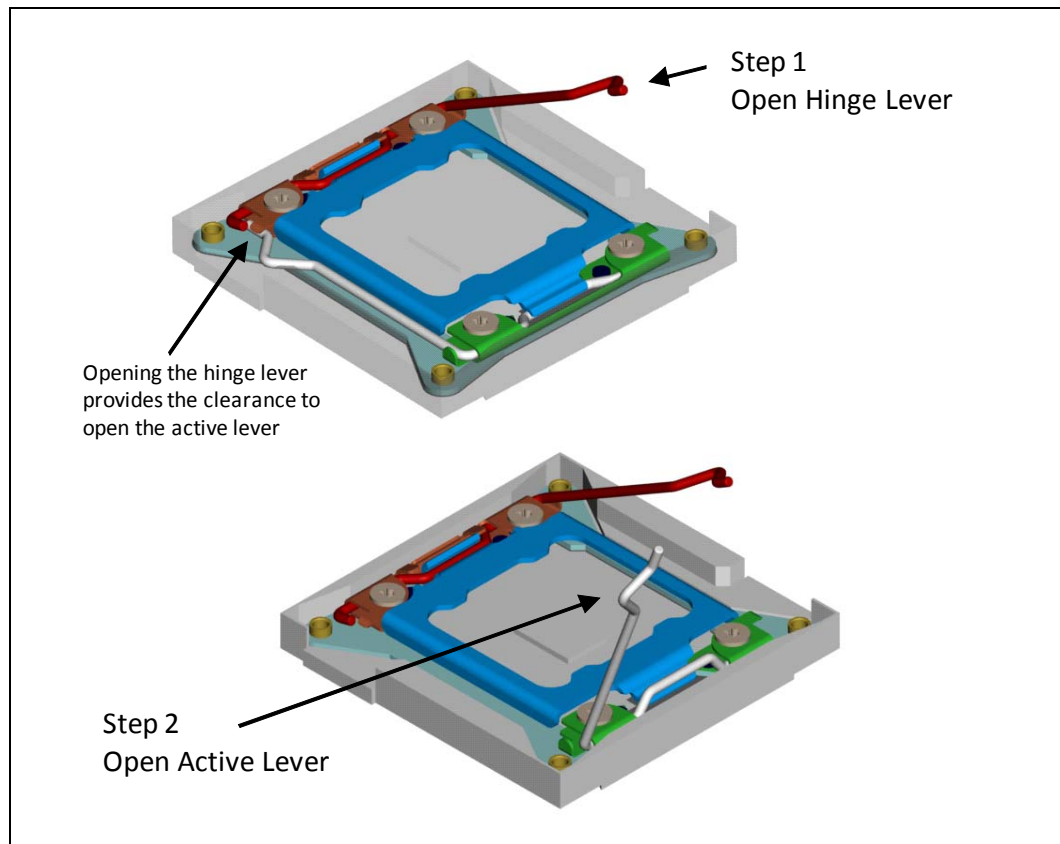
1. Latch Active Lever first.
2. Close Hinge Lever second.

**Note:** The ILM closing sequence is marked on the ILM load plate.

### 3.2.2 ILM Opening Sequence

For the opening sequence, the goal is to always open the hinge lever first to prevent the loadplate from springing open. The only option is to release the hinge lever first. The hinge lever in a closed position will block the active lever from being unlatched. By opening hinge lever first, it creates clearance to open the active lever.

**Figure 3-6. Opening ILM**

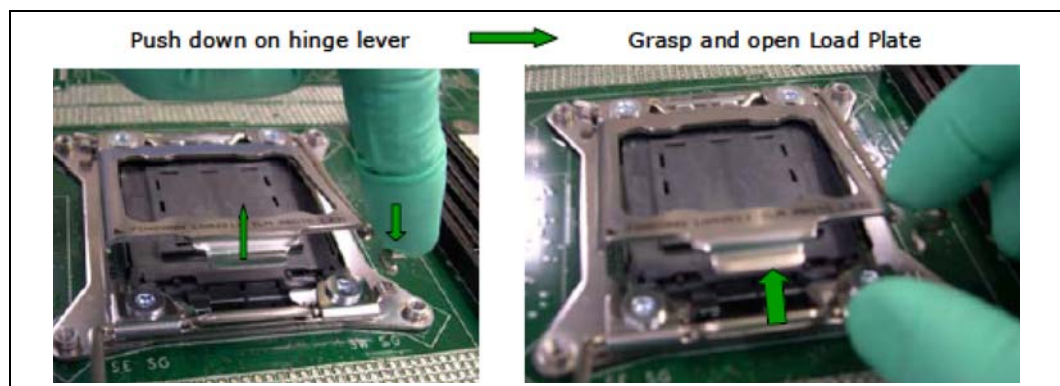


The ILM opening sequence is shown in [Figure 3-6](#).

1. Open hinge lever
2. Open active lever

**Note:** The opening sequence is also marked on the ILM load plate

**Figure 3-7. Opening Sequence for ILM and Loadplate (cont.)**



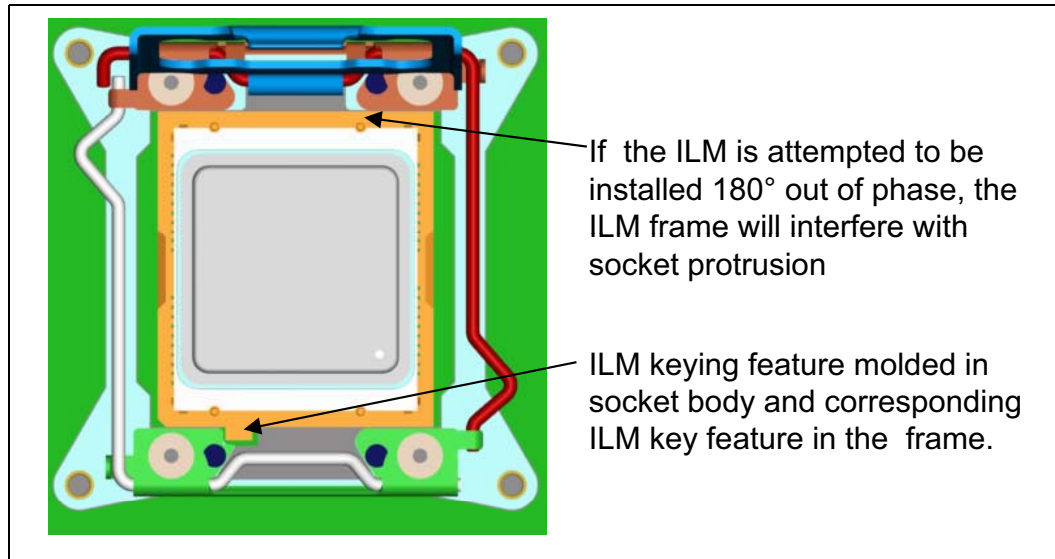
3. Open the load plate by pushing down on the hinge lever [Figure 3-7](#), this will cause the load plate tab to rise above the socket. Grasp the tab, only after it has risen away from the socket, open load plate to full open position.

**Note:** ILM cover not shown for clarity.

### 3.2.2.1 ILM Keying

This feature is incorporated in the square and narrow ILM. As indicated in [Figure 3-8](#), the socket protrusion and ILM key features prevent 180-degree rotation of ILM assembly with respect to socket. This result in a specific orientation with respect to ILM active lever and pin 1 of the socket body.

**Figure 3-8. ILM Keying**

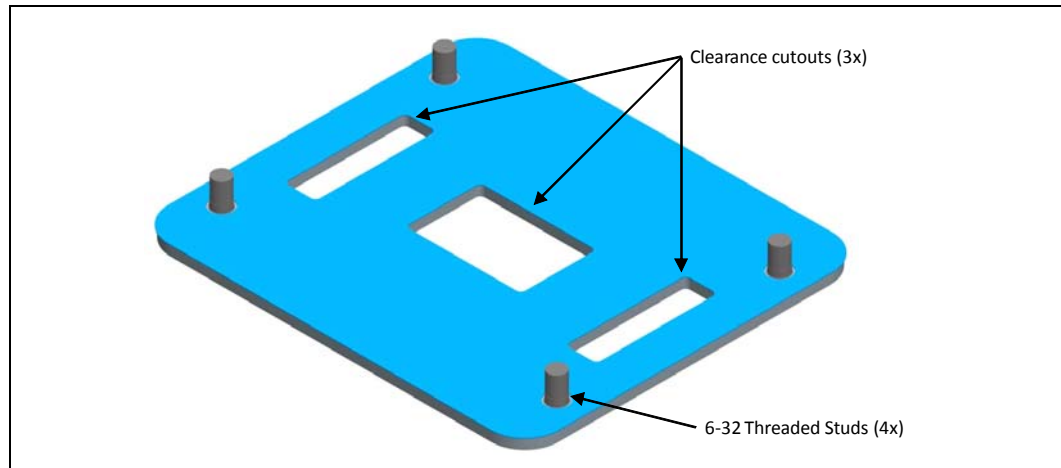


### 3.2.3 ILM Back Plate Design Overview

The backplate design is common for square and narrow ILM. The back plate for dual processor server products consists of a flat steel back plate with threaded studs to attach to the ILM frame. A clearance hole is located at the center of the plate to allow access to test points and backside capacitors. Two additional cut-outs on the backplate provide clearance for backside voltage regulator components. An insulator is pre applied by the vendor to the side with the threaded studs.

**Note:** The ILM Back Plate is designed to work with board thicknesses from 0.062 to 0.100 inches. If the board is outside of this range, the backplate will require modification.

Figure 3-9. ILM Back Plate



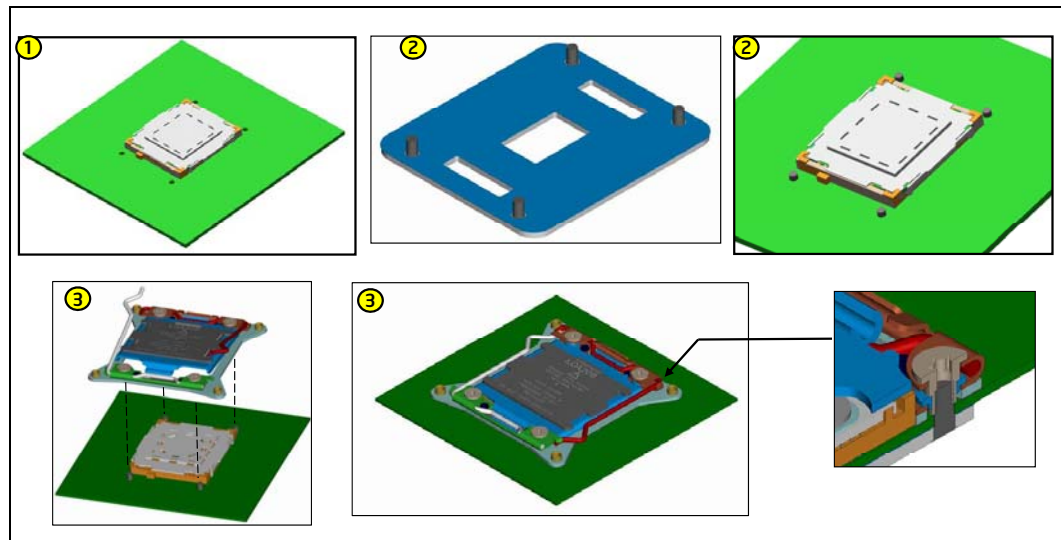
### 3.3 ILM Assembly

The ILM assembly instructions are briefly outlined here. The ILM assembly instructions shown here are for illustration. For High Volume Manufacturing please refer to the appropriate platform Manufacturing Advantage Service document.

#### 3.3.1 Manufacturing Assembly Flow

The assembly of the ILM to the socket is documented in the steps below and graphically in Figure 3-10.

Figure 3-10. Assembling Socket, Back Plate and ILM onto the Motherboard



**Note:** The steps in Figure 3-10 are for illustration only and may not show the most current revision of parts.



1. Using SMT, mount the socket onto the circuit board. Intel provides detailed instruction for lead free manufacturing of complex interconnects on the Intel Learning Network (<http://iln.intel.com/Portal/Scripts/Home/Home.aspx>).
2. Assemble the back plate onto the bottom side of the board ensuring that all 4 studs protrude through the board.
3. Place the Independent Load Mechanism (ILM) with cover onto the board. The load plate should be unlatched. See [Section 3.2.2](#).
4. Tighten the (4) Torx-20 screws to  $9 \pm 1$  in-lb.
5. Lift the load plate to the open position and with the tool remove the PnP cover from the socket body.
6. Close the ILM and latch it per the instructions in [Section 3.2.1](#).

### 3.4 Processor Installation

**Note:** For complete ILM assembly instructions please refer to the appropriate Manufacturing *Advantage Service* document.

The hinge lever can be locked down to keep it out of the way when removing the PnP cover and installing the processor ([Figure 3-11](#)). If the hinge lever is locked down when the ILM is open, then the load plate will be locked in the open position and less likely to fall closed if bumped.

Both the Square and Narrow ILM have a Pin 1 marking on the frame to help indicate proper package alignment ([Figure 3-12](#)).

**Figure 3-11. Optional Step: Lock down the Hinge Lever**

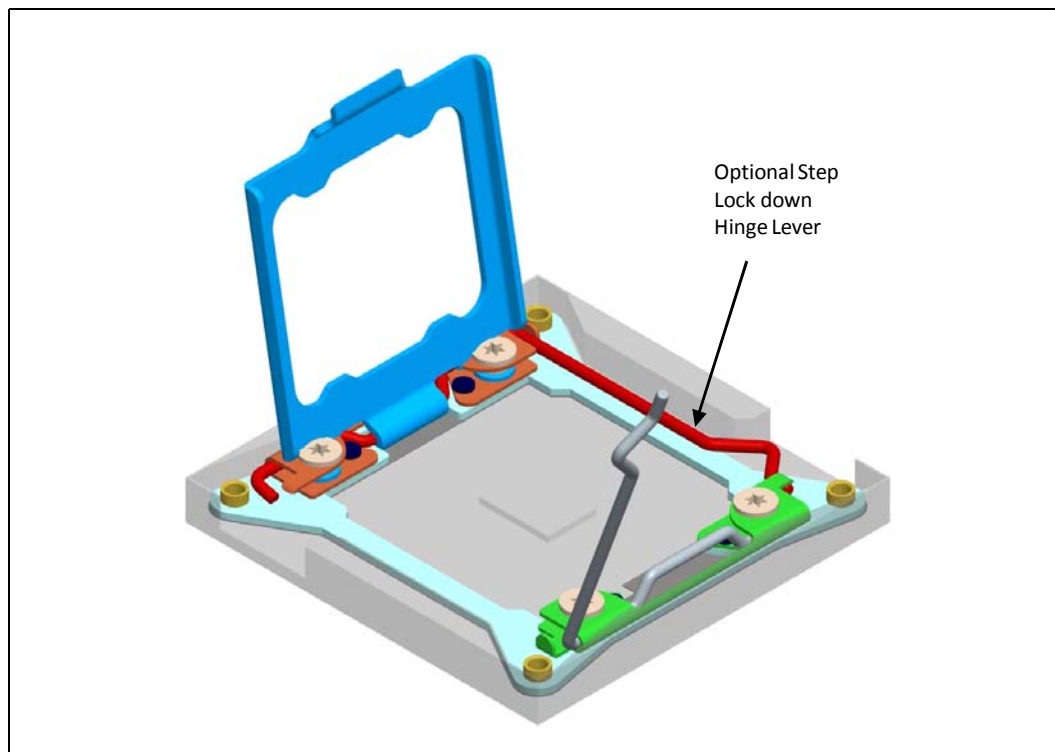




Figure 3-12. Pin 1 Markings on the ILM Frames

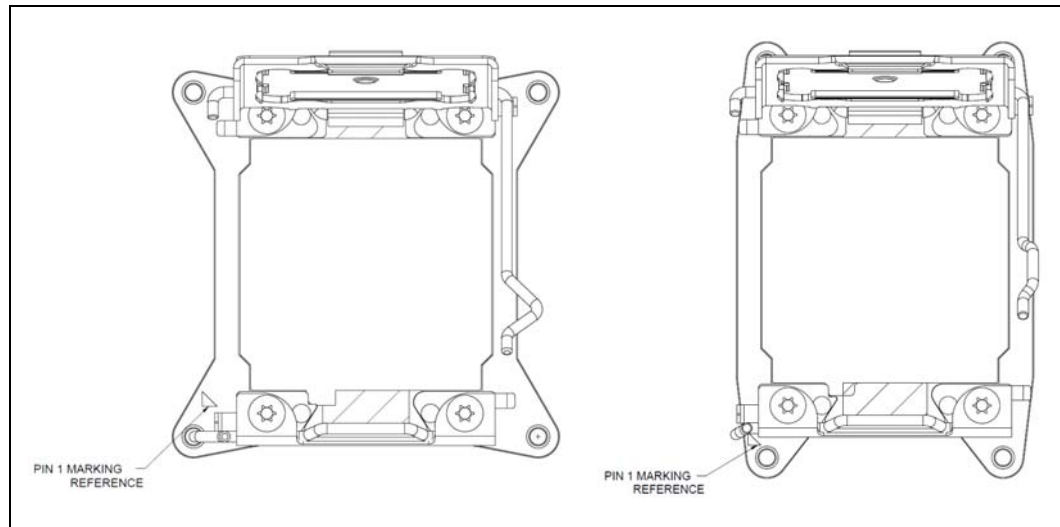
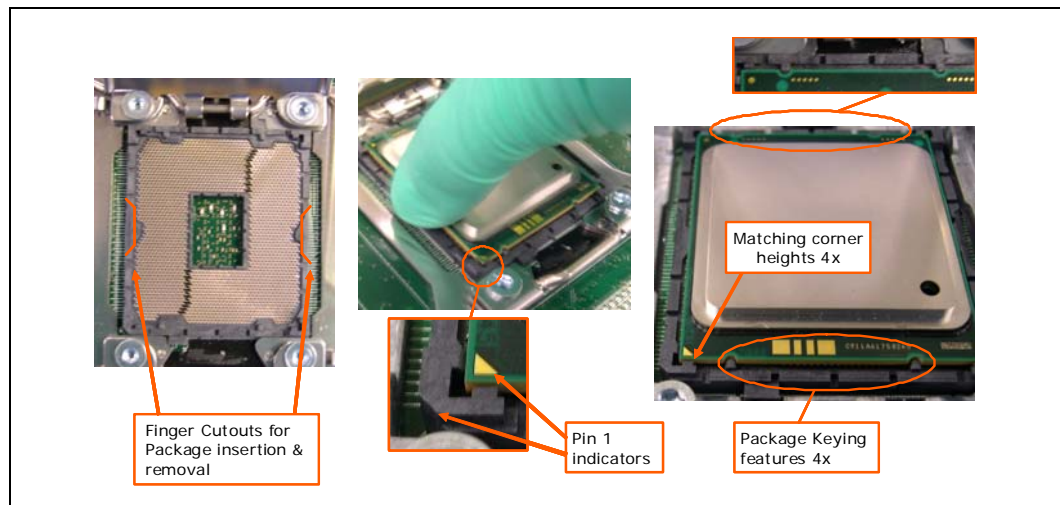


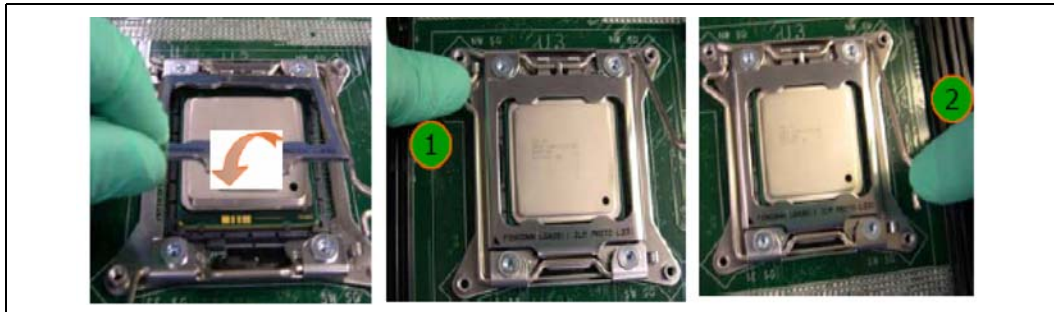
Figure 3-13. Package Insertion



**Note:** *Figure 3-13 is for illustration only and may not show the most current revision of parts. A tool is available for the installation or removal of the processor. Please work with your local CQE for tool availability.*

7. Hold processor along the right and left edges of the package to match socket finger cutouts (East - West edges). Make sure processor's Pin1 indicator is aligned with Pin 1 indicator on the socket corner. Keeping the processor horizontal, lower it gently into the socket with a purely vertical motion. Verify the package is fully seated; package corners must be at the same height with respect to all four socket corners.

Figure 3-14. Closing ILM and Loadplate



**Note:** *Figure 3-14 is for or illustration only and may not show most current parts.*

8. Carefully lower the ILM load plate on top of the processor,
9. Verify that Load-lever-cam is over the load-plate-tab; actuate Load lever with a smooth uniform motion and latch to the ILM (with thumb).
10. Close the Hinge lever with a smooth uniform motion and latch to the ILM.

## 3.5 Narrow ILM

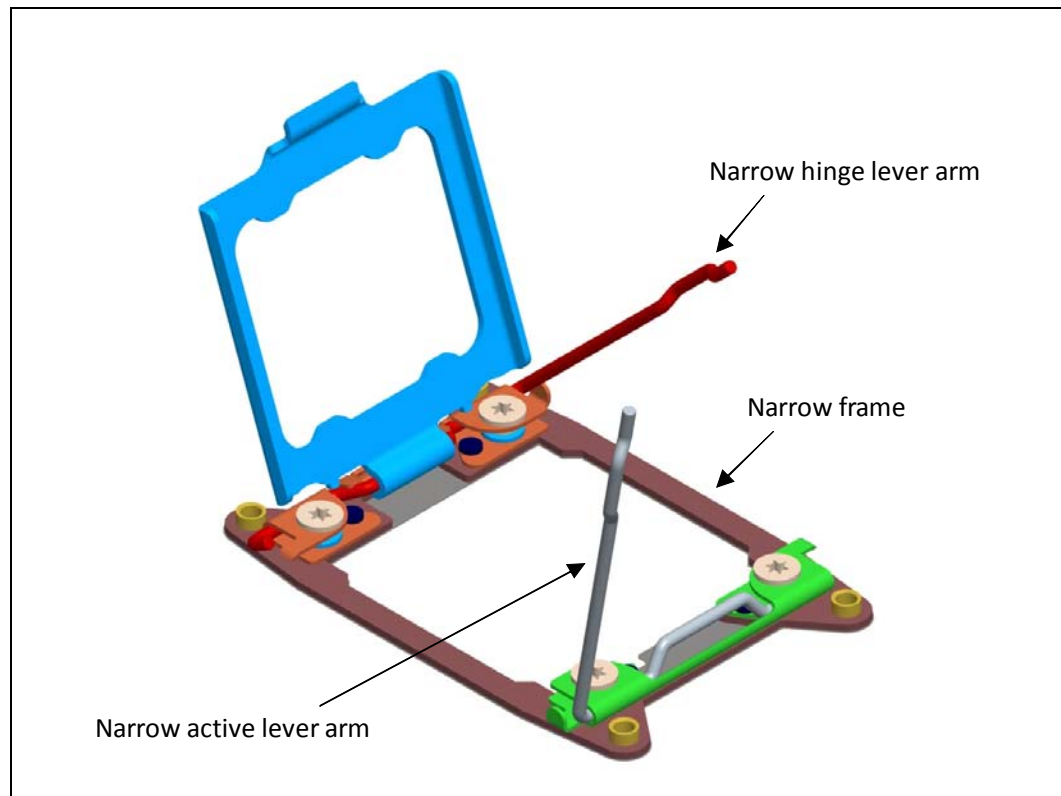
### 3.5.1 Introduction

In addition to the square ILM discussed in [Section 3.1](#), Intel is enabling a second sku of ILM referred to as the narrow ILM ([Figure 3-15](#).) This second ILM is targeted for constrained layouts where the space available on either side of the LGA2011-0 socket requires narrow heatsink mount points.

**Note:** This alternate narrow ILM should only be used if space constraints on the board require it. The topside keepouts and restricted heatsink width associated with this design present increased challenges in routing, component placement, and thermals.

**Note:** This design will be “built to print” from Intel controlled drawings.

Figure 3-15. Narrow ILM



## 3.5.2 Comparison Between Square ILM and Narrow ILM

### 3.5.2.1 Part Comparison

The narrow ILM is a similar design to the square ILM and shares a majority of the parts. The only parts that are different in the narrow ILM are the ILM frame, hinge lever arm, and active lever arm.

### 3.5.2.2 Mechanical Requirements

The narrow ILM has the same mechanical requirements as the square ILM (refer to the LGA2011-0 Socket and ILM Electrical, Mechanical, and Environmental Specifications in this document.)

## 3.5.3 ILM Keepout Zones

ILM keepout zones (KOZ) refer to zones around the socket on the top and bottom of the board that must be kept clear of components to accommodate the ILM assembly and back plate. [Appendix A, "Mechanical Drawings"](#) shows the different KOZ for both the square and the narrow ILM.

**Note:** The keepout zones only account for the mechanical clearance. It is up to the system/board architect to determine additional clearance required for finger and/or tool access.

**Note:** Some customer reference boards (CRB) have four additional outer holes in the board. These holes are legacy and are not required for the current ILM reference design and are thus not shown in the current KOZ.

### 3.6 ILM Cover

Intel has developed a cover that will snap on to the ILM for the LGA2011 socket family.

The ILM cover is intended to reduce the potential for socket contact damage from the operator / customer fingers being close to the socket contacts to remove or install the pick and place cover. By design the ILM cover and pick and place covers can not be installed simultaneously.

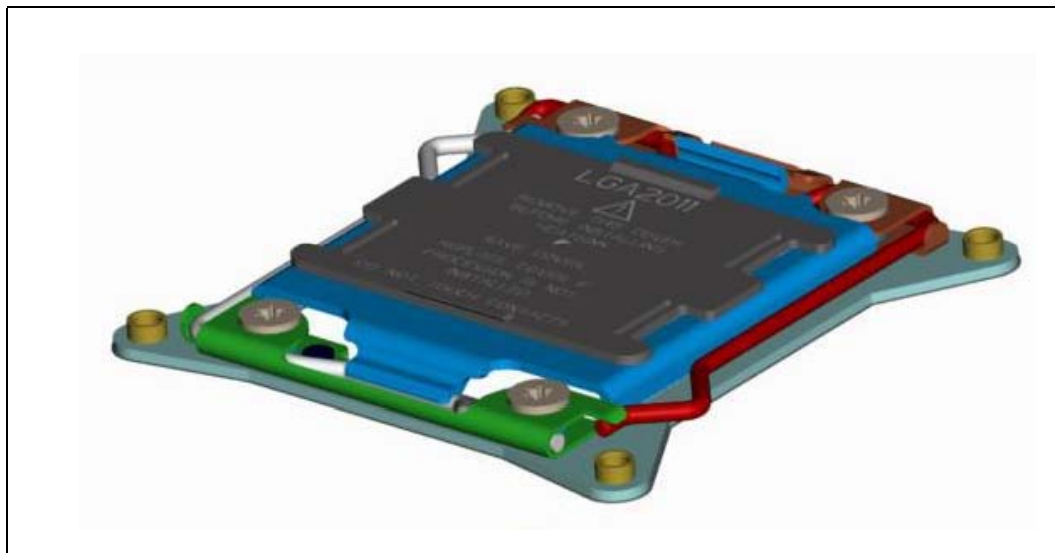
The ILM cover concept is shown in [Figure 3-16](#).

This cover is intended to be used in place of the pick and place cover once the ILM is assembled to the board. The ILM will be offered with the ILM cover pre assembled as well as a discrete part.

ILM cover features:

- Pre-assembled by the ILM vendors to the ILM load plate. It will also be offered as a discrete component.
- The ILM cover will pop off if a processor is installed in the socket.
- ILM Cover can be installed while the ILM is open.
- Maintain inter-changeability between validated ILM vendors for LGA2011-0 socket.
- The ILM cover for the LGA2011-0 socket will have a flammability rating of V-0 per UL 60950-1.

**Figure 3-16. ILM with Cover**



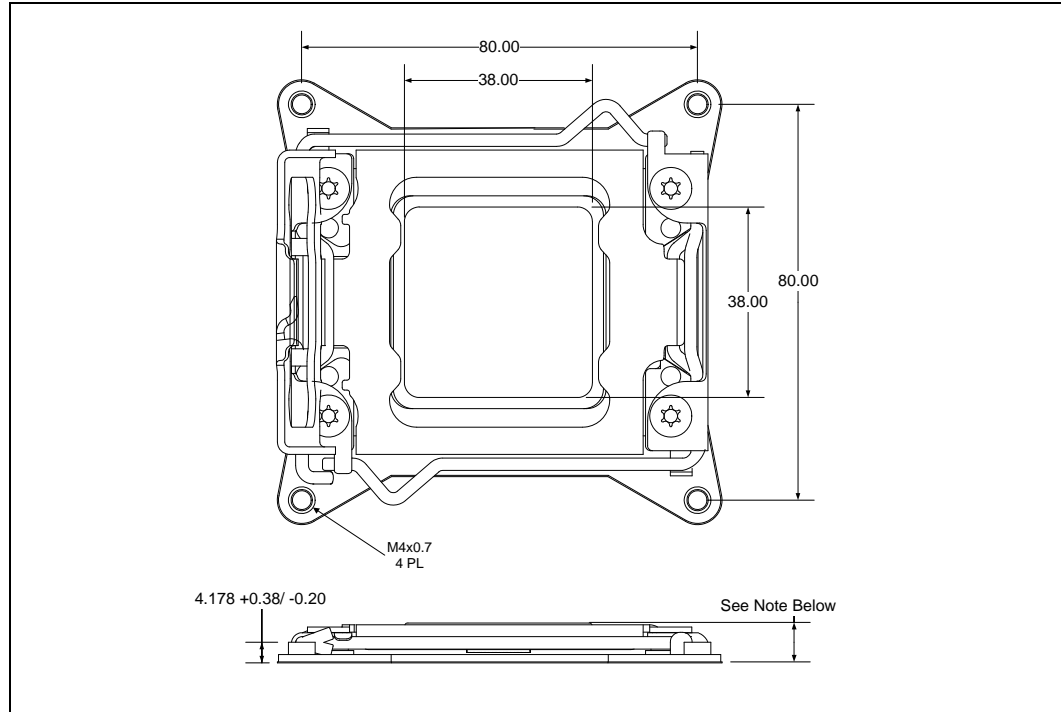
**Note:** Intel recommends removing the Pick and Place cover (PnP) of the socket body in manufacturing as soon as possible at the time when ILM is being installed.



### 3.7 Heatsink to ILM interface

Heatsinks for processors in the LGA2011-0 socket attach directly to the ILM via M4 fasteners. Figure 3-17 shows the critical dimension features the thermal solution vendor must meet.

Figure 3-17. Heatsink to ILM Interface



**Note:** For IHS height above board see [Table 4-1](#)

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# 4 LGA2011-0 Socket and ILM Electrical, Mechanical, and Environmental Specifications

This chapter describes the electrical, mechanical, and environmental specifications for the LGA2011-0 socket and the Independent Loading Mechanism.

## 4.1 Component Mass

**Table 4-1. Socket and Retention Component Mass**

Component	Mass
Socket Body, Contacts and PnP Cover	251g
Square ILM Assembly	82g
Narrow ILM Assembly	79g
Backplate	84g

**Note:**

1. This is an approximate mass.

## 4.2 Package/Socket Stackup Height

Table 4-2 provides the stackup height of a processor in the 2011-0-land LGA package and LGA2011-0 socket with the ILM closed and the processor fully seated in the socket.

**Table 4-2. 2011-land Package and LGA2011-0 Socket Stackup Height**

Integrated Stackup Height (mm) From Top of Board to Top of IHS	8.014 ±0.34 mm
---	----------------

**Notes:**

1. This data is provided for information only, and should be derived from: (a) the height of the socket seating plane above the motherboard after reflow, given in [Appendix B](#), (b) the height of the package, from the package seating plane to the top of the IHS, and accounting for its nominal variation and tolerances that are given in the corresponding processor EDS listed in [Table 1-1](#).
2. This value is a RSS calculation at 3 Sigma.

## 4.3 Loading Specifications

The socket will be tested against the conditions listed in [Section 6](#) with heatsink and the ILM attached, under the loading conditions outlined in this chapter.

[Table 4-3](#) provides load specifications for the LGA2011-0 socket with the ILM installed. The maximum limits should not be exceeded during heatsink assembly, shipping conditions, or standard use condition. Exceeding these limits during test may result in component failure. The socket body should not be used as a mechanical reference or load-bearing surface for thermal solutions.



Table 4-3. Socket and ILM Mechanical Specifications

Parameter	Min	Max	Notes
Static compressive load from ILM cover to processor IHS	445 N [100 lbf]	712 N [160 lbf]	3, 4, 7, 8
Heatsink Static Compressive Load BOL	222 N [50 lbf]	356 N [80 lbf]	1, 2, 3, 4, 8, 10
Heatsink Static Compressive Load EOL	178 N [40 lbf]	356 N [80 lbf]	1, 3, 4, 8, 9
Dynamic Load (with heatsink installed)	N/A	540 N [121 lbf]	1, 3, 5, 6, 8
Pick and Place Cover Insertion / Removal force	N/A	6.2 N [1.7 lbf]	8
Load Lever actuation force	N/A	31 N [7.0 lbf] in the vertical direction	8
Maximum heatsink mass	N/A	550g	11

**Notes:**

1. These specifications apply to uniform compressive loading in a direction perpendicular to the IHS top surface.
2. This is the minimum and maximum static force that can be applied by the heatsink and its retention solution to maintain the heatsink to IHS interface. This does not imply the Intel reference TIM is validated to these limits.
3. Loading limits are for the LGA2011-0 socket.
4. This minimum limit defines the compressive force required to electrically seat the processor onto the socket contacts.
5. Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement.
6. Test condition used a heatsink mass of 550 gm [1.21 lb.] with 50 g acceleration measured at heatsink mass. The dynamic portion of this specification in the product application can have flexibility in specific values, but the ultimate product of mass times acceleration should not exceed this dynamic load.
7. Conditions must be satisfied at the beginning of life (BOL) and the loading system stiffness for non-reference designs need to meet a specific stiffness range to satisfy end of life loading requirements.
8. These loading values are preliminary and subjected to change.
9. End of Life (EOL) minimum heatsink static load. The methods and techniques to evaluate heat sink EOL load are included in [Appendix F](#).
10. Beginning of Life (EOL) heat sink load. The methods and techniques to evaluate heat sink BOL load will be included in a later release of this document.
11. The maximum mass includes all components in the thermal solution. This mass limit is evaluated using the POR heatsink attached to a PCB.

## 4.4 Electrical Requirements

LGA2011-0 socket electrical requirements are measured from the socket-seating plane of the processor to the component side of the socket PCB to which it is attached. All specifications are maximum values (unless otherwise stated) for a single socket contact, but includes effects of adjacent contacts where indicated.





**Table 4-4. Electrical Requirements for LGA2011-0 Socket**

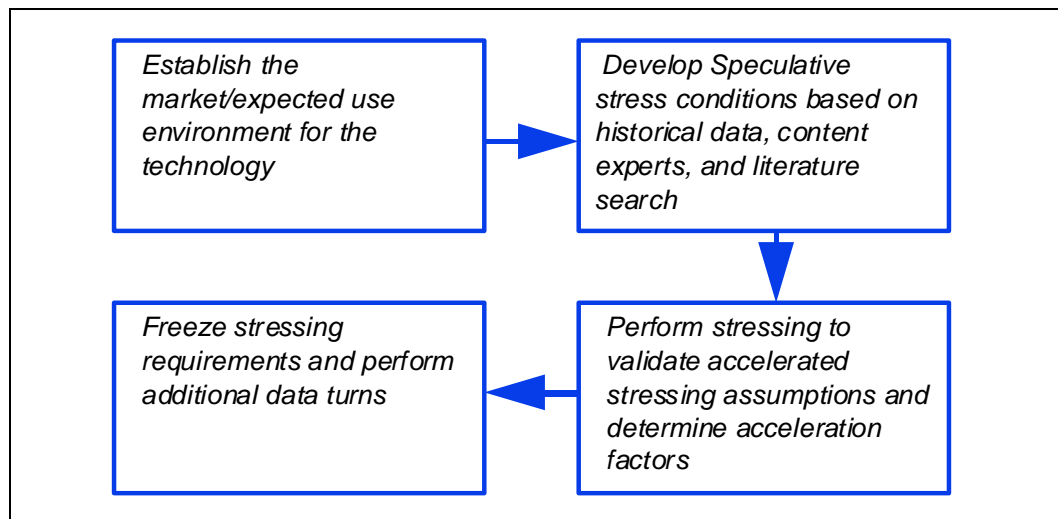
Parameter	Value	Comment
Maximum Socket Part Average Resistance (EOL @ 100°C)	25 mΩ	This is the maximum allowable part average socket resistance allowed under all use conditions (EOL and 100°C). This is monitored by measuring the daisy chain resistance of all socket contacts in series across the socket and dividing by the number of contacts measured. The resulting value must be below 25 mΩ at all use conditions (EOL) and elevated temperature (100C).
Maximum Single Pin Resistance (mean + 4 sigma) (EOL @ 100°C)	38 mΩ	This is the maximum validated single contact resistance on the socket under all use conditions (EOL) and at elevated temperature (100°C). This accounts for resistance variation across the socket. While it is possible that a single contact may reach a resistance of 38 mΩ, the maximum socket part average resistance spec insures that all contacts averaged together will not be higher than 25 mΩ
Dielectric Withstand Voltage	360 Volts RMS	
Insulation Resistance	800 MΩ	

## 4.5 Environmental Requirements

Design, including materials, shall be consistent with the manufacture of units that meet the following environmental reference points.

The reliability targets in this chapter are based on the expected field use environment for these products. The test sequence for new sockets will be developed using the knowledge-based reliability evaluation methodology, which is acceleration factor dependent. A simplified process flow of this methodology can be seen in Figure 4-1.

**Figure 4-1. Flow Chart of Knowledge-Based Reliability Evaluation Methodology**



A detailed description of this methodology can be found at:

<ftp://download.intel.com/technology/itj/q32000/pdf/reliability.pdf>







# 5 Thermal Solutions

This section describes a 1U reference heatsink and design targets for 2U heatsinks.

## 5.1 Performance Targets

### 5.1.1 Performance Targets - Square ILM/Heatsink Application

Table 5-1, Table 5-2, and Table 5-3 provide boundary conditions and performance targets for 1U, 2U, and Tower heatsinks used in conjunction with the square ILM for 8 core/6 core and 4 core processors, respectively. These values are used to generate processor thermal specifications and to provide guidance for heatsink design.

All Boundary Conditions are specified at 35°C system ambient temperature and at sea level. Figure 5-1 shows  $\Psi_{ca}$  and pressure drop for the 1U heatsink versus the airflow provided. Best-fit equations are provided to prevent errors associated with reading the graph.

**Table 5-1. Intel® Xeon® Processor E5-1600/2600/4600 v1 Product Families, 8 Core/6 Core Processor Reference Thermal Boundary Conditions (Square ILM/HS)**

TDP	Heatsink Technology	$\Psi_{CA}^2$ (°C/W)	$T_{LA}^1$ (°C)	Airflow <sup>3</sup> (CFM)	Delta P inch of H <sub>2</sub> O (Pa)	Heatsink Volumetric <sup>4</sup> (mm)
150W (2S WS Only)	Cu Base, Al Fins (Cu-Al)/Heatpipe	0.208	35.2	21.8	0.120	100x100x124
135W(2U)	Cu Base, Al Fins (Cu-Al)/Heatpipe	0.179	47.4	26	0.140	91.5x91.5x64
130W (1S WS Only)	Cu Base, Al Fins (Cu-Al)/Heatpipe	0.192	39	2600 RPM	N/A	100x100x124
130W (1U)	Cu Base, Al Fins (Cu-Al)	0.243	53.3	16	0.406	91.5x91.5x25.5
115W(1U)		0.241	51.7	16		
95W (1U)		0.241	49.5	16		
70W (1U)		0.239	46.8	16	0.406	91.5x91.5x25.5
60W (1U)		0.239	45.7	16		



**Table 5-2. Intel® Xeon® Processor E5-1600/2600/4600 v1 Product Families, 4 Core Processor Reference Thermal Boundary Conditions (Square ILM/HS)**

4 Core Processor	Heatsink Technology	$\Psi_{CA}^2$ (°C/W)	$T_{LA}^1$ (°C)	Airflow <sup>3</sup> (CFM)	Delta P (inch of H <sub>2</sub> O)	Heatsink Volumetric <sup>4</sup> (mm)
130W (1S WS Only)	Cu Base, Al Fins (Cu-Al)/ Heatpipe	0.210	39	2600 RPM	N/A	100x100x124
130W (2U)	Cu Base, Al Fins (Cu-Al)/Heatpipe	0.199	47.1	26	0.140	91.5x91.5x64
95W (1U)	Cu Base, Al Fins (Cu-Al)	0.261	49.5	16	0.406	91.5x91.5x25.5
80W (1U)	Cu Base, Al Fins (Cu-Al)	0.269	47.9	16	0.406	91.5x91.5x25.5

**Notes:**

1. Local ambient temperature of the air entering the heatsink.
2. Max target (mean + 3 sigma) for thermal characterization parameter (Section 5.3.2).
3. Airflow through the heatsink fins with zero bypass. Max target for pressure drop (dP) measured in inches H<sub>2</sub>O.
4. Dimensions of heatsink do not include socket or processor.
5. General note: All heatsinks are Non-Direct Chassis Attach (DCA).

**Table 5-3. Intel® Xeon® Processor E5-1600/2600 v2 Product Families, Processor Reference Thermal Boundary Conditions (Square ILM/HS) (Sheet 1 of 2)**

Processor	Heatsink Technology <sup>6</sup>	$\Psi_{CA}^2$ (°C/W)	$T_{LA}^1$ (°C)	Airflow <sup>3</sup> (CFM)	Delta P inch of H <sub>2</sub> O (Pa)	Heatsink Volumetric <sup>4</sup> (mm)
EP 12-core 130W (1U)	Cu Base, Al Fins (Cu-Al)	0.252	53.3	16	0.406	91.5x91.5x25.5
EP/EP 4S 12-core 115W (1U)	Cu Base, Al Fins (Cu-Al)	0.251	51.7	16	0.406	91.5x91.5x25.5
EP WS 8-core 150W	Cu Base, Al Fins (Cu-Al)/ Heatpipe	0.236	35.2	21.8	0.120	100x100x124
EP/EP 4S 10-core 130W (1U)	Cu Base, Al Fins (Cu-Al)	0.265	53.4	16	0.406	91.5x91.5x25.5
EP 4S 8-core 130W (1U)	Cu Base, Al Fins (Cu-Al)	0.269	52.8	16	0.406	91.5x91.5x25.5
EP 8-core 130W (2U)	Cu Base, Al Fins (Cu-Al)/Heatpipe	0.207	47.1	26	0.140	91.5x91.5x64
EP 6-core 130W (2U)	Cu Base, Al Fins (Cu-Al)/Heatpipe	0.207	47.1	26	0.140	91.5x91.5x64
EP 10-core 115W (1U)	Cu Base, Al Fins (Cu-Al)	0.265	51.7	16	0.406	91.5x91.5x25.5
EP/EP 4S 10-core 95W (1U)	Cu Base, Al Fins (Cu-Al)	0.264	49.5	16	0.406	91.5x91.5x25.5
EP/EP 4S 8-core 95W (1U)	Cu Base, Al Fins (Cu-Al)	0.269	49.5	16	0.406	91.5x91.5x25.5
EP 10-core 70W (1U)	Cu Base, Al Fins (Cu-Al)	0.262	46.8	16	0.406	91.5x91.5x25.5
EP 1S WS 6-core 130W	Cu Base, Al Fins (Cu-Al)/ Heatpipe	0.232	39.0	21.8	0.120	100x100x124



**Table 5-3. Intel® Xeon® Processor E5-1600/2600 v2 Product Families, Processor Reference Thermal Boundary Conditions (Square ILM/HS) (Sheet 2 of 2)**

Processor	Heatsink Technology <sup>6</sup>	$\Psi_{CA}^2$ (°C/W)	$T_{LA}^1$ (°C)	Airflow <sup>3</sup> (CFM)	Delta P inch of H <sub>2</sub> O (Pa)	Heatsink Volumetric <sup>4</sup> (mm)
EP 1S WS 4-core 130W	Cu Base, Al Fins (Cu-Al)/ Heatpipe	0.234	39.0	21.8	0.120	100x100x124
EP 4-core 130W (2U)	Cu Base, Al Fins (Cu- Al)/Heatpipe	0.221	47.1	26	0.140	91.5x91.5x64
EP 4S 6-core 95W (1U)	Cu Base, Al Fins (Cu-Al)	0.283	49.5	16	0.406	91.5x91.5x25.5
EP 4S 4-core 95W (1U)	Cu Base, Al Fins (Cu-Al)	0.285	49.5	16	0.406	91.5x91.5x25.5
EP 6-core 80W (1U)	Cu Base, Al Fins (Cu-Al)	0.281	47.9	16	0.406	91.5x91.5x25.5
EP 4-core 80W	Cu Base, Al Fins (Cu-Al)	0.285	47.9	16	0.406	91.5x91.5x25.5
EP 6-core 60W	Cu Base, Al Fins (Cu-Al)	0.280	45.7	16	0.406	91.5x91.5x25.5

**Notes:**

1. Local ambient temperature of the air entering the heatsink.
2. Max target (mean + 3 sigma) for thermal characterization parameter ([Section 5.3.2](#)).
3. Airflow through the heatsink fins with zero bypass. Max target for pressure drop (dP) measured in inches H<sub>2</sub>O.
4. Dimensions of heatsink do not include socket or processor.
5. General note: All heatsinks are Non-Direct Chassis Attach (DCA).

Figure 5-1. 2U Square Heatsink Performance Curves Using Socket-LGA2011-0 TTV

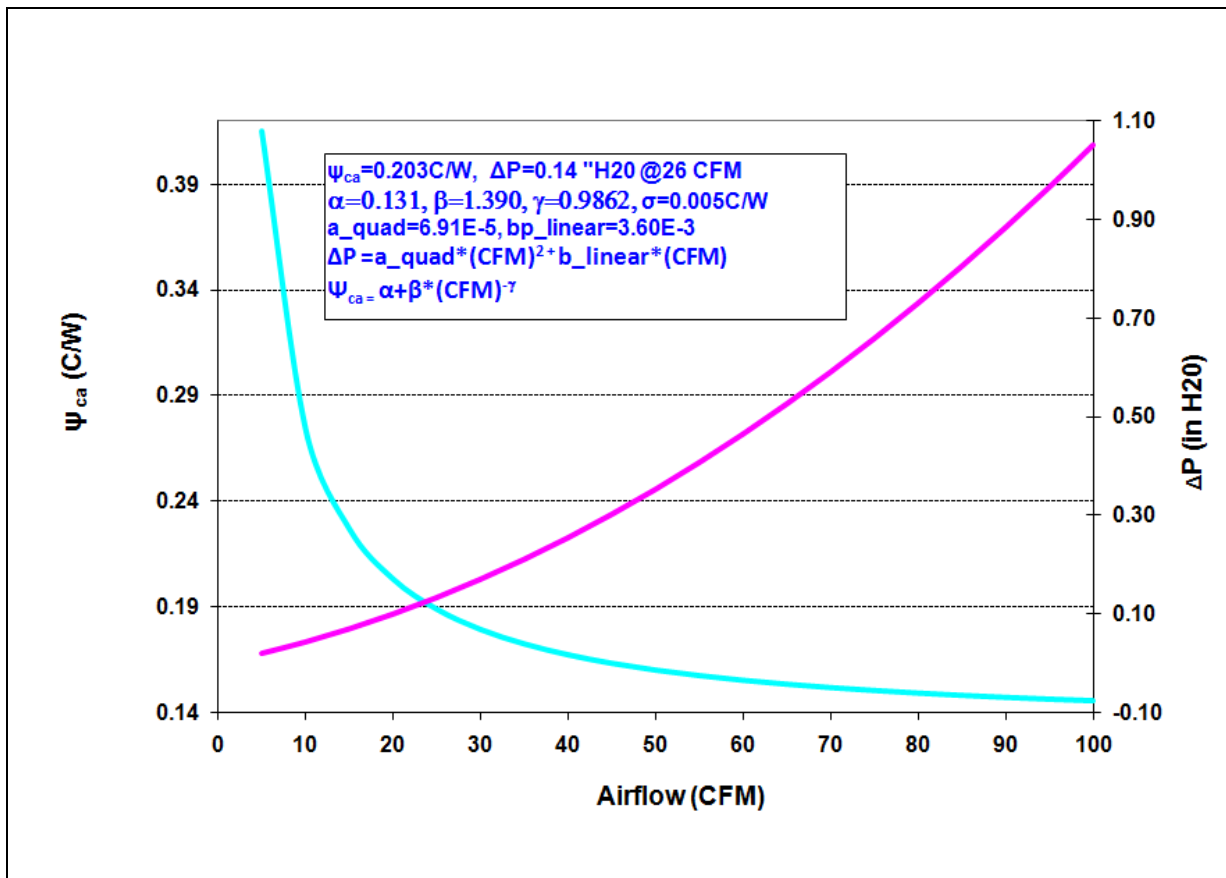
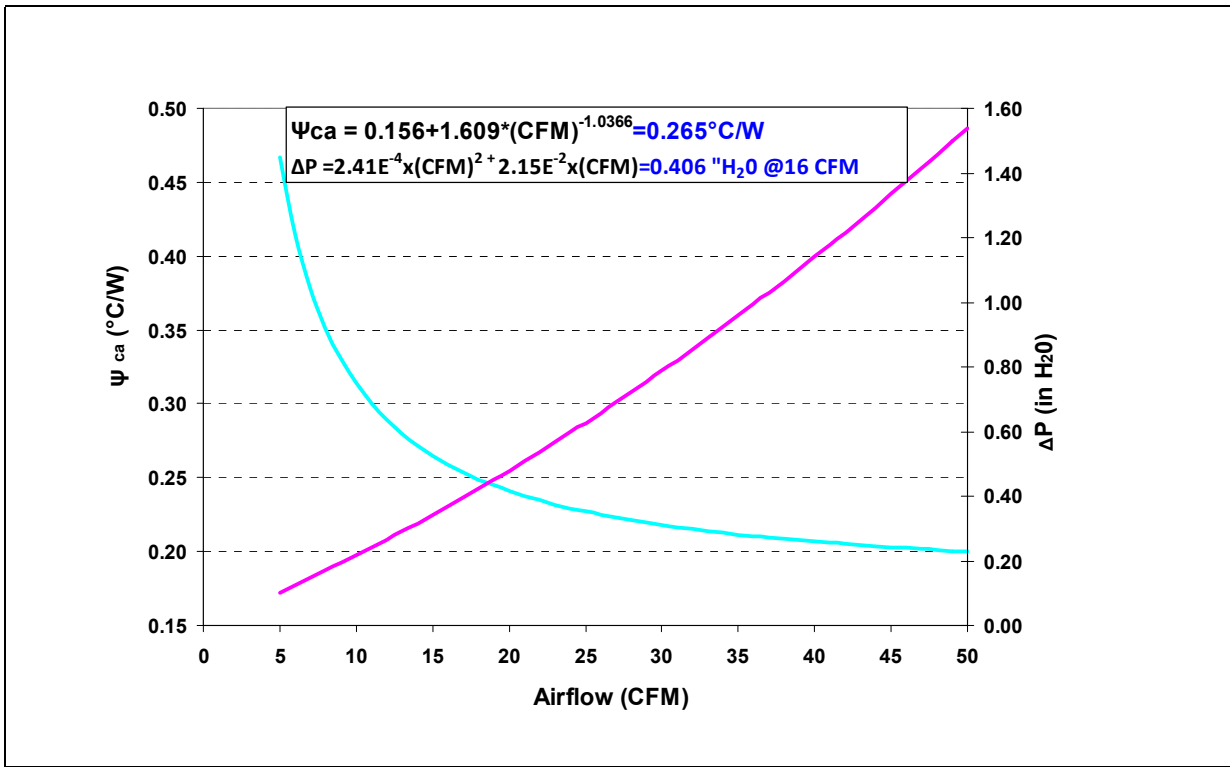


Table 5-4. Performance Curve Data (Graphs in Fig 5-1 and 5-2)

Design Type	$\sigma$	$\alpha$	$\beta$	$\gamma$	A	B	Airflow (CFM)
1U Cu/Al	0.006	0.156	1.609	1.0366	2.41E-04	2.15E-02	16
2U Heatpipe	0.005	0.131	1.39	0.9862	6.91E-05	3.6E-03	26



Figure 5-2. 1U Square Heatsink Performance Curves Using Socket-LGA2011-0 TTV



Equation 5-1.

$$\Psi_{ca}(\text{mean}) = \alpha + \beta x(\text{CFM})^{-\gamma}$$

Equation 5-2.

$$\Delta P = A x(\text{CFM})^2 + B x(\text{CFM})$$



### 5.1.2 Performance Targets - Narrow ILM/Heatsink Application

Table 5-5 and Table 5-6 provides boundary conditions and performance targets for 1U narrow heatsink used in conjunction with the narrow ILM for 8 core/6 core and 4 core processors respectively. These values are used to generate processor thermal specifications and to provide guidance for heatsink design.

All Boundary Conditions are specified at 35°C system ambient temperature and at sea level and Figure 5-3 shows  $\Psi_{CA}$  and pressure drop for the 1U heatsink versus the airflow provided. Best-fit equations are provided to prevent errors associated with reading the graph.

Boundary Conditions added for the narrow ILM/heatsink reference design have no impact on the released thermal profiles/Tcase specifications. There is no change to the Tcase specification.

**Table 5-5. Intel® Xeon® Processor E5-1600/2600/4600 v1 Product Families, 8 Core/6 Core Processor Reference Thermal Boundary Conditions (Narrow ILM/HS)**

TDP	Heatsink Technology	$\Psi_{CA}^2$ (°C/W)	$T_{LA}^1$ (°C)	Airflow <sup>3</sup> (CFM)	Delta P (inch of H <sub>2</sub> O) (Pa)	Heatsink Volumetric <sup>4</sup> (mm)
130W (1U)	Cu Base, Al Fins (Cu-Al)	0.323	43	14	0.347	70x106x25.5
95W (1U)		0.316				
70W (1U)		0.300				
60W (1U)		0.283				

**Table 5-6. Intel® Xeon® Processor E5-1600/2600/4600 v1 Product Families, 4 Core Processor Reference Thermal Boundary Conditions (Narrow ILM/HS)**

4 Core Processor	Heatsink Technology	$\Psi_{CA}^2$ (°C/W)	$T_{LA}^1$ (°C)	Airflow <sup>3</sup> (CFM)	Delta P (inch of H <sub>2</sub> O)	Heatsink Volumetric <sup>4</sup> (mm)
80W (1U)	Cu Base, Al Fins (Cu-Al)	0.325	43	14	0.347	70x106x25.5

**Notes:**

1. Local ambient temperature of the air entering the heatsink.
2. Max target (mean + 3 sigma) for thermal characterization parameter (Section 5.3.2).
3. Airflow through the heatsink fins with zero bypass. Max target for pressure drop (dP) measured in inches H<sub>2</sub>O.
4. Dimensions of heatsink do not include socket or processor.
5. General note: All heatsinks are Non-Direct Chassis Attach (DCA).





**Table 5-7. Intel® Xeon® Processor E5-1600/2600 v2 Product Families, Processor Reference Thermal Boundary Conditions (Narrow ILM/HS)**

Processor	Heatsink Technology	$\Psi_{CA}^2$ (°C/W)	$T_{LA}^1$ (°C)	Airflow <sup>3</sup> (CFM)	Delta P inch of H <sub>2</sub> O (Pa)	Heatsink Volumetric <sup>4</sup> (mm)
12-core 130W (1U)	Cu Base, Al Fins (Cu-Al)	0.331	43	14	0.347	70x106x25.5
12-core 115W (1U)		0.322				
10-core 130W (1U)		0.346				
8-core 130W (1U)		0.352				
10-core 115W (1U)		0.339				
10-core 95W (1U)		0.337				
8-core 95W (1U)		0.337				
10-core 70W (1U)		0.329				
6-core 95W (1U)		0.358				
4-core 95W (1U)		0.358				
6-core 80W (1U)		0.350				
4-core 80W (1U)		0.350				
6-core 60W (1U)		0.334				

**Notes:**

1. Local ambient temperature of the air entering the heatsink.
2. Max target (mean + 3 sigma) for thermal characterization parameter ([Section 5.3.2](#)).
3. Airflow through the heatsink fins with zero bypass. Max target for pressure drop (dP) measured in inches H<sub>2</sub>O.
4. Dimensions of heatsink do not include socket or processor.

General note: All heatsinks are Non-Direct Chassis Attach (DCA).

Figure 5-3. 1U Narrow Heatsink Performance Curves Using Socket-LGA2011-0 TTV

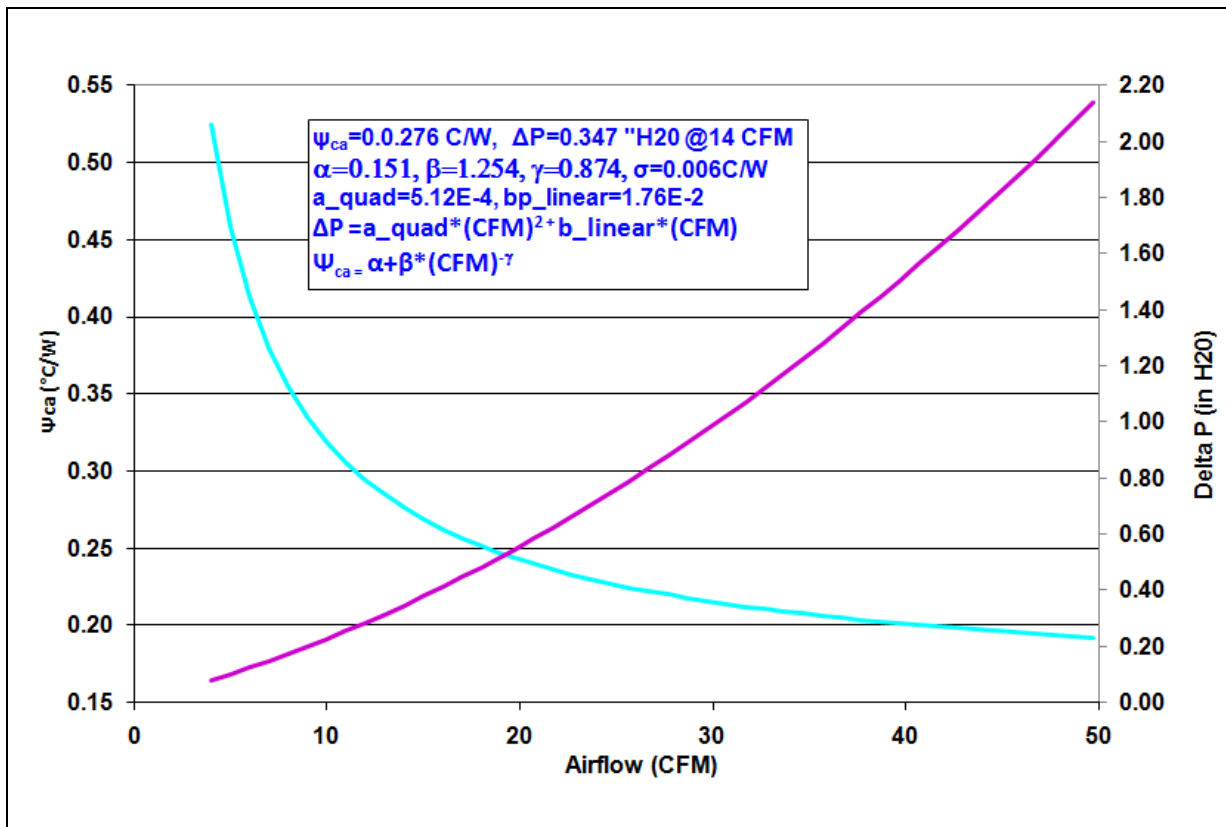


Table 5-8. Performance Curve Data

Design Type	$\sigma$	$\alpha$	$\beta$	$\gamma$	A	B	Airflow (CFM)
1U Cu/Al	0.006	0.151	1.254	0.874	5.12E-04	1.76E-02	14

Equation 5-3.

$$\Psi_{ca}(\text{mean}) = \alpha + \beta x(\text{CFM})^{-\gamma}$$

Equation 5-4.

$$\Delta P = Ax(\text{CFM})^2 + Bx(\text{CFM})$$

### 5.1.3 Reference Heatsink Assembly

The assembly process for the reference heatsink begins with application of PCM45F TIM to improve conduction from the IHS. The recommended TIM to ensure full coverage of the IHS is 35x35 mm square with a thickness of 0.25 mm.

Next, position the heatsink such that the heatsink fins are parallel to system airflow. While lowering the heatsink onto the IHS, align the four captive screws of the heatsink to the four threaded studs on the ILM frame.



Using a #2 Phillips driver, torque the four captive screws to 9 inch-pounds  $\pm 1$  inch-pound.

Fastener sequencing (starting the threads on all four screws before torquing), may mitigate against cross-threading.

Compliance to Board Keepout Zones in [Appendix A](#) is assumed for this assembly process.

Square ILM/Heatsink assembly shown below in [Figure 5-4](#). Narrow ILM/Heatsink assembly shown below in [Figure 5-5](#).

**Figure 5-4. Reference Square ILM/Heatsink Assembly**

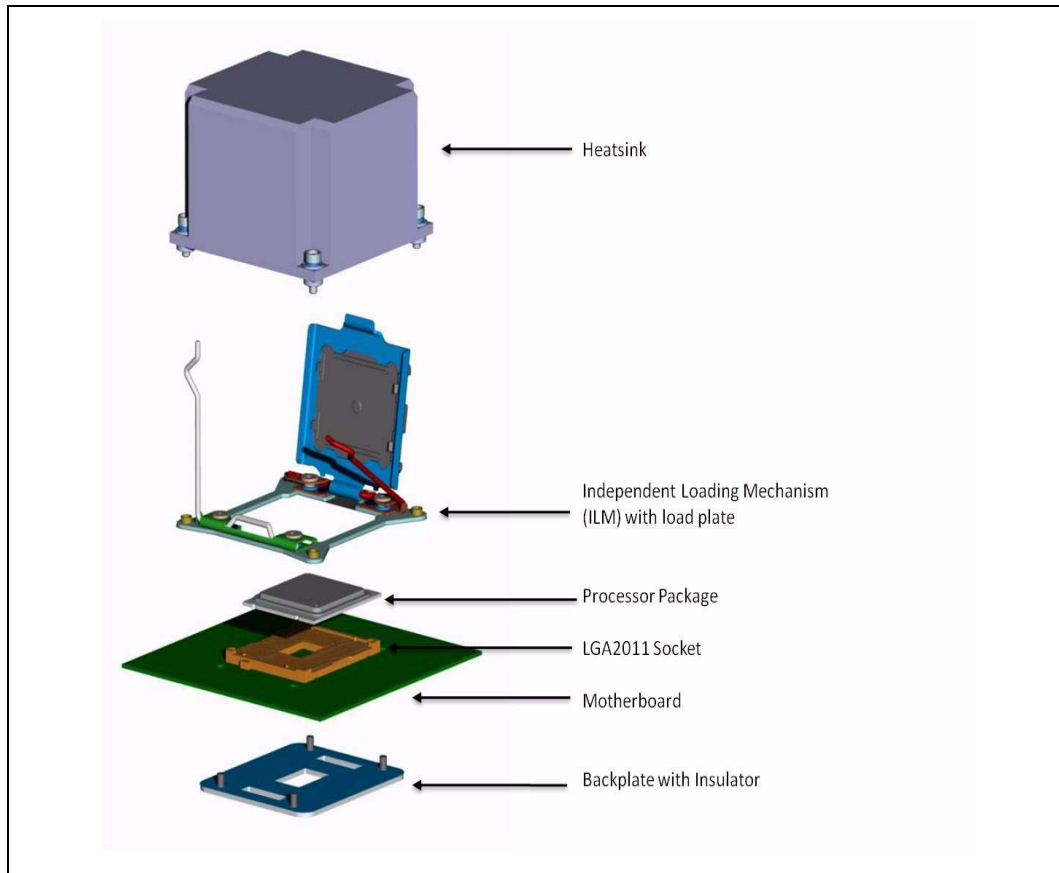
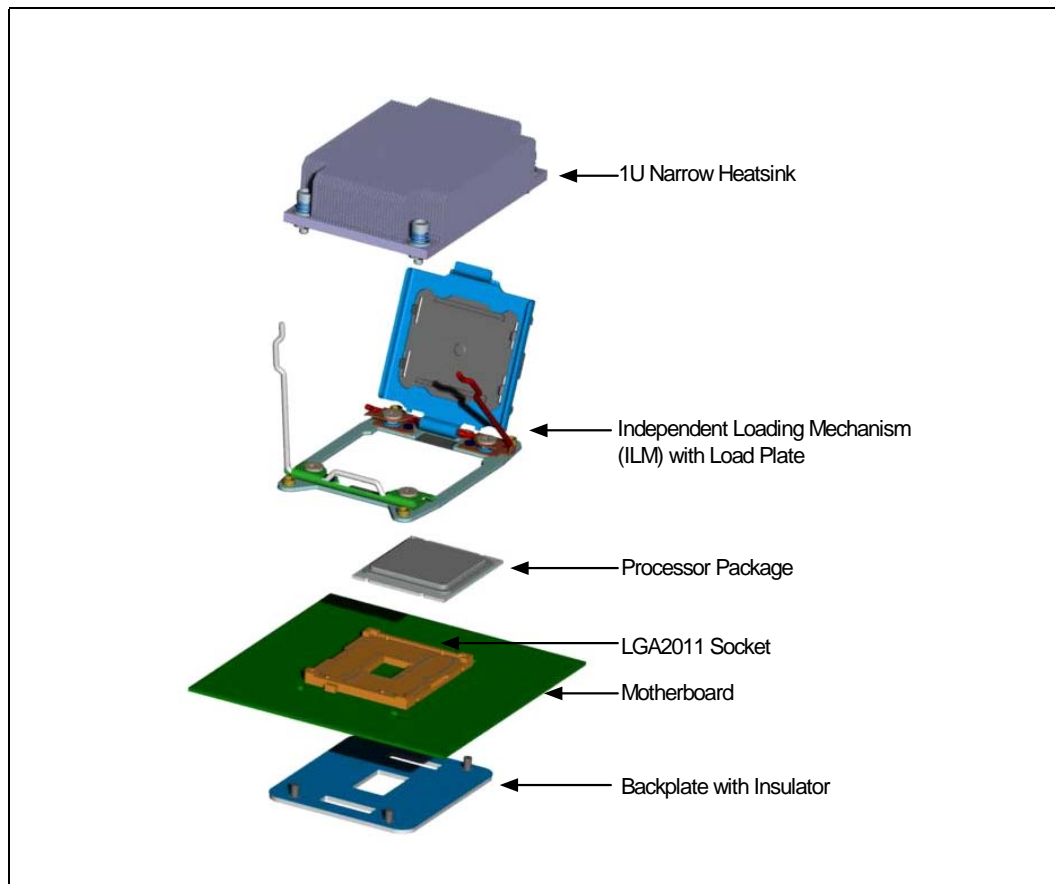


Figure 5-5. Reference Narrow ILM/Heatsink Assembly



## 5.2 Structural Considerations

Mass of the reference heatsink and the target mass for heatsinks does not exceed 550 g (Server segment).

From [Table 4-3](#), the Dynamic Compressive Load of 540N[121 lbf] max allows for designs that exceed 550 g[1.21lb] as long as the dynamic load does not exceed 540N[121 lbf]. The Static Compressive Load ([Table 4-3](#)) should also be considered in dynamic assessments.

The heatsink limit of 550 g[1.21lb] and use of ILM Frame have eliminated the need for Direct Chassis Attach retention (as used with previous Intel® Xeon® processors using socket LGA771).

Placement of board-to-chassis mounting holes also impacts board deflection and resultant socket solder ball stress. Customers need to assess shock for their designs as their heatsink retention, heatsink mass and chassis mounting holes may vary.

## 5.3 Thermal Design Guidelines

Additional information regarding processor thermal features is contained in the appropriate datasheet.



### 5.3.1 Intel® Turbo Boost Technology

Intel® Turbo Boost Technology available on certain processor SKUs, opportunistically, and automatically, allows the processor to run faster than the marked frequency if the part is operating below its power, temperature and current limits.

Heatsink performance (lower  $\Psi_{CA}$  as described in [Section 5.3.2](#)) is one of several factors that can impact the amount of Intel Turbo Boost Technology frequency benefit. Intel Turbo Boost Technology performance is also constrained by ICC, and VCC limits.

Increased IMON accuracy may provide more Intel Turbo Boost Technology benefit on TDP limited applications, as compared to lower  $\Psi_{CA}$ , as temperature is not typically the limiter for these workloads. *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 12.0 Design Guidelines*

With Intel Turbo Boost Technology enabled, the processor may run more consistently at higher power levels (but still within TDP), and be more likely to operate above  $T_{CONTROL}$ , as compared to when Intel Turbo Boost Technology is disabled. This may result in higher acoustics.

### 5.3.2 Thermal Characterization Parameter

The case-to-local ambient Thermal Characterization Parameter ( $\Psi_{CA}$ ) is defined by:

#### Equation 5-5.

$$\Psi_{CA} = (T_{CASE} - T_{LA}) / TDP$$

Where:

- $T_{CASE}$  = Processor case temperature (°C). For  $T_{CASE}$  specification see *Intel® Xeon® Processor E5-1600/E5-2600/E5-4600 Product Families External Design Specification (EDS) - Volume One*.
- $T_{LA}$  = Average ambient temperature entering the processor heat sink fin section (°C).
- $TDP$  = TDP (W) assumes all power dissipates through the integrated heat spreader. This inexact assumption is convenient for heatsink design. TTVs are often used to dissipate TDP. .

#### Equation 5-6.

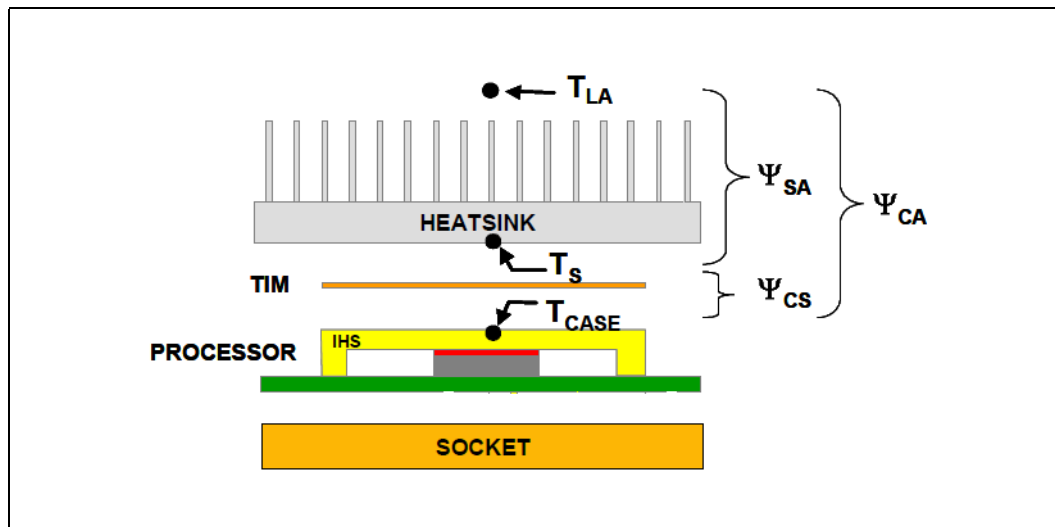
$$\Psi_{CA} = \Psi_{CS} + \Psi_{SA}$$

Where:

- $\Psi_{CS}$  = Thermal characterization parameter of the TIM (°C/W) is dependent on the thermal conductivity and thickness of the TIM.
- $\Psi_{SA}$  = Thermal characterization parameter from heatsink-to-local ambient (°C/W) is dependent on the thermal conductivity and geometry of the heatsink and dependent on the air velocity through the heatsink fins.

Figure 5-6 illustrates the thermal characterization parameters.

Figure 5-6. Processor Thermal Characterization Parameter Relationships



### 5.3.3 Fan Speed Control

In server platforms, processors often share airflow provided by system fans with other system components such as chipset, memory and hard drives. As such, the thermal control features in chipset, memory and other components not covered in this document, should influence system fan speed control to reduce fan power consumption and help systems meet acoustic targets.

The addition of thermal sensors placed in the system (for example, on front panel or motherboard) to augment internal device sensors (for example, in processor, chipset and memory) will improve the ability to implement need-based fan speed control. The placement of system sensors in cooling zones, where each zone has dedicated fan(s), can improve the ability to tune fan speed control for optimal performance and/or acoustics.

System events such as fan or power supply failure, device events such as TCC Activation or THERMTRIP, and maintenance events such as hot swap time allowance, need to be comprehended to implement appropriate fan speed control to prevent undesirable performance or loss of data.

Tcontrol and its upper and lower limits defined by hysteresis, can be used to avoid fan speed oscillation and undesirable noise variations.

### 5.3.4 Thermal Features

More information regarding processor thermal features is contained in the appropriate datasheet.

#### 5.3.4.1 T<sub>CONTROL</sub> and DTS Relationship

Improved acoustics and lower fan power can be achieved by understanding the T<sub>CONTROL</sub> and DTS relationship, and implementing fan speed control accordingly.



**Table 5-9.  $T_{CONTROL}$  and DTS Relationship**

Condition	Fan Speed Control
$DTS \leq T_{CONTROL}$	Adjust fan speed to maintain $DTS \leq T_{CONTROL}$ .
$DTS > T_{CONTROL}$	Adjust fan speed to keep $T_{CASE}$ at or below the $T_{CASE}$ based thermal profile in the EDS, or adjust fan speed to keep DTS at or below the DTS based thermal profile in the EDS.

**5.3.4.2 Sign Convention and Temperature Filtering**

Digital Thermal Sensor (DTS) and  $T_{control}$  are relative die temperatures offset below the Thermal Control Circuit (TCC) activation temperature. As such, negative sign conventions are understood. While DTS and  $T_{control}$  are available over PECEI and MSR, use of these values in fan speed control algorithms requires close attention to sign convention. See Table 5-10 for the sign convention of various sources.

**Table 5-10. Sign Convention**

	MSR (BWG)	PECEI (EDS)
DTS	(+) using PACKAGE_THERM_STATUS (22:16, Digital Readout)	(-) using GetTemp()
$T_{CONTROL}$	(+) using TEMPERATURE_TARGET (15:8, Temperature Control Offset)	(+) using Temperature Target Read from RdPkgConfig()

Where a positive (+) sign convention is shown in Table 5-10, no sign bit is actually assigned, so writers of firmware code may mistakenly assign a positive sign convention in firmware equations. As appropriate, a negative sign should be introduced.

Where a negative (-) sign convention is shown in Table 5-10, a sign bit is assigned, so firmware code will read a negative sign convention in firmware equations, as desired.

DTS obtained thru MSR (PACKAGE\_THERM\_STATUS) is an instantaneous value. As such, temperature readings over short time intervals may vary considerably using this MSR. For this reason, DTS obtained thru PECEI GetTemp() may be preferred since temperature filtering will provide the thermal trend.

**5.3.5  $T_{control}$  Relief**

Factory configured  $T_{CONTROL}$  values are available in the appropriate Dear Customer Letter or may be extracted by issuing a Mailbox or an RDMSR instruction. See the appropriate datasheet for more information.

Due to increased thermal headroom based on thermal characterization on the latest processors, customers have the option to reduce  $T_{CONTROL}$  to values lower than the factory configured values.

In some situations, use of  $T_{CONTROL}$  Relief can reduce average fan power and improve acoustics. There are no plans to change Intel's specification or the factory configured  $T_{CONTROL}$  values on individual processors.

To implement this relief, customers must re-write code to set  $T_{CONTROL}$  to the reduced values provided in the table below. Implementation is optional. Alternately, the factory configured  $T_{CONTROL}$  values can still be used, or some value between factory configured and Relief. Regardless of  $T_{CONTROL}$  values used, BIOS needs to identify the processor type.



**Table 5-11. T<sub>CONTROL</sub> Relief for E5-1600/E5-2600/E5-4600 v1 Product Families**

TDP, # Core	T <sub>CONTROL</sub> Relief	Max Core Frequency	Factory Configured
150W 8C	-6	3.10 GHz or Lower	-10
135W 8C	-6	2.90 GHz or lower	-10
130W 8C	NONE		-6
130W 6C	NONE		-6
130W 8C, 1S	-6	3.30 GHz or lower	-10
115W 8C	-6	2.60 GHz or lower	-10
95W 8C	-6	2.40 GHz or lower	-10
95W 6C	-6	2.50 GHz or lower	-10
70W 8C	-6	1.80 GHz or lower	-10
60W 6C	-6	2.00 GHz or lower	-10
130W 4C, 1S	NONE	3.60 GHz	-18
130W 4C, 1S	-6	3.00 GHz or lower	-10
130W 4C	-6	3.30 GHz or lower	-8
95W 4C, 4S	-6	2.00 GHz or lower	-10
80W 4C	-6	2.40 GHz or lower	-10
80W 2C	-6	3.00 GHz or lower	-10

**Notes:**

1. Unless otherwise specified, Relief values apply to 2-socket and 4-socket SKUs. 1S = 1-socket, 4S = 4-socket.
2. Relief values do not apply to Embedded (NEBS) SKUs.

Implementation of T<sub>CONTROL</sub> Relief above maintains Intel standards of reliability (based on modeling of the Intel Reference Design). Thermal Profile still applies. If PECL >= T<sub>CONTROL</sub> Relief, then the temperature must meet the T<sub>CASE</sub> or the DTS based Thermal Profile.

In some cases, use of Tcontrol Relief as the trigger point for fan speed control may result in excessive TCC activation. To avoid this, the adjusted trigger point for fan speed control (FSC) is defined as:

$$T_{control\_FSC} = - T_{CONTROL} + T_{control\_offset}$$

Tcontrol\_offset must be chosen such that Tcontrol\_FSC < Tcontrol Relief. As such, Tcontrol\_FSC is an earlier trigger point for fan speed control, as compared to Tcontrol Relief, and can be interpreted as overcooling. When overcooling to Tcontrol\_FSC, margin as defined in Section 5.5.3 and Section 5.5.6 can be ignored. As compared to cooling to Tcontrol Relief, overcooling to Tcontrol\_FSC:

- May increase frequency benefit from Intel Turbo Boost Technology as defined in Section 5.3.1.
- Will increase acoustics
- May result in lower wall power

Customers must characterize a Tcontrol\_offset value for their system to meet their goals for frequency, acoustics and wall power.





For for E5-1600/E5-2600/E5-4600 v2 Product Families, Tcontrol\_offset is programmable in the processor. For more information, see the *Digital Thermal Sensor (DTS) Based Thermal Specifications and Overview*.

### 5.3.6 Short Duration TCC Activation and Catastrophic Thermal Management for Intel® Xeon® Processor E5-1600/2600 / 4600 v1 and v2 Product Families

Systems designed to meet thermal capacity may encounter short durations of throttling, also known as TCC activation, especially when running nonsteady processor stress applications. This is acceptable and is functionally within the intended temperature control parameters of the processor. Such short duration TCC activation is not expected to provide noticeable reductions in application performance, and is typically within the normal range of processor to processor performance variation. Normal amounts of TCC activation occur at PECC values less than -0.25. Such occurrences may cause utilities or operating systems to issue error logs.

PECC = -0.25 indicates a catastrophic thermal failure condition in all studies conducted. As such, to help prevent loss of data, a soft shutdown can be initiated at PECC = -0.25. Since customer designs, boundary conditions, and failure scenarios differ, this guidance should be tested in the customer's system to prevent loss of data during shutdown. PECC command GetTemp() can be used to obtain non-integer PECC values. Similar guidance is expected to be available for Intel® Xeon® Processor E5-1600/E5-2600/E5-4600 Product Family v2 processors.

## 5.4 Absolute Processor Temperature and Thermal Excursion

Intel does not test any third party software that reports absolute processor temperature. As such, Intel cannot recommend the use of software that claims this capability. Since there is part-to-part variation in the TCC (thermal control circuit) activation temperature, use of software that reports absolute temperature can be misleading.

See the appropriate External Design Specification (EDS) for details regarding use of TEMPERATURE\_TARGET register to determine the minimum absolute temperature at which the TCC will be activated and PROCHOT# will be asserted.

Under fan failure or other anomalous thermal excursions, Tcase may exceed the thermal profile for a duration totaling less than 360 hours per year without affecting long term reliability (life) of the processor. For more typical thermal excursions, Thermal Monitor is expected to control the processor power level as long as conditions do not allow the Tcase to exceed the temperature at which Thermal Control Circuit (TCC) activation initially occurred. Under more severe anomalous thermal excursions when the processor temperature cannot be controlled at or below this Tcase level by TCC activation, then data integrity is not assured. At some higher threshold, THERMTRIP\_N will enable a shut down in an attempt to prevent permanent damage to the processor. Thermal Test Vehicle (TTV) may be used to check anomalous thermal excursion compliance by ensuring that the processor Tcase value, as measured on the TTV, does not exceed Tcase\_max at the anomalous power level for the environmental condition of interest. This anomalous power level is equal to 75% of the Thermal Design Power (TDP) limit.



This guidance can be applied to 150W, 135W, 130W, 115W, 95W, 80W, 70W, 60W Standard or Basic SKUs in the Intel® Xeon® processor E5-1600/E5-2600/E5-4600 v1 product families. Similar guidance is expected to be available for E5-1600/E5-2600/E5-4600 v2 product families.

## 5.5 DTS Based Thermal Specification

**Note:** This section only applies to Intel® Xeon® Processor E5-1600/2600/4600 v1 Product Families.

### 5.5.1 Implementation

Processor heatsink design must still comply with the Tcase based thermal profile provided in section 5.1 of the Intel® Xeon® Processor E5-1600/E5-2600/E5-4600 v1 Product Families Datasheet - Volume One. Heatsink design compliance can be determined with thermocouple and TTV as with previous processors.

The heat sink is sized to comply with the Tcase based thermal profile. Customers have an option to either follow processor based Tcase spec or follow the DTS based thermal specification. In some situations, implementation of DTS based thermal specification can reduce average fan power and improve acoustics as compared to the Tcase based thermal profile.

When all cores are active, a properly sized heatsink will be able to meet the DTS based thermal specification. When all cores are not active or when Intel Turbo Boost Technology is active, attempting to comply with the DTS based thermal specification may drive system fans to increased speed. In such situations, the T<sub>CASE</sub> temperature will be below the T<sub>CASE</sub> based thermal profile by design.

### 5.5.2 Considerations for Intel® Xeon® Processor E5-1600/E5-2600/E5-4600 v2 Product Family Processors

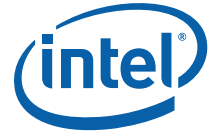
The Intel® Xeon® Processor E5-1600/E5-2600/E5-4600 v2 Product Family processor will have new capabilities as compared to the Intel Xeon Processor E5-1600/E5-2600/E5-4600 v1 Product Family. For example, the v2 processor has a new Package Configuration Space (PCS) command to read margin (M) from the processor: RdPkgConfig(), Index 10. For the Intel Xeon Processor E5-1600/E5-2600/E5-4600 Product Family v1, margin (M) must be calculated in firmware. In the following sections, implementation details specified for the Intel Xeon Processor E5-1600/E5-2600/E5-4600 v1 Product Family can also be used for the Intel® Xeon® Processor E5-1600/E5-2600/E5-4600 v2 Product Family processor.

For more information regarding the differences between the Intel® Xeon® Processor E5-1600/E5-2600/E5-4600 v1 Product Family and the Intel® Xeon® Processor E5-1600/E5-2600/E5-4600 v2 Product Family see *the Platform Digital Thermal Sensor (DTS) Based Thermal Specifications and Overview*.

### 5.5.3 DTS Based Thermal Profile, Tcontrol and Margin for the Intel Xeon Processor E5-1600/E5-2600/E5-4600 v1 Product Family

Calculation of the DTS based thermal specification is based on both Tcontrol and the DTS Based Thermal Profile (T<sub>DTS</sub>):

$$T_{DTS} = \min[T_{LA} + \Psi_{pa} * P * F, \text{TEMPERATURE\_TARGET [23:16]} - T_{cc\_Offset}]$$



Where  $T_{LA}$  and  $\Psi_{pa}$  are the intercept and slope terms from the  $T_{DTS}$  equations in section 5.1 of the Intel® Xeon® Processor E5-1600/E5-2600/E5-4600 v1 Product Families Datasheet - Volume One. To implement the DTS based thermal specification, these equations must be programmed in firmware. Since the equations differ with processor SKU, SKUs can be identified by TDP, Core Count, and a profile identifier (CSR bits). For associated commands, see *Platform Digital Thermal Sensor (DTS) Based Thermal Specifications and Overview*.

Power (P) is calculated in [Section 5.5.4](#). As power dynamically changes, the specification also changes, so power and  $T_{DTS}$  calculations are recommended every 1 second.

Correction factor (F) compensates for the error in power monitoring. The current estimate for F is 0.95.

The Tcontrol portion of the DTS based thermal specification is a one time calculation:

$$T_{\text{control\_spec}} = \text{TEMPERATURE\_TARGET [23:16]} - T_{\text{control}} + T_{\text{control\_offset}}$$

Tcontrol is defined in [Section 5.3.3](#). Tcontrol\_offset is defined in [Section 5.3.5](#)

The final DTS based thermal specification is the maximum of both:

$$T_{\text{DTS\_max}} = \max[T_{\text{control\_spec}}, T_{\text{DTS}}]$$

The margin (M) between the actual die temperature and the DTS based thermal specification is used in the fan speed control algorithm. When  $M < 0$ , increase fan speed. When  $M > 0$ , fan speed may decrease.

$$M = T_{\text{DTS\_max}} - T_{\text{sensor}}$$

OR

$$M = T_{\text{DTS\_ave}} - T_{\text{sensor}}$$

Tsensor represents the absolute temperature of the processor as power changes:

$$T_{\text{sensor}} = \text{TEMPERATURE\_TARGET [23:16]} + \text{DTS}$$

$T_{\text{DTS\_ave}}$  is defined in [Section 5.5.5](#).

TEMPERATURE\_TARGET [23:16], the temperature at which the processor thermal control circuit activates, is a one time PECEI readout: RdPkgConfig(), Temperature Target Read, 23:16.

DTS, the relative temperature from thermal control circuit activation, is negative by definition, and changes instantaneously. DTS command info is given in [Section 5.3.3](#).

#### 5.5.4 Power Calculation for the Intel Xeon Processor E5-1600/E5-2600/E5-4600 v1 Product Family

To implement DTS based thermal specification, average power over time must be calculated:

$$P = (E2 - E1) / (t2 - t1)$$

Where:

t1 = time stamp 1

t2 = time stamp 2

E1 = Energy readout at time t1

E2 = Energy readout at time t2



The recommended time interval between energy readings is 1 second. This helps ensure the power calculation is accurate by making the error between time stamps small as compared to the duration between time stamps.

For details regarding energy readings, see *Platform Digital Thermal Sensor (DTS) Based Thermal Specifications and Overview*.

### 5.5.5 Averaging the DTS Based Thermal Specification for the Intel Xeon E5-1400/E5-2600/E5-4600 v1 Product Family

Averaging the DTS Based Thermal Specification helps keep the rate of change of the temperature specification on the same scale as the actual processor temperature, and helps avoid rapid changes in fan speed when power changes rapidly.

An exponential average of the specification can be calculated using a two time constant model:

$$T_{DTS\_f} = \alpha_f \times \Delta t \times T_{DTS\_max} + T_{DTS\_f\_previous} \times (1 - \alpha_f \times \Delta t)$$

$$T_{DTS\_s} = \alpha_s \times \Delta t \times T_{DTS\_max} + T_{DTS\_s\_previous} \times (1 - \alpha_s \times \Delta t)$$

$$T_{DTS\_ave} = C \times T_{DTS\_f} \times (1 - C) \times T_{DTS\_s}$$

Where:

- $T_{DTS\_max}$  is the instantaneous spec
- $T_{DTS\_f}$  and  $T_{DTS\_s}$  are the fast and slow time averages
- $T_{DTS\_ave}$  is the final two time constant average specification
- $\alpha_f$  and  $\alpha_s$  are the time constant coefficients
- C is a scale factor
- $\Delta t$  is the scan rate and is recommended to be approximately 1 second

Table 5-12 below shows the initial coefficients recommended for averaging. These values may change per processor SKU. Customers should tune these coefficients based on their thermal solutions.

Table 5-12. Averaging Coefficients

Heatsink Performance	$\alpha_f$ (1/s)	$\alpha_s$ (1/s)	C	Comment
Low	1.0	0.04	0.30	Based on typical processor
Medium	1.0	0.07	0.30	Based on typical processor
High	1.0	0.10	0.40	Based on typical processor

### 5.5.6 Capabilities for the Intel® Xeon® Processor E5-1600/E5-2600/E5-4600 v2 Product Family

For Intel® Xeon® Processor E5-1600/E5-2600/E5-4600 v2 Product Family, the intercept and slope terms from the  $T_{DTS}$  equations ( $T_{LA}$ ,  $\Psi_{pa}$ ), as defined in Section 5.5.3, are stored in the processor. This allows margin (M) to be reported by the processor. The PECC command for margin (M) will be `RdPkgConfig()`, Index 10.

- M < 0; gap to spec, fan speed must increase
- M > 0; margin to spec, fan speed may decrease

Use of `RdPkgConfig()`, Index 10 with the Intel Xeon E5-1600/E5-2600/E5-4600 v1 Product Family will return an illegal command.



For Intel® Xeon® Processor E5-1600/E5-2600/E5-4600 Product Family v2, coefficients ( $\alpha_f$ ,  $\alpha_s$ ), scale factor (C), and correction factor (F) will be factory configured.





# 6 Quality and Reliability Requirements

## 6.1 Use Conditions

Intel evaluates reliability performance based on the use conditions (operating environment) of the end product by using acceleration models.

The use condition environment definitions provided in [Table 6-1](#) and [Table 6-2](#) are based on speculative use condition assumptions, and are provided as **examples only**.

Based on the system enabling boundary condition, the solder ball temperature can vary and needs to be comprehended for reliability assessment.

**Table 6-1. Server Use Conditions Environment (System Level)**

Use Environment	Speculative Stress Condition	Example Use Condition	Example 7-Yr Stress Equiv.	Example 10-Yr Stress Equiv.
Slow small internal gradient changes due to external ambient (temperature cycle or externally heated) Fast, large gradient on/off to max operating temp. (power cycle or internally heated including power save features)	Temperature Cycle	$\Delta T = 35 - 44^{\circ}\text{C}$ (solder joint)	550-930 cycles Temp Cycle ( $-25^{\circ}\text{C}$ to $100^{\circ}\text{C}$ )	780-1345 cycles Temp Cycle ( $-25^{\circ}\text{C}$ to $100^{\circ}\text{C}$ )
High ambient moisture during low-power state (operating voltage)	THB/HAST	$T = 25 - 30^{\circ}\text{C}$ 85%RH (ambient)	110-220 hrs at $110^{\circ}\text{C}$ 85%RH	145-240 hrs at $110^{\circ}\text{C}$ 85%RH
High Operating temperature and short duration high temperature exposures	Bake	$T = 95 - 105^{\circ}\text{C}$ (contact)	700 – 2500 hrs at $125^{\circ}\text{C}$	800 – 3300 hrs at $125^{\circ}\text{C}$



Table 6-2. Server Use Conditions Environment (System Level)

Use Environment	Speculative Stress Condition		Example Use Condition
Shipping and Handling	<u>Mechanical Shock</u> <ul style="list-style-type: none"> <li>• System-level</li> <li>• Unpackaged</li> <li>• Trapezoidal</li> <li>• 25 g</li> <li>• velocity change is based on packaged weight</li> </ul>		Total of 12 drops per system: <ul style="list-style-type: none"> <li>• 2 drops per axis</li> <li>• ± direction</li> </ul>
	Product Weight (lbs)	Non-palletized Product Velocity Change (in/sec)	
	< 20 lbs 20 to > 40 40 to > 80 80 to < 100 100 to < 120 ≥120	250 225 205 175 145 125	
Change in velocity is based upon a 0.5 coefficient of restitution.			
Shipping and Handling	<u>Random Vibration</u> <ul style="list-style-type: none"> <li>• System Level</li> <li>• Unpackaged</li> <li>• 5 Hz to 500 Hz</li> <li>• 2.20 g RMS random</li> <li>• 5 Hz @ 0.001 g<sup>2</sup>/Hz to 20 Hz @ 0.01 g<sup>2</sup>/Hz (slope up)</li> <li>• 20 Hz to 500 Hz @ 0.01 g<sup>2</sup>/Hz (flat)</li> <li>• Random control limit tolerance is ± 3 dB</li> </ul>		<u>Total per system:</u> <ul style="list-style-type: none"> <li>• 10 minutes per axis</li> <li>• 3 axes</li> </ul>

## 6.2 Intel Reference Component Validation

Intel tests reference components individually and as an assembly on mechanical test boards and assesses performance to the envelopes specified in previous sections by varying boundary conditions.

While component validation shows a reference design is tenable for a limited range of conditions, customers need to assess their specific boundary conditions and perform reliability testing based on their use conditions.

Intel reference components are also used in board functional tests to assess performance for specific conditions.

### 6.2.1 Board Functional Test Sequence

Each test sequence should start with components (baseboard, heatsink assembly, and so on) that have not been previously submitted to any reliability testing.

Prior to the mechanical shock & vibration test, the units under test should be preconditioned for 72 hours at 45°C. The purpose is to account for load relaxation during burn-in stage.

The test sequence should always start with a visual inspection after assembly, and BIOS/Processor/memory test. The stress test should be then followed by a visual inspection and then BIOS/processor/memory test.





## 6.2.2 Post-Test Pass Criteria Examples

The post-test pass criteria examples are:

1. No significant physical damage to the heatsink and retention hardware.
2. Heatsink remains seated and its bottom remains mated flat against the IHS surface. No visible gap between the heatsink base and processor IHS. No visible tilt of the heatsink with respect to the retention hardware.
3. No signs of physical damage on baseboard surface due to impact of heatsink.
4. No visible physical damage to the processor package.
5. Successful BIOS/Processor/memory test of post-test samples.
6. Thermal compliance testing to demonstrate that the case temperature specification can be met.

## 6.2.3 Recommended BIOS/Processor/Memory Test Procedures

This test is to ensure proper operation of the product before and after environmental stresses, with the thermal mechanical enabling components assembled. The test shall be conducted on a fully operational baseboard that has not been exposed to any battery of tests prior to the test being considered.

Testing setup should include the following components, properly assembled and/or connected:

- Appropriate system baseboard.
- Processor and memory.
- All enabling components, including socket and thermal solution parts.

The pass criterion is that the system under test shall successfully complete the checking of BIOS, basic processor functions and memory, without any errors. *Intel PC Diags* is an example of software that can be utilized for this test.

## 6.3 Material and Recycling Requirements

Material shall be resistant to fungal growth. Examples of non-resistant materials include cellulose materials, animal and vegetable based adhesives, grease, oils, and many hydrocarbons. Synthetic materials such as PVC formulations, certain polyurethane compositions (for example, polyester and some polyethers), plastics which contain organic fillers of laminating materials, paints, and varnishes also are susceptible to fungal growth. If materials are not fungal growth resistant, then MIL-STD-810E, Method 508.4 must be performed to determine material performance. Cadmium shall not be used in the painting or plating of the socket. CFCs and HFCs shall not be used in manufacturing the socket.

Any plastic component exceeding 25 gm should be recyclable per the European Blue Angel recycling standards.

Supplier is responsible for complying with industry standards regarding environmental care as well as with the specific standards required per Supplier's region. More specifically, Supplier is responsible for compliance with the European regulations related to restrictions on the use of Lead and Bromine containing flame-retardants. Legislation varies by geography, European Union (RoHS/WEEE), China, California, and so forth.

The following definitions apply to the use of the terms lead-free, Pb-free, and RoHS compliant.



**Halogen flame retardant free (HFR-Free) PCB:** In future revisions of this document, Intel will be providing guidance on the mechanical impact to using a HFR-free laminate in the PCB. This will be limited to workstations.

**Lead-free and Pb-free:** Lead has not been intentionally added, but lead may still exist as an impurity below 1000 ppm.

**RoHS compliant:** Lead and other materials banned in RoHS Directive are either (1) below all applicable substance thresholds as proposed by the EU or (2) an approved/pending exemption applies.

**Note:** RoHS implementation details are not fully defined and may change.

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# A Mechanical Drawings

Table A-1 lists the Mechanical drawings included in this appendix.

**Table A-1. Mechanical Drawing List**

Description	Figure
Square ILM Board Keepouts 1 of 4	Figure A-1
Square ILM Board Keepouts 2 of 4	Figure A-2
Square ILM Board Keepouts 3 of 4	Figure A-3
Square ILM Board Keepouts 4 of 4	Figure A-4
Narrow ILM Board Keepouts 1 of 4	Figure A-5
Narrow ILM Board Keepouts 2 of 4	Figure A-6
Narrow ILM Board Keepouts 3 of 4	Figure A-7
Narrow ILM Board Keepouts 4 of 4	Figure A-8
2U Square Heatsink Assembly Without TIM 1 of 2	Figure A-9
2U Square Heatsink Assembly Without TIM 2 of 2	Figure A-10
2U Square Heatsink Volumetric 1 of 2	Figure A-11
2U Square Heatsink Volumetric 2 of 2	Figure A-12
Heatsink Screw M4x0.7	Figure A-13
Heatsink Compression Spring	Figure A-14
Heatsink Retaining Ring	Figure A-15
Heatsink Delrin Spacer	Figure A-16
1U Square Heatsink Assembly 1 of 2	Figure A-17
1U Square Heatsink Assembly 2 of 2	Figure A-18
1U Square Heatsink Geometry 1 of 2	Figure A-19
1U Square Heatsink Geometry 2 of 2	Figure A-20
Heatsink Cup For Spring Retention	Figure A-21
1U Narrow Heatsink Assembly 1 of 2	Figure A-22
1U Narrow Heatsink Assembly 2 of 2	Figure A-23
1U Narrow Heatsink Geometry 1 of 2	Figure A-24
1U Narrow Heatsink Geometry 2 of 2	Figure A-25





Figure A-2. Square ILM Board Keepouts 2 of 4

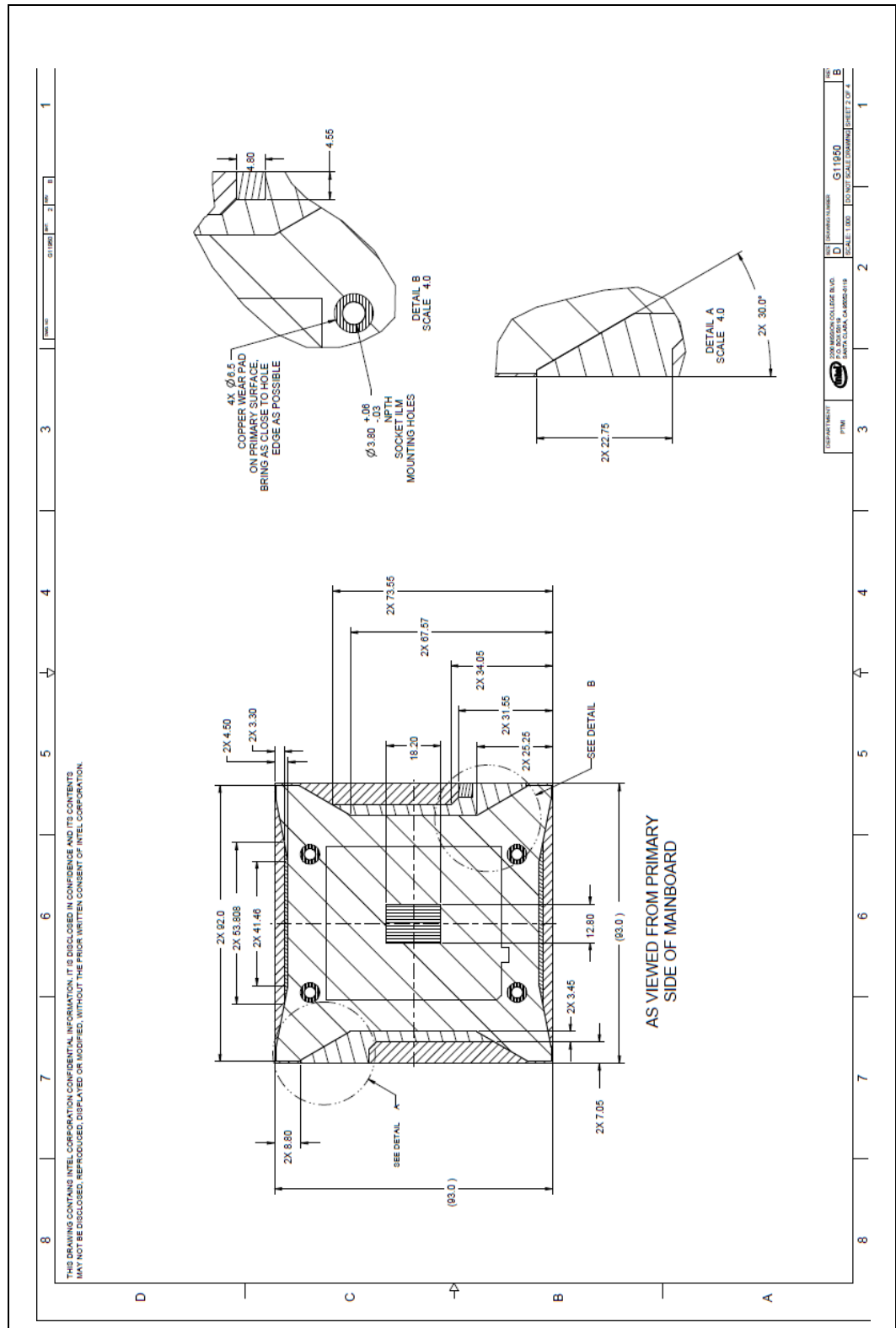


Figure A-3. Square ILM Board Keepouts 3 of 4

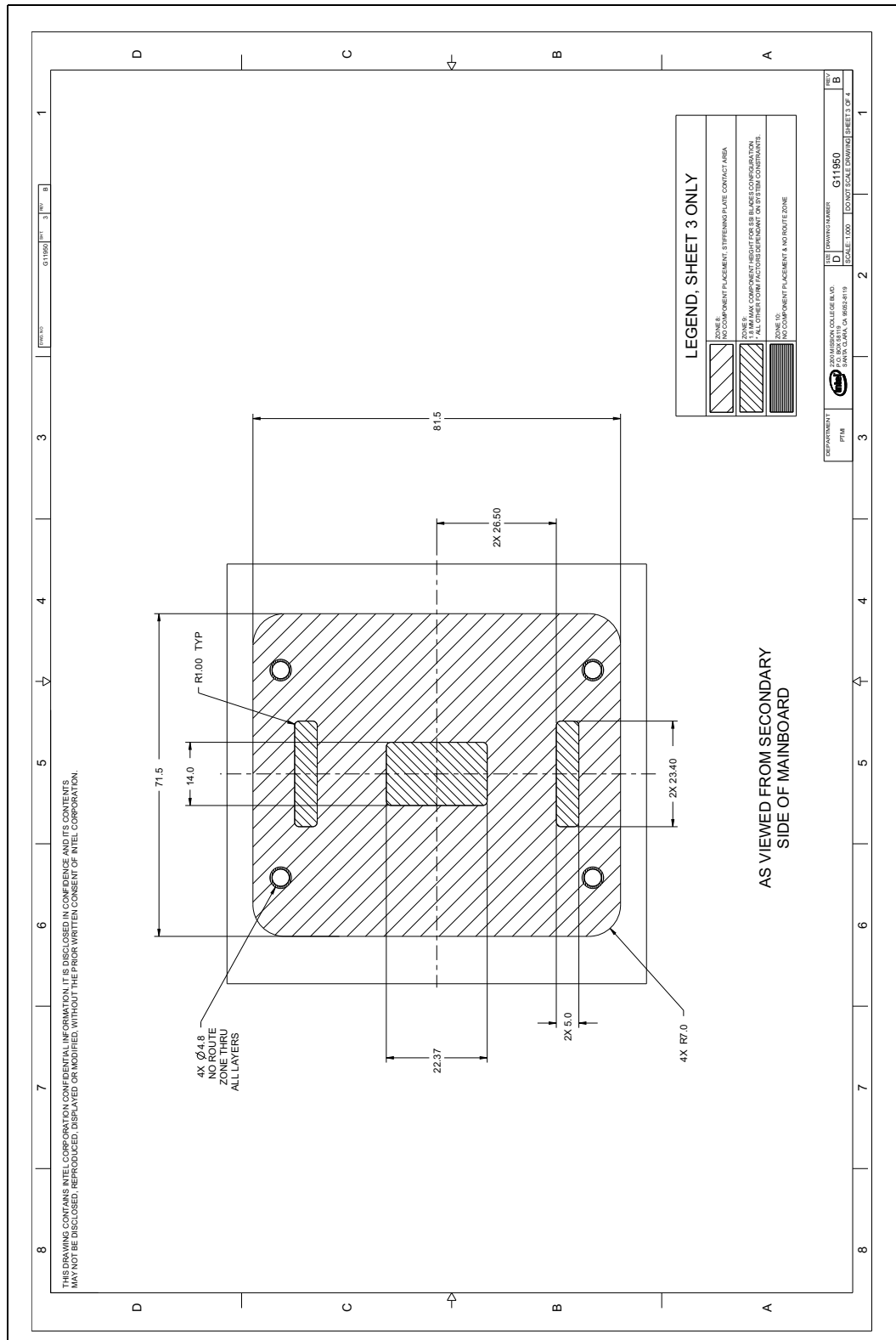




Figure A-4. Square ILM Board Keepouts 4 of 4

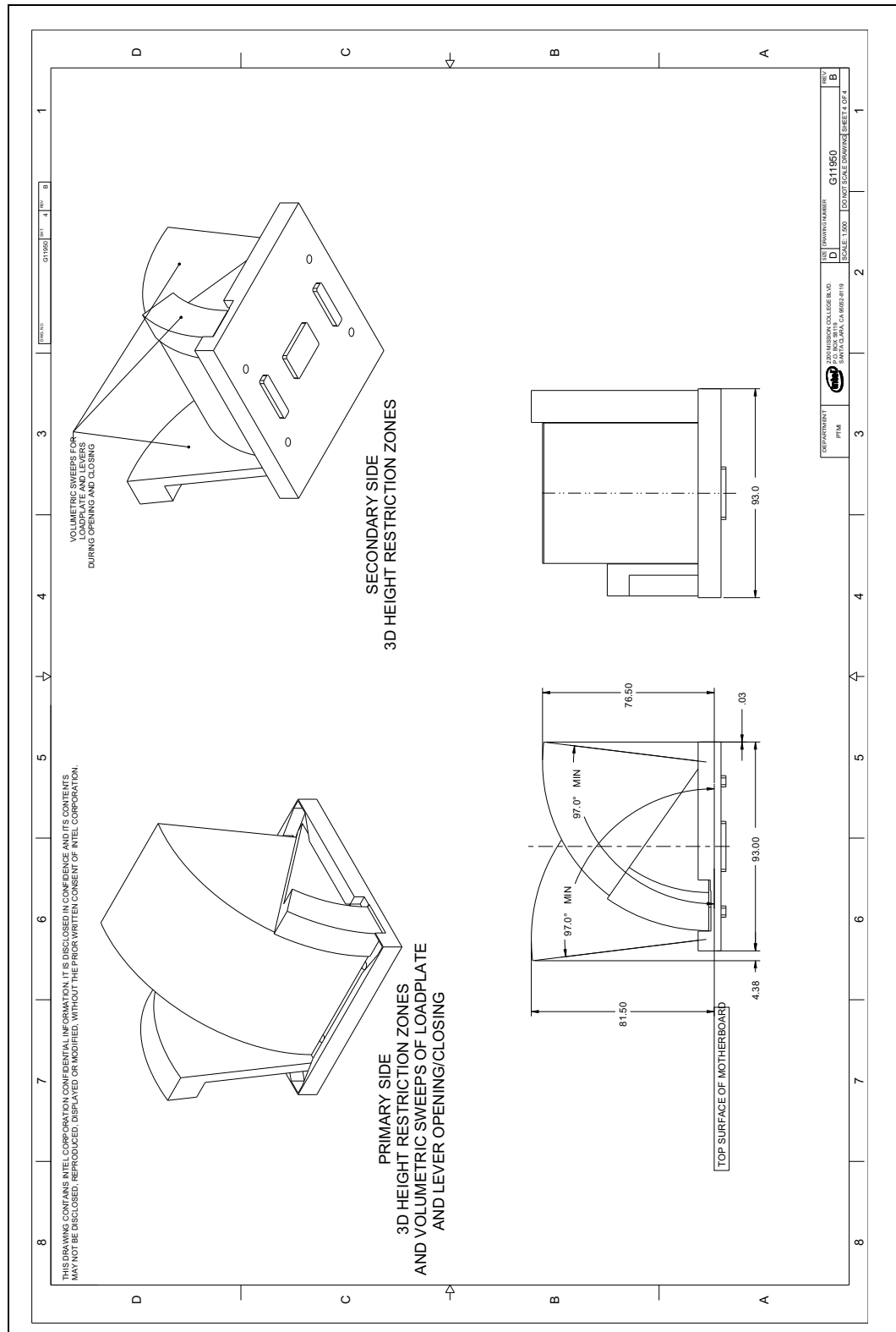


Figure A-5. Narrow ILM Board Keepouts 1 of 4

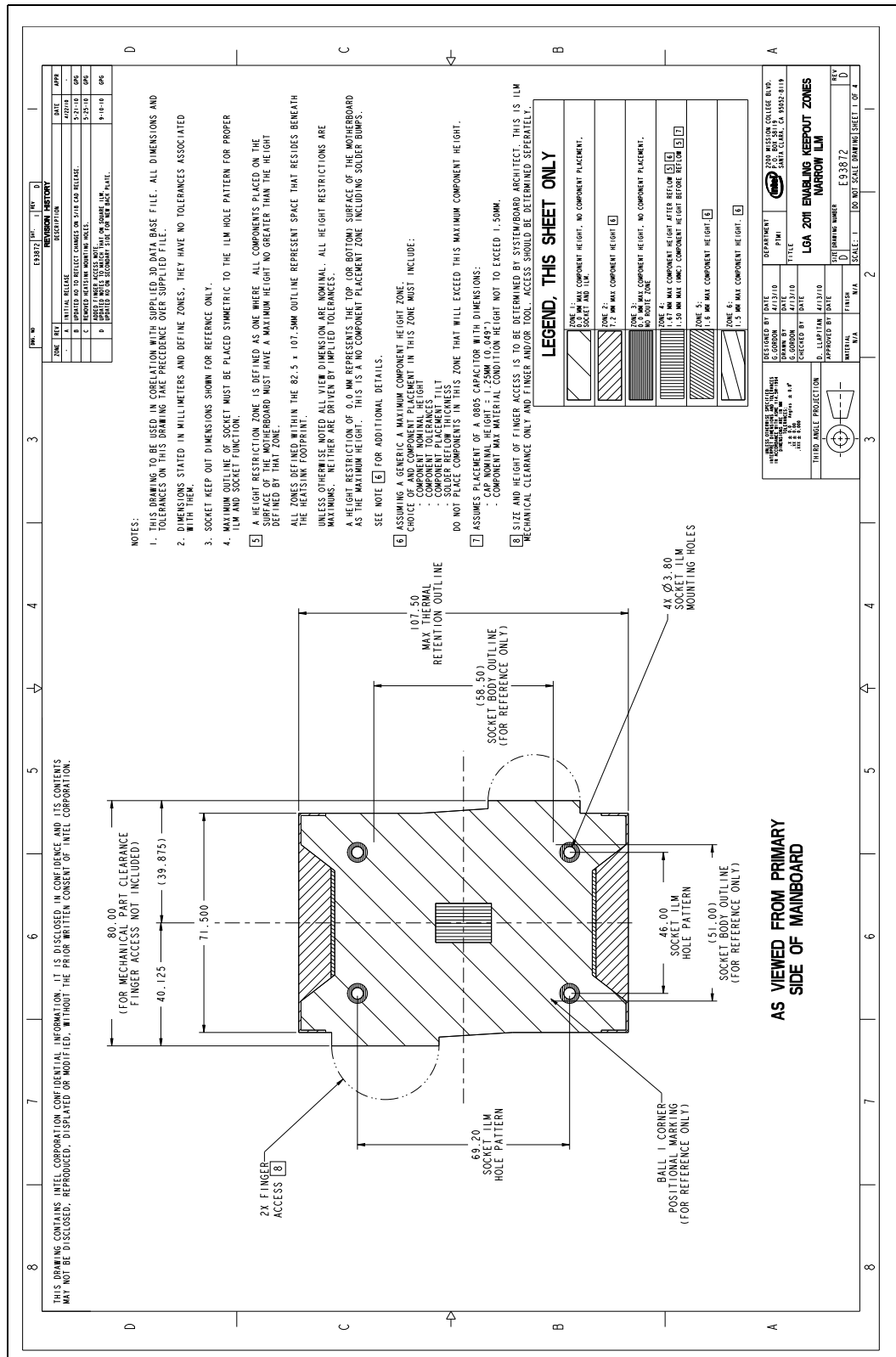






Figure A-6. Narrow ILM Board Keepouts 2 of 4

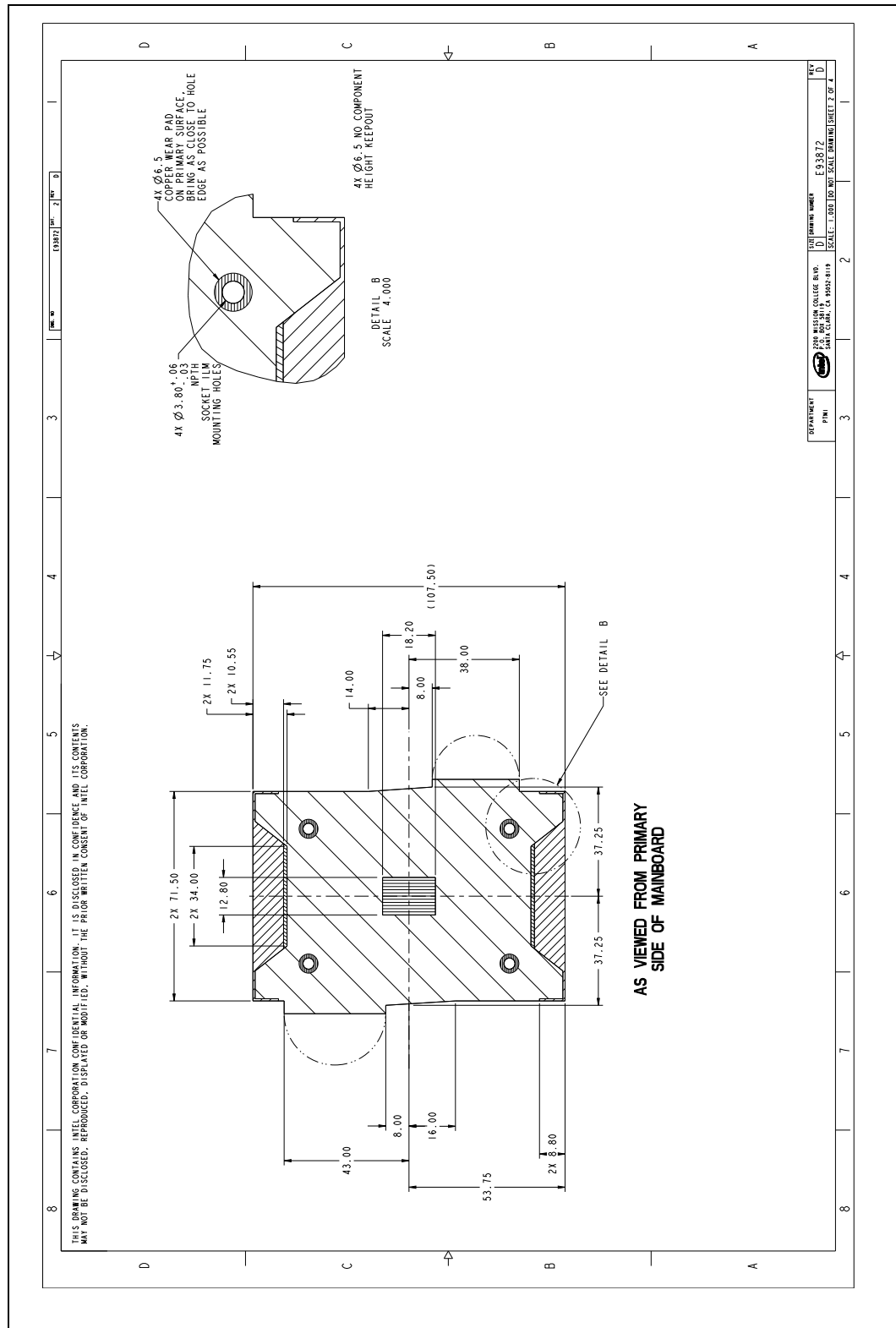


Figure A-7. Narrow ILM Board Keepouts 3 of 4

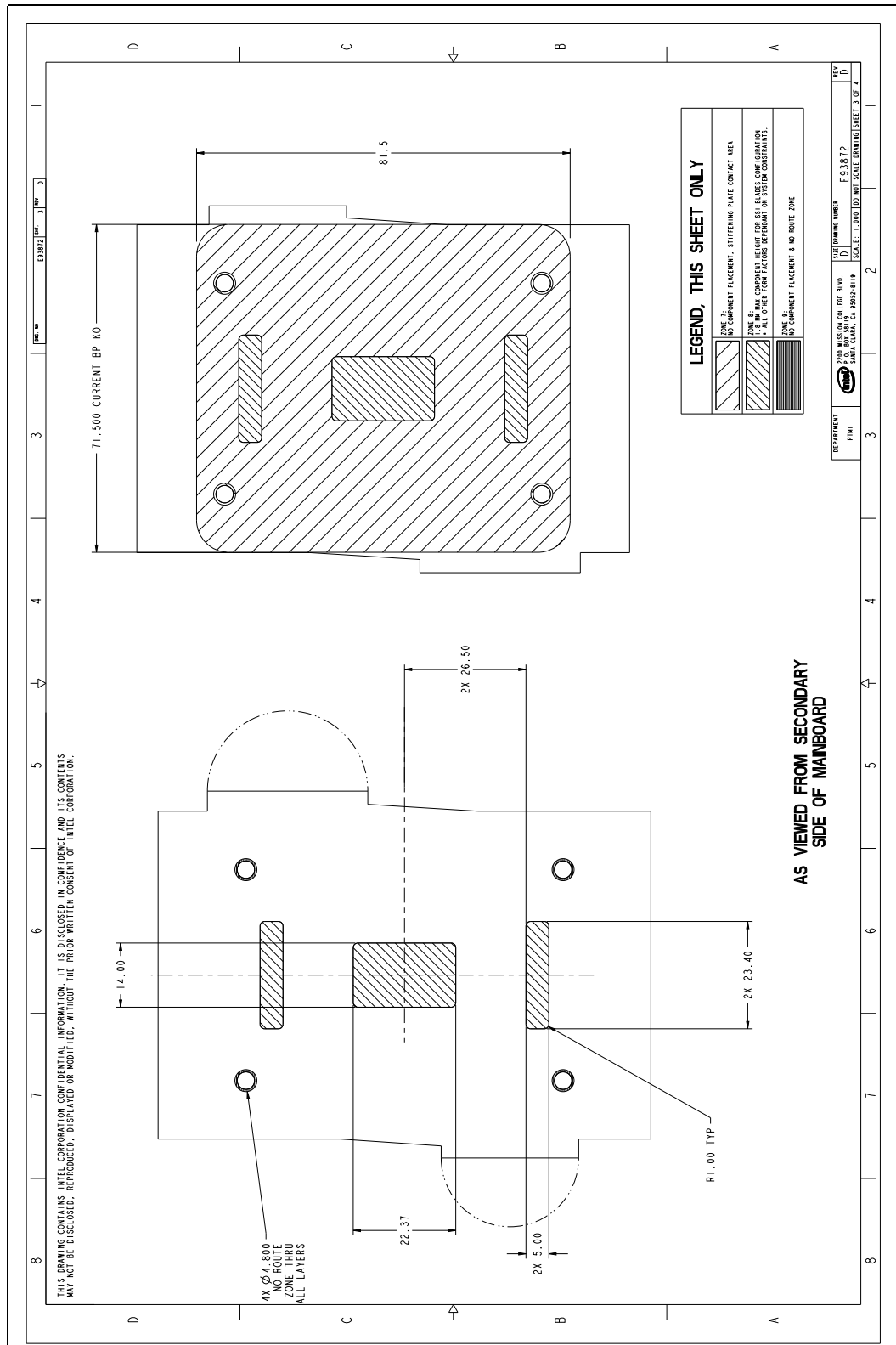


Figure A-8. Narrow ILM Board Keepouts 4 of 4

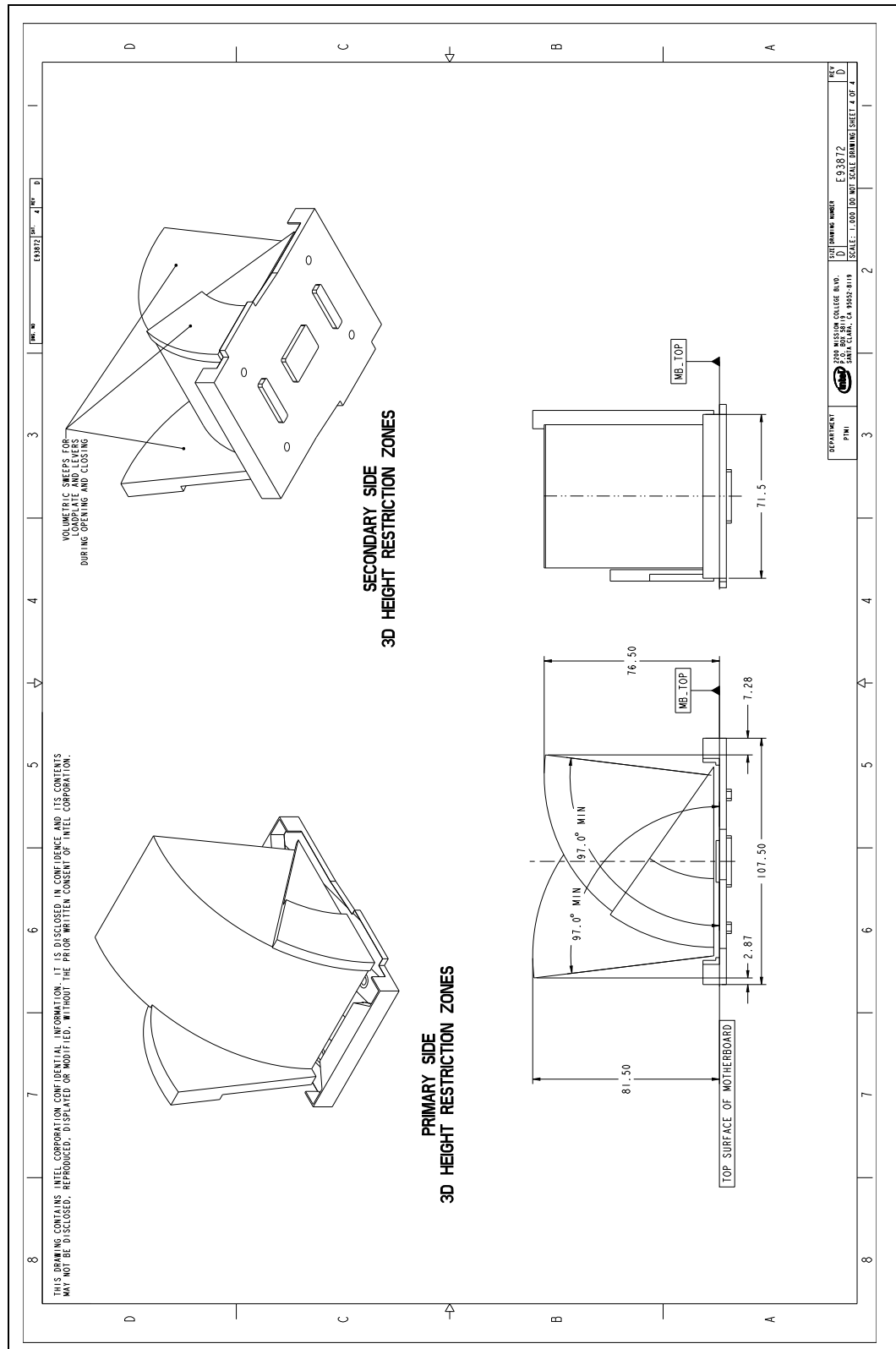






Figure A-11. 2U Square Heatsink Volumetric 1 of 2

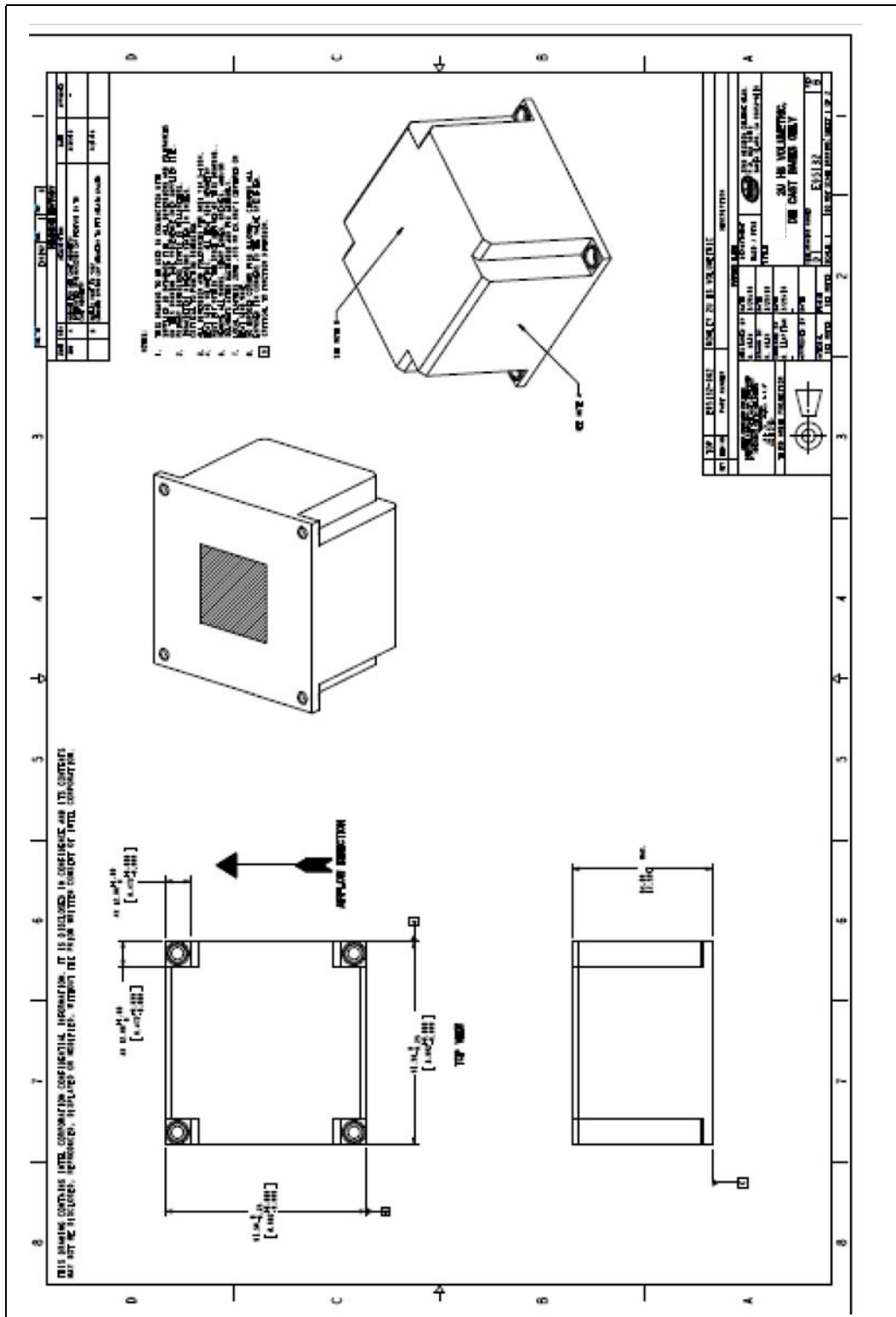




Figure A-12. 2U Square Heatsink Volumetric 2 of 2

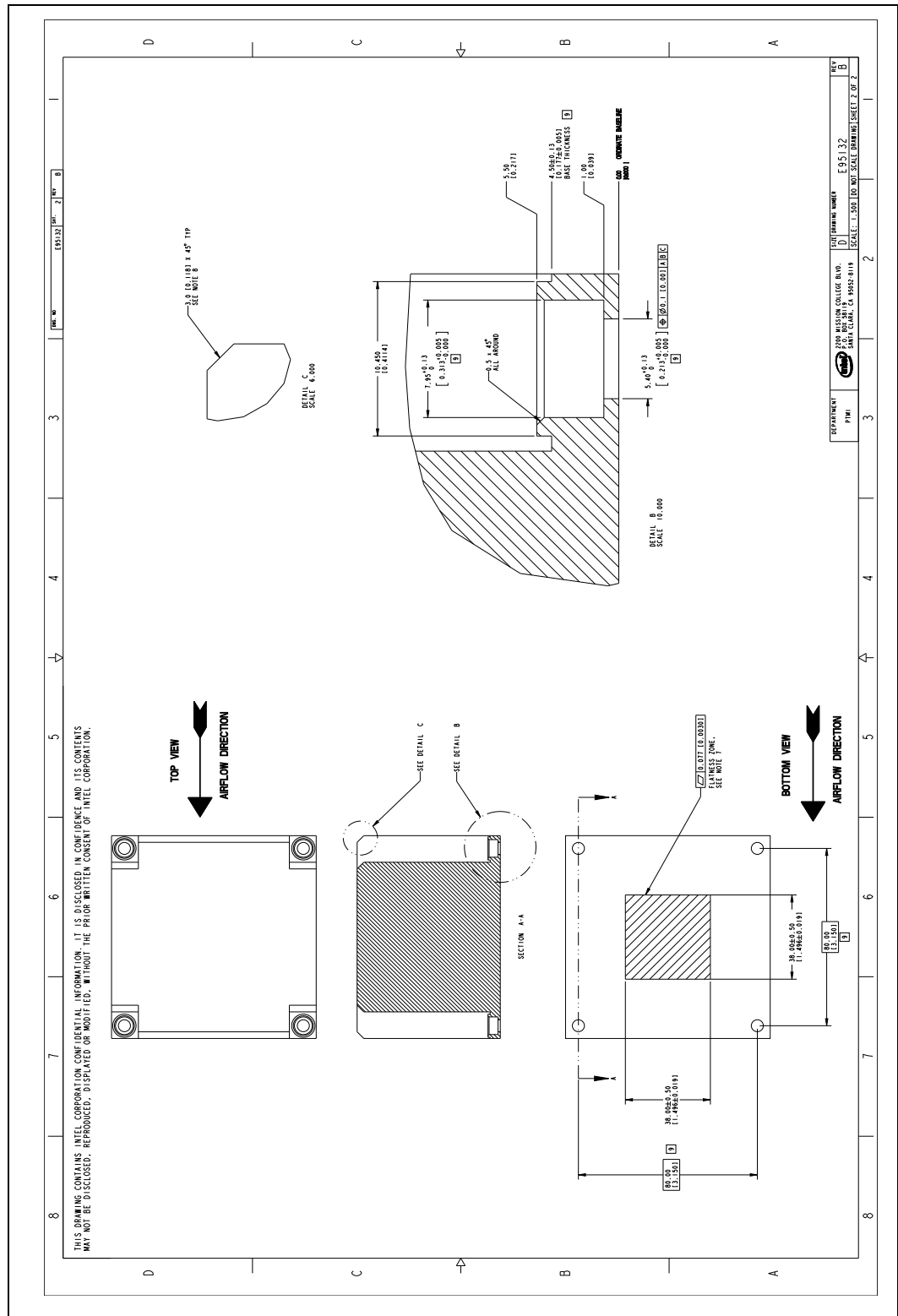
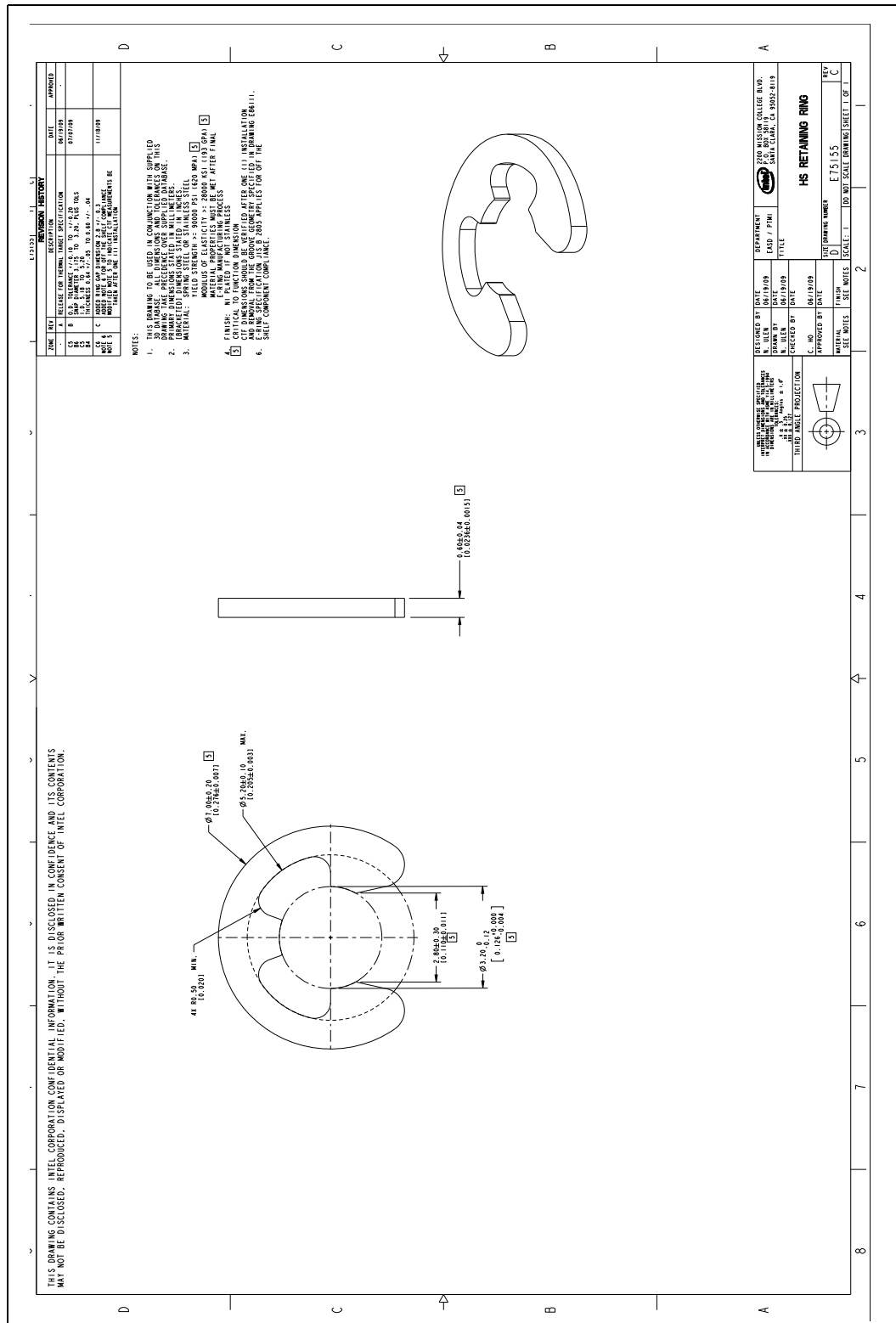








Figure A-15. Heatsink Retaining Ring



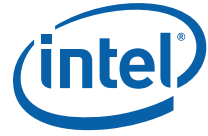


Figure A-16. Heatsink Delrin Spacer

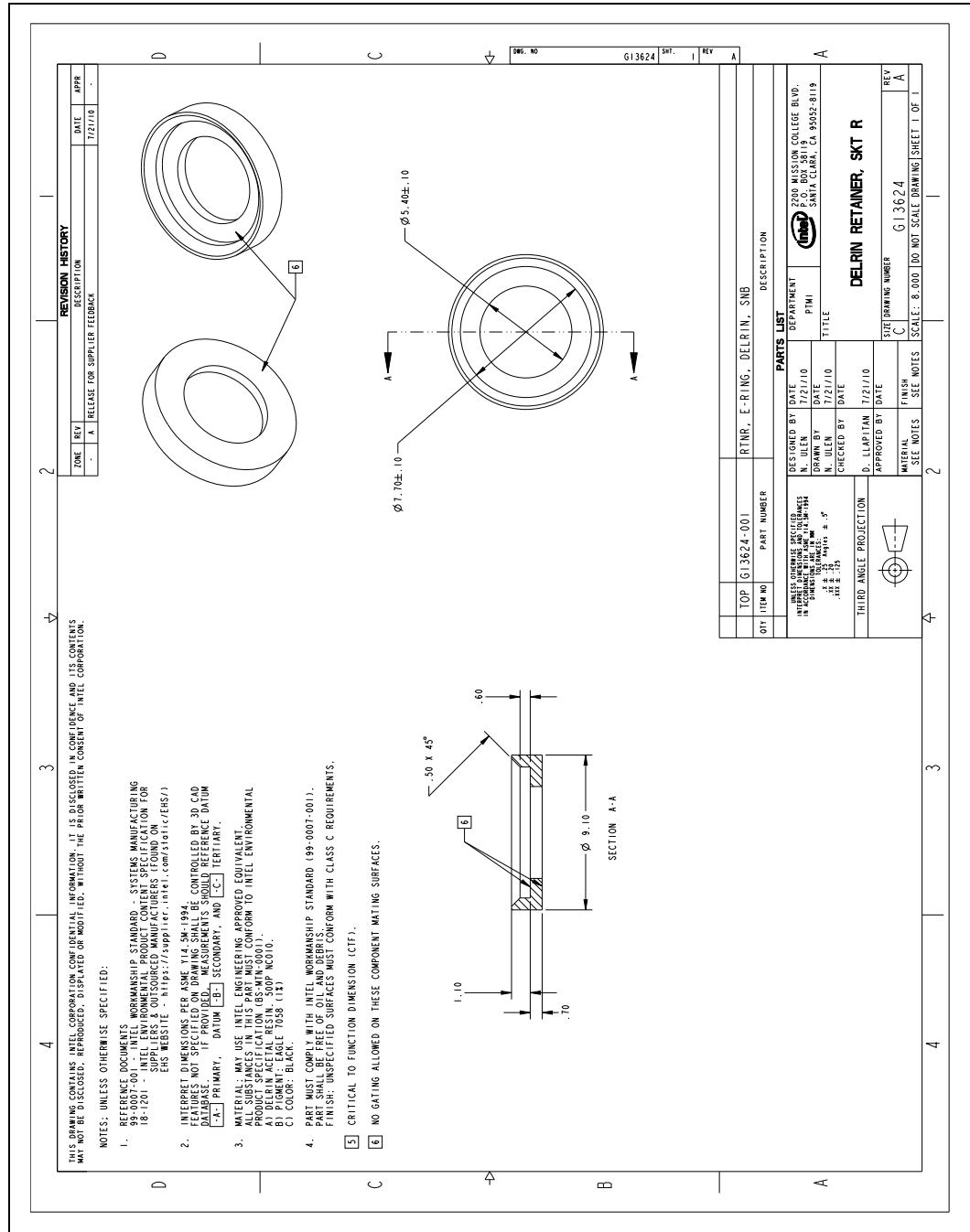


Figure A-17. 1U Square Heatsink Assembly 1 of 2

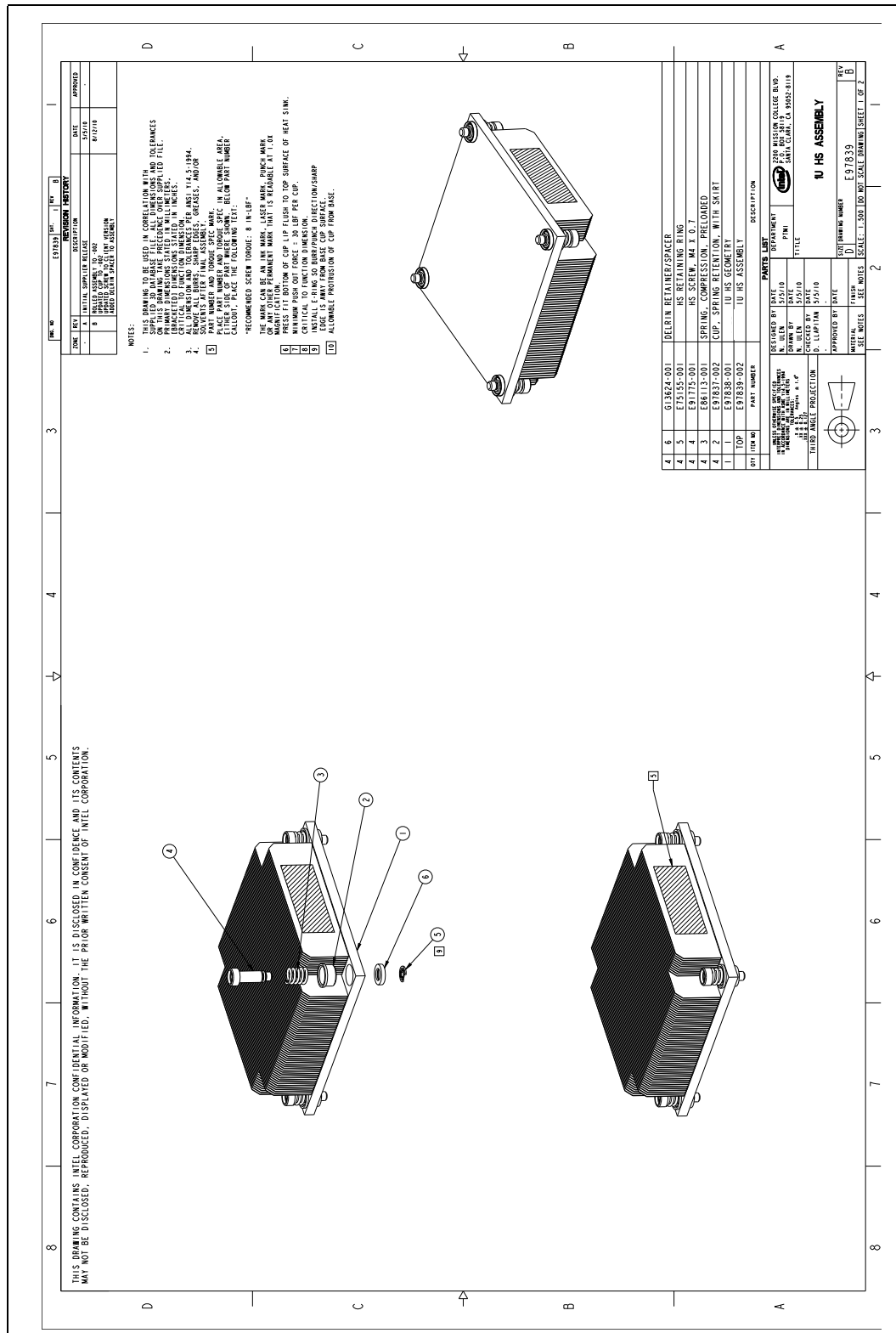








Figure A-20. 1U Square Heatsink Geometry 2 of 2

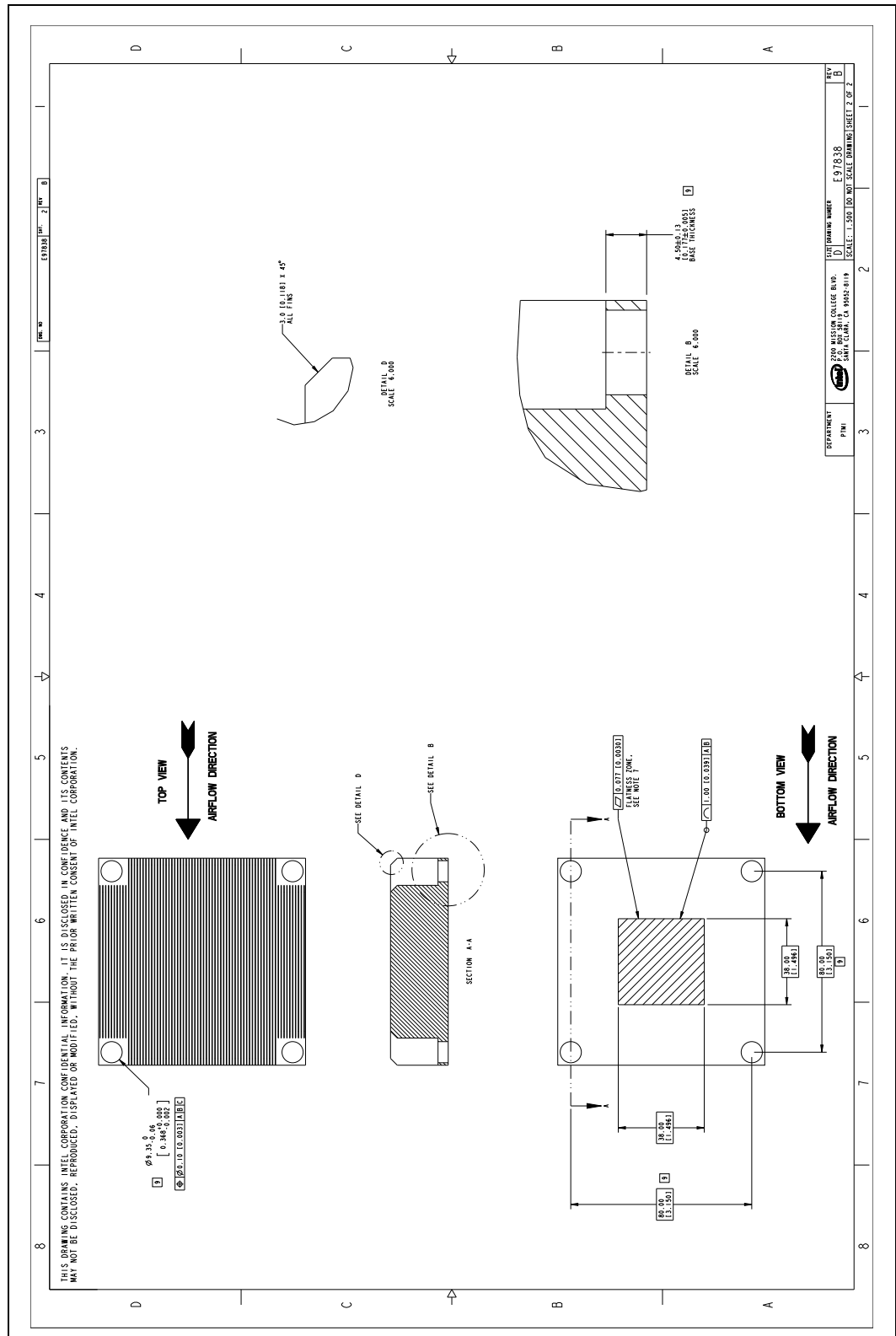


Figure A-21. Heatsink Cup For Spring Retention

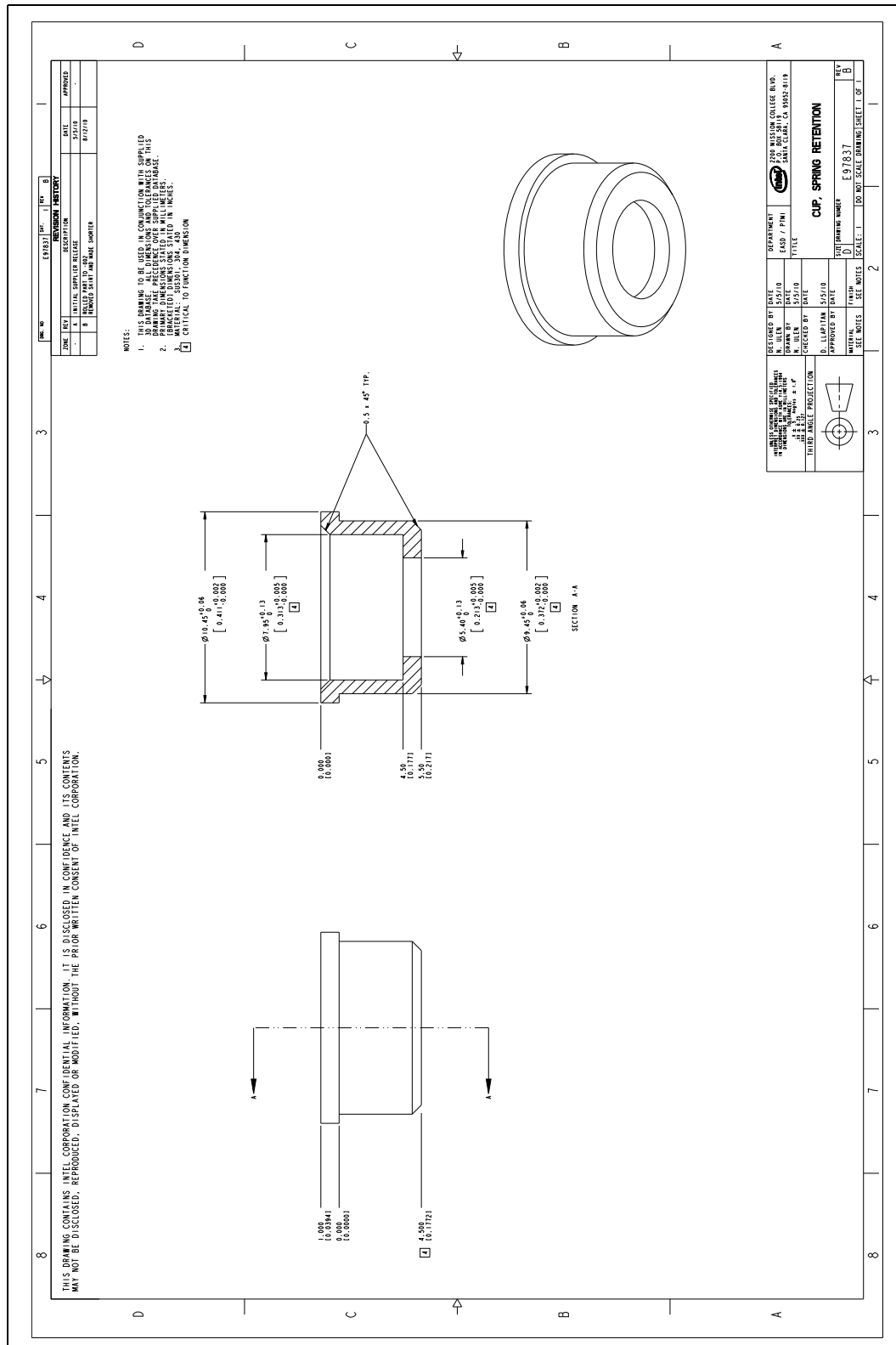




Figure A-22. 1U Narrow Heatsink Assembly 1 of 2

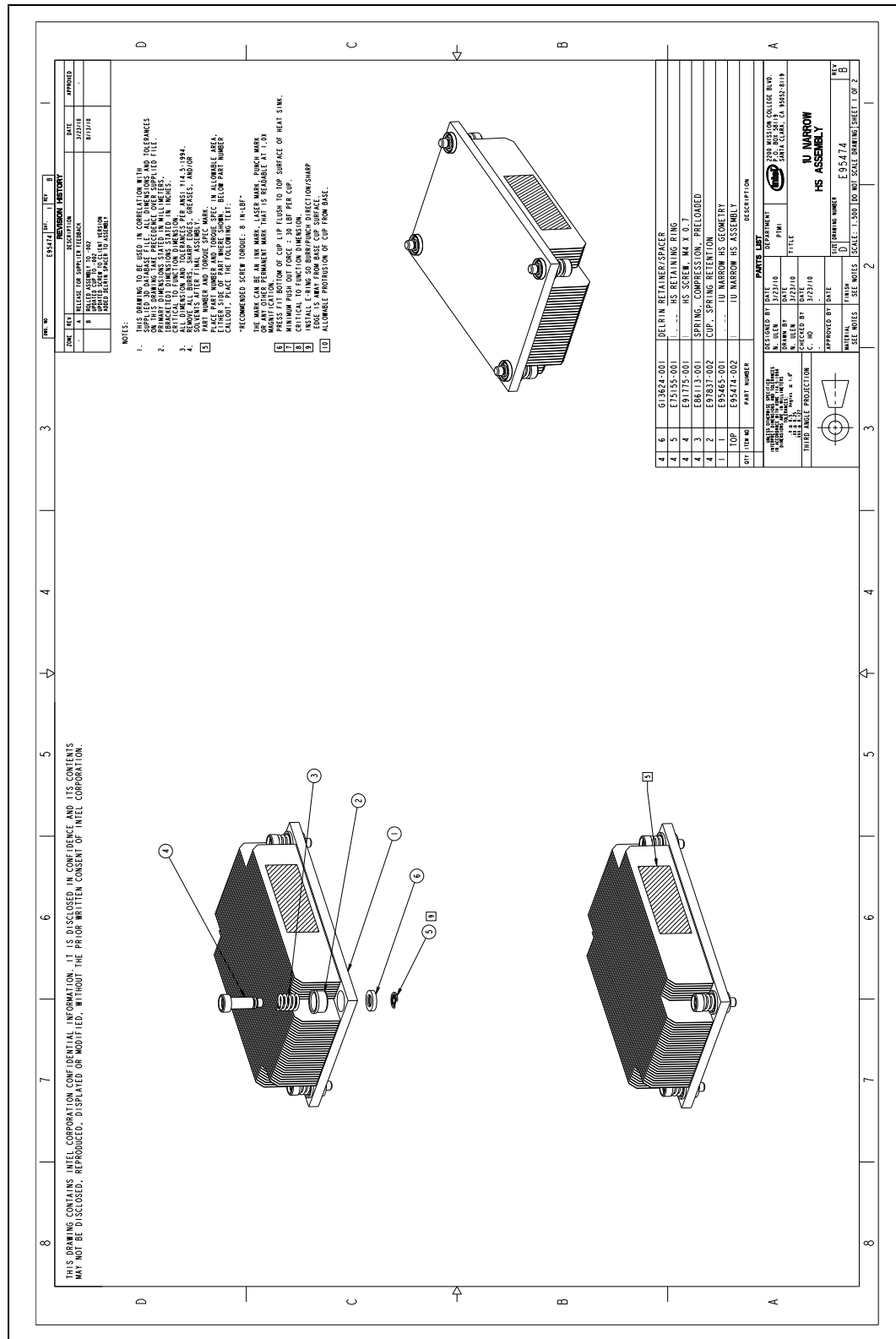


Figure A-23. 1U Narrow Heatsink Assembly 2 of 2

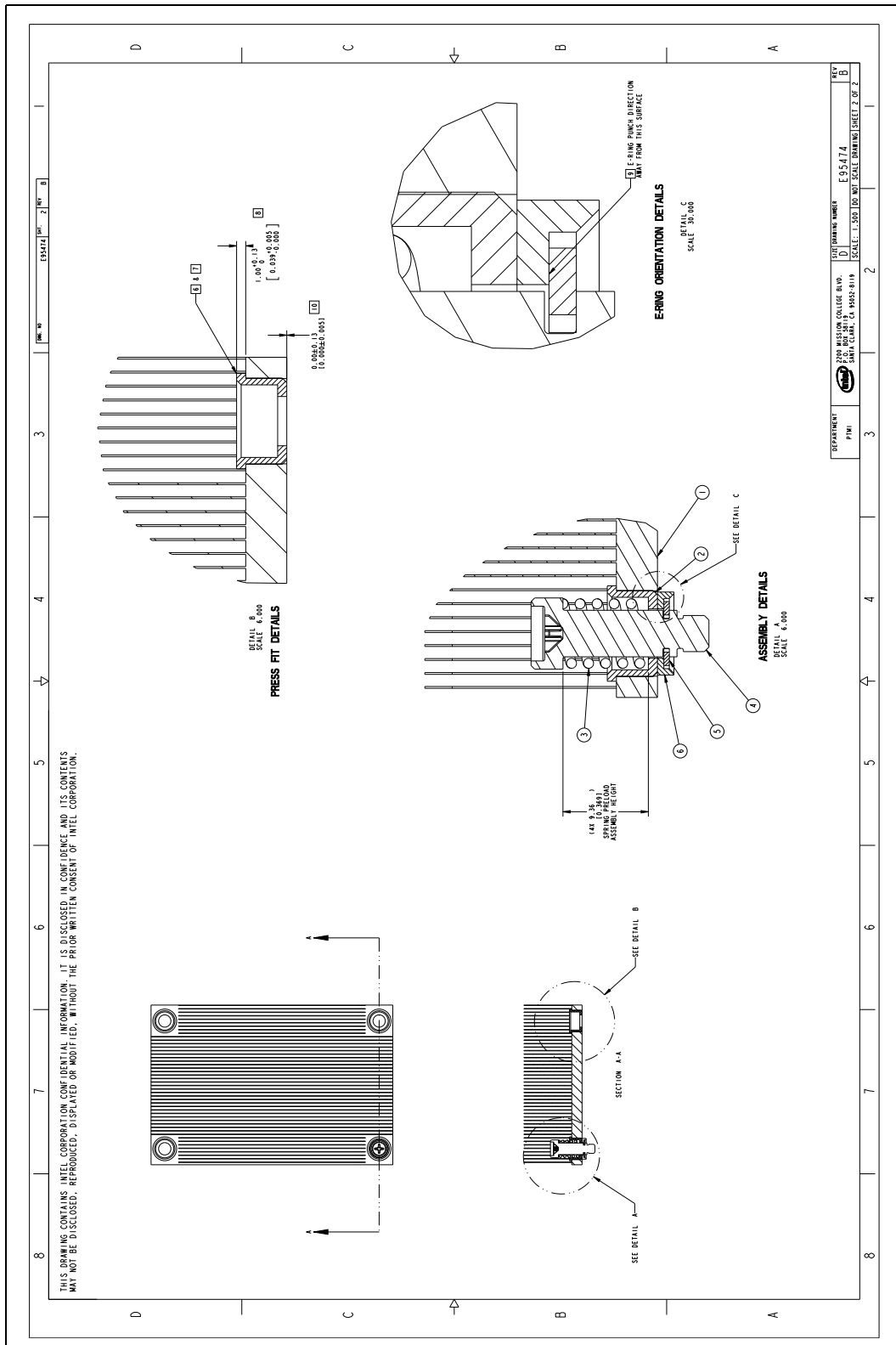




Figure A-24. 1U Narrow Heatsink Geometry 1 of 2

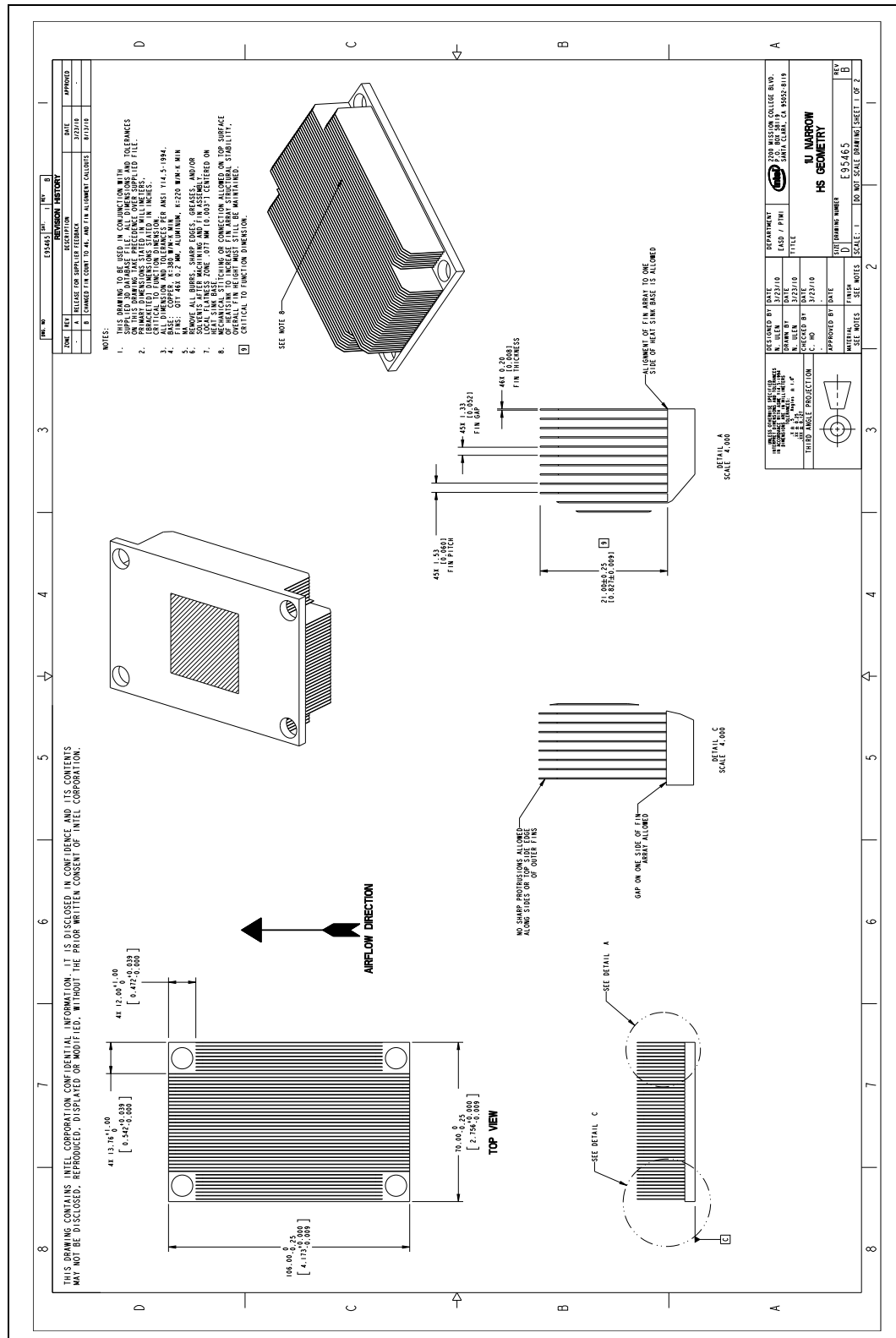
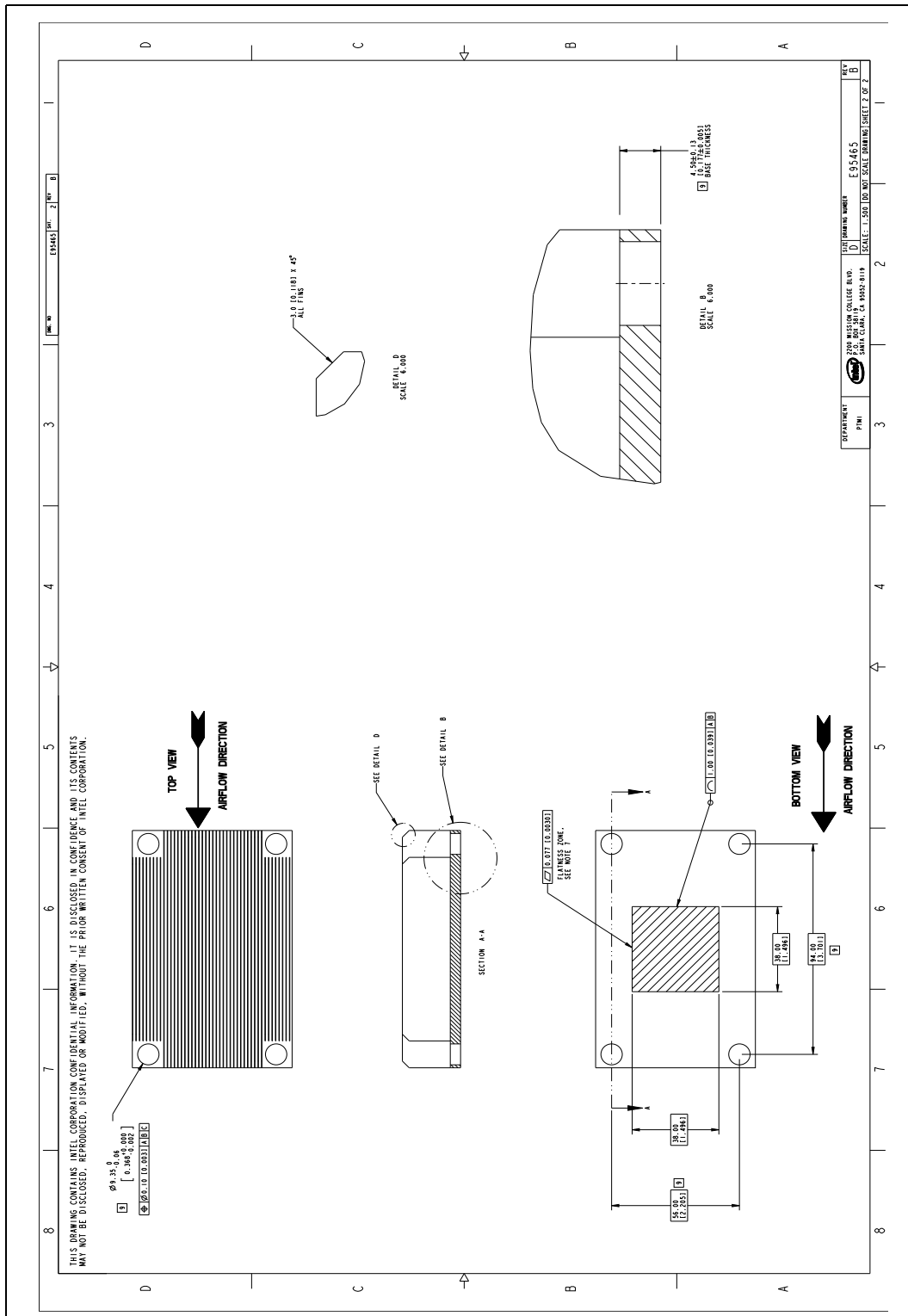


Figure A-25. 1U Narrow Heatsink Geometry 2 of 2



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# B Socket Mechanical Drawings

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Table B-1 lists the socket drawings included in this appendix.

**Table B-1. Socket Drawing List**

Drawing Description	Figure Number
Socket Mechanical Drawing (Sheet 1 of 4)	Figure B-1
Socket Mechanical Drawing (Sheet 2 of 4)	Figure B-2
Socket Mechanical Drawing (Sheet 3 of 4)	Figure B-3
Socket Mechanical Drawing (Sheet 4 of 4)	Figure B-4

Figure B-1. Socket Mechanical Drawing (Sheet 1 of 4)

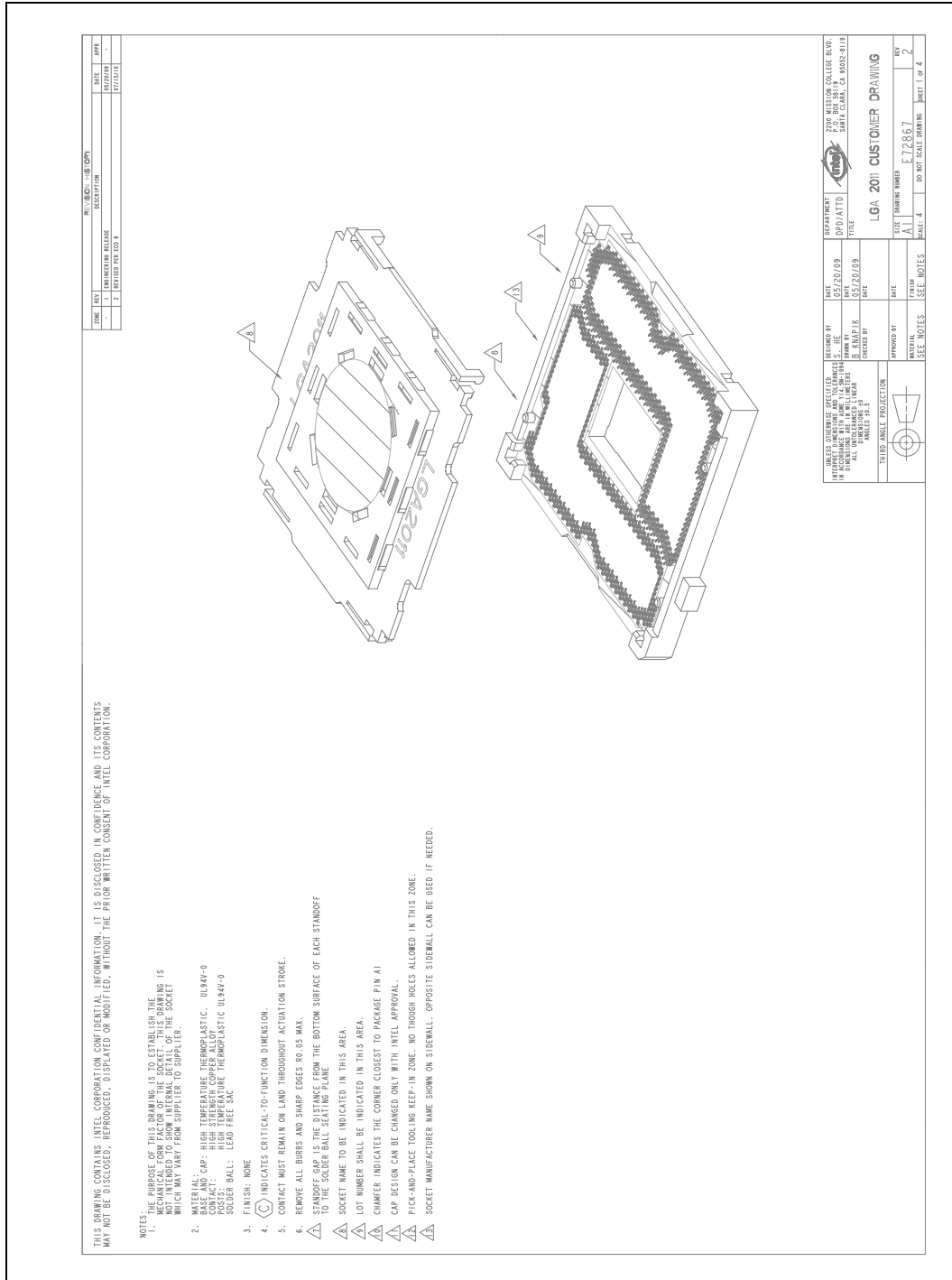


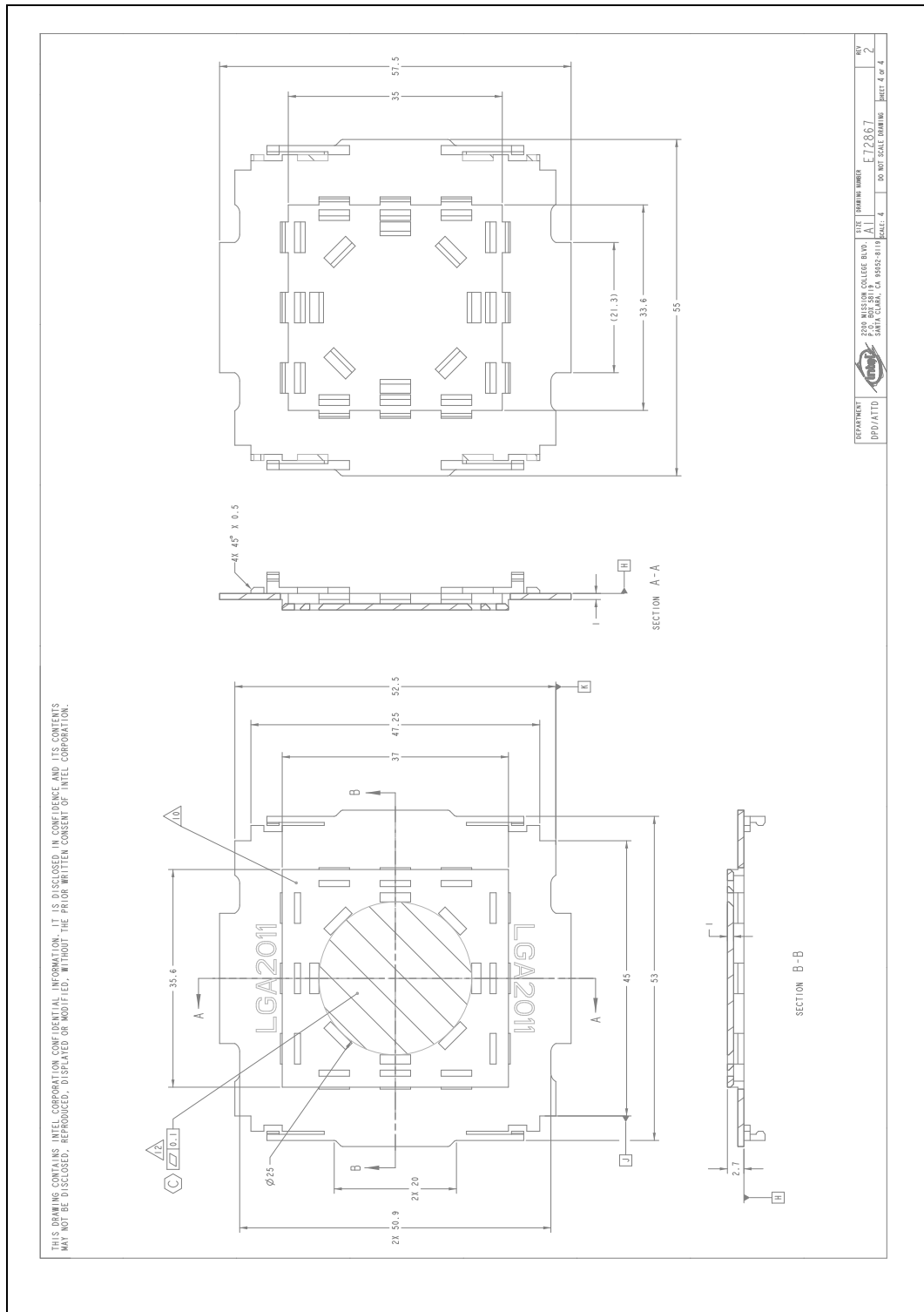








Figure B-4. Socket Mechanical Drawing (Sheet 4 of 4)



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# C Component Suppliers

## C.1 Intel Enabled Supplier Information

Performance targets for heatsinks are described in [Section 5.1](#). Mechanical drawings are provided in [Appendix A](#). Mechanical models of the keep in zone and socket are listed in [Table 1-1](#).

### C.1.1 Intel Reference or Collaboration Thermal Solutions

Customers can purchase the Intel reference or collaboration thermal solutions from the suppliers listed in [Table C-1](#) and [Table C-2](#).

**Table C-1. Suppliers for the Intel Reference Thermal Solutions (Sheet 1 of 2)**

Item	Intel Part Number	Supplier PN	Supplier	Supplier Contact Info
1U Square Heatsink Assy with TIM (91.5x91.5x25.5)	E89208-002	1A22KDL00_XP01	Foxconn	Ray Wang (worldwide) ray.wang@foxconn.com +1-512-351-1493 x273
1U Narrow Heatsink Assy with TIM (70x106x25.5)	G16544-001	1A22JRB00_XP01	Foxconn	Ray Wang (worldwide) ray.wang@foxconn.com +1-512-351-1493 x273
2U Active/Combo Heatsink Assy w/TIM, Fan Guard	E62452-004	1A014QD00-NRC_XA14	Foxconn	Ray Wang (worldwide) ray.wang@foxconn.com +1-512-351-1493 x273
Delrin eRing retainer	G13624-001	FT1008-A	ITW Electronics Business Asia Co., Ltd.	Chak Chakir Chak.Chakir@itweba.com 512-989-7771
Thermal Interface Material (TIM)	N/A	PCM45F	Honeywell	Judy Oles Judy.Oles@Honeywell.com +1-509-252-8605
	N/A	TC-5022	Dow Corning	Ed Benson e.benson@dowcorning.com +1-617-803-6174
2U Square Heatpipe Heatsink 150W, 135W, 130W 1S WS, 130W, 115W, 95W, 80W, 70W, 60W	N/A	SR41H00001	Asia Vital Components (AVC)*	www.avc.com.tw
2U Narrow Heatpipe Heatsink 150W, 135W, 130W, 115W, 95W, 80W, 70W, 60W	N/A	HEL00007-N1-GP	Coolermaster*	www.coolermaster.com  (Not recommended for shadowed processor configurations)
1U Square Heatpipe Heatsink 130W, 115W, 95W, 80W, 70W, 60W	N/A	SQ42Q00001	Asia Vital Components (AVC)*	www.avc.com.tw



**Table C-1. Suppliers for the Intel Reference Thermal Solutions (Sheet 2 of 2)**

Item	Intel Part Number	Supplier PN	Supplier	Supplier Contact Info
1U Square Vapor-Chamber Heatsink 150W, 130W, 115W, 95W, 80W, 70W, 60W	N/A	R2	Dynatron Corporation* (Top Motor/Dynaenon)	www.dynatron-corp.com  (Exceeds SSI blade height standard)
1U Narrow Heatpipe Heatsink 130W, 115W, 95W, 80W, 70W, 60W	N/A	SQ42T00001	Asia Vital Components (AVC)*	www.avc.com.tw  (Not recommended for shadowed processor configurations)
1U Narrow Vapor-Chamber Heatsink 130W, 115W, 95W, 80W, 70W, 60W	N/A	98-12038-M43	Taiwan Microloops*	www.microloops.com

### C.1.2 Socket and ILM Components

The LGA2011-0 Socket and ILM Components are described in [Chapter 2](#) and [Chapter 3](#), respectively. Socket mechanical drawings are provided in [Appendix A](#). Mechanical models are listed in [Table 1-1](#).

**Table C-2. Suppliers for the LGA2011-0 Socket and ILM**

Item	Intel PN	Amtek	Foxconn (Hon Hai)	Lotes
LGA2011-0 Socket	E64556-002	None	PE201127-4351-01H	TBD
LGA2011-0 ILM Square	E91838-003	ITLE91838003	PT44L41-4411	ACA-ZIF-129-Y02
LGA2011-0 ILM Narrow	E93875-002	ITLE93875002	PT44L43-4411	ACA-ZIF-130-Y02
LGA2011-0 Backplate	E91834-001	ITLE91834001	PT44P41-4401	DCA-HSK-182-T02
Supplier Contact Info		SJ Yeoh sjyeoh@amtek.com.cn  (86) 752 263 4562	(Socket) Katie Wang katie.wang@foxconn.com Tel: +1-714-608-2085 Fax: +1-714-680-2099 (ILM) Julia Jiang juliaj@foxconn.com +1-408-919-6178	Cathy Yang Cathy@lotes.com.cn Tel: +1-86-20-84686519



**Table C-3. Suppliers for the LGA-2011-0 Socket and ILM (Continued)**

Item	Intel PN	Molex	Tyco
LGA2011-0 Socket	E64556-002	1051420132	2069458-1
LGA2011-0 ILM Square	E91838-003	1051428100	2134439-2
LGA2011-0 ILM Narrow	E93875-002	1051429100	2134439-1
LGA2011-0 Backplate	E91834-001	1051427000	2134440-1
Supplier Contact Info		Carol Liang carol.liang@molex.com	Josh Moody jdmoody@te.com Tel: +1-503-327-8348; +1-503-327-8346  (Asia) Billy Hsieh billy.hsieh@te.com

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## D Thermal Test Vehicle

For thermal analysis of Intel® Xeon® Processor E5-1600 / E5-2600 / E5-4600 v1 and v2 Product Families, the Thermal Test Vehicle (TTV) can be used with appropriate correction factors, as shown in [Table D-1](#).

Actual processors experience non-uniform heating that is not simulated by the uniform heating of the Thermal Test Vehicle (TTV). As a result, to find the actual thermal characterization parameter ([Section 5.3.2](#)), correction offsets must be added to the thermal characterization parameter found for each TTV.

### Equation D-1. $\Psi_{CA}$ , Intel Xeon processor = mean $\Psi_{CA}$ , TTV + $3\sigma$ + Correction Offset

Mean  $\Psi_{CA}$ , TTV +  $3\sigma$  accounts for variation (standard deviation) in heatsink and thermal interface material performance and is determined by the customer.

There are two versions of TTV, depending on Intel® Xeon® Processor E5-1600/E5-2600/E5-4600 v1 or v2 Product Family processor. Refer to the appropriate processor datasheet to determine the package size. The correction factors for the processors along with applicable TTV are listed below.

**Table D-1. Correction Offsets Intel® Xeon® Processor E5-1600 / E5-2600 / E5-4600 v1 Product Families**

Processor	TDP (Watts)	Correction Offset for TTV (°C/W)
8-core/6-core	150	-0.027
8-core	135	-0.024
8-core/6-core	130	-0.023
8-core/6-core	115	-0.026
8-core/6-core	95	-0.026
8-core/6-core	70	-0.031
8-core/6-core	60	-0.030
4-core	130	-0.006
4-core	95	-0.008
4-core	80	-0.009
2-core	80	0.005

**Table D-2. Correction Offsets Intel® Xeon® Processor E5-1600/ E5-2600/ E5-4600 v2 Product Families (Sheet 1 of 2)**

Processor	TDP (Watts)	Correction Offset for TTV (°C/W)	Applicable TTV <sup>1</sup>
EP 12-core 130W (1U)	130	0.007	---
EP/EP 4S 12-core 115W (1U)	115	0.006	---
EP WS 8-core 150W	150	0.005	---
EP/EP 4S 10-core 130W (1U)	130	-0.001	---



**Table D-2. Correction Offsets Intel® Xeon® Processor E5-1600/ E5-2600/ E5-4600 v2 Product Families (Sheet 2 of 2)**

Processor	TDP (Watts)	Correction Offset for TTV (°C/W)	Applicable TTV <sup>1</sup>
EP 4S 8-core 130W (1U)	130	0.003	---
EP 8-core 130W (2U)	130	0.004	---
EP 6-core 130W (2U)	130	0.003	---
EP 10-core 115W (1U)	115	-0.002	---
EP/EP 4S 10-core 95W (1U)	95	-0.002	---
EP/EP 4S 8-core 95W (1U)	95	0.003	---
EP 10-core 70W (1U)	70	-0.004	---
EP 1S WS 6-core 130W	130	0.018	---
EP 1S WS 4-core 130W	130	0.020	---
EP 4-core 130W (2U)	130	0.017	---
EP 4S 6-core 95W (1U)	95	0.018	---
EP 4S 4-core 95W (1U)	95	0.020	---
EP 6-core 80W (1U)	80	0.016	---
EP 4-core 80W	80	0.019	---
EP 6-core 60W	60	0.014	---

**Notes:**

1. Refer to appropriate Processor Datasheet for package size.

## D.1 LGA2011-0 TTV

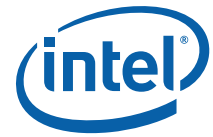
As with past programs, a TTV has been developed to allow thermal solution development. The LGA2011-0 TTV fits in the LGA2011-0 socket to have the correct mechanical stack up in the testing.

The TTV can be powered using the socket or through pads on the top of the package substrate.

Either method will provide the user a uniform heating of the embedded thermal source.

Contact your Intel Field Representative for a thermal test board and the collateral for that board.



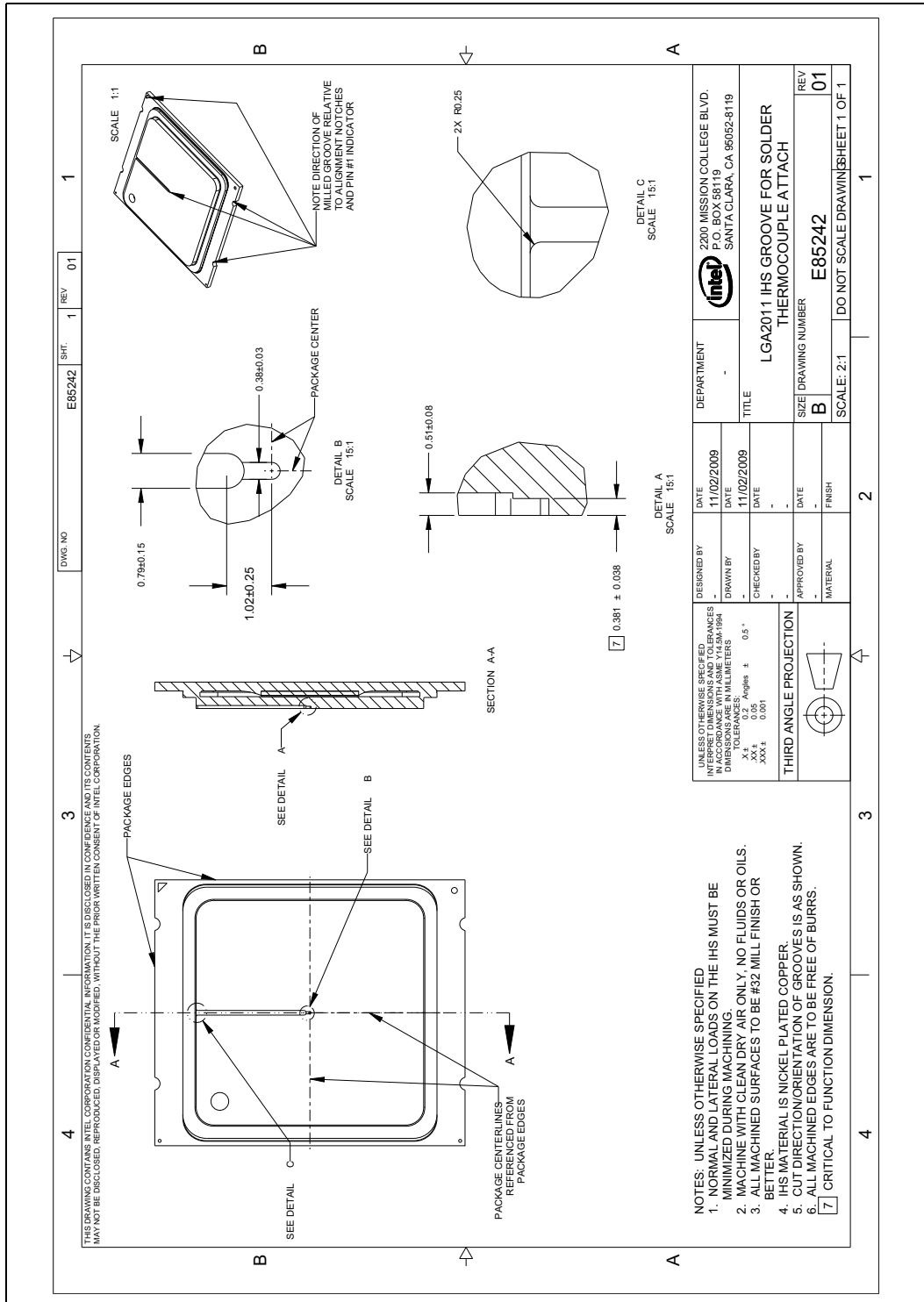


## D.2 Thermocouple Attach Drawing

Figure D-1 shows groove dimensions for thermocouple attach on Intel® Xeon® Processor E5-1600 / E5-2600 / E5-4600 Product Families and Intel® Xeon® Processor E5-1600 V2/ E5-2600 V2/ E5-4600 V2 Product Families TTV. This drawing is also applicable to the larger Lukeville test vehicle as it shares the same IHS with the smaller TTV.

**Note:** The following supplier can machine the groove and attach a thermocouple to the IHS. The supplier information is provided s a convenience to Intel's general customers and the list may be subject to change without notice. THERM-X OF CALIFORNIA, 3200 Investment Blvd., Hayward, Ca 94544. Ernesto B Valencia +1-510-441-7566 Ext. 242 ernestov@therm-x.com. The vendor part number is XTMS1565.

Figure D-1. Groove for Thermocouple Attach on Intel® Xeon® Processor E5-2600 Product Family Thermal Test Vehicle





# E Embedded Thermal Solutions

Embedded Server SKU's target higher case temperatures and/or NEBS thermal profiles for embedded communications server and storage form factors. This section describes reference heatsinks for NEBS (Network Equipment Building Systems) compliant ATCA (Advanced Telecommunications Computing Architecture) systems. These higher case temperature processors are good for any form factor that needs to meet NEBS requirements.

## E.1 Performance Targets

Table E-1 and Table E-2 provide boundary conditions and performance targets for 1U and ATCA heatsinks. These values are used to generate processor thermal specifications and to provide guidance for heatsink design.

**Table E-1. 8-Core/6-Core Processor Reference Thermal Boundary Conditions (E5 v1 Product Family)**

TDP	Heatsink Technology <sup>5, 6</sup>	$\Psi_{ca}^2$ (°C/W)	$T_{LA}^{1, 4}$ (°C)	Heatsink Volumetric <sup>3</sup> (mm)
LV95W (8-core)	1U or Custom	0.265	52/67	90x90x25.5
LV70W (6-core)	ATCA Cu Base/Cu Fins	0.506	52/67	90x90x12.6

**Notes:**

1. Local ambient temperature of the air entering the heatsink.
2. Max target (mean + 3 sigma + offset) for thermal characterization parameter (Section 5.3.2).
3. Dimensions of heatsink do not include socket or processor.
4. Local Ambient Temperature written X/Y° C means X° C under Nominal conditions but Y° C is allowed for Short-Term NEBS excursions.
5. All heatsinks are Non-Direct Chassis Attach (DCA)
6. See Section 5.1 for standard 1U solutions that do not need to meet NEBS.

**Table E-2. Processor Reference Thermal Boundary Conditions (E5 v2 Product Family)**

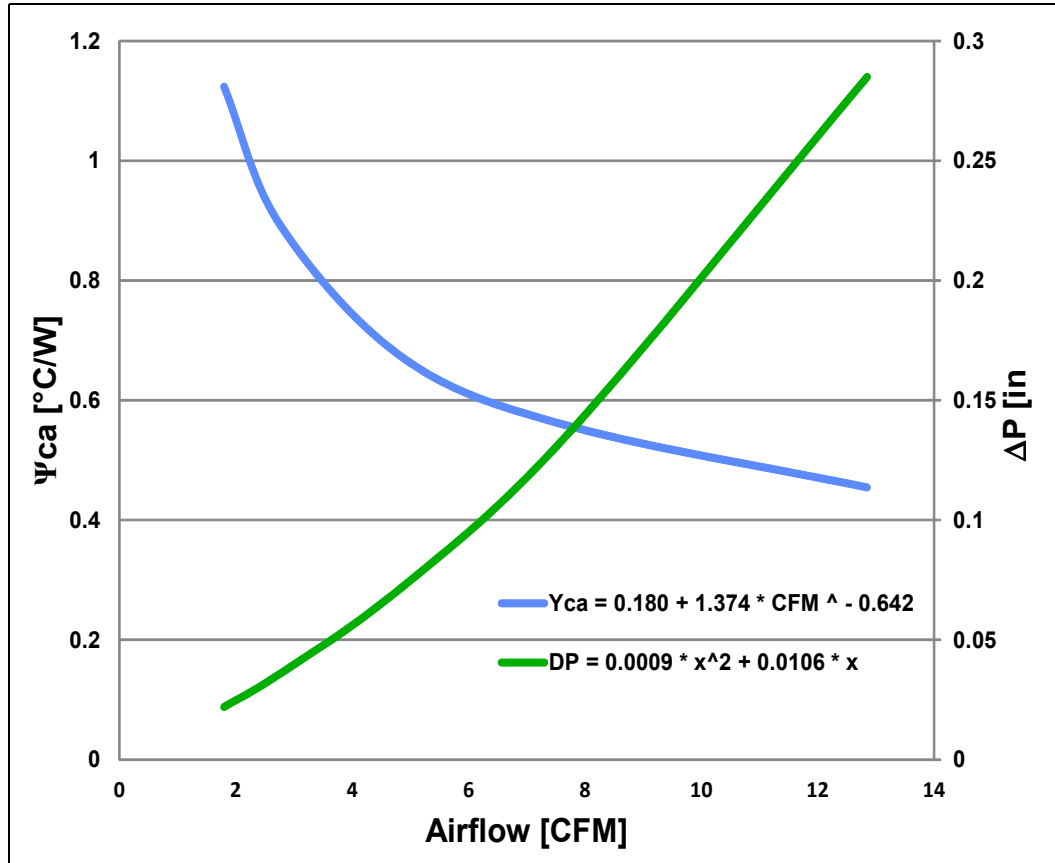
TDP	Heatsink Technology <sup>5, 6</sup>	$\Psi_{ca}^2$ (°C/W)	$T_{LA}^{1, 4}$ (°C)	Heatsink Volumetric <sup>3</sup> (mm)
10-core 95W	1U or Custom	0.235	51/66	90x90x25.5
10-core 70W	ATCA Cu Base/Cu Fins	0.400	49/64	90x90x12.6
8-core 70W	ATCA Cu Base/Cu Fins	0.403	49/64	90x90x12.6
6-core 50W	ATCA Cu Base/Cu Fins	0.541	52/67	90x90x12.6

**Notes:**

1. Local ambient temperature of the air entering the heatsink.
2. Max target (mean + 3 sigma + offset) for thermal characterization parameter (Section 5.3.2).
3. Dimensions of heatsink do not include socket or processor.
4. Local Ambient Temperature written X/Y° C means X° C under Nominal conditions but Y° C is allowed for Short-Term NEBS excursions.
5. All heatsinks are Non-Direct Chassis Attach (DCA)
6. See Section 5.1 for standard 1U solutions that do not need to meet NEBS.

Detailed drawings for the ATCA reference heatsink can be found in [Section E.3](#). [Table E-1](#) above specifies  $\Psi_{CA}$  and pressure drop targets and [Figure E-1](#) below shows  $\Psi_{CA}$  and pressure drop for the ATCA heatsink versus the airflow provided. Best-fit equations are provided to prevent errors associated with reading the graph.

**Figure E-1. ATCA Heatsink Performance Curves**



**Note:** Other LGA1366 compatible thermal solutions may work with the same retention. ATCA heatsink performance curves were created using Socket R TTV.

## E.2 Thermal Design Guidelines

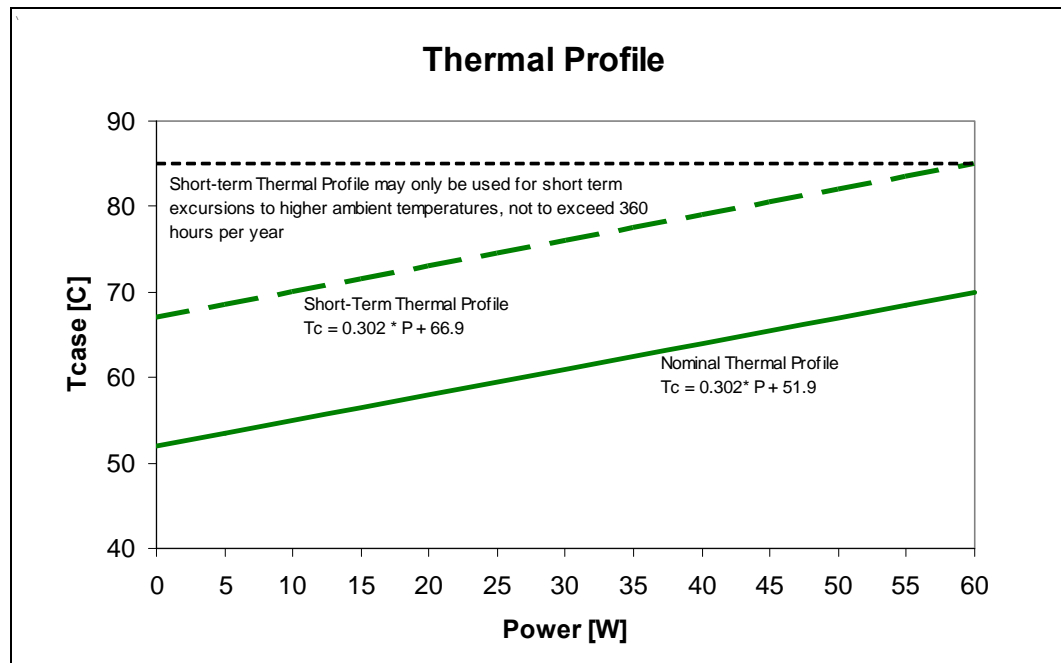
### E.2.1 High Case Temperature Thermal Profile

High case temperature thermal profiles help relieve thermal constraints for Short-Term NEBS conditions. To ensure reliability, processors must meet the nominal thermal profile under standard operating conditions and can only rise up to the Short-Term specification for NEBS excursions (see [Figure E-2](#)). The definition of Short-Term time is defined for NEBS Level 3 conditions but the key is that it cannot be longer than 360 hours per year.

Fan speed control is treated the same as standard processors. When DTS (Digital Temperature Sensor) value is less than  $T_{control}$ , the thermal profile can be ignored.



Figure E-2. High Case Temperature Thermal Profile



**Notes:**

- 1.) The thermal specifications shown in this graph are for reference only. In case of conflict, the data in the datasheet supersedes any data in this figure.
- 2.) The Nominal Thermal Profile must be used for all normal operating conditions, or for products that do not require NEBS Level 3 compliance.
- 3.) The Short-Term Thermal Profile may only be used for short-term excursions to higher ambient operating temperatures, not to exceed 360 hours per year as compliant with NEBS Level 3.
- 4.) Implementation of either thermal profile should result in virtually no TCC activation.
- 5.) Utilization of a thermal solution that exceeds the Short-Term Thermal Profile, or which operates at the Short-Term Thermal Profile for a duration longer than the limits specified in Note 3 above, do not meet the processor thermal specifications and may result in permanent damage to the processor.

### E.3 Mechanical Drawings and Supplier Information

See [Appendix B](#) for assembly, retention, and keep out drawings.

The part number below represent Intel reference designs for an ATCA reference heatsink. Customer implementation of these components may be unique and require validation by the customer. Customers can obtain these components directly from the supplier below.

Table E-3. Embedded Heatsink Component Suppliers

Component	Description	Supplier PN	Supplier Contact Info
ATCA Reference Heat Sink Intel P/N: G47264-001	ATCA Copper Fin, Copper Base	10A01NE500	Foxconn/FTC Technology, Inc. Cary Huang cary.huang@foxconn.com (512) 670-2638 x191



**Table E-4. Mechanical Drawings List**

Parameter	Value
ATCA Reference Heatsink Fin and Base (Sheet 1 of 2)	Figure E-3
ATCA Reference Heatsink Fin and Base (Sheet 2 of 2)	Figure E-4



Figure E-3. ATCA Reference Heatsink Fin and Base (Sheet 1 of 2)

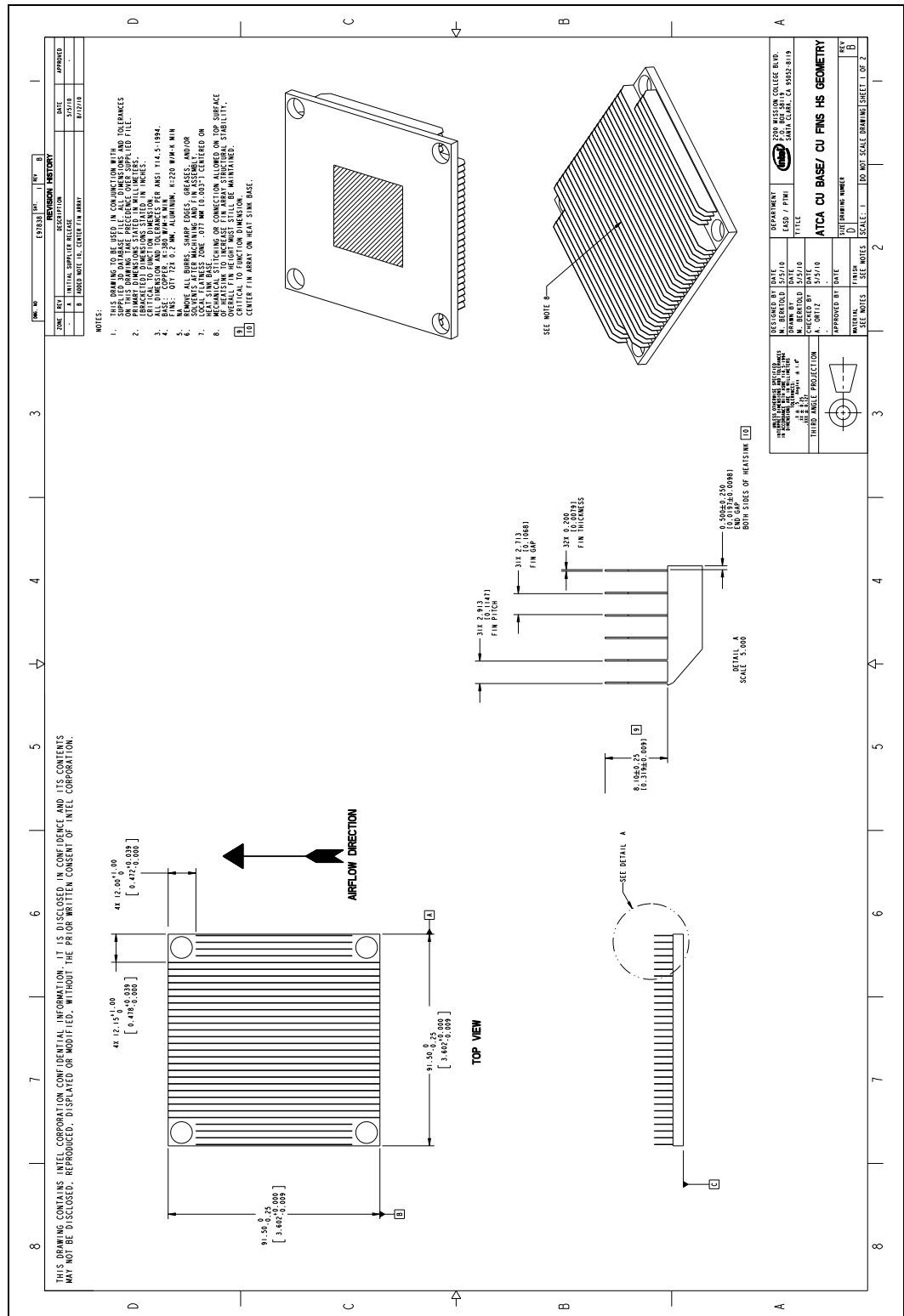
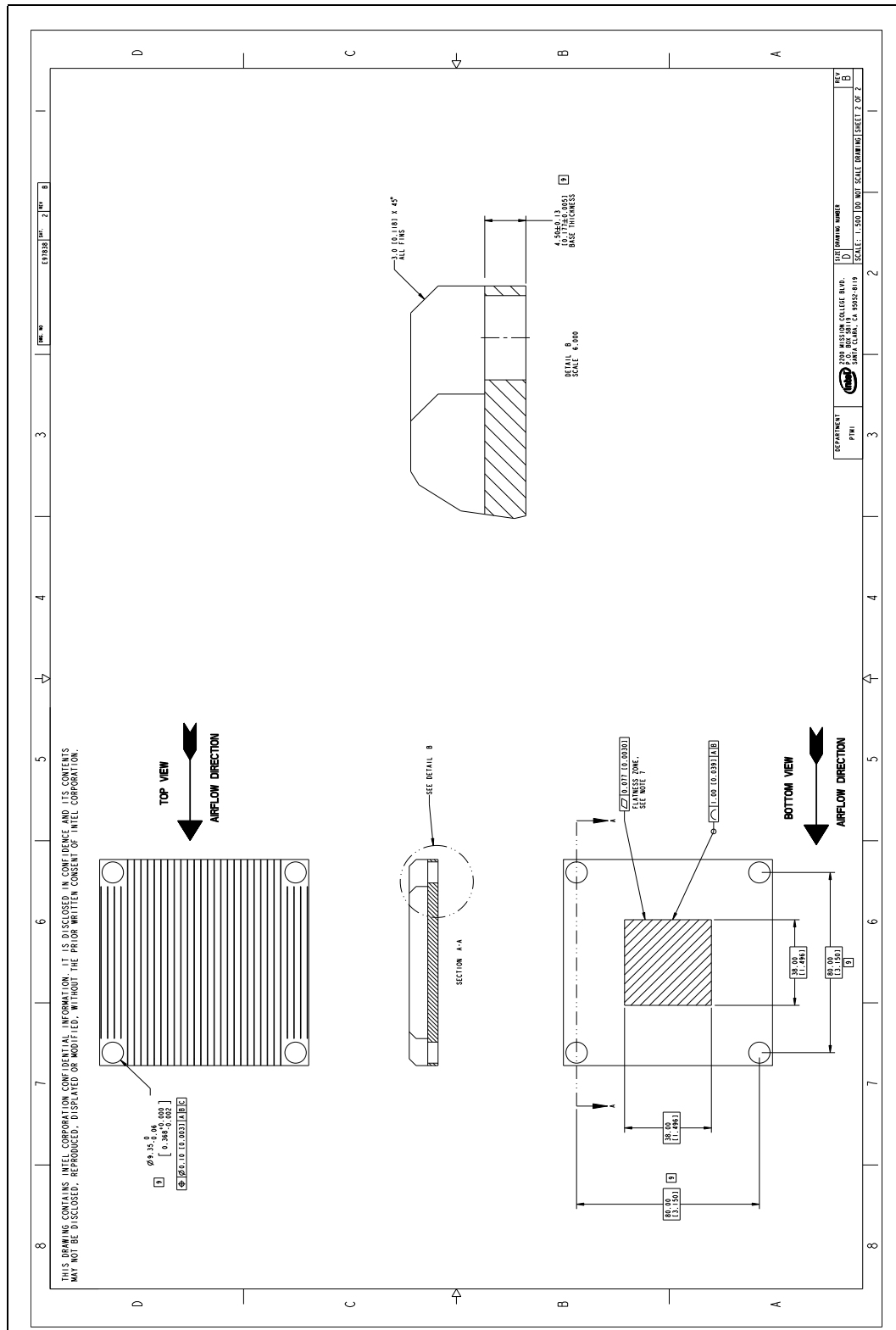


Figure E-4. ATCA Reference Heatsink Fin and Base (Sheet 2 of 2)







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# F Heatsink Load Characterization

## F.1 Introduction

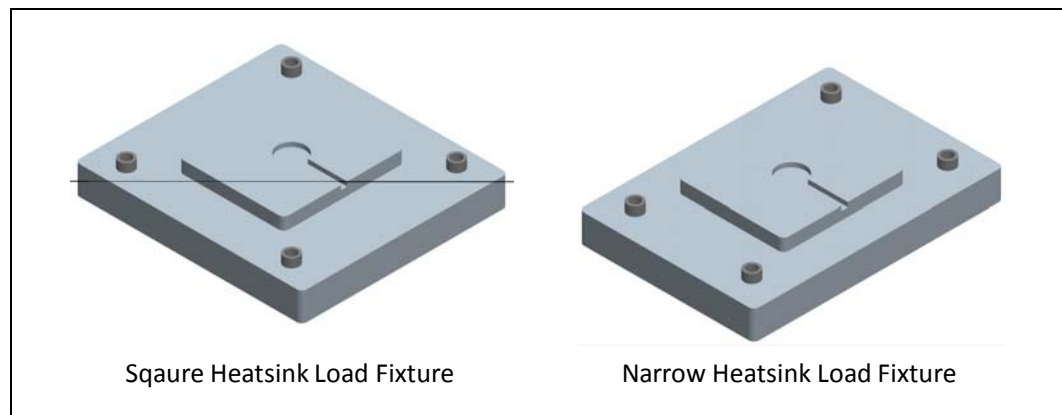
Socket LGA2011-0 requires load sharing with the ILM and heatsink for end of life (EOL) performance. This places additional requirements on the heatsink beyond just providing the minimum pressure for thermal interface performance.

This Appendix outlines the recommended procedure for verifying the heatsink load on a fixture that simulates an ILM and processor interface.

## F.2 Heatsink Load Fixture

The heatsink load fixtures shown in [Figure F-1](#) has four mount points for the heatsink, a middle protrusion simulating the surface of the processor's integrated heat spreader, and a machined pocket to accept a load cell. There are two versions, one simulating the square ILM heatsink mount pattern, and one with the narrow ILM geometry.

**Figure F-1. Heatsink Load Fixtures**



Heatsink load fixtures, square and narrow version, aluminum block with steel threaded inserts.

The recommended load cell is the Omega\* LCKD-100 available separately from Omega\*. Additionally, a system is needed to query the load cell to obtain the force provided by the heatsink. Loadcell calibration certification is also recommended.

## F.3 Procedure for Measuring Heatsink Load

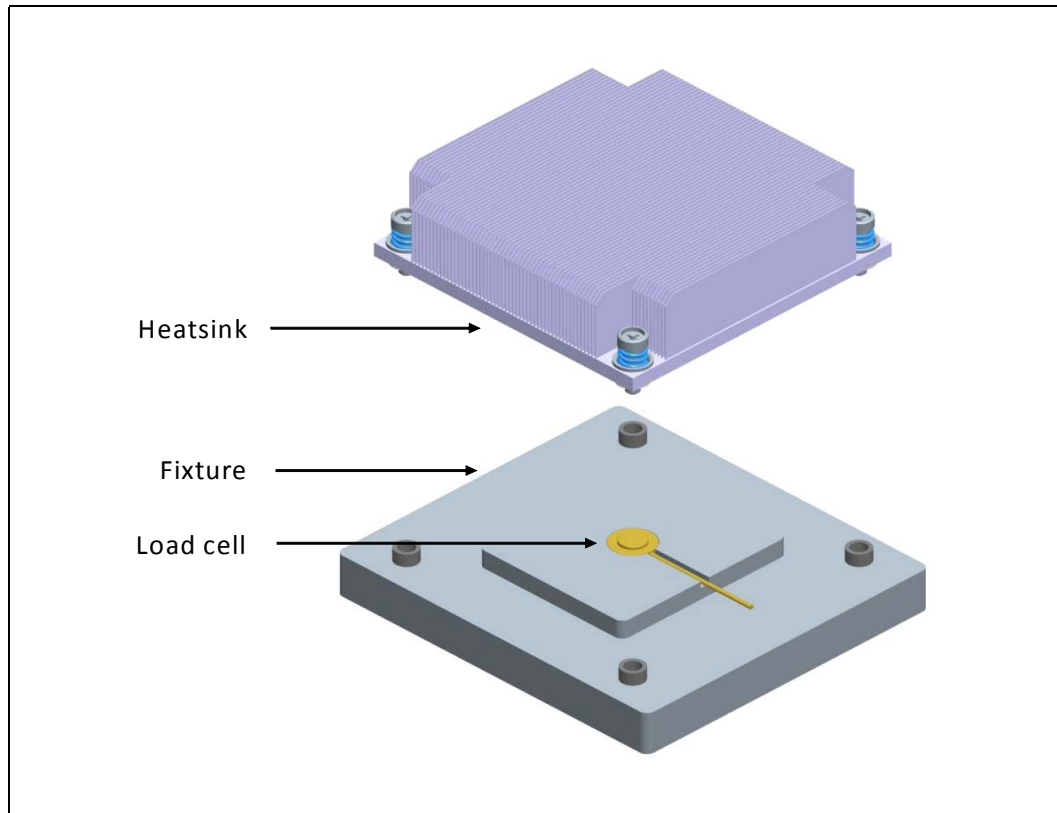
The following steps are suggested for characterizing the heatsink load with the heatsink load fixture and load cell.

**Note:** This fixture will only measure beginning of life (BOL) load and not end of life load (EOL). However, if BOL loads as measured here are between approximately 60 and

70 lbf at low and high stack respectively, then there should be no EOL concerns for the socket.

- Insert Omega\* LCKD-100 load cell into pocket in fixture ensuring no debris is between the interface that would skew the load measurement. See Figure F-2 for example assembly.
- Install the heatsink (without any TIM material) to be characterized using a #2 Phillips driver and torque the four captive screws to 9 inch-pounds  $\pm 1$  inch-pound. It is recommended that each thread be started before final torquing to avoid any cross-threading.
- The fixture is designed to provide a low stack height (8.014 minus 0.34 mm), simulating the low tolerance side of the processor IHS above the board. With this low stack height, the heatsink load should be above approximately 60 lbf to ensure adequate end of life load.
- Once the minimum heatsink load from the previous step has been recorded, shim the fixture by placing a spacer with thickness 0.68 mm between the top of the load cell and the heatsink base to bring the base of the heatsink to the high tolerance stack (8.014 plus 0.34 mm) and measure the load. This load should be kept under approximately 70 blf.

Figure F-2. Heatsink Fixture Assembly



Assembly for measuring heatsink load

**Note:** The loadcell has a point on it. For heatsinks susceptible to damage in this area of contact, it is recommended to insert the load cell with the point down.