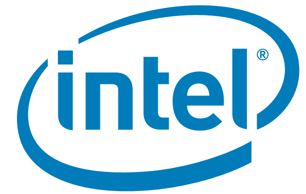
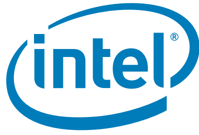


Intel® Xeon® Processor E7-2800/4800/8800 v2 Product Family

Thermal/ Mechanical Specifications and Design Guide

February 2014

Reference Number: 329596-001



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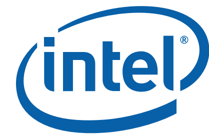

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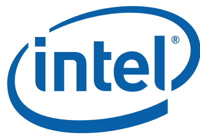

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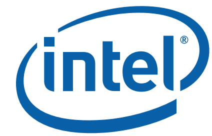

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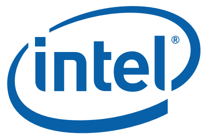

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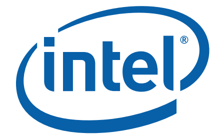

Revision History

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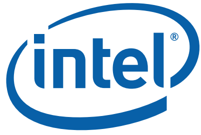
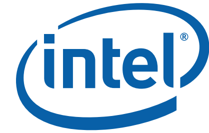




1 Introduction

This document provides specifications and guidelines for the design of an Intel® Xeon® processor E7-2800/4800/8800 v2 product family compatible thermal and mechanical solutions in 2 and 4-socket Intel® Xeon® processor E7-2800/4800/8800 v2 product family-based platform servers.

1.1 Objective

It is the intent of this document to explain and demonstrate the processor thermal and mechanical solution features and requirements. This document also provides an understanding of the processor thermal characteristics, and discusses guidelines for meeting the thermal requirements imposed on the entire life of the processor. As such, the purpose of this design guide is to describe the reference thermal solution and design parameters required for the processor. The thermal/mechanical solutions described in this document are intended to aid component and system designers in developing and evaluating processor compatible solutions.

The goals of this document are:

- To assist board and system thermal mechanical designers.
- To assist designers and suppliers of processor heatsinks.

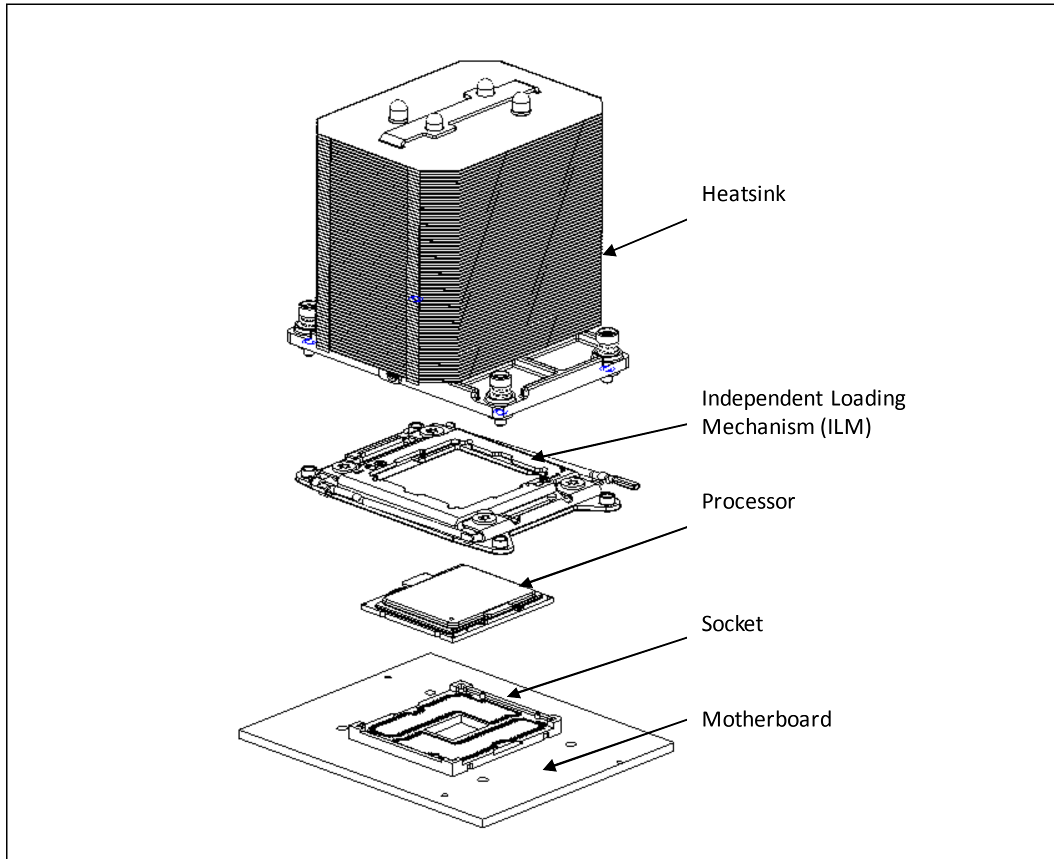
1.2 Scope

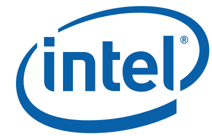
The thermal/mechanical solutions described in this document pertain only to a solution(s) intended for use with the Intel® Xeon® processor E7-2800/4800/8800 v2 product family in 4U form factor systems. This guide contains the mechanical and thermal requirements of the processor cooling solution. Thermal profiles and other processor specifications are provided in the processor datasheet. In case of conflict, the data in the *Intel® Xeon® Processor E7-2800/4800/8800 v2 Product Family Datasheet, Volume 1 - Electrical, Mechanical, and Thermal Specifications* supersedes any data in this document.

Additional reference information is provided in the appendices of this document. The components described in this document include:

- The processor package
- The LGA2011-1 socket
- The Independent Loading Mechanism (ILM) and back plate
- The processor thermal solution (heatsink) and associated retention hardware

Figure 1-1. Intel® Xeon® Processor E7 2800/4800/8800 v2 Product Family-based Platform Socket Stack





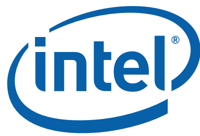
1.3 References

Material and concepts available in the following documents may be beneficial when reading this document.

Table 1-1. Reference Documents

Document	Notes
Intel® Xeon® Processor E7-2800/4800/8800 v2 Product Family Datasheet - Volume One	1
Platform Environment Control Interface (PECI) Specification	1
Intel® Turbo Boost Technology 2.0	1
Intel® Xeon® Processor E7-2800/4800/8800 v2 Product Family – Intel® Turbo Boost Technology Addendum	1
Intel® Turbo Boost Technology Test Application	1
Platform Environment Control Interface (PECI) 3.0 Test Software, Device Drivers and User Guide	1
Manufacturing With Intel Components Using Lead-Free Technology	4
European Blue Angel Recycling Standards	2

Notes:
1. Contact your Intel representative for availability.
2. Available at http://www.blauer-engel.de
3. Available at http://ssiforum.org/specifications.aspx
4. Available at https://learn.intel.com/portal/scripts/general/logon.aspx.



1.4 Terminology

Table 1-2. Terms and Descriptions

Term	Description
Bypass	Bypass is the area between a passive heatsink and any object that can act to form a duct. For this example, it can be expressed as a dimension away from the outside dimension of the fins to the nearest surface.
DTS	Digital Thermal Sensor reports a relative die temperature as an offset from TCC activation temperature.
FSC	Fan Speed Control
HTg	Printed circuit board material, such as FR4, with high glass transition temperature
IHS	Integrated Heat Spreader: a component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
ILM	Independent Loading Mechanism - Provides the force required to seat the 2011-Land FCLGA package onto the socket to maintain the interface between the processor and the socket.
LGA2011-1 Socket	Surface mounted socket with 2011-contacts enabling the processor to interface with the system board.
Pad Crater	Mechanically induced fracture in the resin between copper foil and outermost layer of fiberglass of a printed circuit board
PECI	The Platform Environment Control Interface (PECI) is a one-wire interface that provides a communication channel between Intel processor and chipset components to external monitoring devices.
Ψ_{CA}	Case-to-ambient thermal characterization parameter. A measure of thermal solution performance. Defined as ($T_{CASE} - T_{LA}$) / Total Package Power. Heat source should always be specified for Ψ measurements.
Ψ_{CS}	Case-to-sink thermal characterization parameter. A measure of thermal interface material performance. Defined as ($T_{CASE} - T_S$) / Total Package Power.
Ψ_{SA}	Sink-to-ambient thermal characterization parameter. A measure of heatsink thermal performance using total package power. Defined as ($T_S - T_{LA}$) / Total Package Power.
T_{CASE}	The case temperature of the processor measured at the geometric center of the topside of the IHS.
$T_{CASE-MAX}$	The maximum case temperature as specified in a component specification.
TCC	Thermal Control Circuit: Thermal monitor uses the TCC to reduce the die temperature by using clock modulation and/or operating frequency and input voltage adjustment when the die temperature is very near its operating limits.
$T_{CONTROL}$	$T_{CONTROL}$ is a static value below TCC activation used as a trigger point for fan speed control. When DTS > $T_{CONTROL}$, the processor must comply to the thermal profile.
TDP	Thermal Design Power: Thermal solution should be designed to dissipate this target power level. TDP is not the maximum power that the processor can dissipate.
Thermal Monitor	A power reduction feature designed to decrease temperature after the processor has reached its maximum operating temperature.
Thermal Profile	Line that defines case temperature specification of a processor at a given power level.
TIM	Thermal Interface Material: The thermally conductive compound between the heatsink and the processor case. This material fills the air gaps and voids, and enhances the transfer of the heat from the processor case to the heatsink.
T_{LA}	The measured ambient temperature locally surrounding the processor. The ambient temperature should be measured just upstream of a passive heatsink or at the fan inlet for an active heatsink.
T_{SA}	The system ambient air temperature external to a system chassis. This temperature is usually measured at the chassis air inlets.
U	A unit of measure used to define server rack spacing height. 1U is equal to 1.75 in, 2U equals 3.50 in, and so forth.

2 Thermal and Mechanical Design

In this section, mechanical and thermal requirements of the processor as well as its enabling solution are discussed. These specifications will enable a designer to identify and establish set of design requirements for the motherboard and the system in addressing compliance with the processor and the enabled components specifications.

2.1 Mechanical Requirements

The mechanical performance of the processor retention and thermal solution are to satisfy the requirements and volumetric keep-outs of the processor and the LGA2011-1 socket, as described in this section to ensure compatibility with the processor and the platform.

2.1.1 Processor Package Mechanical Specifications

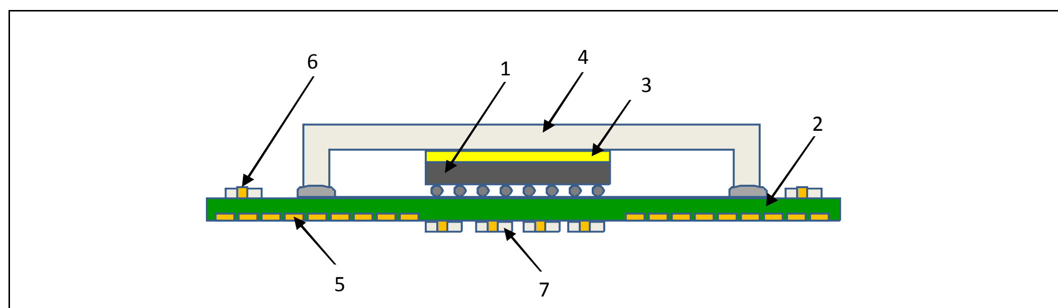
2.1.1.1 Processor Package Description

The processor is housed in an Flip-Chip Land Grid Array (FC-LGA10) package that interfaces with the motherboard via an LGA2011-1 SMT socket. The package consists of a processor integrated heat spreader (IHS), which is attached to the package substrate and die and serves as the mating surface for the processor component thermal solutions, such as a heatsink. The bottom side of the package has 2011 lands, a 43.18 x 50.24 mm pad array which interfaces with the LGA2011-1 SMT socket. Figure 2-1 shows a sketch of the processor package components and how they are assembled together.

The package components include the following:

1. Processor Die
2. Package Substrate
3. TIM - Thermal Interface Material, also known as TIM1
4. Integrated Heat Spreader (IHS)
5. LGA lands (LGA2011-1 socket interface)
6. Decoupling and server management components (top side)
7. Discrete components (bottom side)

Figure 2-1. Processor Package Assembly Sketch



Note: This drawing is not to scale and is for reference only. The socket is not shown.

Figure 2-2. Processor Package ISO View

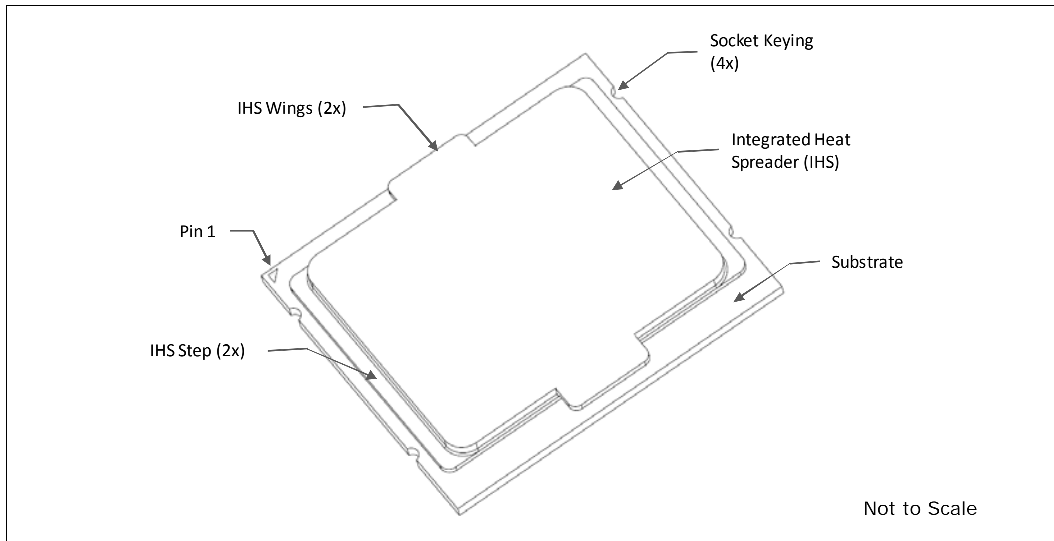
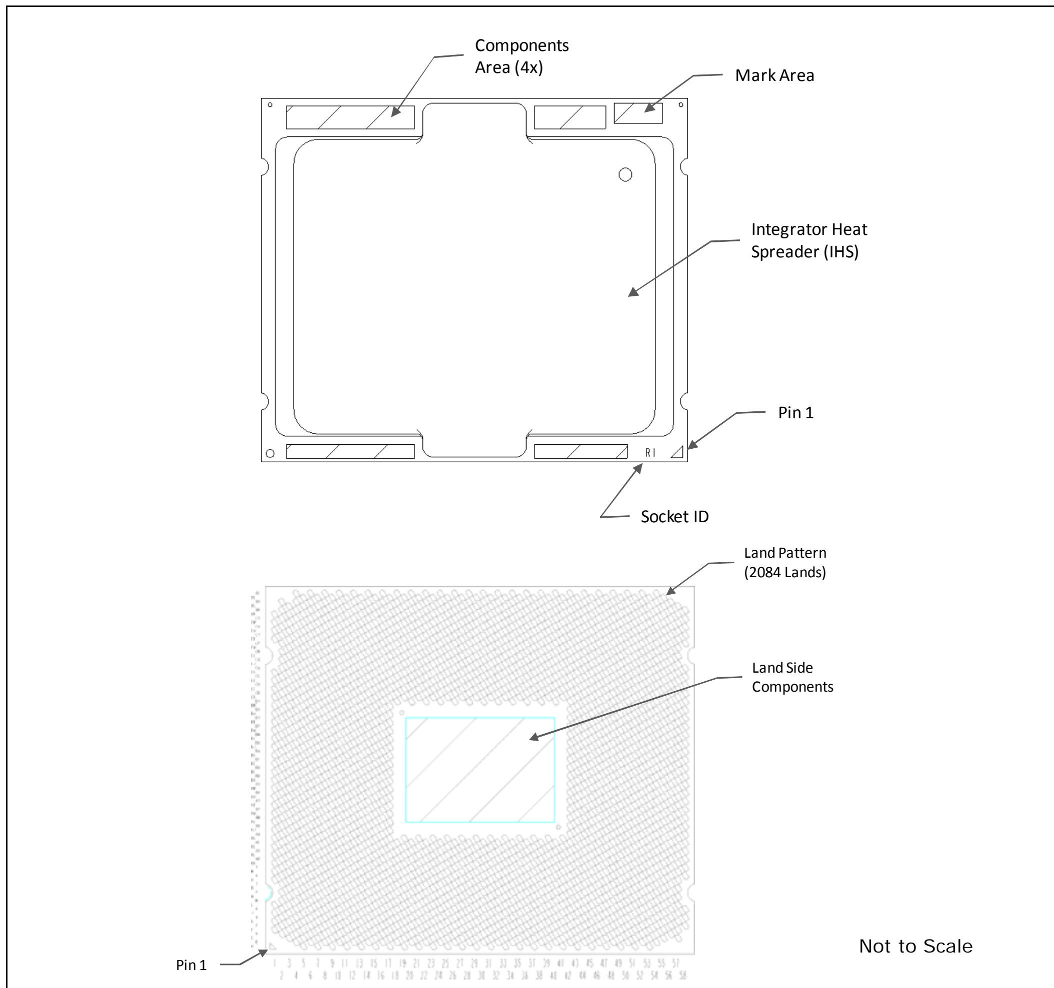
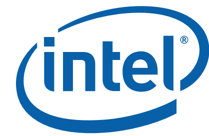


Figure 2-3. Processor Package Top and Bottom View





2.1.1.2 Processor Mechanical Dimensions

The package includes an integrated heat spreader (IHS). The IHS transfers the non-uniform heat from the die to the top of the IHS, out of which the heat flux is more uniform and spread over a larger surface area (not the entire IHS area). This allows more efficient heat transfer out of the package to an attached cooling device. The IHS is designed to be the interface for contacting a heatsink.

The processor connects to the baseboard through a surface-mount-type LGA socket. A description of the socket can be found in Section 2.1.2.

Note: Processor package land count is greater than the socket contact count.

The processor package mechanical drawings are provided in the Appendix D as a reference. The processor package mechanical drawings include dimensions necessary to design a thermal solution for the processor. These dimensions will include:

1. Package reference with tolerances (total height, length, width, and so on)
2. IHS parallelism and tilt
3. Land dimensions
4. Top-side and back-side component keep-out dimensions
5. Reference datum

2.1.1.3 Processor Mechanical Loads

The processor package has mechanical load limits should not be exceeded during the processor ILM actuation, heatsink installation and removal, mechanical stress testing, or standard shipping conditions as permanent damage to the processor may occur. For example, when a compressive static load is necessary to ensure thermal performance of the Thermal Interface Material (TIM2) between the heatsink base and the IHS, it should not exceed the corresponding specification. The processor substrate should not be used as a mechanical reference or load-bearing surface for thermal solutions.

Table 2-1. Processor Mechanical Parameters

Parameter	Value	Unit	Notes
Max Allowable Static Compressive Load	1068	N	5
Max Allowable Dynamic Compressive Load	589	N	4, 5, 6
Shear Load (max)	36.3	kg	1
Tensile Load (max)	15.9	kg	2
Torsion Load (max)	15.9	kg-cm	3

Notes:
1. Shear load that can be applied to the package IHS.
2. Tensile load that can be applied to the package IHS.
3. Torque that can be applied to the package IHS.
4. Duration of the load not to exceed one second (1 s).
5. These specifications apply to uniform compressive loading in a direction normal to the processor IHS.
6. Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement.

The heatsink and ILM mass will also add additional dynamic compressive load to the package during a mechanical shock event. Amplification factors due to the impact force during shock must be taken into account in dynamic load calculations. The total combination of dynamic and static compressive load should not then exceed the processor compressive dynamic load specified in the process datasheet and in Table 2-1 during a vertical shock. Using any portion of the processor substrate as a

load-bearing surface in either static or dynamic compressive load conditions is not recommended.

2.1.1.4 Processor Component Keep-Out Zones

The processor may contain components on the substrate that define component keep-out zone requirements. A thermal and mechanical solution design must not intrude into the required keep-out zones. Decoupling capacitors are typically mounted on either the topside or land-side of the package substrate. See processor package mechanical drawing for location, size, and additional information on keep-out zones. The location and quantity of package capacitors may change due to manufacturing efficiencies but will remain within the component keep-in areas.

2.1.1.5 Package Insertion Specifications

The processor can be inserted into and removed from an LGA2011-1 socket 15 times. The socket should meet the LGA2011-1 requirements detailed in the Section 2.1.2.

2.1.1.6 Processor Mass Specification

The typical mass of the processor is ~50 grams. This mass [weight] includes all the components that are included in the package.

2.1.1.7 Processor Materials

Table 2-2 lists some of the package components and associated materials.

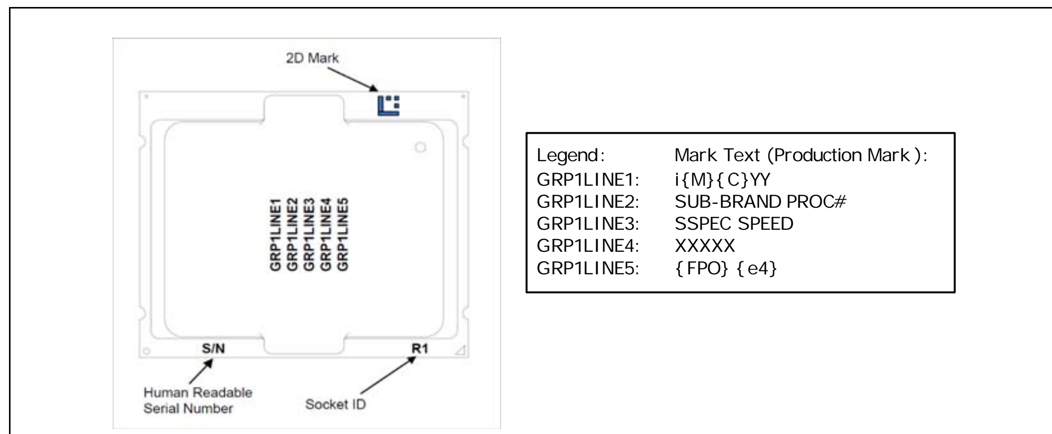
Table 2-2. Processor Materials

Component	Material
Integrated Heat Spreader (IHS)	Nickel Plated Copper
Substrate	Halogen Free, Fiber Reinforced Resin
Substrate Lands	Gold Plated Copper

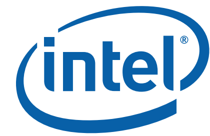
2.1.1.8 Processor Markings

Figure 2-4 shows the topside markings on the processor. This diagram is to aid in the identification of the processor.

Figure 2-4. Processor Top-Side Markings



XXXXX = Country of Origin



2.1.2 LGA2011-1 Socket Mechanical Specifications

2.1.2.1 Socket Overview

This section describes a surface mount LGA (Land Grid Array) socket that provides I/O, power, and ground contacts. The socket has two main components, the socket body and Pick and Place (PnP) cover. They are delivered by the socket supplier as a single integral assembly. The main body of the socket, which is made of electrically insulated material with resistance to high temperature, houses the socket contacts. Key components of the socket are the main body of the socket, socket contacts, surface mount features, and protective cover and its keying features. Figure 2-5 illustrates the socket features. Keying features (wall protrusions) within the contact array area and raised edges of the socket body help align the package with respect to the socket contacts.

Figure 2-5. LGA2011-1 Socket with Cover

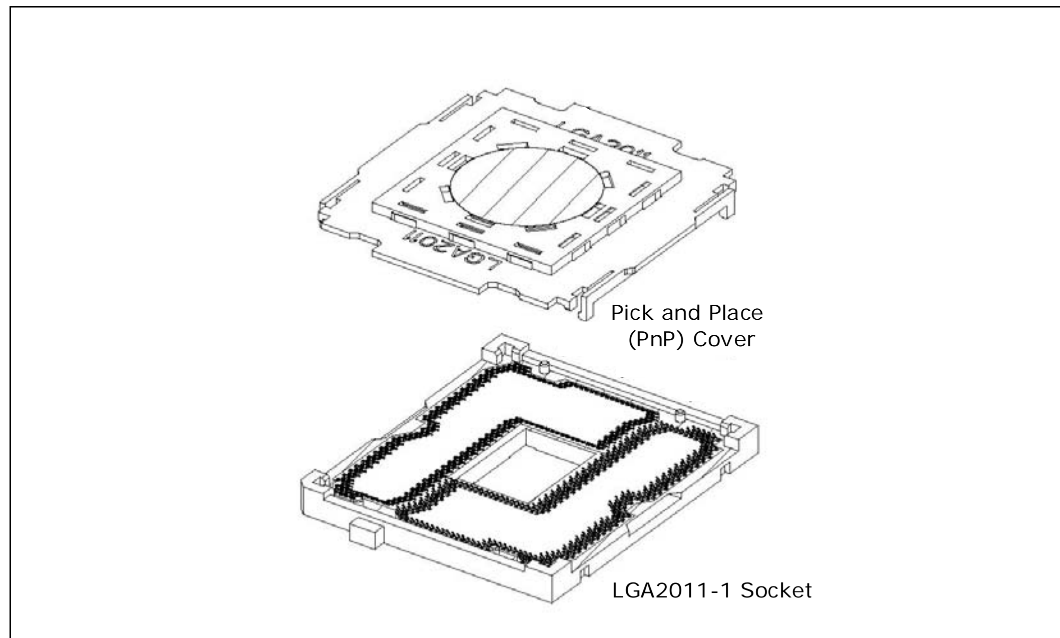


Table 2-3. LGA2011-1 Socket Attributes

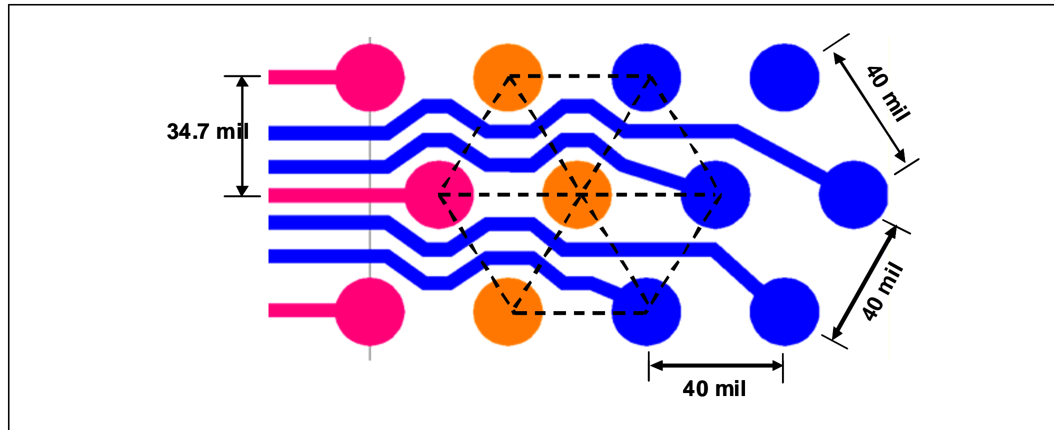
LGA2011-1 Socket	Attributes
Component Size	58.5 mm (L) x 51 mm (W)
Pitch	1.016 mm (Hex Array)
Ball Count	2011

2.1.2.2 Socket Features

LGA2011-1 socket contacts are in 1.016 mm (0.040") hexagonal pitch in a 58 x 43 grid array with 24x16 grid depopulation in the center of the array and selective depopulation elsewhere, see Appendix F. The tips of the contacts will extend beyond the surface of the socket to make contact with the pads located at the bottom of the processor package.

Solder balls enable the socket to be surface mounted to the processor board. Each contact will have a corresponding solder ball. Solder ball position may be at an offset with respect to the contact tip and base. Hexagonal area array ball-out increases contact density by 12% while maintaining 40 mil minimum via pitch requirements.

Figure 2-6. Hexagonal Array in LGA2011-1



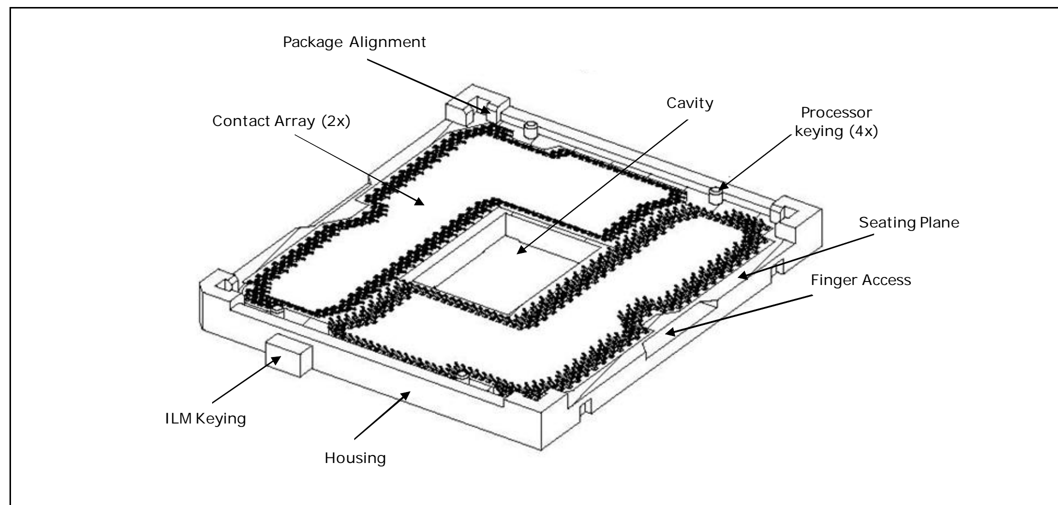
The socket interfaces with the package (processor) and the Independent Loading Mechanism (ILM). The ILM design includes a back plate which is integral to having a uniform load on the socket solder joints.

The socket cover is intended to be reusable and recyclable. It will enable socket pick and placing during motherboard assembly. The socket cover will also protect the socket contacts from contamination and damage during board assembly and handling.

Features of the socket includes:

- Contact housing
- Processor package keying (4x)
- Package seating plane
- ILM keying (1x)
- side walls for package alignment (8x)
- Finger access for ease of package insertion and removal
- Center cavity for the processor secondary side and motherboard primary side components

Figure 2-7. LGA2011-1 Socket Features



2.1.2.3 Socket Mechanical

2.1.2.3.1 Socket Size

The socket dimensions are shown in Appendix F; allow for full insertion of the package into the socket without interference.

This information should be used in conjunction with the reference motherboard keep-out drawings provided in Appendix G to ensure compatibility with the reference thermal mechanical components.

2.1.2.3.2 Socket Standoffs

Standoffs must be provided on the solder ball side of the socket base in order to ensure the minimum socket height after solder reflow. A minimum gap of 0.1 mm between the solder-ball seating plane and the standoff prior to reflow is required to prevent solder ball-to-board land open joints.

2.1.2.3.3 Package Seating Plane

A seating plane on the top side of the socket body defines the minimum package height from the motherboard. See Section 2.4.4.3 for calculated IHS height above the mother board.

2.1.2.3.4 Package Translation

The socket shall be built so that the post-actuated seating plane of the package is flush with the seating plane of the socket. Movement will be along the axis normal to the seating plane.

2.1.2.3.5 Insertion/Removal/Actuation Forces

Any actuation must meet or exceed *SEMI S8-95 Safety Guidelines for Ergonomics/Human Factors Engineering of Semiconductor Manufacturing Equipment*, example Table R2-7 (Maximum Grip Forces).

The socket must be designed so that it requires no force to insert the package into the socket.

2.1.2.3.6 Orientation in Packaging, Shipping, and Handling

Packaging media needs to support high-volume manufacturing. Media design must be such that no component of the socket (solder balls, contacts, housing, and so on) is damaged during shipping and handling.

2.1.2.3.7 Pick and Place, and Handling Cover

To facilitate high-volume manufacturing, the socket shall have a detachable cover to support the vacuum type Pick and Place system. The cover will remains on the socket during reflow to help prevent contamination during reflow. The cover can withstand 260°C for 40 seconds (typical reflow/rework profile) and the conditions listed in Appendix B without degrading. The cover could also be used as a protective device to prevent damage to the contact field during handling.

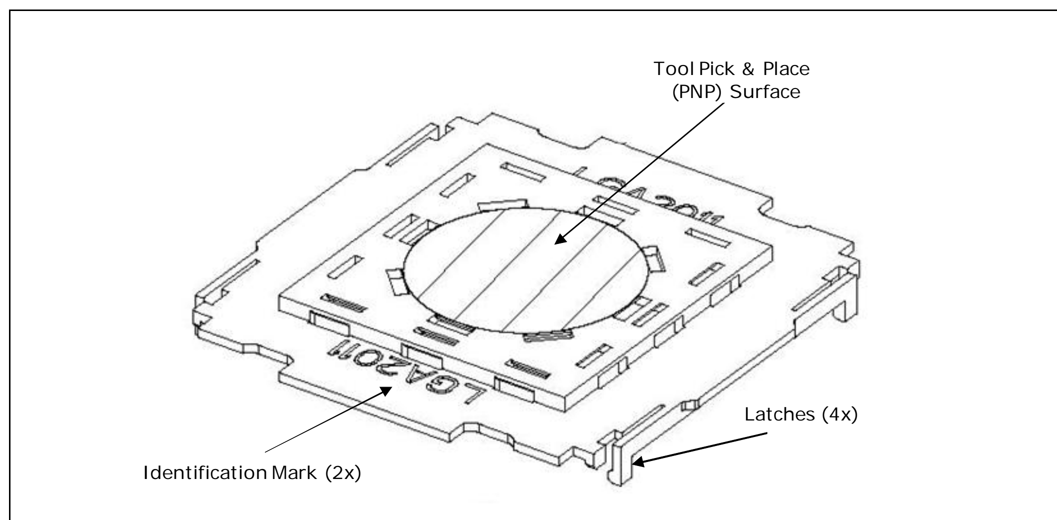
Cover retention must be sufficient to support the socket weight during lifting, translation, and placement (board manufacturing), and during board and system shipping and handling. Cover design shall allow use of tool to remove the cover. The force required for removing of the cover shall meet or exceed the applicable requirements of SEMI S8-0999 Safety Guidelines for Ergonomics/Human Factors Engineering of Semiconductor Manufacturing Equipment. The removal of the cover shall not cause any possible damage to the socket body nor to the cover itself within the cover durability limit.

Table 2-4. Socket PnP Cover Insertion/Removal

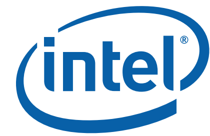
Parameter	Value	Note
Insertion Force	1 kgf [2.3 lbf] Max	
Removal force, Pre-SMT	0.23 kgf [0.5 lbf] min	To support socket vertical lift-off during SMT process
Removal Force, Post SMT	0.77 kgf [1.7 lbf] max	PnP cover shall not fall-off in rework
Durability	15 cycles min	number of cap insertion/removal cycles

The pick and place cover designed shall be interchangeable between socket suppliers.

Figure 2-8. Socket Pick and Place Cover



Note: The cover will remain on the socket with intent to continue providing contact protection during the ILM installation. Once the ILM with its cover is installed, the socket PnP cover must be removed to prevent damage to the socket contacts.



2.1.2.3.8 Durability

The socket must withstand 30 cycles of processor insertion and removal. The maximum part average and single pin resistances from Table E-1 must be met when mated in the 1st and 30th cycles.

2.1.2.3.9 Socket Keep-in/Keep-out Zone

Socket keep-in and keep-out zones are identified on the motherboard to ensure that sufficient space is available for the socket, and to prevent interference between the socket and the components on the motherboard. These areas are illustrated in Appendix G. It is the responsibility of the socket supplier and the customer to identify any required deviation from specifications identified here.

2.1.2.3.10 Attachment

The socket will be attached to the motherboard via its 2011 contact solder balls. There are no additional external methods (that is, screw, extra solder, adhesive, and so on) to attach the socket.

The socket will be tested against the mechanical shock and vibration requirements such as listed in Appendix B under the expected use conditions with all assembly components under the loading conditions outlined in Section 2.1.2.3.11.

2.1.2.3.11 Socket Loading and Deflection Specifications

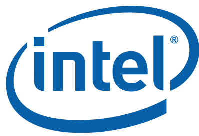
Table 2-5 provides loading and board deflection specifications for the LGA2011-1 Socket. These mechanical load limits should not be exceeded during component assembly, mechanical stress testing, or standard drop and shipping conditions. All dynamic requirements are under room temperature conditions while all static requirements are under 125°C conditions.

Table 2-5. Socket Loading and Deflection Specifications

Parameter		SI Units			Notes
		Min	Max	Unit	
Static Compressive per Contact		10	38	gf	1, 2
Static Compressive Load		490	1068	N	2, 3
Dynamic Compressive Load			589	N	5, 6
Board Transient Strain	93 and 130 mil board		450	ue	4

Notes:
1. Socket load specification is for throughout the product life cycle.
2. The compressive load applied on the LGA contacts to meet electrical performance.
3. The total load applied by both the ILM and the heatsink onto the socket through the processor package.
4. Maximum allowable strain below socket BGA corners during transient loading events (i.e., slow displacement events) which might occur during board manufacturing, assembly or testing. See the LGA2011-1 BFI Strain Guidance Sheet. Contact your Intel CQE representative on how to obtain a copy of this datasheet.
5. Dynamic compressive load applies to all board thicknesses.
6. Dynamic loading is defined as an 11ms duration average load superimposed on the static load requirement. This load is superimposed onto the socket static compressive load to obtain total dynamic load.

The minimum *Static Total Compressive* load will ensure socket reliability over the life of the product and that the contact resistance between the processor and the socket contacts meets the values outlined in Table E-1.



2.1.2.3.12 Socket Critical-to-Function Interfaces

Critical-to-function (CTF) dimensions for motherboard layout and assembled components' interface to the socket are identified in Table 2-6. The CTF values are detailed on the socket drawing provided in Appendix F and take precedence over all values presented in this document. All sockets manufactured must meet the specified CTF dimensions.

Table 2-6. Critical-to-Function Interface Dimensions

Description	Sheet/Zone
Socket Package Alignment Cavity Length *	Sheet 2, H7
Socket Package Alignment Cavity Width *	Sheet 2, F5
Socket Height (from Package Seating Plane to MB after Reflow) **	Sheet 2, B6-7
Seating Plane Co-planarity *	Sheet 2, C7
Through Cavity Length	Sheet 2, G6
Through Cavity Width	Sheet2, F5-6
Through Cavity X-Position Virtual Condition	Sheet2, D7-8
Through Cavity Y-Position Virtual Condition	Sheet2, F5-6
Stand-Off Gap (Solder Ball to Stand-Off)	Sheet2, C6
Solder Ball Pattern Locating True Position	Sheet3, B3-4, B1-C2
Solder Ball Feature Relating True Position	Sheet3, B3-4, B1-C2
Solder Ball Co-planarity	Sheet2, B6
Contact Height Above Seating Plane *	Sheet2, B7-8
Contact Pattern Locating True Position *	Sheet2, B1-2, C3-4
Contact Feature Relating True Position*	Sheet2, B1-2, C3-4
Contact Co-planarity *	Sheet2, B7-8

* This feature is a pre-and post-SMT CTF
** This feature is post-SMT only

2.1.2.4 Socket Housing

2.1.2.4.1 Housing Material

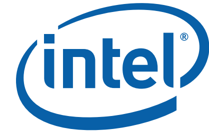
The socket housing material should be of thermoplastic or equivalent, UL 94 V-0 flame rating, temperature rating and design capable of maintaining structural integrity following a temperature of 260°C for 40 seconds, which is typical of a reflow/rework profile for solder material used on the socket. The material must have a thermal coefficient of expansion in the XY plane capable of passing reliability tests rated for an expected high operating temperature, mounted on HTg FR4-type motherboard material. The creep properties of the material must be such that the mechanical integrity of the socket is maintained for the stress conditions outlined in Appendix B.

2.1.2.4.2 Housing Color

The color of the socket housing must be dark as compared to the solder balls to provide the contrast needed for OEM's pick and place vision systems. Components of the socket may be different colors, as long as they meet the above requirement.

2.1.2.4.3 Package Installation/Removal Access

Access must be provided to facilitate the manual insertion and removal of the package. No tool should be required to install or remove the package from the socket.



2.1.2.4.4 Package Alignment/Orientation

A means of providing fixed alignment and proper orientation with the pin 1 corner of the package must be provided. The package substrate will have two pairs of keying notches at the two opposing slides of the package. The socket will utilize the four protrusions in the contact array area to serve as alignment features to mate with the notches on the package. In addition, the socket raised walls at the four corners of the socket facilitate the fine alignment between the package and socket contacts. The package must sit flush against the socket contacts when aligned.

2.1.2.4.5 ILM Compatibility

The socket must provide ILM keying feature to ensure compatibility with the LGA2011-1 Independent Loading Mechanism (ILM).

2.1.2.4.6 Markings

All markings required in this section must withstand a temperature of 260°C for 40 seconds, which is typical of a reflow/rework profile for solder material used on the socket, as well as any environmental test procedure outlined in Appendix B, without degrading. Socket marks must be visible after it is mounted on the motherboard.

- **Name**
- **LF-LGA2011-1** . (Font type is Helvetica Bold – minimum 6 point [or 2.125 mm]).

Note: This mark shall be stamped or laser-marked into the sidewall of the stiffener plate on the actuation lever side.

Manufacturer's Insignia (font size at supplier's discretion).

This mark will be molded or laser-marked into the top side of the socket housing.

Both socket name and manufacturer's insignia must be visible when first seated on the motherboard.

- **Lot Traceability**

Each socket will be marked with a lot identification code to allow traceability of all components, date of manufacture (year and week), and assembly location. The mark must be placed on a surface that is visible after the socket is mounted on the motherboard. In addition, this identification code must be marked on the exterior of the box in which the unit is shipped.

- **Visual Aids**

The socket will have markings identifying Pin 1. This marking will be represented by a clearly visible triangular symbol in the location specified.

2.1.2.4.7 Contacts Characteristics

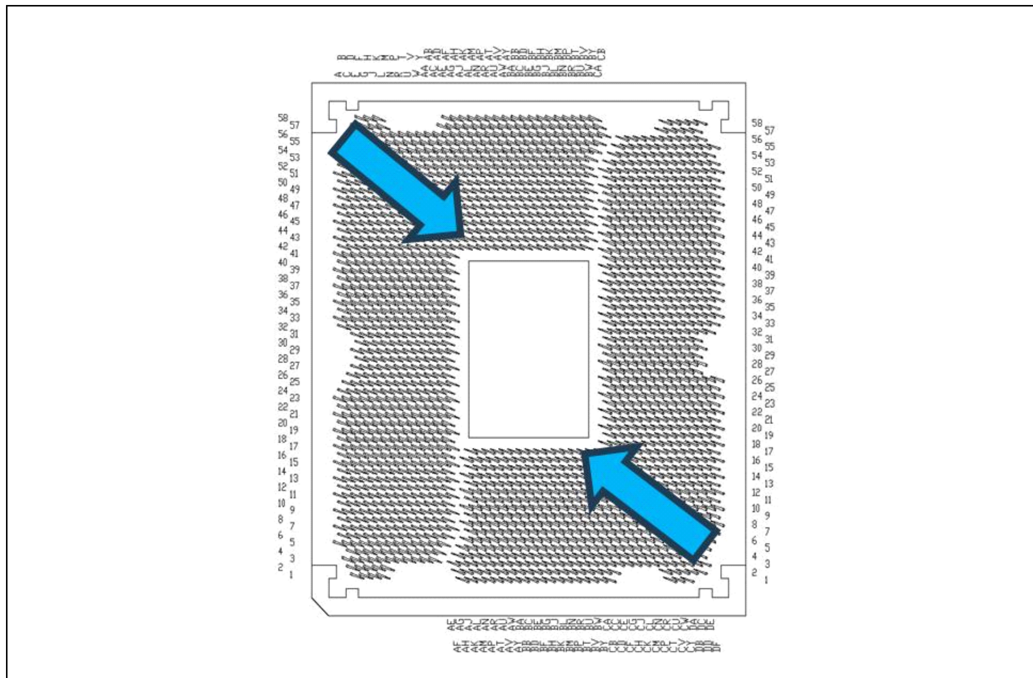
- **Number of Contacts**

Total number of contacts: 2011

- **Layout**

The contacts are laid out in two 'L' shape regions opposing each other as shown in Figure 2-9. The arrows in the figure indicate the orientation of the contacts in the two regions. There are 1005 and 1006 contacts in regions A and B, respectively.

Figure 2-9. Contact Orientation



- **Base Material**

High-strength copper alloy.

- **Contact Area Plating**

For the area on socket contacts where processor lands will mate, there is a 0.381 µm [15 µinches] minimum gold plating over 1.27 µm [50 µinches] minimum nickel under-plating in critical contact areas (area on socket contacts where processor lands will mate) is required. No contamination by solder in the contact area is allowed during solder reflow.

- **Lubricants**

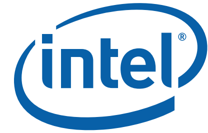
For the final assembled product, no lubricant is permitted on the socket contacts. If lubricants are used elsewhere within the socket assembly, these lubricants must not be able to migrate to the socket contacts.

- **Co-Planarity**

The co-planarity (profile) requirement for all contacts mating to the top side of the socket is defined in Appendix F.

- **True Position**

The contact pattern has a true position requirement with respect to applicable datum in order to mate with the package land pattern. Refer to Appendix F for more details.



- **Stroke/Load**

The minimum vertical height of the contact above the package seating plane is defined in Appendix F. The minimum vertical stroke of the contact must, under all tolerance and warpage conditions, generate a normal force load to ensure compliance with all electrical requirements of the socket defined in Appendix E. The cumulative normal force load of all contacts must not exceed the load limits defined in Table 2-5.

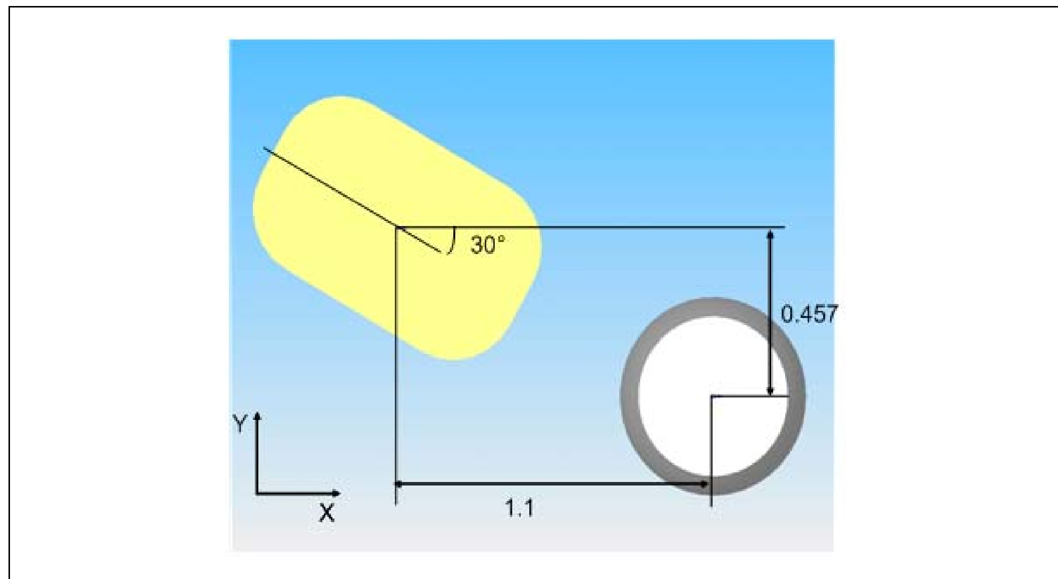
2.1.2.4.8 Contact/Pad Mating Location

All socket contacts should be designed such that the contact tip lands within the substrate pad boundary before any actuation load is applied and remains within the pad boundary at final installation after actuation load is applied.

The offset between LGA land center and solder ball center is defined in Figure 2-10.

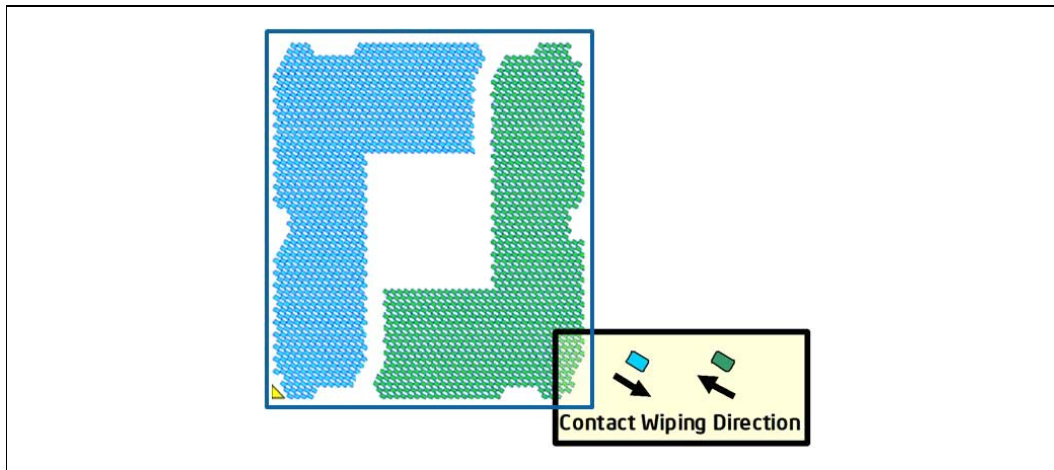
Note: It is recommended that the center of the contact landing zone coincides with the processor pad center.

Figure 2-10. Offset between LGA Land Center and Solder Ball Center



Note: All dimensions are in mm.

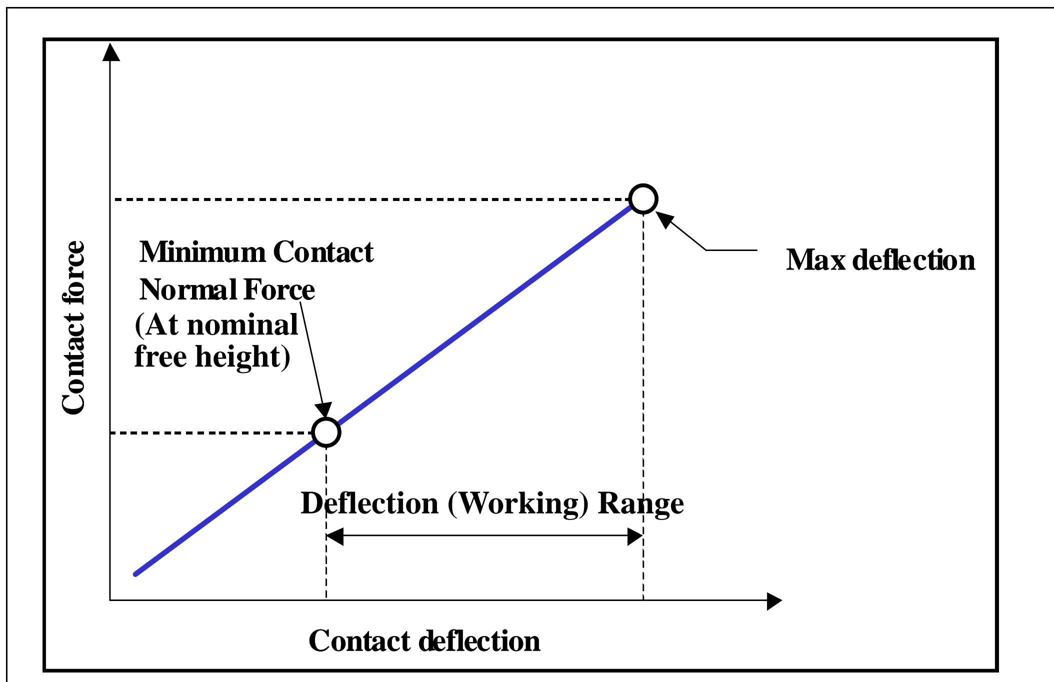
Figure 2-11. Contact Wiping Direction

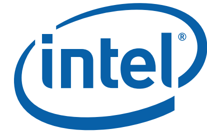


2.1.2.4.9 Contact Load-Deflection Curve

The contact shall be designed with an appropriate spring rate and deflection range, as illustrated in Figure 2-12, to ensure adequate contact normal force in order to meet EOL performance at all contact locations. The load-deflection curve is not necessary to be linear between the minimum and maximum deflection points. The LGA contact working range is defined as the difference of contact deflection at the minimum contact load and the maximum contact deflection. Minimum contact normal force should be 15 gf (gram force). The deflection (working) range shall be no less than 0.25 mm from nominal contact free height.

Figure 2-12. Contact Force versus Contact Deflection Range





2.1.2.4.10 Solder Ball Characteristics

- **Number of Solder Balls**

Total number of solder balls: 2011.

- **Layout**

The solder balls are laid out in two 'L' shape regions, as shown in Appendix F.

- **Material**

Lead free SAC solder alloy with a silver content between 3% and 4% with a melting point temperature of 217 C maximum (for example, SnAgCu) and be compatible with standard lead free processing such as Immersions silver (ImAg) and OSP MB surface finish with SnAg/SnAgCu solder paste.

The co-planarity (profile) and true position requirements are defined in Appendix F.

- **Co-Planarity**

The co-planarity (profile) requirement for all solder balls on the underside of the socket is defined in Appendix F.

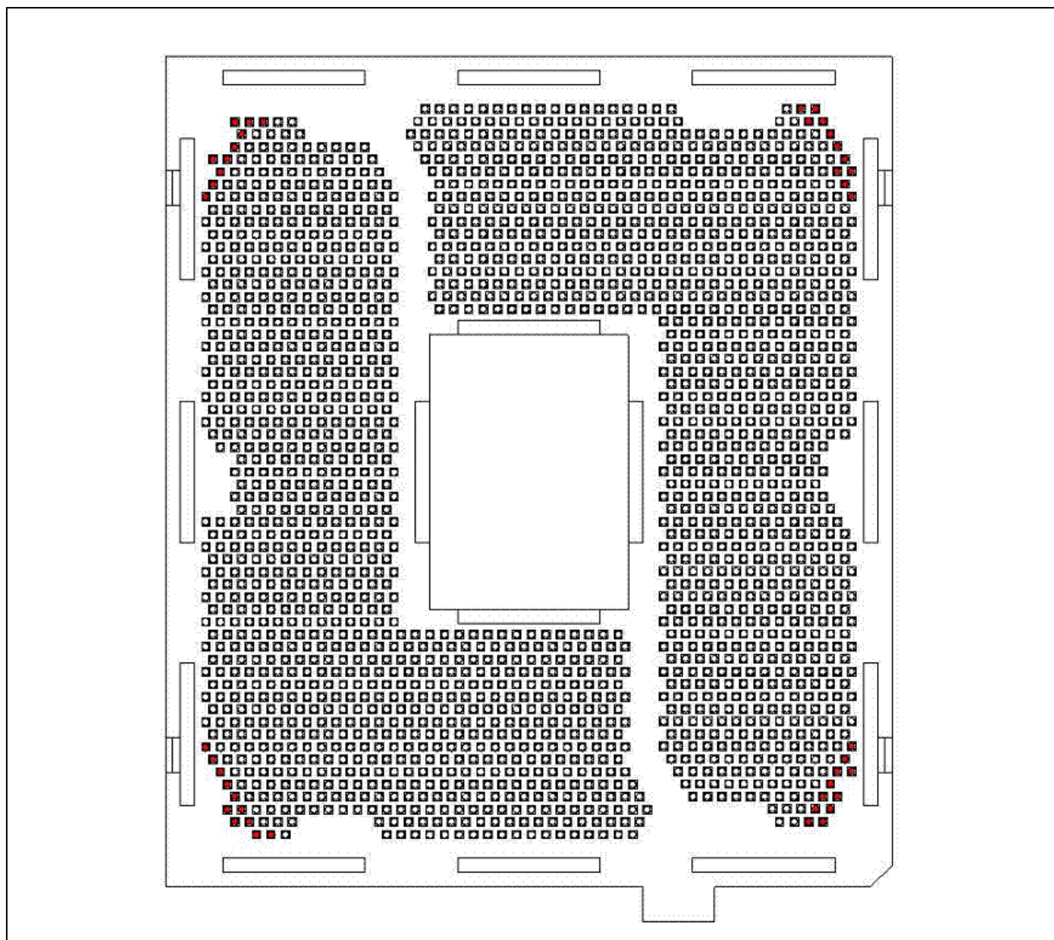
- **True Position**

The solder ball pattern has a true position requirement with respect to applicable datum in order to mate with the motherboard land pattern. Refer to Appendix F for details.

2.1.2.5 LGA2011 Socket NCTF Solder Joints

Intel has defined selected 43 solder joints of the socket as non-critical to function (NCTF) when evaluating package solder joints post environmental testing. NCTF solder joints are located at four corners, 10 contacts in NE corner and 11 contacts per all other corners, as shown in Figure 2-13.The signals at NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.

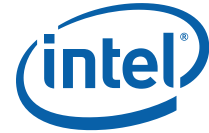
Figure 2-13. LGA2011 Socket NCTF Solder Joints (Bottom View)



2.1.3 Mechanical Considerations

An retention/loading mechanism must be designed to support the processor heatsink and to ensure processor interface with the socket contact is maintained since there are no features on the LGA2011-1 socket for direct attachment of the heatsink or retaining the processor. In addition to supporting the processor heatsink over the processor, this mechanism plays a significant role in the robustness of the system in which it is implemented, in particular:

- Ensuring that thermal performance of the TIM applied between the IHS and the heatsink is achievable. TIMs, especially those based on phase change materials, are very sensitive to applied pressure: the higher the pressure, the better the initial performance. TIMs such as thermal greases are not as sensitive to applied pressure. Refer to Section 2.2.6, Section 2.4.3 for information on trade-offs made with TIM selection. Designs should consider the impact of shock and vibration events on TIM performance as well as possible decrease in applied pressure over time due to potential structural relaxation in enabled components.
- Ensuring that system electrical, thermal, and structural integrity is maintained under shock and vibration events. The mechanical requirements of the attach mechanism depend on the weight of the heatsink, as well as the level of shock and vibration that the system must support. The overall structural design of the



baseboard and system must be considered when designing the heatsink and ILM attach mechanism. Their design should provide a means for protecting the LGA2011-1 socket solder joints as well as preventing package pullout from the socket.

Note: The load applied by the attachment mechanism and the heatsink must comply with the package specifications, along with the dynamic load added by the mechanical shock and vibration requirements.

Note: Load induced onto the package and socket by the ILM may be influenced with heatsink installed. Determining the performance for any thermal/mechanical solution is the responsibility of the customer.

A potential mechanical solution for heavy heatsink is the use of a supporting mechanism such as a backer plate or the utilization of a direct attachment of the heatsink to the chassis pan. In these cases, the strength of the supporting component can be utilized rather than solely relying on the baseboard strength. In addition to the general guidelines given above, contact with the baseboard surfaces should be minimized during installation in order to avoid any damage to the baseboard.

Placement of board-to-chassis mounting holes also impacts board deflection and resultant socket solder ball stress. Customers need to assess the shock for their designs as heatsink retention (back plate), heatsink mass and chassis mounting holes may vary.

2.1.4 Mechanical Load Specifications

2.1.4.1 ILM Load Specifications

The ILM is designed to achieve the minimum Socket *Static Pre-Load Compressive* load specification. The minimum *Static Pre-Load Compressive* load is the force provided by the ILM and should be sufficient for rudimentary continuity testing of the socket and/or board. *This load value will not ensure normal operation throughout the life of the product.* Please see Table 2-7.

The thermal solution (heatsink) should apply additional load to achieve the Socket Static Total Compressive load (see Table 2-5). The heatsink load will be applied to the IHS (Integrated Heat Spreader). The dual-loading approach is represented by the following equation:

$$F_{ILM} + F_{HEATSINK} = F_{SOCKET}$$

Table 2-7 provides load specifications for the ILM and heatsink. The maximum limits should not be exceeded during assembly, shipping conditions, or standard use condition. Exceeding these limits may result in component failure. The socket body or the processor substrate should not be used as a mechanical reference or load-bearing surface for the thermal solution.

Table 2-7. ILM and Heatsink Mechanical Load Specifications (Sheet 1 of 2)

Parameter	Min	Max	Notes
Total Static Compressive Load BOL (HS+ILM)	667 N [150 lbf]	1068 N [240 lbf]	1, 2
Heatsink Static Compressive Load BOL	222 N [50 lbf]	356 N [80 lbf]	1, 3, 4, 5
Heatsink Static Compressive Load EOL	178 N [40 lbf]		

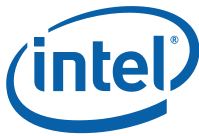


Table 2-7. ILM and Heatsink Mechanical Load Specifications (Sheet 2 of 2)

Parameter	Min	Max	Notes
Static compressive load from ILM load plate to processor IHS BOL	445 N [100 lbf]	712 N [160 lbf]	1, 4, 5, 7
Static compressive load from ILM load plate to processor IHS EOL	311 N [70 lbf]		
Dynamic Load	N/A	589 N [132 lbf]	1, 6
TIM2 Activation Pressure	137.9	kPa	
Pick and Place Cover Insertion / Removal force	N/A	6.2 N	
Load Lever actuation force	N/A	12.7 N in the vertical direction	

Notes:
1. These specifications apply to uniform compressive loading in a direction perpendicular to the IHS top surface.
2. These load limits defines load limits at the beginning of life (BOL) for the Intel's reference enabling solution in order to meet the socket End of Life (EOL) loading requirement. Load distribution between HS and ILM maybe different for custom ILM and heatsink designs. Intel will validate only the stated load distribution. Customer bears the responsibility of verifying the ILM and HS loads to ensure compliance with the package and socket loading as well as validating the socket reliability within their system implementation.
3. This is the minimum and maximum static force that can be applied by the heatsink and it's retention solution to maintain the interface between the heatsink and the IHS. This does not imply the Intel reference TIM is validated to these limits.
4. This minimum limit defines the compressive force required to electrically seat the processor onto the socket contacts.
5. This maximum load limit defines the allowable compressive load by the component.
6. Dynamic loading is defined as heatsink mass (0.6kg) x 50g load superimposed for an 11 ms duration average on the static load requirement.
7. Conditions must be satisfied at the beginning of life (BOL) and the loading system stiffness for non-reference designs need to meet a specific stiffness range to satisfy end of life loading requirements.

2.1.5 Independent Loading Mechanism (ILM)

The Independent Loading Mechanism (ILM) provides the force needed to seat the 2011-Land FCLGA package (that is, processor) onto the socket contacts. The ILM is physically separate from the socket body. The ILM consists of two major components, the ILM assembly and the back plate, that will be procured as a set from the enabled vendors.

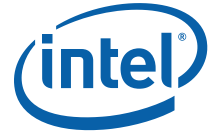
The installation of the ILM onto the motherboard will occur after the socket is surface mounted. Insulating materials integrated on both sub assemblies ensure that the PCB is protected from contact with the ILM components. The exact process step sequence within the board and system assembly is dependent on customer manufacturing preference and test flow. See the Manufacturing Advantage Service collateral for this platform for additional guidance.

The ILM has three critical functions:

- Deliver the force to seat the processor onto the socket contacts
- Distribute the resulting load evenly through the socket solder balls
- Ensure electrical integrity/performance of the socket and package.

2.1.5.1 ILM Overview

The ILM consists of two assemblies, ILM assembly and back plate. The ILM assembly is installed on the topside of the board via 4 captive fasteners that secure it to the backplate assembly on the opposite side of the board.



The ILM assembly consists of a top frame, load plate, and two load levers. These components together will provide the mechanism to apply uniform loading to the processor’s IHS.

The frame provides the hinge locations for the Active lever and Hinge levers. While secured to the backer plate, the ILM design ensures that the only features touching the board are the insulator at the bottom of the ILM frame and on the top of the back plate.

2.1.5.2 ILM Design

The ILM is targeted to optimize the space available on either side of the LGA 2011-1 socket requires. The ILM assembly consists of 6 major pieces as shown in Figure 2-15: hinge lever, active lever, load plate, ILM frame, ILM cover, and the captive fasteners.

Figure 2-14. ILM Assembly (Closed Orientation)

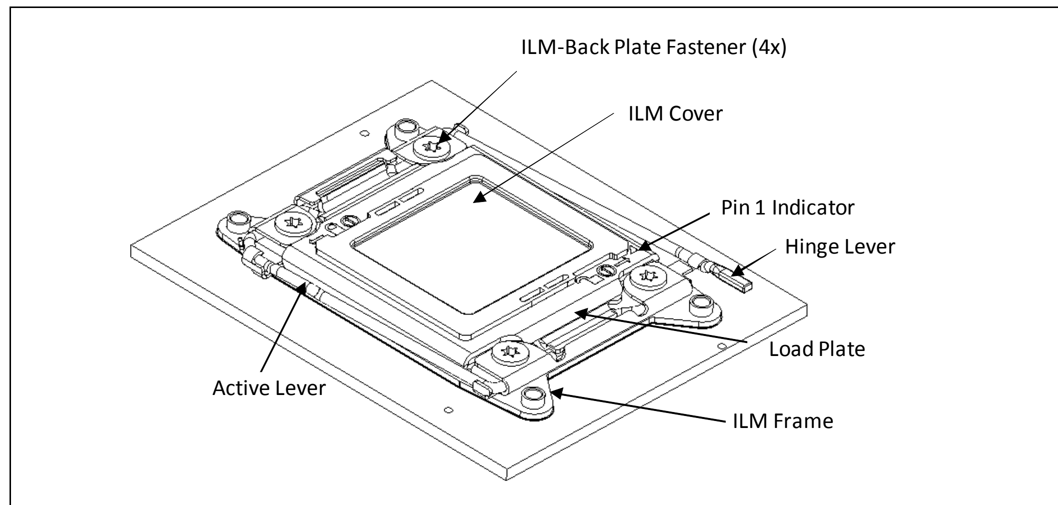
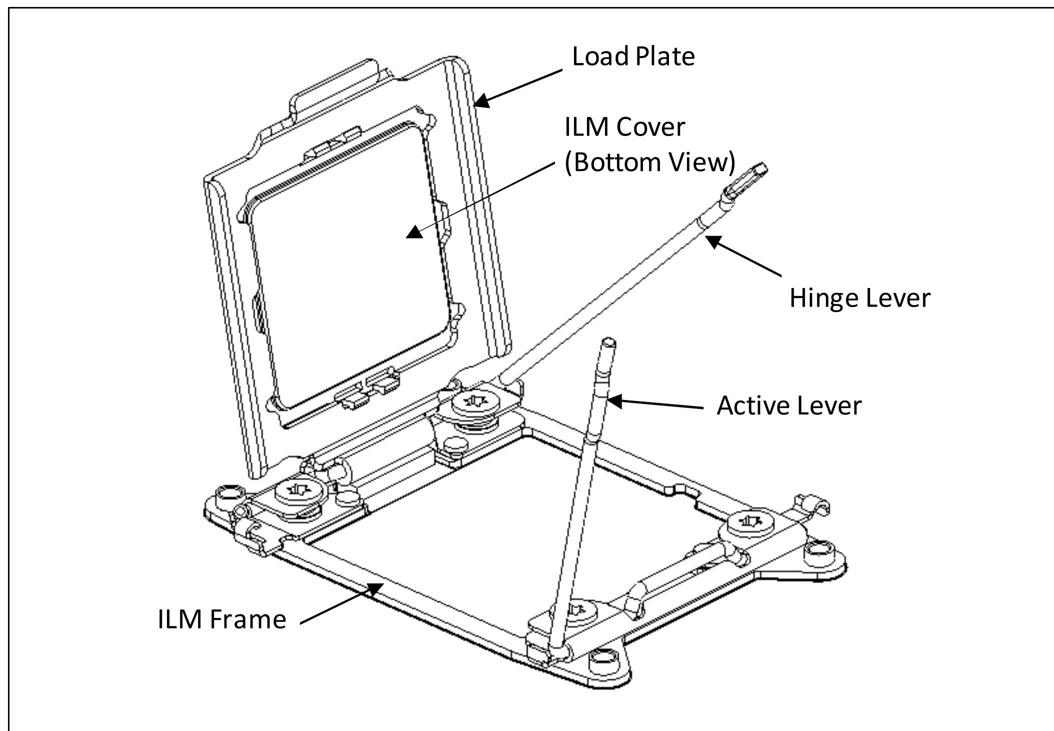


Figure 2-15. ILM Assembly (Open Orientation)



The hinge lever and active lever are designed to place equal force on both ends of the ILM load plate.The frame provides the hinge locations for the levers. The hinge lever connects the load plate to the frame. When closed, the load plate applies load onto the IHS at four loading zones. Four point loading contributes to minimizing package and socket warpage under non uniformly distributed load. The reaction force from closing the load plate is transmitted to the frame and through the captive fasteners to the back plate. Some of the load is passed through the socket body to the board inducing a slight compression on the solder joints.

ILM assembly attaches to motherboard via the back plate and is keyed to the socket body for proper orientation. ILM holds the heatsink and the back plate all together.

Thermal solution attaches directly to ILM frame as shown in Figure 2-16. Since heatsink attaches directly to ILM frame, only 4 holes (for ILM) on the motherboard is required.

Figure 2-16. ILM as a Universal Retention Mechanism

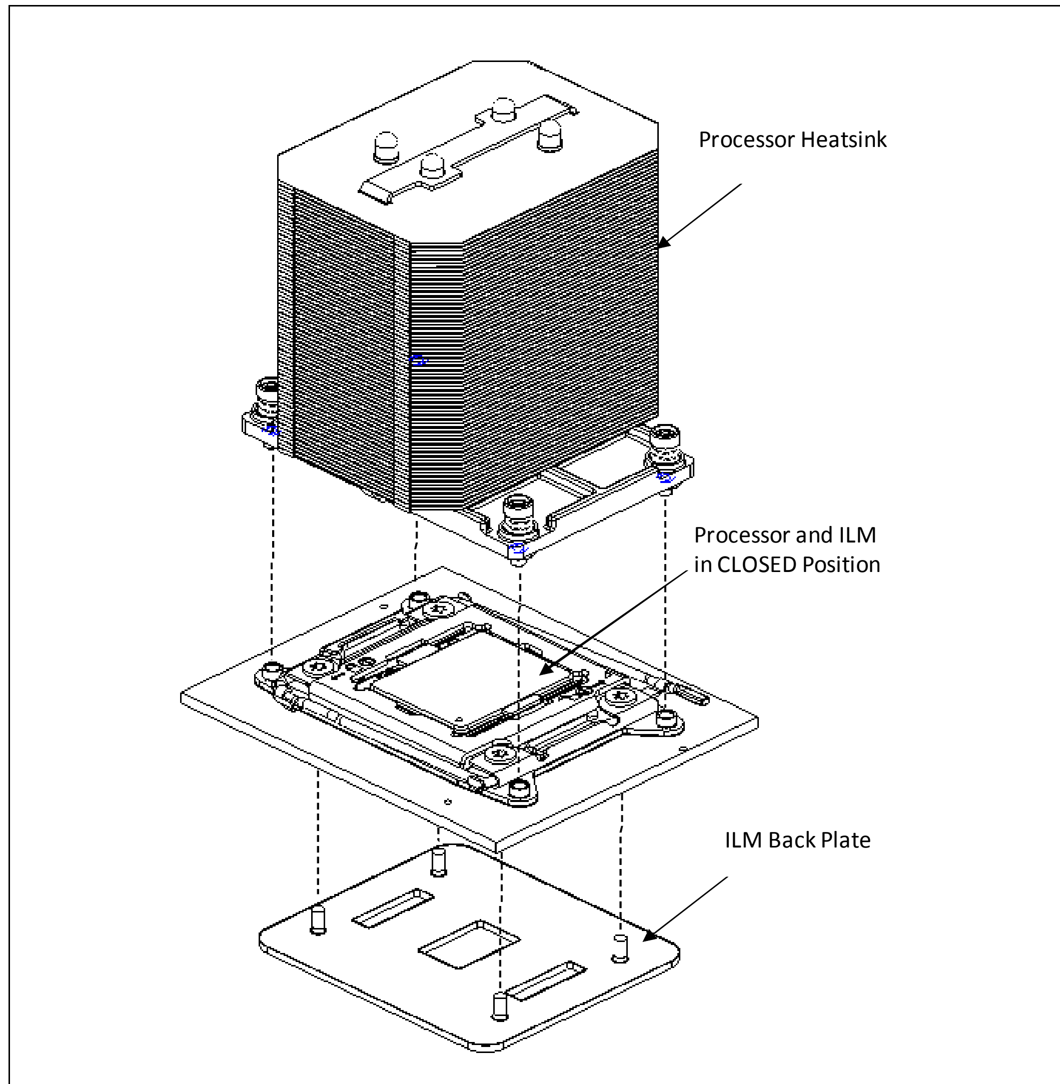
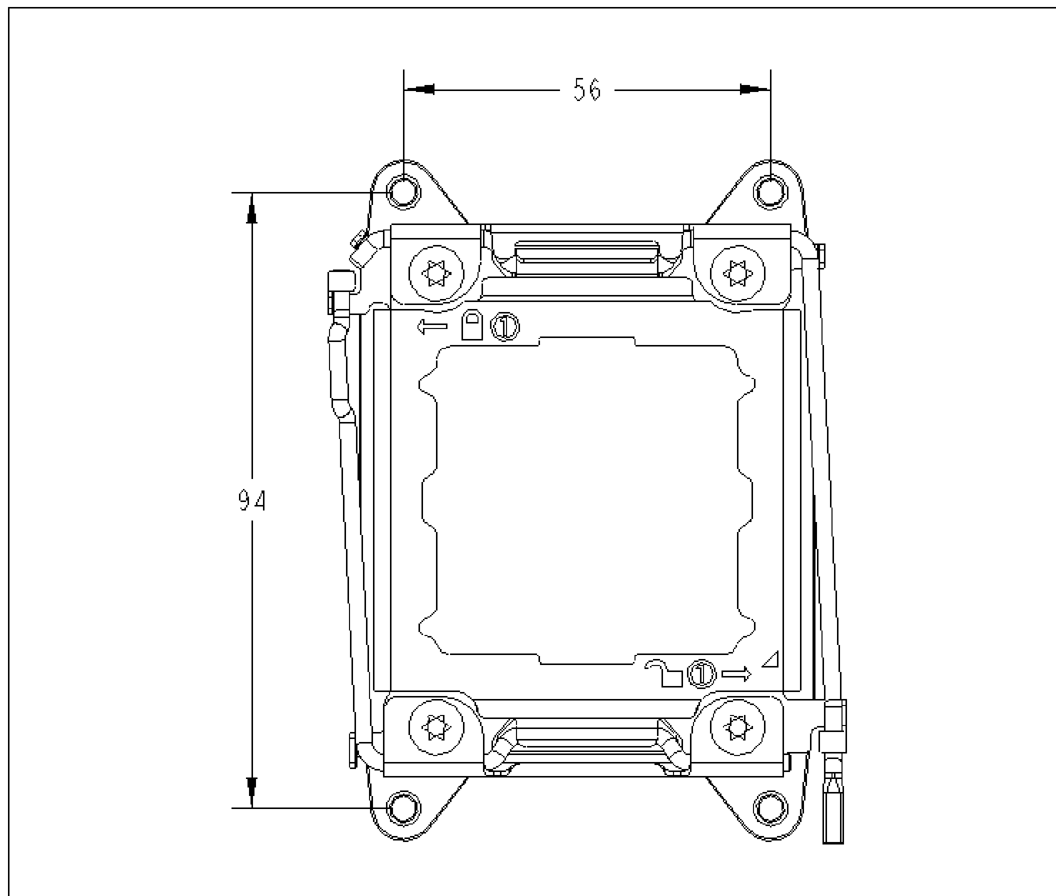


Figure 2-17. ILM Attachment Holes

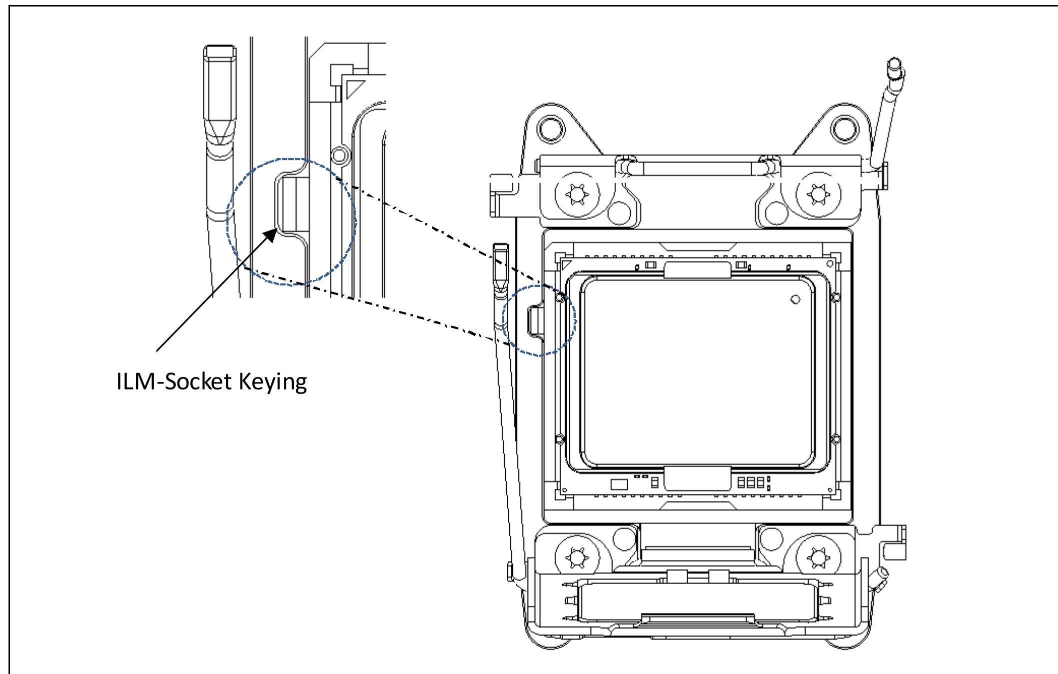


2.1.5.2.1 ILM Features

- Eliminates the motherboard thickness dependency from the stack-up because the heatsink attach points are located on the top side of the board.
- Nuts clamp the ILM frame to the board, providing good clamping and hence reduced board bending leading to more solder joint reliability.
- Socket keying ensures ILM is used with an intended socket, in this case LGA2011-1 socket.
- Dual lever helps in reducing the lever actuation force and enables applying uniformly distributed load onto the socket.
- Raised taps prevents levers from pulling out at the hinge locations.
- ILM interlocking enforces the levers opening and closing sequence.

Socket protrusion and ILM keying features prevent 180-degree rotation of ILM assembly with respect to socket, see Figure 2-18. This result in a specific orientation with respect to ILM lever.

Figure 2-18. ILM Keying



2.1.5.3 ILM Back Plate Design Overview

The backplate assembly consists of a supporting plate and captive standoffs. It provides rigidity to the system to ensure minimal board and socket deflection. Four externally threaded (male) inserts which are press fit into the backplate are for ILM attachment. Three cavities are located at the center of the plate to allow access to the baseboard test points and backside capacitors. An insulator is pre-applied to prevent shorting the board.

Table 2-8. ILM Back Plate Design Criteria

Parameter	Value	Note
Material thickness	2.2 ± 0.05 mm	To meet the PCB secondary side clearance requirement Does not include insulator thickness.
Insulator thickness	0.178 mm min	See insulator drawing for details
Material strength	Yield 250 MPa min Ultimate 300 MPa min	
Flatness	0.2mm	
PEM Insert Push-out Force	1110 N	
PEM Insert Torque Out	1.4 N-m	
Outside perimeter	90 x 78 mm min	Customizing beyond this perimeter of back plate should meet the reliability objectives.
Cavity (3x)	Center: 24.4 x 16 mm Sides (2x): 25.4 x 7 mm	See back plate mechanical drawings for details

Figure 2-19. Back Plate Assembly

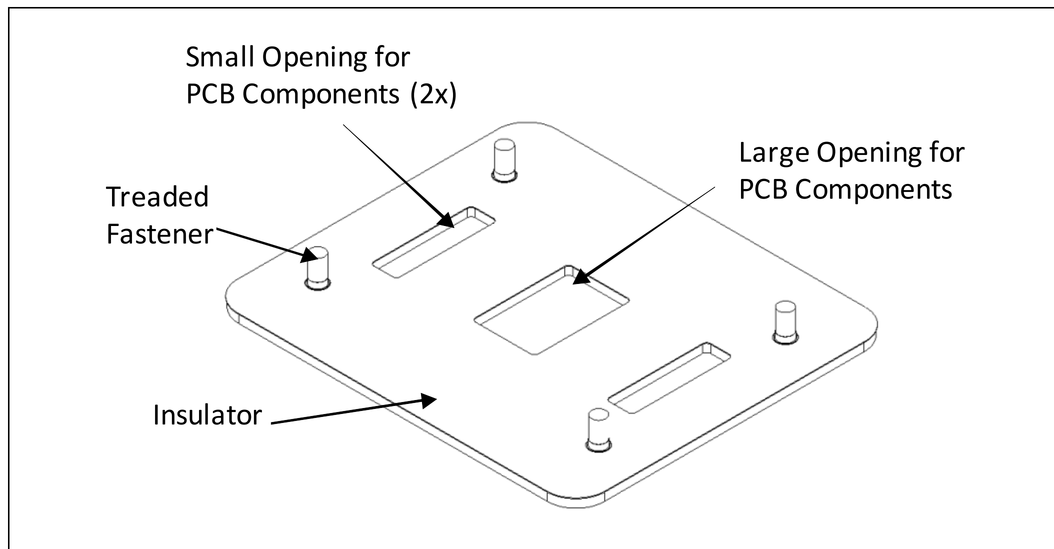


Table 2-9. ILM Assembly Component Thickness and Material

Component	Thickness (mm)	Material
ILM Frame	1.5	301 Stainless Steel
ILM Load plate	1.5	301 Stainless Steel
ILM Back plate	2.2	S50C Low Carbon Steel or equivalent.

All pieces in the ILM assembly, except the fasteners, are fabricated from stainless steel. The fasteners are fabricated from a high-carbon steel.

2.1.5.4 ILM Cover

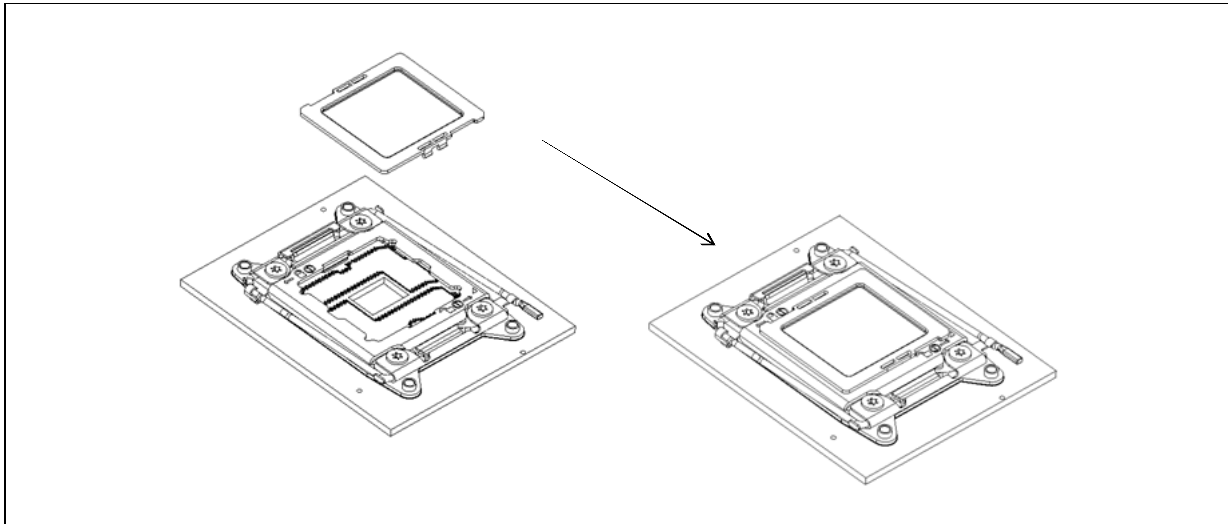
An ILM cover is defined to help mitigate damaging socket contacts, and to provide additional protection during the manufacturing and handling of the components. The ILM cover provides protection until a processor is installed.

The ILM cover *cannot* coexist with the LGA2011-1 socket Pick and Place cover. Meaning that the socket cap must be removed in order to close the ILM load plate.

2.1.5.5 ILM Cover Attach/Removal Force

The required force to remove the ILM cover shall not exceed 12.68 N when the load is applied by finger at the center of cover.

Figure 2-20. ILM Cover



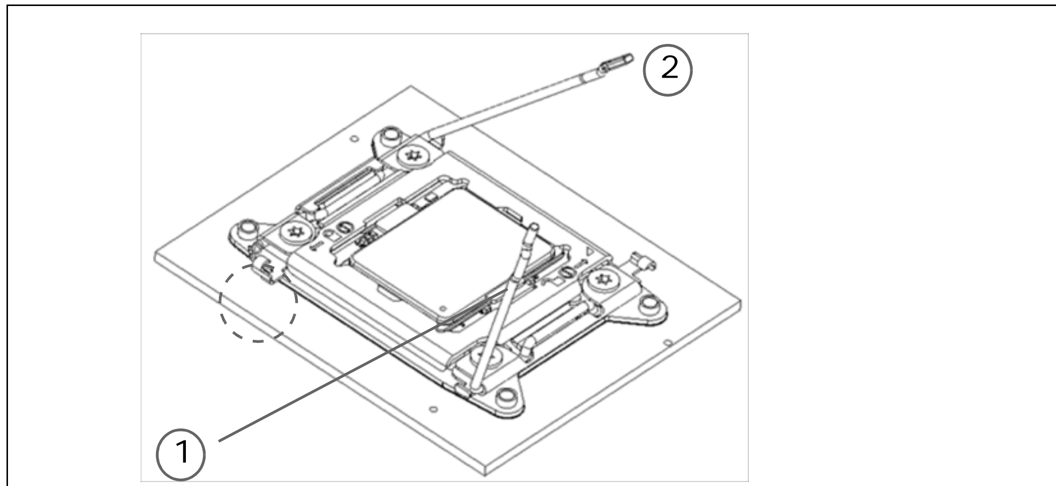
2.1.5.5.1 Lever Actuation/Release Forces

Nominal force to actuate the levers is 21 N at the point of typical finger placement.

2.1.5.5.2 Closing sequence

To ensure proper operation, the ILM design provides features to ensure that the proper closing sequence is followed. The load plate is placed in the down position, then the Active lever engages the load plate tongue and is latched first. This is then followed by the latching of the Hinge lever. This sequence is ensured by the sequencing tang on the Active lever, and the fact that the load plate angle will prevent engagement of the Hinge lever. See Figure 2-21 and Figure 2-22.

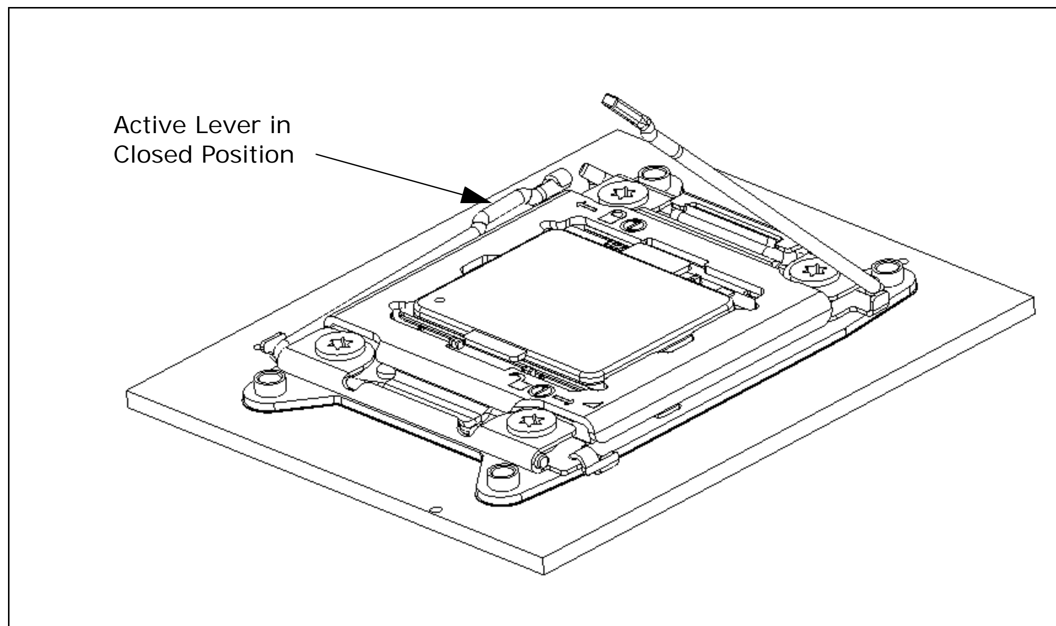
Figure 2-21. Preventing Hinge Lever from Latching First



ILM lever closing sequence is

1. Latch Active lever first
2. Close Hinge lever second.

Figure 2-22. ILM Lever Closing Sequence



2.1.5.5.3 Opening Sequence

For the opening sequence, the goal is to always open the Hinge lever first to prevent the load plate from springing open. The only option is to release the Hinge lever first. The Hinge lever in a closed position will block the Active lever from being unlatched. By opening the Hinge lever first, it creates clearance to open the Active lever.

Opening sequence is shown in Figure 2-23.

1. Open Hinge lever
2. Open Active lever

After opening Active lever, The Hinge lever tail could be pushed to lift the load plate up.

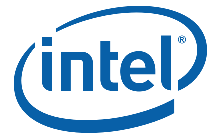
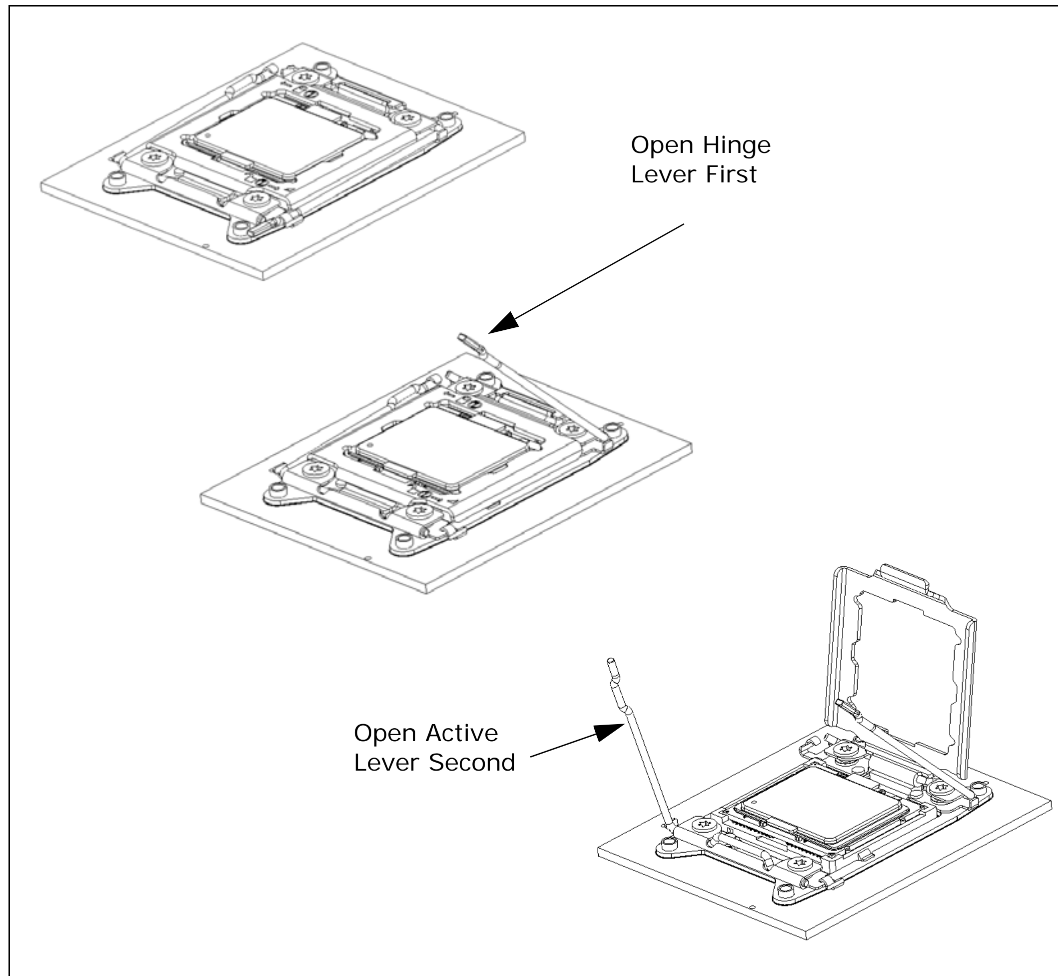


Figure 2-23. Opening Sequence

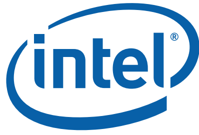


2.1.6 Heatsink Mechanical Requirements

The mass of the heatsink should not exceed 600 g. The heatsink mass limit and the use of a back plate have eliminated the need for Direct Chassis Attach retention in some implementations. Direct contact between back plate and chassis pan will help minimize board deflection during shock.

2.2 Thermal Specifications

The processor requires a thermal solution to maintain the die temperature within its operating limits. Any attempt to operate the processor outside these limits may result in permanent damage to the processor and potentially other components within the system, see "Storage Conditions Specifications" section of the processor datasheet. Maintaining the proper thermal environment is key to reliable, long-term system operation.



A complete solution includes both component and system level thermal management features. Component level thermal solutions can include active or passive heatsinks attached to the processor integrated heat spreader (IHS). Typical system level thermal solutions may consist of system fans combined with ducting and venting. This section provides data necessary for developing a complete thermal solution.

2.2.1 Thermal Management

To allow optimal operation and long-term reliability of Intel processor-based systems, the processor must remain within the minimum and maximum case temperature (T_{CASE}) specifications as defined by the applicable thermal profile. Thermal solutions not designed to provide sufficient thermal capability may affect the long-term reliability of the processor and system.

Intel® Xeon® Processor E7 2800/4800/8800 v2 Product Family implement a methodology for managing processor temperatures which is intended to support acoustic noise reduction through fan speed control and to assure processor reliability. Selection of the appropriate fan speed is based on the relative temperature data reported by the processor's Platform Environment Control Interface (PECI) as described in processor datasheet.

If the DTS value is less than $T_{CONTROL}$, then the case temperature is permitted to exceed the Thermal Profile, but the DTS value must remain at or below $T_{CONTROL}$.

For T_{CASE} implementations, if DTS is greater than $T_{CONTROL}$, then the case temperature must meet the T_{CASE} based Thermal Profiles.

For DTS implementations:

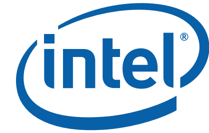
- T_{CASE} thermal profile can be ignored during processor run time.
- If DTS is greater than $T_{CONTROL}$ then follow DTS thermal profile specifications for fan speed optimization.

The temperature reported over PECI is always a negative value and represents a delta below the onset of thermal control circuit (TCC) activation, as indicated by PROCHOT_N (see Electrical Specification section of the process datasheet). Systems that implement fan speed control must be designed to use this data. Systems that do not alter the fan speed need to guarantee the case temperature meets the thermal profile specifications.

With single thermal profile, it is expected that the Thermal Control Circuit (TCC) would be activated for very brief periods of time when running the most power intensive applications. Utilization of a thermal solution that does not meet the thermal profile will violate the thermal specifications and may result in permanent damage to the processor. The upper point of the thermal profile consists of the Thermal Design Power (TDP) and the associated T_{CASE} value.

(x = TDP and y = TCASE_MAX @ TDP) represents a thermal solution design point. In actuality the processor case temperature will not reach this value due to TCC activation.

Intel recommends that complete thermal solution designs target the Thermal Design Power (TDP). The Adaptive Thermal Monitor feature is intended to help protect the processor in the event that an application exceeds the TDP recommendation for a sustained time period. To ensure maximum flexibility for future requirements, systems should be designed to the Flexible Motherboard (FMB) guidelines, even if a processor with lower power dissipation is currently planned. The Adaptive Thermal Monitor feature must be enabled for the processor to remain within its specifications.



2.2.2 T_{CASE} and DTS Based Thermal Specifications

To simplify compliance to thermal specifications at processor run time, processor has added a Digital Thermal Sensor (DTS) based thermal specification. Digital Thermal Sensor reports a relative die temperature as an offset from TCC activation temperature. T_{CASE} thermal based specifications are used for heatsink sizing and DTS based specs are used for acoustic and fan speed optimizations. For the Intel® Xeon® Processor E7 2800/4800/8800 v2 Product Family, firmware (for example, BMC or other platform management devices) will have DTS based specifications for all SKUs programmed by the customer. SKUs may share T_{CASE} thermal profiles but they will have separate T_{DTS} based thermal profiles.

The processor fan speed control is managed by comparing DTS thermal readings via PECI against the processor-specific fan speed control reference point, or Tcontrol. Both $T_{CONTROL}$ and DTS thermal readings are accessible via the processor PECI client. At a one time readout only, the Fan Speed Control firmware will read the following:

- IA32_TEMPERATURE_TARGET MSR
- Tcontrol via PECI - RdPkgConfig()
- TDP via PECI - RdPkgConfig()
- Core Count - RdPCIConfigLocal()

DTS PECI commands will also support DTS temperature data readings. Please see "DTS Temperature Data" section of the processor datasheet for PECI command details.

Table 2-10. Processor SKU Thermal Profiles

TDP	Core Count	Minimum T_{CASE} (°C)	Tcase_max @ TDP (°C)	Thermal Profile		$T_{CONTROL}$
				Tcase	DTS	
155 W	15	5	77	Y=0.184X+49.0	Y=0.258X+49.0	10
	10				Y=0.310X+49.0	15
	6				Y=0.361X+49.0	10
130 W	15	5	73	Y=0.185X+49.0	Y=0.262X+49.0	10
	12				Y=0.262X+49.0	10
105 W	15	5	68	Y=0.181X+49.0	Y=0.248X+49.0	10
	12				Y=0.248X+49.0	10
	10				Y=0.305X+49.0	10
	8				Y=0.305X+49.0	10
	6				Y=0.352X+49.0	10

Notes:
1. SKUs are subject to change. Please contact your Intel Field Representative to obtain the latest SKU information.
2. These values are specified at V_{CC_MAX} for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} at specified ICC.
3. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum T_{CASE}.
4. Tcase (Y) at a particular power is obtain by applying the thermal profile and replacing (X) with the desired power value. Tcase_max per specific SKU may be obtained by replacing (X) with the SKU TDP value.
5. These specifications are based on initial pre-silicon simulations, which will be updated as further characterization data becomes available.
6. Power specifications are defined at all VIDs. Processor may be delivered under multiple VIDs for each frequency.
7. FMB, or Flexible Motherboard, guidelines provide a design target for meeting all planned processor frequency requirements.
8. Some processor units may be tested to lower TDP and the IA32_TEMPERATURE_TARGET MSR will be aligned to that lower TDP.

9. Minimum Tcase represents the lowest processor operating temperature.

2.2.3 Thermal Metrology

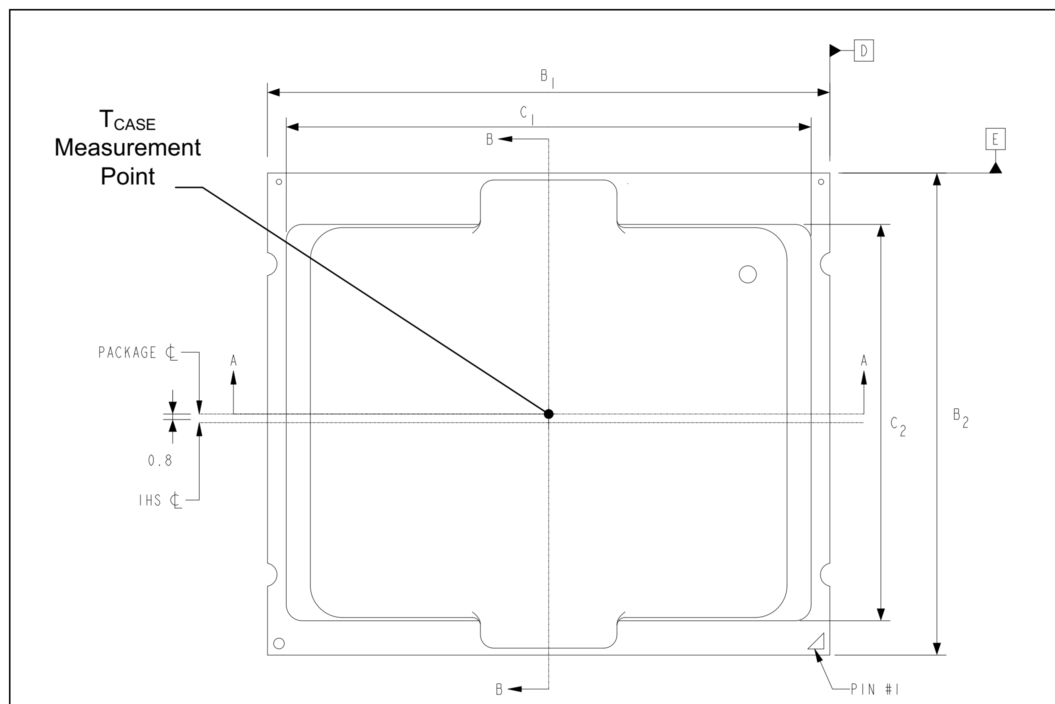
2.2.3.1 Case Temperature

The minimum and maximum case temperatures (T_{CASE}) specified in Table 2-10 are measured at the geometric center of the processor substrate on top of the processor integrated heat spreader (IHS).

Figure 2-24 contains dimensions for the thermocouple location on the processor package. Note that thermocouple location is centered with respect to the processor package substrate, but is offset with respect to center of IHS. This is due to location offset between the IHS and package substrate. This is the recommended location for the placement of a thermocouple for case temperature measurement.

Multi-core processors may exhibit higher temperature on the IHS at the locations coinciding with the core locations. Because of the IHS thermal power spreading effect, delta temperature between the core location and IHS center may diminish at the lower power. Component thermal solution designers may utilize IHS power gradient at the core locations to optimize the processor cooling solution or to verify the thermal solution capability in meeting the processor thermal requirement.

Figure 2-24. Processor Package Thermocouple Location

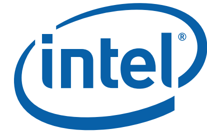


Note: See the processor package drawing for the feature dimensions.

2.2.3.2 DTS Based Thermal Specification

2.2.3.2.1 DTS Based Thermal Profile, Tcontrol and Margin

Calculation of the DTS based thermal specification is based on both Tcontrol and the DTS Based Thermal Profile (T_{DTS}):



$T_{DTS} = T_{LA} + \Psi_{pa} * P * F$

Where T_{LA} and Ψ_{pa} are the intercept and slope terms from the T_{DTS} equations. To implement the DTS based thermal specification, these equations must be programmed in firmware. Since the equations differ with processor SKU, SKUs can be identified by TDP and Core Count. The following PECI commands can be used to read TDP and Core Count from the processors:

TDP: RdPkgConfig(), Package Power SKU [LOW] Read, 14:0

Core Count: RdPCIConfigLocal()

Power (P) is calculated in Section 2.2.3.2.2. As power dynamically changes, the specification also changes, so power and T_{DTS} calculations are recommended every 1 second.

Correction factor (F) compensates for the error in power monitoring. The current estimate for F is 0.95.

The Tcontrol portion of the DTS based thermal specification is a one time calculation:

$T_{control_spec} = T_{LA} + \Psi_{pa} * TDP - Tcontrol + Tcontrol_offset$

Tcontrol is defined in Section 2.3.2.Tcontrol_offset is defined in Section 2.3.3

The final DTS based thermal specification is the maximum of both:

$T_{DTS_max} = max[T_{control_spec}, T_{DTS}]$

The margin (M) between the actual die temperature and the DTS based thermal specification is used in the fan speed control algorithm. When $M < 0$, increase fan speed. When $M > 0$, fan speed may decrease.

$M = T_{DTS_max} - Tsensor$

OR

$M = T_{DTS_ave} – Tsensor$

Tsensor represents the absolute temperature of the processor as power changes:

Tsensor = TEMPERATURE_TARGET + DTS

T_{DTS_ave} is defined in Section 2.2.3.2.3.

TEMPERATURE_TARGET, the temperature at which the processor thermal control circuit activates, is a one time PECI readout: RdPkgConfig(), Temperature Target Read, 23:16.

DTS, the relative temperature from thermal control circuit activation, is negative by definition, and changes instantaneously. DTS command info is given in Section 2.3.2.

2.2.3.2.2 Power Calculation

To implement DTS based thermal specification, average power over time must be calculated:

$$P = (E2 - E1) / (t2 - t1)$$

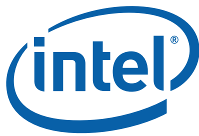
Where:

t1 = time stamp 1

t2 = time stamp 2

E1 = Energy readout at time t1

E2 = Energy readout at time t2



The recommended time interval between energy readings is 1 second. This helps ensure the power calculation is accurate by making the error between time stamps small as compared to the duration between time stamps.

The PECI command for energy is RdPkgConfig(), the service is called Accumulated CPU Energy, the bit numbers 31:0.

2.2.3.2.3 Averaging the DTS Based Thermal Specification

Averaging the DTS Based Thermal Specification helps keep the rate of change of the temperature specification on the same scale as the actual processor temperature, and helps avoid rapid changes in fan speed when power changes rapidly.

An exponential average of the specification can be calculated using a two time constant model:

$T_{DTS_f} = \alpha_f \times \Delta t \times T_{DTS_max} + T_{DTS_f_previous} \times (1- \alpha_f \times \Delta t)$

$T_{DTS_s} = \alpha_s \times \Delta t \times T_{DTS_max} + T_{DTS_s_previous} \times (1- \alpha_s \times \Delta t)$

$T_{DTS_ave} = C \times T_{DTS_f} \times (1-C) \times T_{DTS_s}$

Where:

T_{DTS_max} is the instantaneous spec

T_{DTS_f} and T_{DTS_s} are the fast and slow time averages

T_{DTS_ave} is the final two time constant average specification

α_f and α_s are the time constant coefficients

C is a scale factor

Δt is the scan rate and is recommended to be approximately 1 second

Table 2-11 below shows the initial coefficients recommended for averaging. These values may change per processor SKU. Customers should tune these coefficients based on their thermal solutions.

2.2.3.2.4 Absolute Processor Temperature

Intel does not test any third party software that reports absolute processor temperature. As such, Intel cannot recommend the use of software that claims this capability. Since there is part-to-part variation in the TCC (thermal control circuit) activation temperature, use of software that reports absolute temperature can be misleading.

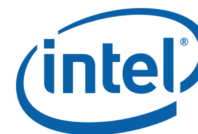
Please consult the BIOS Writer's Guide for details regarding the use of the IA32_TEMPERATURE_TARGET register which reports the minimum absolute temperature at which the TCC will be activated and PROCHOT# will be asserted. The IA32_TEMPERATURE_TARGET register may be different for each processor SKU.

2.2.3.2.5 Considerations for Follow-on Processor

The follow-on processor will have new capabilities as compared to Intel® Xeon® Processor E7 2800/4800/8800 v2 Product FamilySheet. As such, customers may want to write fan speed control algorithms that are tolerant of the follow-on processor's capabilities.

For the follow-on processor, the intercept and slope terms from the T_{DTS} equations (T_{LA}, Ψ_{pa}), as defined in Section 2.2.3.2.1, are stored in the processor. This allows margin (M) to be reported by the processor. The PECI command for margin (M) will be RdPkgConfig(), Index 10.

$M < 0$; gap to spec, fan speed must increase



M > 0; margin to spec, fan speed may decrease

Use of RdPkgConfig(), Index 10 with an Intel® Xeon® Processor E7 2800/4800/8800 v2 Product Family will return an illegal command.

For the follow-on processor, coefficients (α_f, α_s) and scale factor (C) as defined in Section 2.2.3.2.3, will be programmable and available via a register. If the two time constant average specification (T_{DTS_ave}) is not desired, set α_f = 1.0 and C = 1.0 to force $T_{DTS_ave} = T_{DTS_max}$.

For the follow-on processor, Tcontrol_offset as defined in Section 2.3.3, can be programmed via a register.

Table 2-11. Averaging Coefficients

Heatsink Performance	α_f (1/s)	α_s (1/s)	C	Comment
Low	1.0	0.05	0.32	based on typical processor
Medium	1.0	0.07	0.38	based on typical processor
High	1.0	0.29	0.49	based on typical processor
TTV Coefficients	1.0	0.07	0.55	based on TTV

2.2.4 Processor Thermal Solution Performance Targets

Processor heatsink design must comply with the Tcase based thermal profile. System that do not monitor the processor die temperature by monitoring the thermal sensor output must ensure processor cooling solution is capable of meeting the processor based Tcase spec. In some situations, implementation of DTS based thermal specification can reduce average fan power and improve acoustics as compared to the Tcase based thermal profile.

When all cores are active, a properly sized heatsink will be able to meet the processor thermal specification. When all cores are not active or when Intel® Turbo Boost Technology is active, attempting to comply with the DTS based thermal specification may drive system fans to increased speed. In such situations, the T_{CASE} temperature will be below the T_{CASE} based thermal profile by design.

Table 2-12 provides thermal boundary conditions and performance targets. These values serve as guide for designing a process compatible thermal solution.

Table 2-12. Heatsink Boundary Conditions and Performance Targets

Parameter	Value			Notes
TDP (W)	155	130	105	
T_{LA} (°C)	47			1
Ψ_{CA_MAX} (°C/W)	0.197	0.200	0.200	1,3,6,7
System height (form factor)	4U			4
Heatsink volumetric	Overall: 95x105.5x100 (WxLXH) Base 70x105.5x10.1 (WxLxH) Fins: 95x70 (WxL)			5
Heatsink Technology	Cu/Al base / Al fins / heatpipes			

Notes:
1. Heatsink Ψ_{CA_MAX} is for the highest processor core count within the specified power SKU.

2. Local ambient temperature of the air entering the heatsink.
3. Defined as (T_{CASE_MAX} - T_{LA}) / TDP
4. Reference system configuration. 1U = 1.75".
5. Dimensions of heatsink do not include socket or processor.
6. Heatsink performance value (Ψ_{CA_MAX}) includes TIM performance.
7. Values are preliminary and subject to change.

2.2.5 Socket Maximum Temperature

The power dissipated within the socket is a function of the current at the pin level and the effective pin resistance. To ensure socket long term reliability, Intel defines socket maximum temperature using a via on the underside of the motherboard. Exceeding the temperature guidance may result in socket body deformation, or increases in thermal and electrical resistance which can cause a thermal runaway and eventual electrical failure. The guidance for socket maximum temperature is listed below:

- Via temperature under socket < 75°C
- The specific via used for temperature measurement is located on the bottom of the motherboard between pins BC1 and BE1. See Figure 2-25.

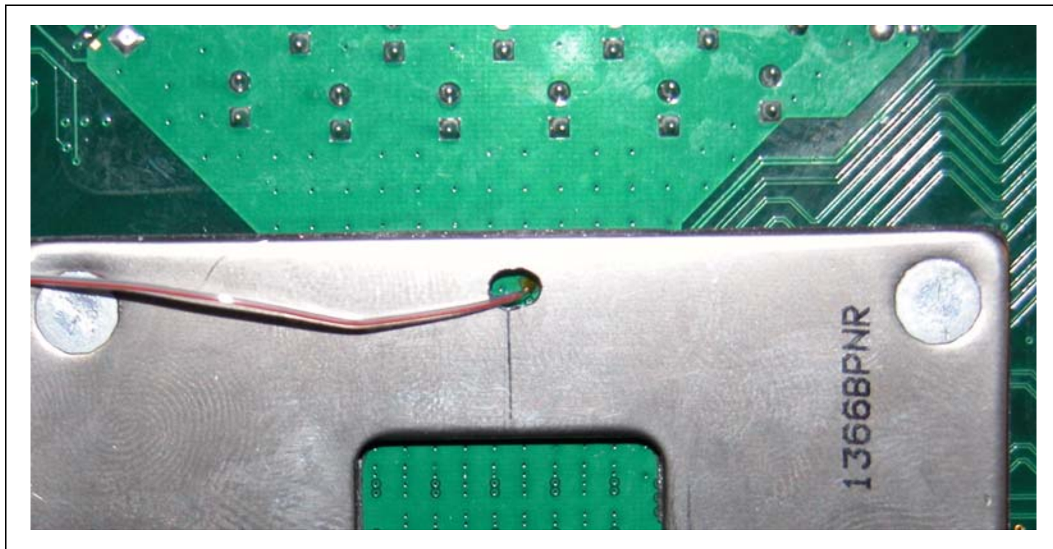
The socket maximum temperature is defined at Thermal Design Current (TDC). In addition, the heatsink performance targets and boundary conditions must be met to limit power dissipation through the socket.

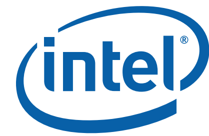
Note: The maximum allowable temperature is dependent on the use conditions for the LGA2011-1 socket. See Appendix B for more information on determining use conditions.

To measure via temperature:

1. Drill a hole through the back plate at the specific via defined above.
2. Thread a T-type thermocouple (36 - 40 gauge) through the hole and glue it into the specific via on the underside of the motherboard.
3. Once the glue dries, reinstall the back plate and measure the temperature.

Figure 2-25. Socket Temperature Measurement Location





2.2.6 Thermal Interface Material (TIM)

Applying thermal interface material between the processor IHS and the Heatsink base will improve the heat transfer between the IHS and the heatsink. Honeywell* PCM45F material is selected for use with the Intel reference heatsink design.

The recommended size ensures adequate coverage at the interface between the processor IHS and heatsink pedestal.

Table 2-13. TIM Specification

Parameter	Value	Unit	Notes
TIM Size	35x35x0.25	mm	Dimensions applies to Honeywell* PCM45F p/n: G34186
PCM45F Activation Load	125	N	Load required to meet min. TIM pressure (15 psi)

Refer to the TIM manufacturer's guidelines for specifications and handling instructions.

2.3 Thermal Design Guidelines

2.3.1 Intel® Turbo Boost Technology

Additional information regarding processor thermal features is contained in the processor datasheet.

Intel® Turbo Boost Technology available on certain processor SKUs, opportunistically, and automatically, allows the processor to run faster than the marked frequency if the part is operating below its power, temperature and current limits.

Heatsink performance (lower Ψ_{CA} as described in Table 2-12) is one of several factors that can impact the amount of Intel Turbo Boost Technology frequency benefit. Other factors are operating environment, workload and system design. Intel Turbo Boost Technology performance is also constrained by ICC, and VCC limits.

Increased IMON accuracy may provide more Intel Turbo Boost Technology benefit on TDP limited applications, as compared to lower Ψ_{CA}, as temperature is not typically the limiter for these workloads. See *VR12/IMVP7 Pulse Width Modulation (PWM) Product-Specification* and *VR12.5 Pulse Width Modulation (PWM) Haswell Input VR Enabling–Product Specification* for more information regarding IMON accuracy.

With Intel Turbo Boost Technology enabled, the processor may run more consistently at higher power levels (but still within TDP), and be more likely to operate above TCONTROL, as compared to when Intel Turbo Boost Technology is disabled. This may result in higher acoustics.

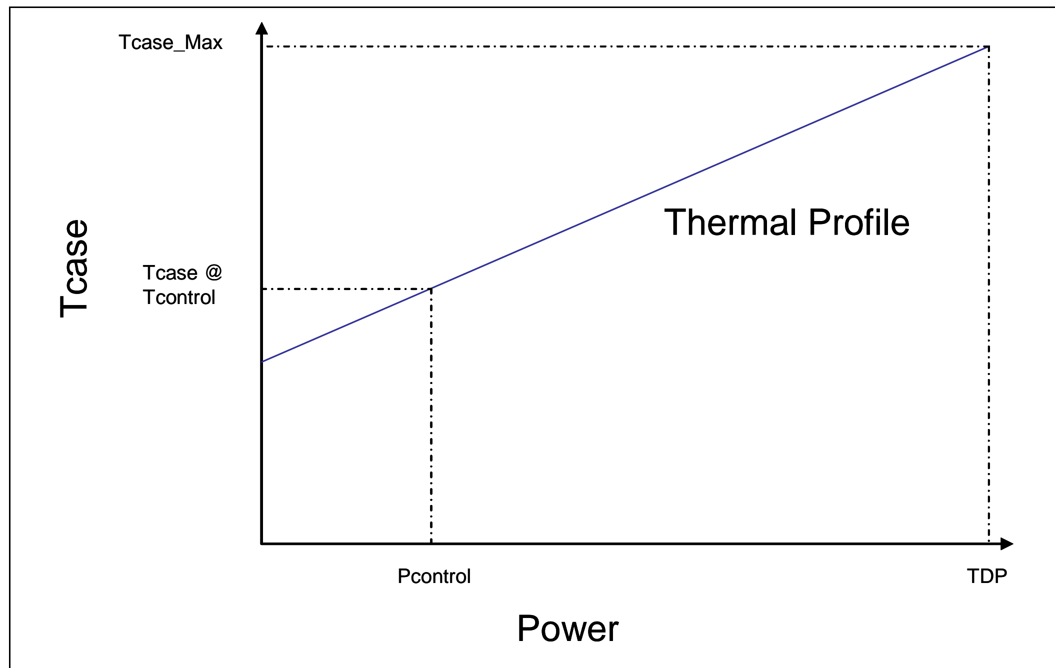
Intel Turbo Boost Technology is a feature available on certain processor SKUs that opportunistically, and automatically allow the processor to run faster than the marked frequency if all of the following conditions are met:

1. Processor operating at Base Frequency (that is, P1 P-state)
2. Power management not active (that is, not throttling)
3. Processor operating below its temperature limit (that is, DTS < 0)
4. Processor operating below its power and current limits (that is, < TDP and $< I_{CC_MAX}$).

2.3.2 Fan Speed Control

Fan speed control (FSC) techniques to reduce system-level acoustic noise are a common practice in server designs. The fan speed is one of the parameters that determines the amount of airflow provided to the thermal solution. Additionally, airflow is proportional to a thermal solution's performance, which consequently determines the T_{CASE} of the processor at a given power level. Because the T_{CASE} of a processor is an important parameter in determining the long-term reliability of a processor, the FSC implemented in a system directly correlates to the processor's ability to meet the Thermal Profile. For this purpose, the parameter called $T_{CONTROL}$, as explained in the datasheet, is to be used in FSC designs to ensure that the long-term reliability of the processor is met while keeping the system-level acoustic noise down. Figure 2-26 depicts the relationship between $T_{CONTROL}$ and FSC methodology.

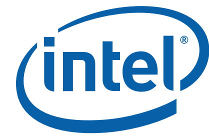
Figure 2-26. $T_{CONTROL}$ and Fan Speed Control



When DTS (Digital Temperature Sensor) value is less than Tcontrol, the thermal profile can be ignored. The DTS value is a relative temperature to PROCHOT which is the maximum allowable temperature before the thermal control circuit is activated. In this region, the DTS value can be utilized to not only ensure specification compliance but also to optimize fan speed control resulting in the lowest possible fan power and acoustics under any operating conditions. When DTS goes above Tcontrol, fan speed must increase to bring the sensor temperature below Tcontrol or to ensure compliance with the Tcase profile.

Table 2-14. Fan Speed Control, $T_{CONTROL}$ and DTS Relationship

Condition	FSC Scheme
DTS $\leq T_{CONTROL}$	FSC can adjust fan speed to maintain DTS $\leq T_{CONTROL}$ (low acoustic region).
DTS $> T_{CONTROL}$	FSC should adjust fan speed to keep T_{CASE} at or below the Thermal Profile specification (increased acoustic region).



The PECI temperature reading from the processor can be compared to this $T_{CONTROL}$ value. A fan speed control scheme can be implemented as described in Table 2-14 without compromising the long-term reliability of the processor.

The PECI command for DTS is GetTemp(). Though use of a sign bit, the value returned from PECI is negative.

The PECI command for $T_{CONTROL}$ is RdPkgConfig(), Temperature Target Read, 15:8. The value returned from PECI is unsigned (positive), however is negative by definition.

There are many different ways of implementing fan speed control, including FSC based on processor ambient temperature, FSC based on processor Digital Thermal Sensor (DTS) temperature, or a combination of the two. If FSC is based only on the processor ambient temperature, low acoustic targets can be achieved under low ambient temperature conditions. However, the acoustics cannot be optimized based on the behavior of the processor temperature. If FSC is based only on the Digital Thermal Sensor, sustained temperatures above $T_{CONTROL}$ drive fans to maximum RPM. If FSC is based both on the ambient and Digital Thermal Sensor, ambient temperature can be used to scale the fan RPM controlled by the Digital Thermal Sensor. This would result in an optimal acoustic performance. Regardless of which scheme is employed, system designers must ensure that the Thermal Profile specification is met when the processor Digital Thermal Sensor temperature exceeds the T_{CONTOL} value for a given processor.

2.3.3 Tcontrol Relief

Near launch, Intel may provide $T_{CONTROL}$ Relief, in other words provide $T_{CONTROL}$ values closer to 0, as compared to the factory configured $T_{CONTROL}$ values.

Factory configured $T_{CONTROL}$values are available in the appropriate Dear Customer Letter or may be extracted by issuing a Mailbox or an RDMSR instruction.

In some situations, use of $T_{CONTROL}$ Relief can reduce average fan power and improve acoustics. There are no plans to change Intel's specification or the factory configured $T_{CONTROL}$ values on individual processors.

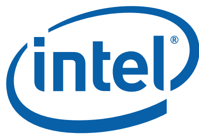
Implementing $T_{CONTROL}$ Relief is optional. To implement this relief, customers must rewrite the code and set the $T_{CONTROL}$ to the reduced values. Alternately, the factory configured $T_{CONTROL}$ values or a value between the factory configured and the relief guidance can still be used. Regardless of $T_{CONTROL}$ values used, BIOS needs to identify the processor type.

Implementation of $T_{CONTROL}$ Relief maintains Intel standards of reliability (based on modeling of the Intel Reference Design). Thermal Profile still applies. If PECI $>= T_{CONTROL}$ Relief, then the temperature must meet the T_{CASE} or the DTS based Thermal Profile.

In some cases, use of $T_{CONTROL}$ Relief as the trigger point for fan speed control may result in excessive TCC activation. To avoid this, the adjusted trigger point for fan speed control (FSC) is defined as:

$T_{control_FSC} = - T_{CONTROL} + T_{control_offset}$

$T_{control_offset}$ must be chosen such that $T_{control_FSC} < T_{CONTROL}$ Relief. As such, $T_{control_FSC}$ is an earlier trigger point for fan speed control, as compared to Tcontrol Relief, and can be interpreted as over cooling. When over cooling to $T_{control_FSC}$, margin as defined in Section 2.2.3.2.1 and Section 2.2.3.2.5 can be ignored. Overcooling to $T_{control_FSC}$ as compared to cooling to $T_{CONTROL}$ Relief:



- May increase frequency benefit from Intel Turbo Boost Technology.
- Will increase acoustics
- May result in lower wall power

Customers must characterize a $T_{control_offset}$ value for their system to meet frequency, acoustics, and wall power goals. $T_{control_offset}$ is programmable for the follow-on processor in this platform.

2.3.4 Thermal Excursion Power

Under fan failure or other anomalous thermal excursions, processor temperature (T_{CASE} or DTS) may exceed the thermal profile for a duration totaling less than 360 hours per year without affecting long term reliability (life) of the processor. For more typical thermal excursions, Thermal Monitor is expected to control the processor power level as long as conditions do not allow the T_{CASE} to exceed the temperature at which Thermal Control Circuit (TCC) activation initially occurred.

Under more severe anomalous thermal excursions when the processor temperature cannot be controlled at or below thermal profile by TCC activation, then data integrity is not assured. At some higher thresholds, THERMTRIP# will enable a shut down in an attempt to prevent permanent damage to the processor.

Compliance to anomalous thermal excursion can be evaluated by ensuring the processor T_{CASE} value does not exceed T_{CASE_MAX} at the anomalous power level for the environmental condition of interest, such as fan failure. This anomalous power level is equal to 75% of the TDP limit.

2.3.5 System Thermal Environmental Conditions

2.3.5.1 Ambient Temperature

The temperature of the inlet air entering the processor is referenced in this document as the ambient temperature (T_{LA}). This is not a system requirement. It is measured from the air upstream and in close vicinity to the processor cooling device. For the cooling systems, the ambient temperature is measured from the inlet air to the cooling device.

2.3.5.2 Airflow

Airflow should be provided by a system fan or blower in order to cool the processor package. See the recommended airflow rate in Table 2-15.

2.3.5.3 Pressure Drop

The value identified Table 2-15 is the allowable pressure drop in the airflow to ensure cooling requirements for the system components at downstream from the processor are met while achieving processor cooling requirements.

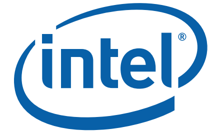


Table 2-15. Thermal Solution Performance Design Targets and Environment

Parameter	Maximum	Unit	Notes
T_{LA}	47	°C	This is the temperature at the processor cooling devices.
Pressure Drop (ΔP)	57.2 (0.23)	Pa (inch H_2O)	Total pressure drop across the processor heatsink fins with zero bypass.
Altitude	Sea-level		Heatsink designed at 0 meters
Airflow	15.8 (33.5)	l/s (CFM)	Airflow through the heatsink fins.

Thermal boundary conditions are applied in establishing the processor heatsink cooling solution.

2.3.6 Thermal Solution Performance Characterization

The case-to-local ambient Thermal Characterization Parameter (Ψ_{CA}) is defined by:

Equation 2-1. $\Psi_{CA} = (T_{CASE} - T_{LA}) / TDP$

Where:

- T_{CASE} = Processor case temperature (°C).
- T_{LA} = Local ambient temperature in chassis at processor (°C).
- **TDP** = TDP (W) assumes all power dissipates through the integrated heat spreader. This inexact assumption is convenient for heatsink design. TTVs are often used to dissipate TDP. Correction offsets account for differences in temperature distribution between processor and TTV.

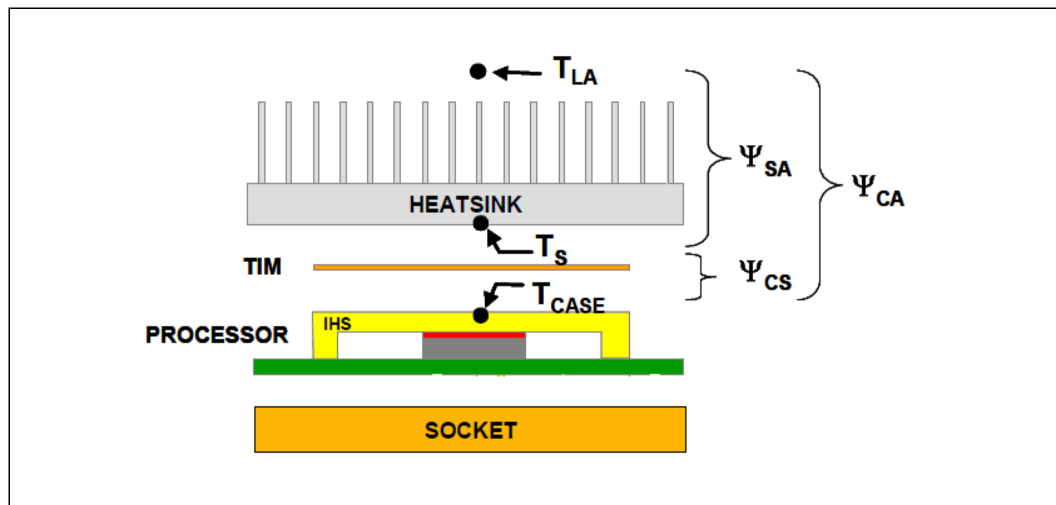
Equation 2-2. $\Psi_{CA} = \Psi_{CS} + \Psi_{SA}$

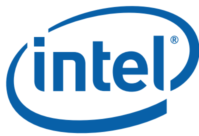
Where:

- Ψ_{CS} = Thermal characterization parameter of the TIM (°C/W) is dependent on the thermal conductivity and thickness of the TIM.
- Ψ_{SA} = Thermal characterization parameter from heatsink-to-local ambient (°C/W) is dependent on the thermal conductivity and geometry of the heatsink and dependent on the air velocity through the heatsink fins.

Figure 2-27 illustrates the thermal characterization parameters.

Figure 2-27. Processor Thermal Characterization Parameter Relationships





2.4 Design Considerations

2.4.1 System Design Considerations

When designing a thermally capable system, all critical components must be simultaneously considered. The responsible engineer must determine how each component will affect another, while ensuring target performance for all components. The term "target performance" is used because some components (for example, LRDIMM) have better performance, depending on how well they are cooled. The system design team must set these target performance goals during the design phase so that they can be achieved with the selected component layout.

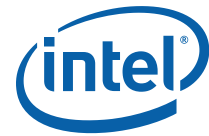
The location of components and their interaction must be considered during the layout phase. For example, memory that is heated by a processor will have worse performance than a layout that does not shadow memory behind a processor. Although the memory components have fixed thermal specifications, the performance management of RDIMM will limit memory throughput to ensure that the temperature limits are met. Consequently, a poorly cooled memory subsystem will have worse performance. The processor is somewhat different in that it enables full performance at all times, as defined by its specifications. The thermal engineer's responsibility is to ensure that each and every component meets its performance goals bounded by thermal and acoustic specifications but also computing performance such as memory throughput.

The thermal engineer directly influences the critical thermal parameters affecting processor cooling capability. For a given heatsink and retention solution, the layout and air-mover selection must ensure that all thermal specifications are met. It is desirable to drive chassis air temperature rise as low as reasonably possible while maximizing flow to each component. However, higher chassis temperature rise can be accommodated as long as the design implements a countering flow increase. These trade-offs are essential in designing a thermally capable system.

The number, size, and position of fans, vents, and other heat-generating components determine the component thermal performance and the resultant local ambient and airflow to the processor. The size and type (passive or active) of the thermal solution and the amount of system airflow can be traded off against each other to meet specific system design constraints.

In choosing the boundary conditions for a passive heatsink, the following methodology is recommended to ensure that a system can deliver the required boundary conditions. The Intel reference solution was developed by considering various system implementations to ensure that the boundary conditions were within reason.

- Conceptualize the layout with the system architect, including approximate volumetric constraints for the heatsink
- Select air movers that will deliver airflow and local temperatures within reason to all system components (also account for Trise across the air-movers)
- Create a Computational Fluid Dynamics (CFD) model of the system
- Run the CFD model with varying flow resistance representing the finned section of the heatsink
- Extract an effective air-mover curve from the CFD results
- Optimize the heatsink (fin thickness, quantity, base thickness, and so on) based on the effective air-mover curve



- Determine whether that optimized thermal solution can meet processor specifications
- Iterate through the previous steps to find a solution that will meet thermal requirements

To develop a reliable and cost-effective thermal solution, thermal characterization and simulation should be carried out at the entire system level, accounting for the thermal requirements of each component. In addition, acoustic noise constraints may limit the size, number, placement, and types of air-movers that can be used in a particular design. A number of collaterals, such as thermal and mechanical models, are made available to aid in performing system and component level thermal characterizations. See Section 1.3 for the listing of available collaterals.

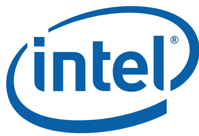
2.4.2 Heatsink Design Consideration

To remove the heat from the processor, three basic parameters should be considered:

- **The area of the surface on which the heat transfer takes place –** Without any enhancements, this is the surface of the processor package IHS. One method used to improve thermal performance is to attach a heatsink to the IHS. A heatsink can increase the effective heat transfer surface area by conducting heat out of the IHS and into the surrounding air through fins attached to the heatsink base.
- **The conduction path from the heat source to the heatsink fins –** Providing a direct conduction path from the heat source to the heatsink fins and selecting materials with higher thermal conductivity typically improves heatsink performance. The length, thickness, and conductivity of the conduction path from the heat source to the fins directly impact the thermal performance of the heatsink. In particular, the quality of the contact between the package IHS and the heatsink base has a higher impact on the overall thermal solution performance as processor cooling requirements become strict. Thermal interface material (TIM) is used to fill in the gap between the IHS and the bottom surface of the heatsink, and thereby improves the overall performance of the thermal stack-up (IHS-TIM-Heatsink). With extremely poor heatsink interface flatness or roughness, TIM may not adequately fill the gap. The TIM thermal performance depends on its thermal conductivity as well as the pressure load applied to it. Refer to Section 2.2.6 for further information on the TIM between the IHS and the heatsink base.
- **The heat transfer conditions on the surface upon which heat transfer takes place –** Convective heat transfer occurs between the airflow and the surface exposed to the flow. It is characterized by the local ambient temperature of the air, T_{LA}, and the local air velocity over the surface. The higher the air velocity over the surface, the more efficient the resulting cooling. The nature of the airflow can also enhance heat transfer via convection. Turbulent flow can provide improvement over laminar flow. In the case of a heatsink, the surface exposed to the flow includes the fin faces and the heatsink base.

An active heatsink typically incorporates a fan that helps manage the airflow through the heatsink.

Passive heatsink solutions require in-depth knowledge of the airflow in the chassis. Typically, passive heatsinks see slower air speed. Therefore, these heatsinks are typically larger (and heavier) than active heatsinks due to the increase in fin surface necessary to meet a required performance. As the heatsink fin density (the number of fins in a given cross-section) increases, the resistance to the airflow increases; it is more likely that the air will travel around the heatsink instead of through it, unless air bypass is carefully managed. Using air-ducting techniques to manage bypass area is an effective method for maximizing airflow through the heatsink fins.



2.4.3 Thermal Interface Material (TIM) Considerations

Thermal Interface Material between the processor IHS and the heatsink base is necessary to improve thermal conduction from the IHS to the heatsink. Many thermal interface materials can be pre-applied to the heatsink base prior to shipment from the heatsink supplier without the need for a separate TIM dispense or attachment process in the final assembly factory.

All thermal interface materials should be sized and positioned on the heatsink base in a way that ensures that the entire area is covered. It is important to compensate for heatsink-to-processor positional alignment when selecting the proper TIM size.

When pre-applied material is used, it is recommended to have a protective cover. Protective tape is not recommended as the TIM could be damaged during its removal step.

Thermal performance usually degrades over the life of the assembly and this degradation needs to be accounted for in the thermal performance. Degradation can be caused by shipping and handling, environmental temperature, humidity conditions, load relaxation over time, temperature cycling or material changes (most notably in the TIM) over time. For this reason, the measured T_{CASE} value of a given processor may increase over time, depending on the type of TIM material.

2.4.4 Mechanical Design Considerations

Any thermal mechanical design using some of the reference components in combination with any other thermal mechanical solution needs to be fully validated according to the customer criteria. Also, if customer thermal mechanical validation criteria differ from the Intel criteria, the reference solution should be validated against the customer criteria.

2.4.4.1 Components Volumetric

The baseboard keep-out zones on the primary and secondary sides and height restrictions under the enabling component region are shown in detail in Appendix G. The overall volumetric keep in zone encapsulates the processor, socket, and the entire thermal/mechanical enabling assembly.

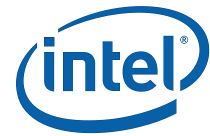
2.4.4.2 Components Mass

The Static Compressive Load should also be considered in dynamic assessments.

Direct contact between back plate and chassis pan will usually help minimize board deflection during shock.

Table 2-16. Socket and Retention Component Mass

Component	Mass
Socket Body, Contacts and PnP Cover	25[1]g
Narrow ILM Assembly	79g
Backplate	84g
Heatsink	600g
ILM Assembly	82g



2.4.4.3 Package/Socket Stack-up Height

Table 2-17 provides the stack-up height of a processor in the 2011-1-land LGA package and LGA2011-1 socket with the ILM closed and the processor fully seated in the socket.

Table 2-17. 2011-land Package and LGA2011-1 Socket Stack-up Height

Description	Height
Integrated Stackup Height (mm) From Top of Board to Top of IHS (Accounting for Intel Xeon processor E7-2800/4800/8800 V2 product family and future socket compatible processor package heights)	8.091 ± 0.221 mm
Integrated Stackup Height (mm) From Top of Board to Top of IHS (Intel Xeon processor E7-2800/4800/8800 V2 product family only)	8.051 ± 0.200 mm

Notes:
1. This data is provided for information only, and should be derived from: (a) the height of the socket seating plane above the motherboard after reflow, given in Appendix F, (b) the height of the package, from the package seating plane to the top of the IHS, and accounting for its nominal variation and tolerances that are given in the corresponding processor datasheet.
2. This value is a RSS calculation at 3 Sigma

2.4.5 PCB Design Consideration

2.4.5.1 Allowable Board Thickness

The components described in this document (namely ILM, back plate and heatsink) will support board thickness in the range of 2.36 - 3.3 mm (0.093" - 0.130"). Boards (PCBs) not within this range may require modifications to the back plate and heatsink retention.

2.4.5.2 Board Layout

Assumed 4x1 board configuration

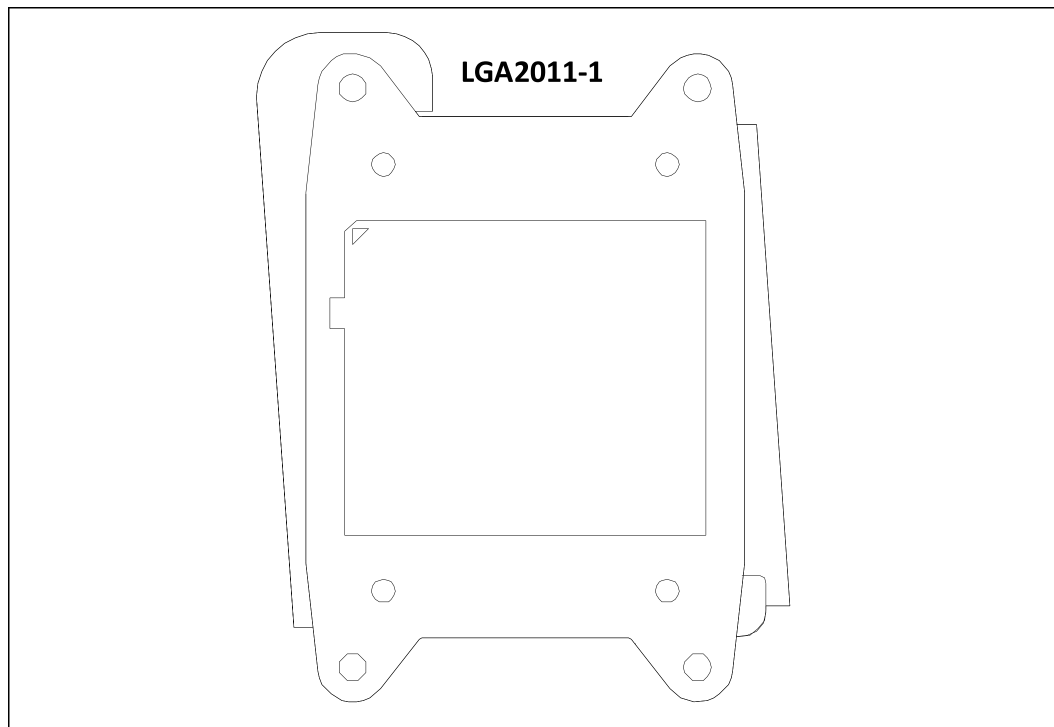
2.4.5.3 Board Keep-outs

Each of the components described in this document require an area beyond its physical size to accommodate components movement such as ILM levers. In identifying the board keep-outs one should also consider board and system assembly process and tools. As a reference, recommended board keep-outs drawings (PCB top and bottom side) for the LGA2011-1 socket, ILM, and heatsink are made available in Appendix G. PCB keep-outs includes ILM attach hole locations and sizes, components height limits in vicinity of the socket and ILM, as well as recommended area to allow access to ILM and socket for processor installation

2.4.5.4 Suggested Silkscreen Marking for Socket Identification

Intel is recommending that customers mark the socket name approximately where shown in Figure 2-28.

Figure 2-28. Suggested Board Marking



2.4.5.4.1 Socket-Socket Pitch

2.4.5.5 LGA2011-1 Socket Land Pattern Guidance

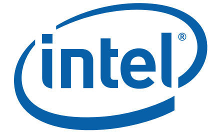
The land pattern guidance provided in this section applies to printed circuit board design. Recommendation for Printed Circuit Board (PCB) Land Patterns is to ensure solder joint reliability during dynamic stresses, often encountered during shipping and handling and hence to increase socket reliability.

2.4.5.6 Pad Type Recommendations

Intel defines two types of pad types based on how they are constructed. A metal defined (MD) pad is one where a pad is individually etched into the PCB with a minimum width trace exiting it. The solder mask defined (SMD) pad is typically a pad in a flood plane where the solder mask opening defines the pad size for soldering to the component.

In thermal cycling a MD pad has shown to be more robust than a SMD pad type. The solder mask that defines the SMD pad can create a sharp edge on the solder joint as the solder ball / paste conforms to the window created by the solder mask.

For certain failure modes the MD pad may not be as robust in shock and vibration (S&V). During S&V, the predominant failure mode for a MD pad in the corner of the BGA layout is pad craters and solder joint cracks. A corner MD pad can be made more robust and behave like a SMD pad by having a wide trace enter the pad. This trace should be 10 mil minimum but not to exceed the pad diameter and exit the pad at a 45 degree angle (parallel to the diagonal of the socket). During board flexure that results from shock & vibration a SMD pad is less susceptible to a crack initiating due to the larger surface area.



2.4.5.6.1 Socket Land Pattern

The land pattern for the LGA2011-1 socket is 40 mils hexagonal array. For CTF (Critical to Function) joints, the pad size will primarily be a circular Metal Defined (MD) pad and these pads should be designated as a Critical Dimension to the PCB vendors with a 17 mil ±1 mil tolerance. Some CTF pads will have a SMD Pad (20 x 17 mil). For additional pad configurations details including the NCTF (Non-Critical to Function) joints, see Section 2.4.5.5.

There is no round-off (conversion) error between socket pitch (1.016 mm) and board pitch (40 mil) as these values are equivalent.

Figure 2-29. LGA2011-1 Socket Land Pattern (Top View of Board)

45°

17 X 20 mil Oblong Partially SMD Pad Overview

Thick Trace

.010" Min

Soldermask

SRO Exposing Copper Pad

.017"

.020"

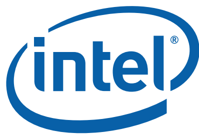


Table 2-18. Recommended Land Pattern for LGA2011-1 Socket

Pad Description	Recommendation Details
NCTF Pads - 43 pads in the four corners	• Oblong partially SMD Pad (20 x 17 mil) oriented at 45° to the socket edge. • The pad end closest to the center of the socket should have the Solder Resist Opening (SRO) of 17 ±1 mil. This is a critical to function dimension. • A thick trace ideally oriented at 45° toward the package corner and parallel to the long axis of the pad is required for optimal solder joint reliability (SJR) protection. • Pads affected: (SE) A53, B54, C55, D56, E57, F58, A51, B52, C53, G57, H58 (NE) CU1, CW1, CY2, DA3, DB4, DC5, DD6, DE7, DF8, DB2, DC3 (NW) E1, D2, C3, A5, G1, F2, E3, D4, C5, B6, A7 (SW) DF52, DE53, DD54, DC55, DB56, DA57, CY58, CV58, DE55, DB58
Critical to Function Pads along the socket sides.	• Oblong partially SMD Pad (20 x 17mil) oriented perpendicular to the socket edge. • The pad end closest to the center of the socket should have the SRO of 17±1 mil. This is a critical to function dimension. • A thick trace oriented parallel to the long axis of the pad is required for optimal SJR protection.
All other Critical to function pads.	• Circular MD • 17 ±1 mil Solder Resist Opening (SRO). This is a critical to function dimension

2.4.5.7 Strain Guidance

Intel provides manufacturing strain guidance commonly referred to as Board Flexure Initiative or BFI Strain Guidance. The BFI strain guidance apply only to transient bend conditions seen in board manufacturing assembly environment with no ILM, for example during In Circuit Test. BFI strain guidance limits do not apply once ILM is installed. It should be noted that any strain metrology is sensitive to boundary conditions.

Intel recommends the use of BFI to prevent solder joint defects from occurring in the test process. For additional guidance on BFI, see Manufacturing With Intel® Components - Strain Measurement for Circuit Board Assembly, also referred as BFI MAS (Manufacturing Advantage Services) and BFI STRAIN GUIDANCE SHEET (LGA2011-1 socket). Consult your Intel Customer Quality Engineer for additional guidance in setting up a BFI program in your factory.

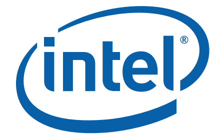
When the ILM is attached to the board, the boundary conditions change and the BFI strain limits are not applicable. The ILM, by design, increases stiffness in and around the socket and places the solder joints in compression. Intel does not support strain metrology with the ILM assembled

2.4.5.8 Board Deflection

Exceeding the maximum Board Deflection called out in Table 2-5, "Socket Loading and Deflection Specifications", may result in socket solder joint failure. Board deflection under the LGA2011-1 socket will be kept to an acceptable level by adhering to the following conditions:

1. Using the Intel reference ILM and back plate
2. Maintaining compliance to maximum load values

Placement of board-to-chassis mounting holes also impacts board deflection and resultant socket solder ball stress. Customers need to assess shock for their designs as their heatsink retention, heatsink mass and chassis mounting holes may vary.



Designs that do not meet the design objectives of the back plate or exceed the maximum Heatsink Static Compressive Load, should follow Board Deflection Measurement Methodology as outlined to assess risk to socket solder joint reliability.

2.5 Reference Thermal Solution

This section describes the Intel reference heatsink design and performance specifications in accordance with the Intel® Xeon® Processor E7 2800/4800/8800 v2 Product Family thermal and mechanical specifications. System form factor compatibility and thermal boundary conditions applied in designing the Intel reference heatsink are provided in Table 2-19.

2.5.1 Processor Heatsink Design Boundary Conditions

Heatsink thermal characteristics vary with change in its thermal environment such as, airflow rate, air temperature passing through (Tla), and the processor power dissipation. Only one set of boundary conditions is considered in design the reference solution. By varying the air flow rate, heatsink performance under various conditions is achievable.

Table 2-19. Processor Boundary Conditions and Performance Targets

Parameter	Value	Notes
Altitude, system ambient temp	Sea level, 35ºC	
TDP	105-165W	1
T_{LA}	47 ˚C	2
Ψ_{CA}	0.197 ºC/W	3, 4
Airflow	33.5 CFM @ 0.23″ ΔP	5
System height (form factor)	4U	6
Heatsink volumetric	95 x 105.5 x 100 mm	7
Thermal Interface Material (TIM)	Honeywell* PCM45F	8
Heatsink Mass	< 600g	

Notes:
1. Identifies processor power dissipation. Range is based on the processor SKUs. See processor thermal specification for support SKUs.
2. Local ambient temperature of the air entering the heatsink.
3. Heatsink performance target is based on the processor highest TDP SKU power dissipation, the system form factor, and environmental conditions.
4. Defined as (T_{CASE_MAX} - T_{LA}) / TDP
5. Airflow through the heatsink fins with zero bypass. Max target for pressure drop (ΔP) measured in inches H_2O.
6. Reference system configuration. 1U = 1.75″.
7. Dimensions of heatsink do not include socket or processor.
8. Thermal Interface Material is phase change material. See supplier specification for additional information.

2.5.2 Tower Heatsink Design

Intel reference heatsink design utilizes heatpipe technology with aluminum frame base with cooper slug and aluminum fins.

Figure 2-30. Processor Reference Heatsink Isometric View

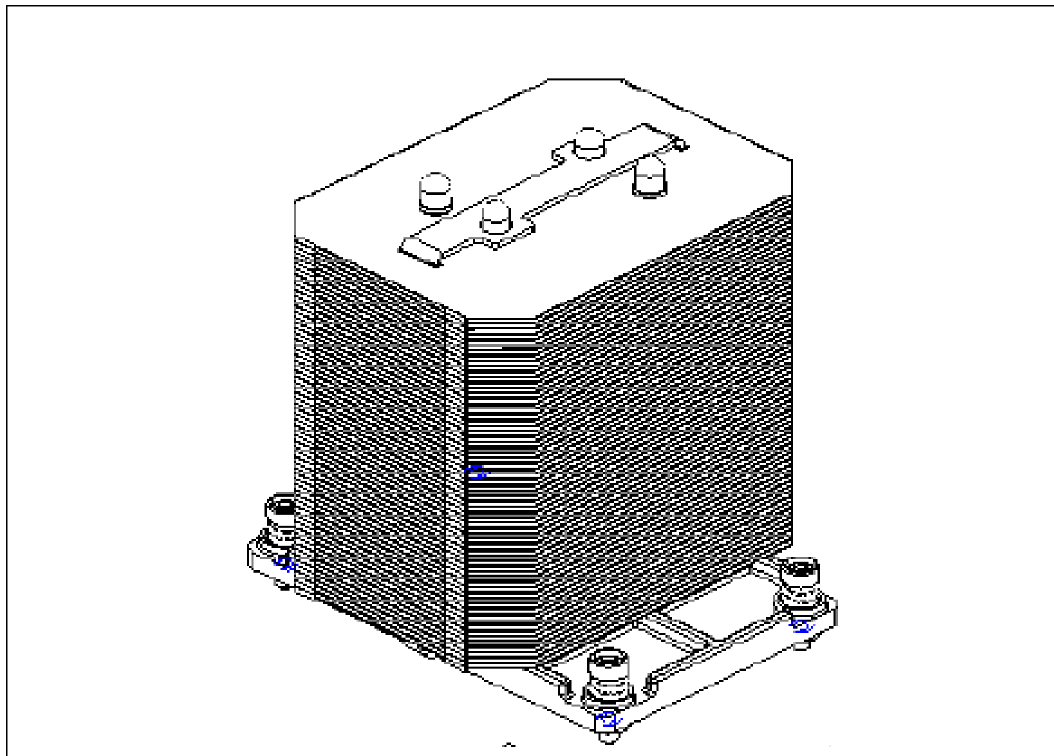


Table 2-20. Tower Heatsink Design

Parameter	Value	Notes
Heatsink technology	Cu/Al base / Al fins / heatpipes	
Heatpipe Quantity	4	
TIM Size	35 x 35 mm	
Fin Quantity		See heatsink drawing in Appendix G
Fin Size		See heatsink drawing in Appendix G
Weight	~580g	
Fin Support Mechanism	Yes	See heatsink drawing in Appendix G

2.5.3 Tower Heatsink Performance

Figure 2-31 shows thermal resistance (Ψ_{CA}) and pressure drop (ΔP) for the 4U heatsink versus the airflow. Best-fit equations are provided to prevent errors associated with reading the graph.

- $\Delta P = (2.106 \times 10^{-05}) * CFM^2 + (5.51 \times 10^{-03}) * CFM$
- $\Psi_{CA} = 0.1292 + 1.35 * CFM^{-0.9637}$

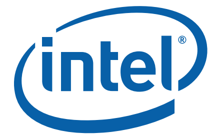
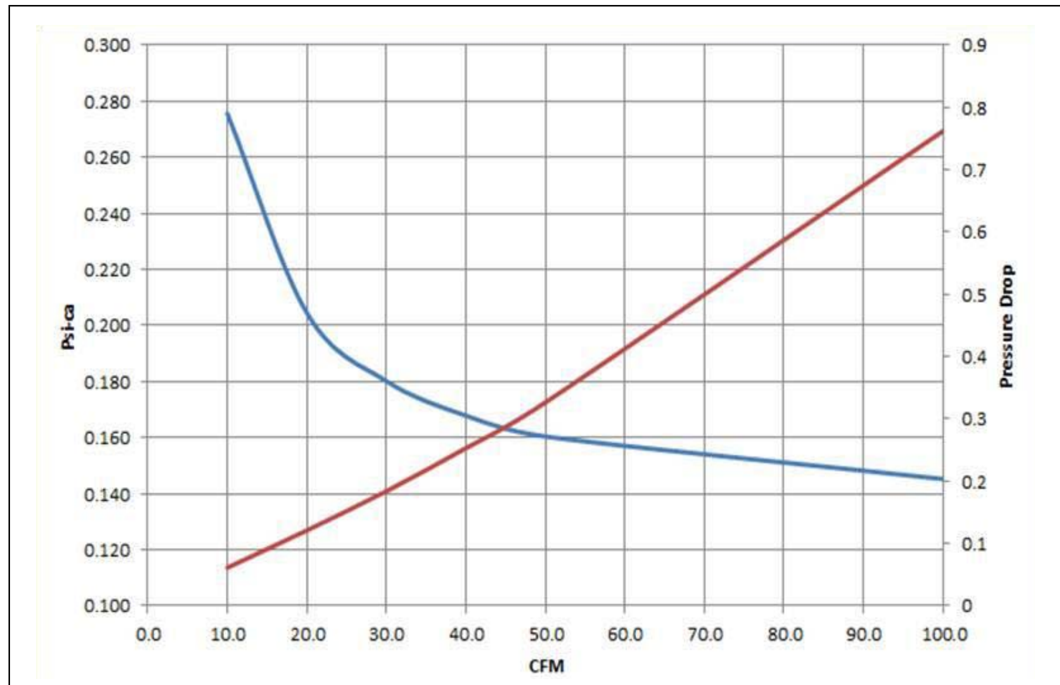


Figure 2-31. Tower Heatsink Performance Curves for 130W



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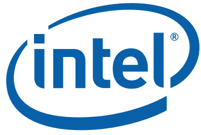
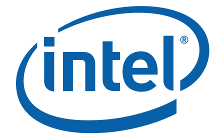




A Components Assembly Instructions

Reference Enabling components are designed for compatibility with the Intel Xeon processor E7-800/4800/8800 v2 product family and to ease board and system assembly. The processor enabling solution is illustrated in Figure A-1. Processor and its thermal/mechanical solution is installed onto a motherboard at the board or system assembly site. Assembly instructions described in this section assumes board and system assembly site maintain an controlled manufacturing environment. That is tools and processes are well controlled and maintained in achieve compliance with the processor and components specifications. Field upgrade and replacement is outside the scope of this section as it depends on system and board design.

The processor and its enabling components assembly are divided into three areas. First is the ILM installation onto the motherboard. The second is the processor installation, and last is the processor heatsink installation and securing it to the ILM.

Instructions provided hereon are an overview of the components assembly and installation onto a board or a system and are subject to change. *For additional details, see the components assembly instructional guide which can be obtain by contacting your Intel field engineer.*

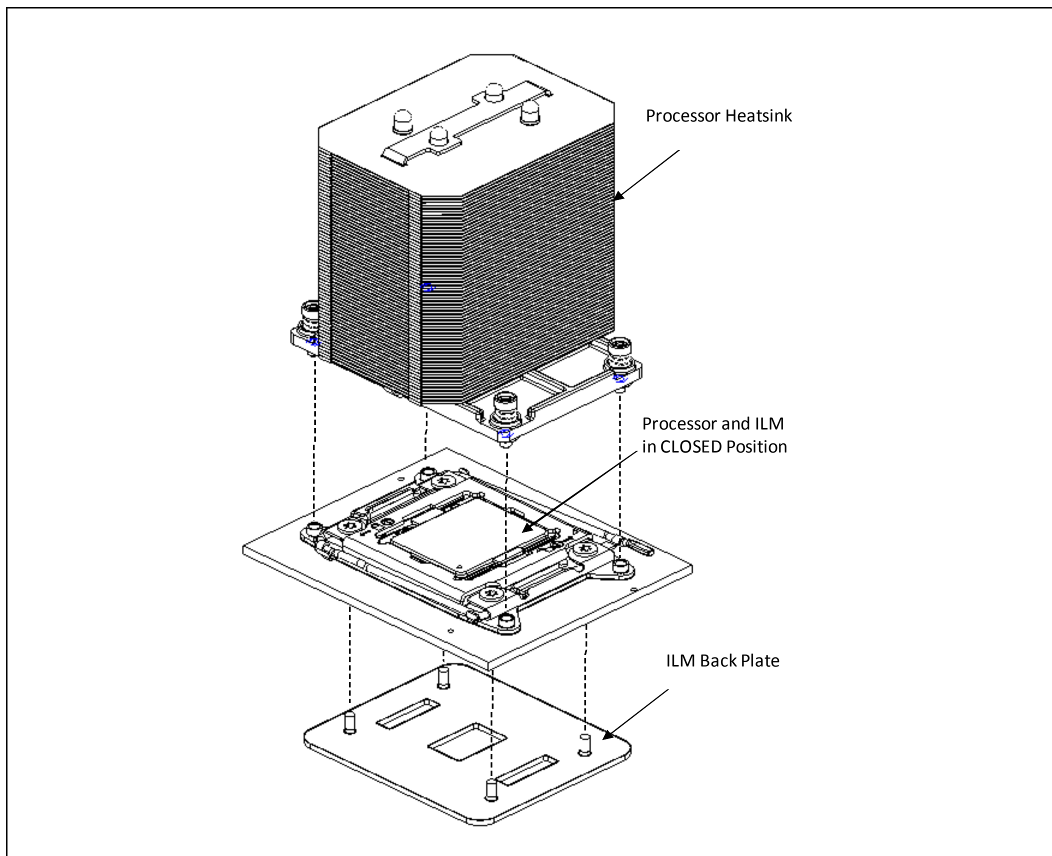
A.1 Processor Enabling Components

Processor enabling components consist of a set of components that enable integration of the processor with the board and system. Processor enabling components are listed in Table A-1 and are illustrated in Figure A-1.

Table A-1. Processor Enabling Components

Item	Description	Notes
1	Motherboard	Customer board with LGA2011-1 socket attached
2	ILM Back Plate	Assembled at the supplier to include: Insulator, and standoffs (4x)
3	ILM	Assembled at the supplier to include: Insulator and cover and the captive hardware
4	Processor	
5	Processor Heatsink	Processor Heatsink assembly includes: heatsink base with fins and the captive hardware and pre-applied thermal interface material

Figure A-1. Processor and Enabling Components Mechanical Assembly

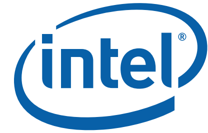


Note: The processor thermal mechanical solution assembly begins with surface mounting the LGA2011-1 socket onto the baseboard. The remaining steps presumed that the socket(s) have already been surface-mounted onto the board. Intel provides detailed instruction for lead free manufacturing of complex interconnects on the Intel Learning Network (www.learn.intel.com). For more detailed installation instructions as well as recommendations on board manufacturing, please download the Intel® Xeon® E7-2800/4800/8800 v2 product family-based Platform Manufacturing Advantage Service.

A.2 ILM Installation

- **Backplate**

The standoff pattern on the back plate also acts as a key-in feature. Align the back plate standoff pattern to the secondary side of baseboard's hole pattern before mating the back plate to the baseboard. While installing the back plate or placing the motherboard on the back plate, care should be taken to visually align them to prevent damaging the motherboard. Insert the back plate fasteners through the holes and hold the back plate against the board ensuring that all 4 studs have protruded through the board holes.



- **ILM**

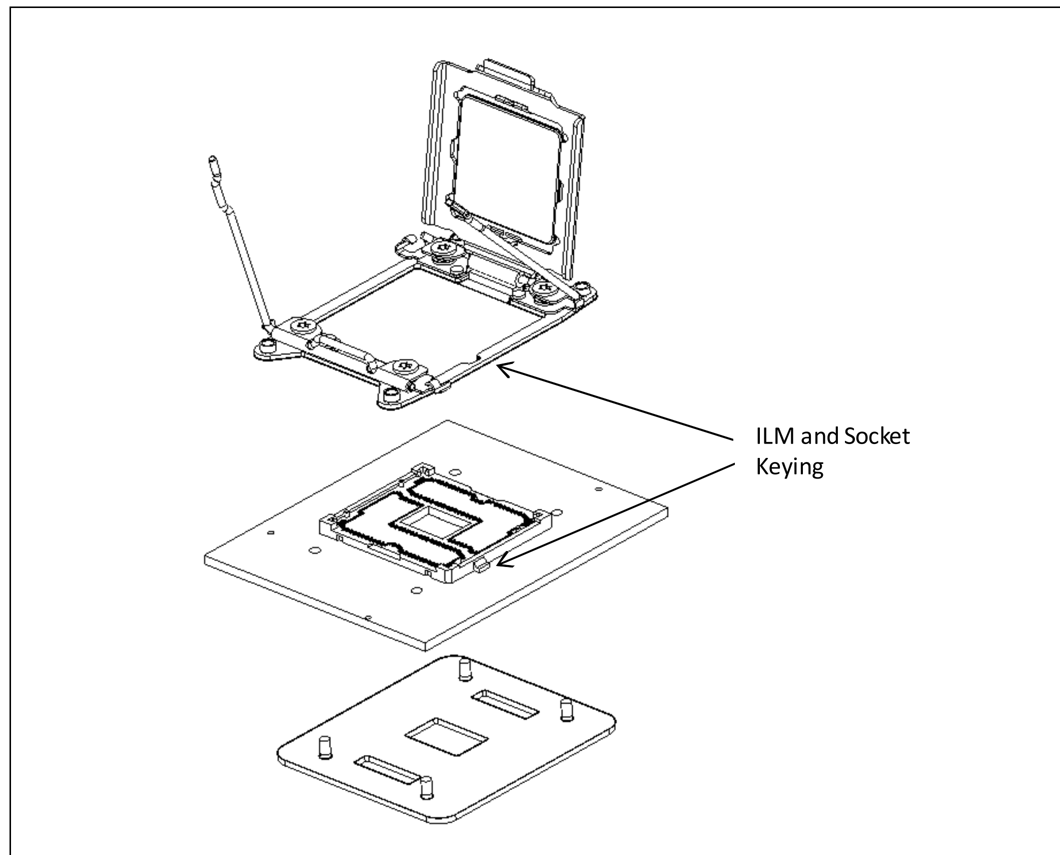
ILM is delivered with its cover in place. Verify the load plate is unlocked and the levers are in their latched position. This will prevent damage to the socket during the ILM installation.

The ILM fastener pattern also acts as a keying feature. Orient the ILM with respect to the baseboard such that the pin-1 indicator on the ILM is oriented in the same direction as the pin-1 on the socket.

Caution: Damage to the socket may occur if ILM is not properly oriented.

Align the ILM fastener pattern to the hole pattern on the baseboard. Verify the Torx-20 fasteners are resting on the back plate standoffs. Tighten the four (4) Torx-20 fasteners with the matching torque driver set to 0.9 N.m [~8 in-lbf]. Damage to the processor and its enabling components may result if the fasteners are not properly tightened. Verify that the ILM and the backer plate are properly installed. There should be a zero gap at the location of the ILM fasteners, and virtually no gap between the backer plate and the baseboard.

Figure A-2. ILM Installation onto Baseboard

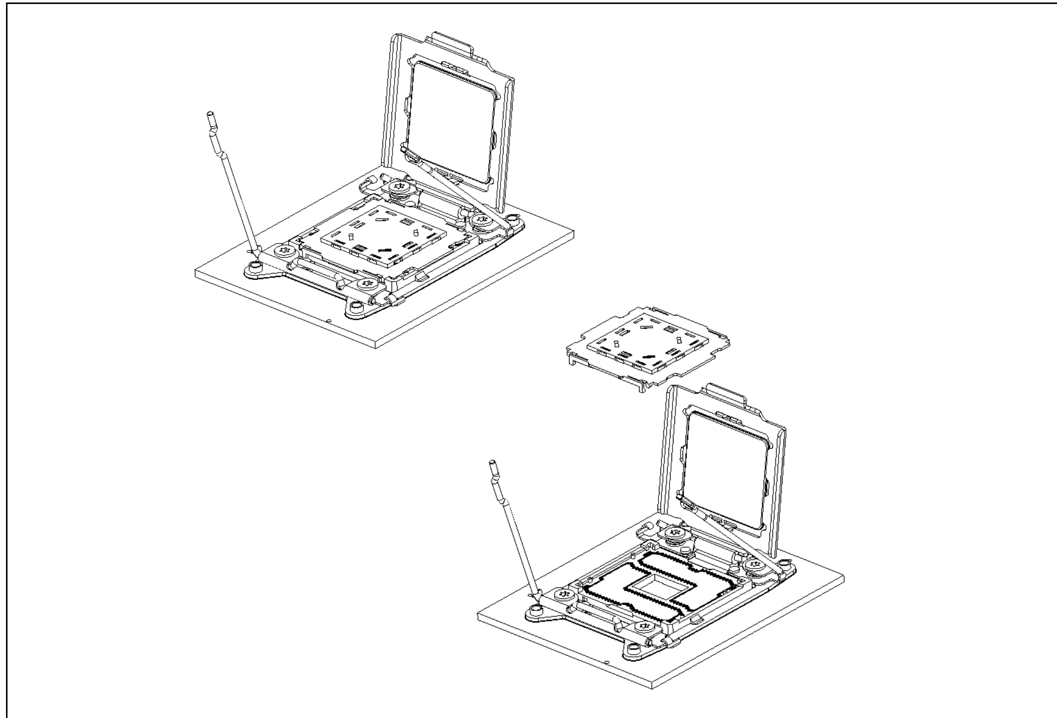


- **Socket Cover Removal**

Note: To access the socket Pick'n'Place cover, lift the ILM load plate. While the Active lever is unlatched and in its up position, press gently downward on the Hinge lever to aid in raising the load plate tab such that it can be easily be held and lifted. (This step will make it easier to lift the load plate and will potentially prevent damage to the socket contacts when they are exposed.) Carefully remove the socket Pick'n'Place cover per

socket handling instructions. The socket Pick'n'Place cover can be discarded. Essentially the ILM cover will perform the same function as the socket Pick'n'Place cover in protecting the socket contacts. With the ILM cover in place, close the load plate and secure it by actuating the Active lever and Hinge lever in that sequence until ready for the processor installation.

Figure A-3. Socket Pick and Place Cover Removal



A.3 Processor Installation

Open the ILM by releasing and lifting the ILM Active lever to its full open position. Then open the load plate by pushing down on the Hinge lever, this will cause the load plate tab to rise above the socket. Grasp the tab, only after it has risen away from the socket, open load plate to full open position.

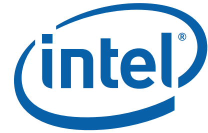
Carefully remove the socket cover to avoid damaging the socket contacts. Inspect the socket for visual defects such as contact damage or foreign materials.

Caution: Care should be taken in removing the cover. Improper removal may damage the socket contacts.

Warning: Do not install the processor if the socket contains defects, as it may damage the processor.

Grab and hold the processor along the right and left edges of the package to match socket finger cutouts (East - West edges). Care should be taken to ensure that the processor is properly oriented, that is the processor pin-1 faces the same direction as the socket pin-1, and that there are no contaminations or foreign material on the top or bottom LGA pads.

Keeping the processor horizontal, lower it gently into the socket with a purely vertical motion. Carefully place the processor on the socket and verify that it is seated properly. Four (4) side protrusions on the socket will prevent the package from resting flat on the



socket if it is not properly aligned to the socket. The processor should be inspected to ensure that it is properly seated on the socket, such that the guiding features are visible on all four keying sites.

Once the processor is properly seated on the socket, lower the ILM load plate, and completely actuate and latch the Active and Hinge lever in that order to load the entire assembly. Inspect the assembly to ensure that it is properly installed.

Figure A-4. Processor Installation Sequence

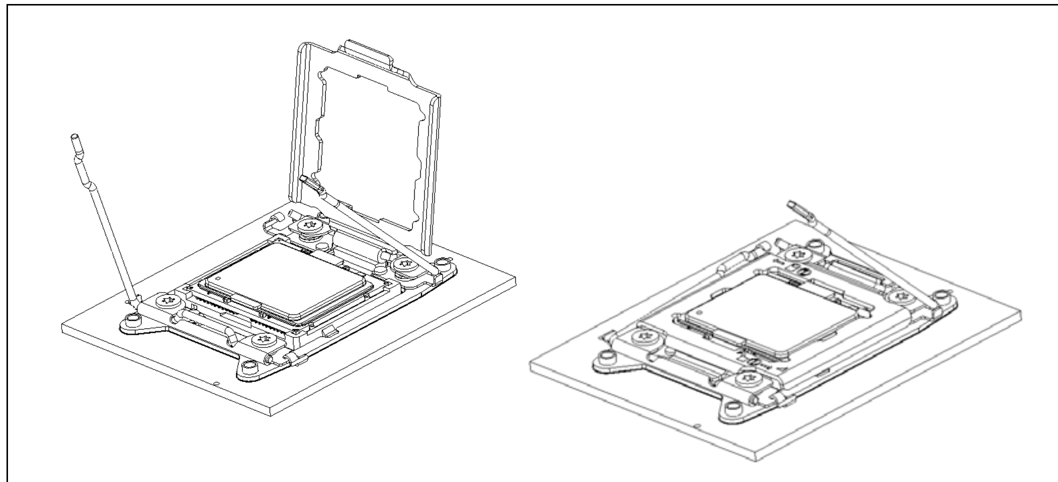
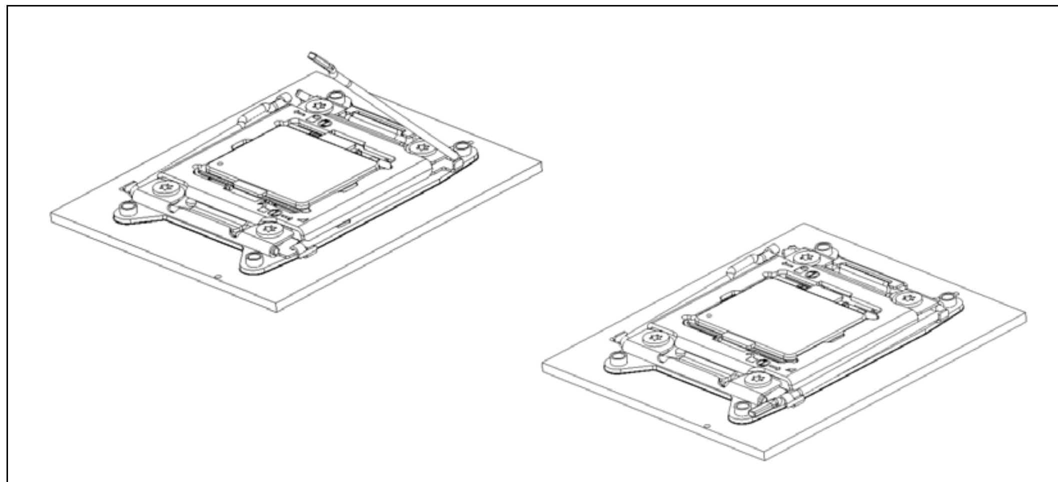


Figure A-5. Processor in Installed Position



A.4 Heatsink Installation

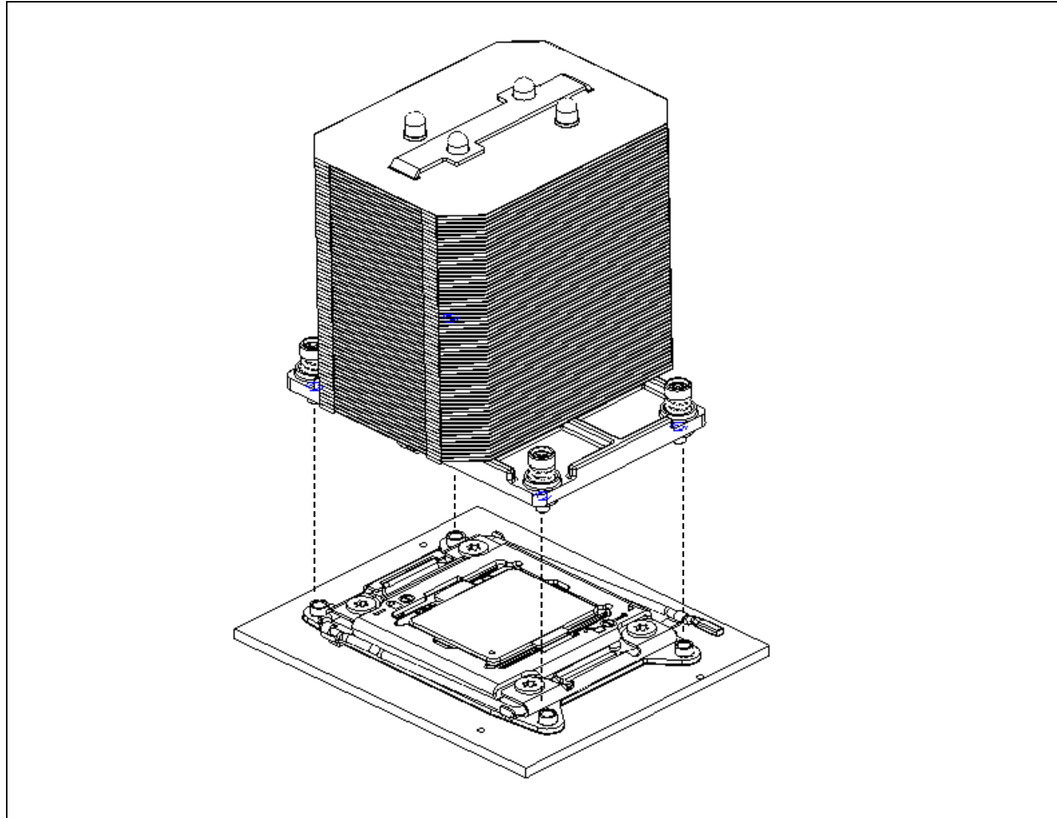
The assembly process for the reference heatsink begins with application of PCM45F TIM to improve conduction from the IHS. The recommended TIM to ensure full coverage of the IHS is 35x35 mm square.

Position the heatsink with the pre-applied TIM such that the heatsink fasteners are properly oriented and aligned to the ILM. While lowering the heatsink onto the IHS, align the four captive screws of the heatsink to the four threaded studs on the ILM frame.

Warning: Care should be taken not to touch the TIM during the assembly sequence as contamination or defect in TIM may impact its performance. Additionally, avoid exposing the socket or other components on the processor and the base board to the TIM as it may impact their performance and long term reliability.

Secure the heatsink to the ILM using a #2 Phillips torque driver tighten the four captive fasteners to 1 N-m (9 ±1 in-lbf). Verify that the heatsink is properly seated and secured to the ILM.

Figure A-6. Heatsink Installation



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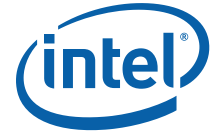


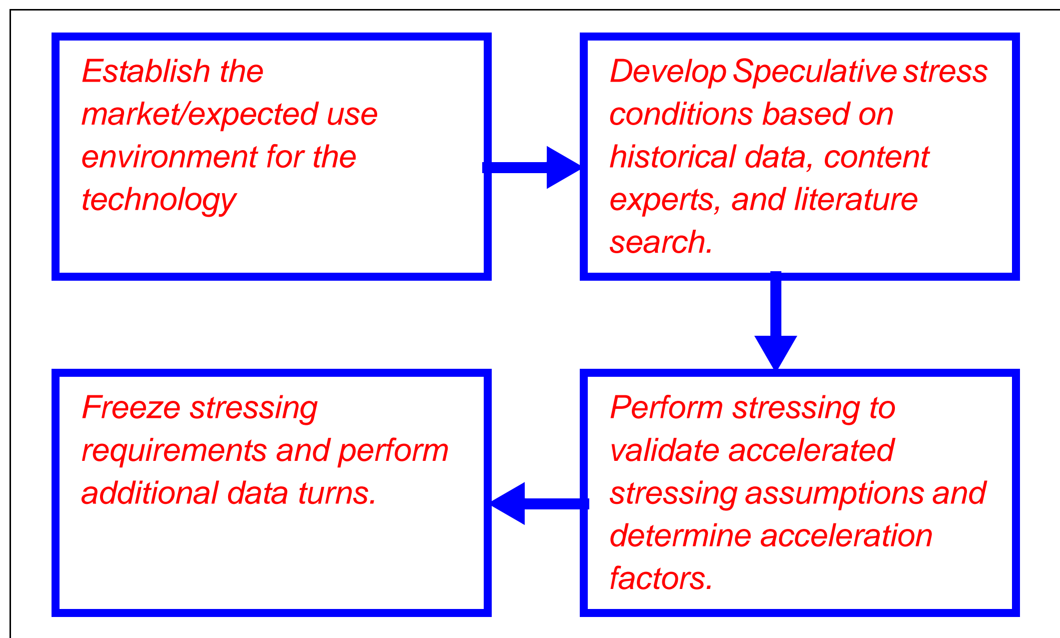
B Quality and Reliability Requirements

B.1 Thermal/Mechanical Solution Stress Test

Design, including materials, shall be consistent with the manufacture of units that meet the following environmental reference points.

The reliability targets in this section are based on the expected field use environment for a server product. The test sequence for the components will be developed using the knowledge-based reliability evaluation methodology, which is acceleration factor dependent. A simplified process flow of this methodology can be seen in Figure B-1.

Figure B-1. Flow Chart of Knowledge-Based Reliability Evaluation Methodology



The stress tests described in Table B-1 can be used as guidelines in setting a mechanical reliability test suite towards validation.

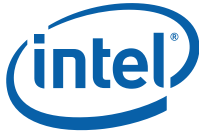


Table B-1. Typical Stress Tests

Stress Test	Example Test Description	Purpose/Failure Mechanism
Temperature Cycle	IPC 9701 or -40C to 85°C	Solder joint fatigue, via barrel cracking, and TIM separation/disbond under thermo-mechanical stresses
Temperature/Humidity (unbiased)	85% RH/85°C	Corrosion and material migration induced by moisture/temperature
Bake	125°C	Creep induced failure mechanisms, for example contact relaxation, solder ball creep, and thermal TIM degradation
Mechanical Shock	System level unpackaged test 2 drops for + and - directions in each of 3 perpendicular axes (that is, total 12 drops). Profile: 25g, Trapezoidal waveform, velocity change depending on system weight	Mechanical induced brittle solder joint failures and TIM separation/disbond
Random Vibration	System-level unpackaged test Duration: 10 min/axis, 3 axes Frequency Range: .001 g2/Hz @ 5Hz, ramping to .01 g2/Hz @20 Hz, .01 g2/Hz @ 20 Hz to 500 Hz Power Spectral Density (PSD) Profile: 2.20 g RMS	Example mechanisms include cyclic mechanical fatigue stress and TIM separation disbond

Note: Need to pass customer visual, thermal, mechanical, and electrical requirements.

B.1.1 Customer Environmental Reliability Testing

The conditions of the tests outlined here may differ from the customers' system requirements. Board/system level requirements are to be identified and performed by customers planning on using Intel reference thermal/mechanical solution.

B.1.2 Socket Durability Test

The socket must withstand 30 mating cycles. Test per EIA-364, test procedure 09. Measure contact resistance when mated in 1st and 30th cycles. The package must be removed at the end of each de-actuation cycle and reinserted into the socket.

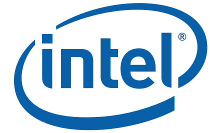
B.2 Ecological Requirement

General requirements: Materials used in this product must comply with customers' Environmental Product Content Specification. Intel's is available at:

<http://supplier2.intel.com/EHS/Environmental_Product_Content_Specification_9-16-03.doc>

Material shall be resistant to fungal growth. Examples of non-resistant materials include cellulose materials, animal- and vegetable-based adhesives, grease, oils, and many hydrocarbons. Synthetic materials such as PVC formulations, certain polyurethane compositions (for example, polyester and some polyethers), plastics which contain organic fillers of laminating materials, paints, and varnishes also are susceptible to fungal growth. If materials are not fungal growth resistant, then MIL-STD-810E, Method 508.4 must be performed to determine material performance.

Material used shall not have deformation or degradation in a temperature life test.



Any plastic component exceeding 25 grams must be recyclable per the European Blue Angel recycling standards.

Particular requirements: Cadmium shall not be used in painting or plating. No Quaternary salt electrolytic capacitors shall be used. Examples of prohibited caps are: United Chemi-Con type: LXF, LXY, LXZ. No brominated plastics shall be used. Also, plastics heavier than 25 g must be labeled per ISO 10469 and may not contain halogenated flame retardant compounds.

Chemical Restrictions:

The components must be 'halogen-free', that is, they are assembled without the intentional use of halogen in the raw materials and these elements are not intentionally present in the end product.

1. IEC 61249-2-21
   a. 900 ppm maximum chlorine
   b. 900 ppm maximum bromine
   c. 1500 ppm maximum total halogens
2. IPC-4101B
   d. 900 ppm maximum chlorine
   e. 900 ppm maximum bromine
   f. 1500 ppm maximum total halogens

It is **required** that the production version of the socket, Independent Loading Mechanism (ILM), and the thermal interface material (TIM) be RoHS compliant, by using 100% Lead-Free technology. RoHS (Restriction of Hazardous Substances) reference info source:

http://europa.eu.int/eur-lex/pri/en/oj/dat/2003/l_037/l_03720030213en00190023.pdf

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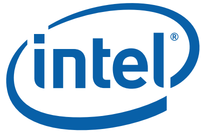

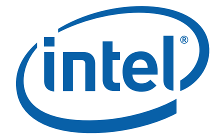

C Supplier Listing

Third-part suppliers are enabled to ensure that reference thermal and mechanical components are available.

C.1 Intel Enabled Supplier Information

Notes:

1. Supplier listing is provided by Intel as a convenience to its customers. Intel does not make any representations or warranties whatsoever regarding the quality, reliability, functionality, or compatibility of these devices.
2. All "Part Numbers" listed are in prototype phase and have not been verified to meet performance targets or quality and reliability requirements and are subject to change.
3. Supplier information provided in the table was deemed accurate when this document was released.
4. Customers planning on using the Intel reference design should contact the suppliers for the latest information on their product(s).
5. Customers must evaluate performance against their own product requirements.

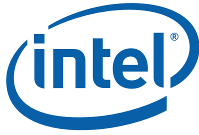

Table C-1. Supplier Listing (Sheet 1 of 2)

Component	Intel Part Number	Supplier PN	Supplier	Supplier Contact Info
LGA2011-1 Socket	G44924-001 (with 4 package keying)	PE201127-4353-01H (with 4 package keying)	Foxconn (Hon Hai)	Katie Wang katie.wang@foxconn.com Tel: +1-714-608-2085 Fax: +1-714-680-2099
		2174987-1 (with 4 package keying)	Tyco Electronics	Josh Moody jdmoody@tycoelectronics.com Tel: +1-503-327-8348; +1-503-327-8346 (Asia) Billy Hsieh billy.hsieh@te.com
Thermal Interface Material (TIM) [35x35x0.25 mm]	G34186	PCM45F	Honeywell	Judy Oles (Customer Service) Judy.Oles@Honeywell.com 509-252-8605 Andrew S.K. Ho (APAC) andrew.ho@honeywell.com (852) 9095-4593 Andy Delano (Technical) Andrew.Delano@Honeywell.com 509-252-2224
4U Heatsink Assembly with TIM	G48321-001	00Z89400101	Chaun-Choung Technology Corp. (CCI)	Monica Chih 12F, No.123-1, Hsing-De Rd., Sanchung, Taipei, Taiwan, R.O.C. Tel. +886 (2) 2995-2666 x1131 Fax: +886 (2) 2995-8258 monica_chih@ccic.com.tw Sean Wu sean_wu@ccic.com.tw (408) 768-7629

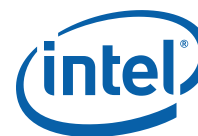

Table C-1. Supplier Listing (Sheet 2 of 2)

Component	Intel Part Number	Supplier PN		Supplier	Supplier Contact Info
		ILM Top Assembly	Back Plate Assembly		
LGA2011-1 ILM Assembly	G20917-003 (ILM Top Assembly) E94309-001 (Back Plate Assembly)	PT44L13-4511	PT44P11-4501	Foxconn (Hon Hai)	Eric Ling eric.ling@foxconn.com 503-693-3509 x225
		ACA-ZIF-150-Y01	DCA-HSK-182-Y06	Lotes	Cathy Yang Cathy@lotes.com.cn Tel: +1-86-20-84686519
		ITLG20917002	ITLE94309001	Amtek	Alvin Yap alvinyap@amtek.com.cn Tel +(86)752-2634562 Cathy Yu cathy_yu@amtek.com.cn Tel +(86)752-2616809
		2201068-1	2201069-1	Tyco Electronics	Josh Moody jdmoody@te.com Tel: +1-503-327-8348; 1-503-327-8346 (Asia) Billy Hsieh billy.hsieh@te.com
		1051971000	1051972000	Molex	Carol Liang carol.liang@molex.com Tel +86 (21) 5048-0889 #3301

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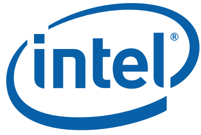
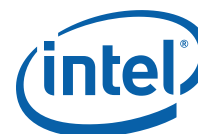




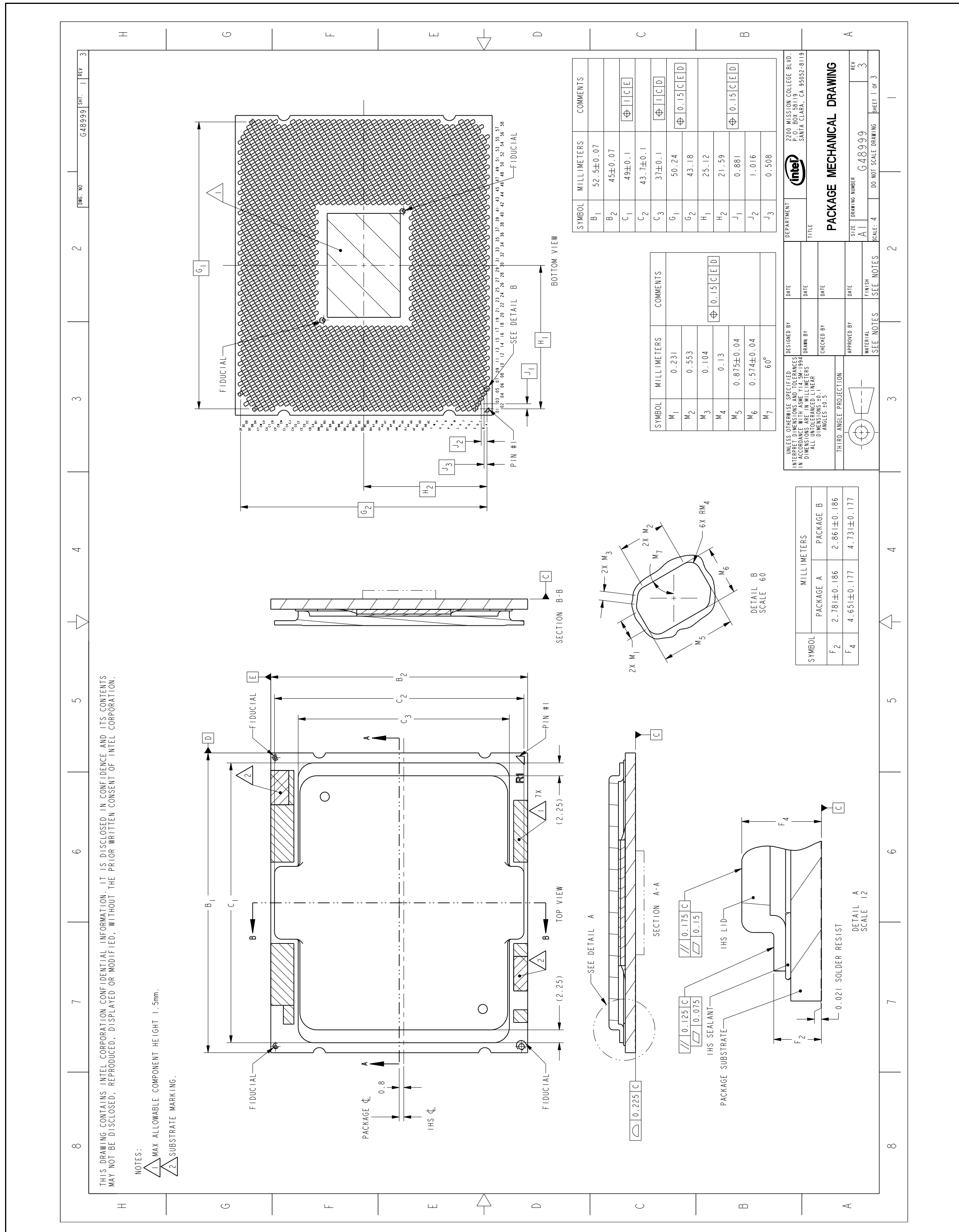
D Processor Package Mechanical Drawings

Table D-1 lists the socket drawings included in this appendix.

Table D-1. Socket Drawing List

Drawing Description	Figure Number
Processor Package Mechanical Drawing (Sheet 1 of 3)	Figure D-1
Processor Package Mechanical Drawing (Sheet 2 of 3)	Figure D-2
Processor Package Mechanical Drawing (Sheet 3 of 3)	Figure D-3

Figure D-1. Processor Package Mechanical Drawing (Sheet 1 of 3)



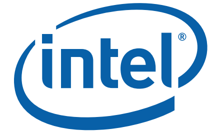


Figure D-2. Processor Package Mechanical Drawing (Sheet 2 of 3)

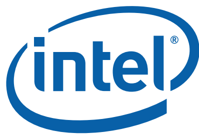


Figure D-3. Processor Package Mechanical Drawing (Sheet 3 of 3)

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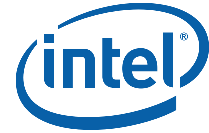
ZONE	REV	DESCRIPTION	DATE	APPR
	1	ENGINEERING RELEASE		
S1-H8 S1-F6 S1-D6 S1-E3 S1-B4 S1-C1 S2-F6 S1-C7	2	REVISED PER ECO #7723241 REVISE NOTE 1 REMOVE HATCH ON IHS TOP VIEW ADD R1 IN COSMETIC J3 WAS J1 ADD 6X RM4 MOVE POSITIONAL TOLERANCE TO C3 FROM C2 V2 WAS V1 CHANGED GD&T CALLOUT VALUES ON DETAL A		
	3	REVISED PER ECO #7775957 UPDATED LAND PATTERN ADDED A55		

DWG. NO G48999 SHT. 3 REV 3

DEPARTMENT
2200 MISSION COLLEGE BLVD.
P.O. BOX 58119
SANTA CLARA, CA 95052-8119
SIZE A1 DRAWING NUMBER G48999 REV 3
SCALE: 1.5 DO NOT SCALE DRAWING SHEET 3 OF 3



E LGA2011-1 Socket Electrical

E.1 Socket Electrical Requirements

LGA2011-1 electrical requirements (see Table E-1) are measured from the socket-seating plane of the processor (end of the contacts) to the socket solder ball attach at the motherboard. All specifications are maximum values (unless otherwise stated) for a single socket contact, but includes effects of adjacent contacts where indicated. Socket inductance includes exposed metal from mated contact to the PCB land array.

Table E-1. LGA2011-1 Electrical Requirements (Sheet 1 of 2)

Parameter	Value	Notes
S-parameters	See Table E-3	Measurements/simulations conditions: 1. Termination impedance: 85-Ohm differential, 50-Ohm single ended 2. Maximum test frequency: 10 GHz 3. Measurement structure consists of pin / pins under test surrounded by ground pins. For crosstalk, two pins or pin pairs are immediately adjacent to one another and the entire structure is surrounded by ground pins. Appropriate de-embedding is used to isolate the characteristics of the pin(s) under test, but the measurement result does include the effect of the test package via.
Mated loop inductance, Loop	<3.9 nH	The inductance calculated for two contacts, considering one forward conductor and one return conductor. These values must be satisfied at the worst-case height of the socket. Test frequency is 1 GHz.
Socket Average Contact Resistance (EOL)	22 milli-Ohms	The socket maximum average contact resistance target is calculated from the following equation: sum(Ni X LLCRi) / sum(Ni) LLCRi is the chain resistance defined as the resistance of each chain minus resistance of shorting bars divided by number of lands in the daisy chain. Ni is the number of contacts within a chain. i is the number of daisy chains, ranging from 1 to 119 (total number of daisy chains). The specification listed is at room temperature and has to be satisfied at all time.
Max Chain Resistance (EOL)	Refer to Table E-2 for criterion for varying chain length	The chain resistance is derived from the resistance of each chain minus resistance of shorting bars divided by number of lands in the daisy chain, and shall not exceed the Max Chain Resistance target. The Max Chain Resistance is defined by assuming only one contact reaches a maximum of 97 milli-Ohms and the rest meet the Socket Average Contact Resistance. It is calculated from the following equation: ((Ni-1) X Socket Average Contact Resistance + 97)/Ni; where Ni is the number of contacts within a chain. The specification listed is at room temperature and has to be satisfied at all time.
Bulk Resistance Increase	≤3 milli-Ohms	The bulk resistance increase per contact from 25°C to 100°C

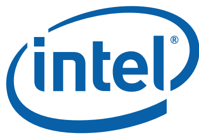


Table E-1. LGA2011-1 Electrical Requirements (Sheet 2 of 2)

Parameter	Value	Notes
Material Characterization: Dielectric Constant & Loss Tangent	Read & record	Report the dielectric constant and loss tangent over a frequency range from 3 GHz to 10 GHz. Include in reporting any differences due to material anisotropy. Measurements are at room temperature.
Dielectric Withstand Voltage	360 Volts RMS	
Insulation Resistance	800 Mega-Ohms	

Table E-2. Max Chain Average Resistance

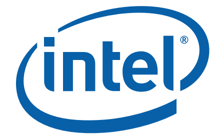
Contacts per Chain	Max Chain LLCR Limit (milli-Ohms)
2	59.5
4	40.75
6	34.5
8	31.4
10	29.5
12	28.25
14	27.4

Table E-3. S-parameters Requirements

	Metric	Value	Frequency
Single-Ended	S11	<-12 dB	0-3 GHz
	S12	<0.6 dB	
	Near-End Xtalk	<-18 dB	
	Far-End Xtalk	<-20 dB	
Differential	DS11	<-12 dB	0-3.5 GHz
	DS12	<-75 dB	
	Near-End Xtalk	<-30 dB	
	Far-End Xtalk	<-35 dB	

E.2 S-Parameters

S-parameter data is to be collected for both single-ended and differential structures using a 4-port PNA. Test structures must be designed to isolate the contact/contacts under test (that is, contact(s) must be surrounded by grounds). Data is to be collected and reported up to 10 GHz. Appropriate de-embedding should be used to isolate the contact(s) under test but the test package via will be included as part of the structure. For single-ended structures, the insertion and return loss and the near-end and far-end crosstalk shall be measured. For differential structures, the differential insertion and return loss and the near-end and far-end crosstalk shall be measured. For crosstalk measurements, the two contacts (or contact pairs for differential) shall be located adjacent to one another at the minimum pitch and the entire structure shall be surrounded by grounds.



E.3 Dielectric Withstand Voltage

No disruptive discharge or leakage greater than 0.5 mA is allowed when subjected to 360 V RMS. The sockets shall be tested according to EIA-364, Test Procedure 20A, Method 1. The sockets shall be tested in fully mated condition. Barometric pressure shall be equivalent to Sea Level. The sample size is 25 contact-to-contact pairs on each of four sockets. The contacts shall be randomly chosen.

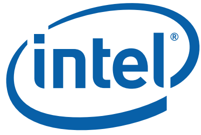
E.4 Insulation Resistance

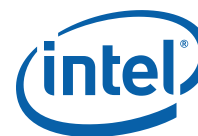
The Insulation Resistance shall be greater than 800 MΩ when subjected to 500 V DC. The sockets shall be tested according to EIA-364, Test Procedure 21. The sockets shall be tested in unmounted and unmated. The sample size is 25 contact-to-contact pairs on each of 4 sockets. The contacts shall be randomly chosen.

E.5 Contact Current Rating

Measure and record the temperature rise when the socket is subjected to rate current of 0.8 A. The sockets shall be tested according to EIA-364, Test Procedure 70 A, Test Method 1.

§





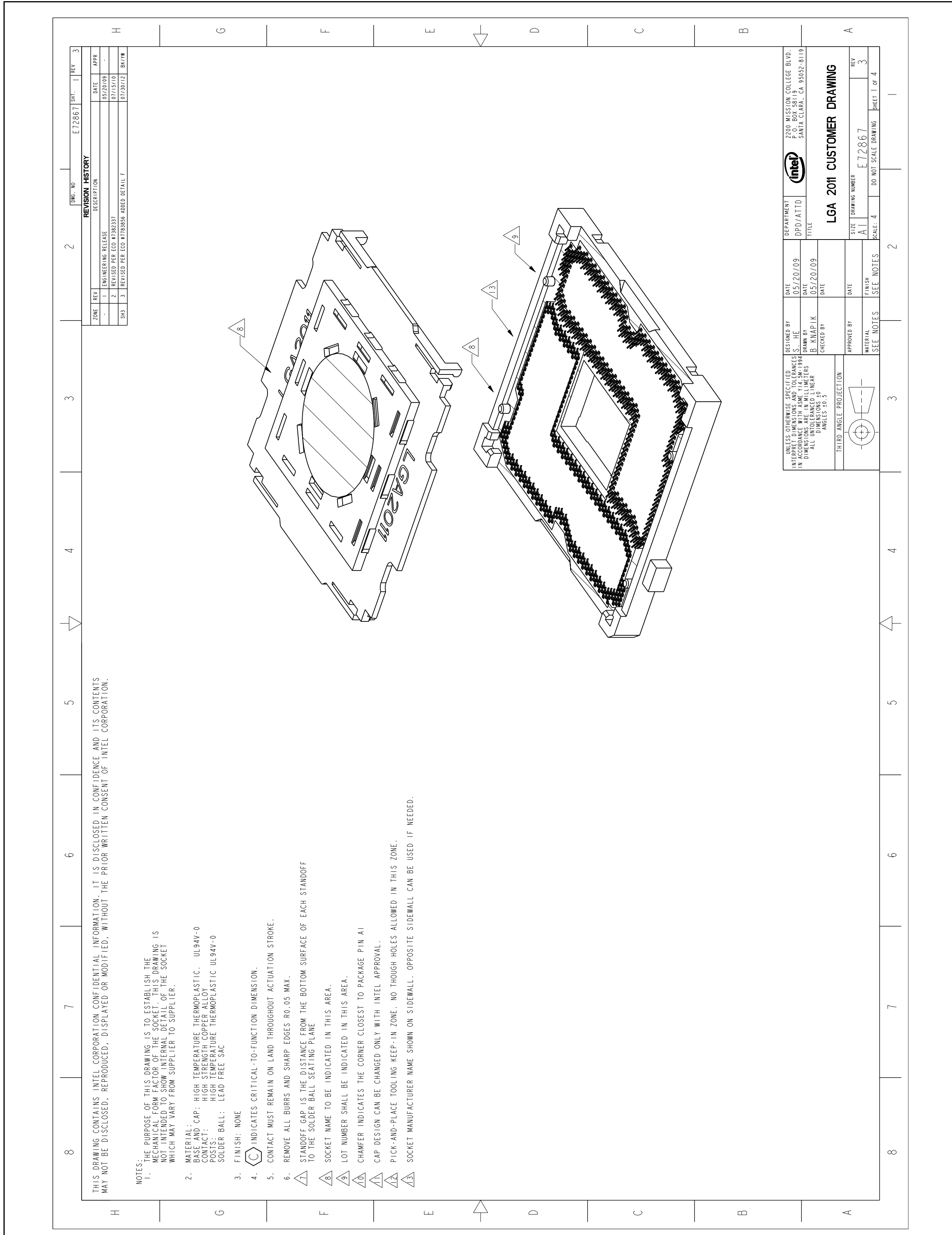
F Socket Mechanical Drawings

Table F-1 lists the socket drawings included in this appendix.

Table F-1. Socket Drawing List

Drawing Description	Figure Number
Socket Mechanical Drawing (Sheet 1 of 4)	Figure F-1
Socket Mechanical Drawing (Sheet 2 of 4)	Figure F-2
Socket Mechanical Drawing (Sheet 3 of 4)	Figure F-3
Socket Mechanical Drawing (Sheet 4 of 4)	Figure F-4

Figure F-1. Socket Mechanical Drawing (Sheet 1 of 4)



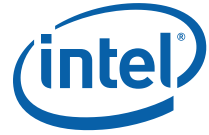
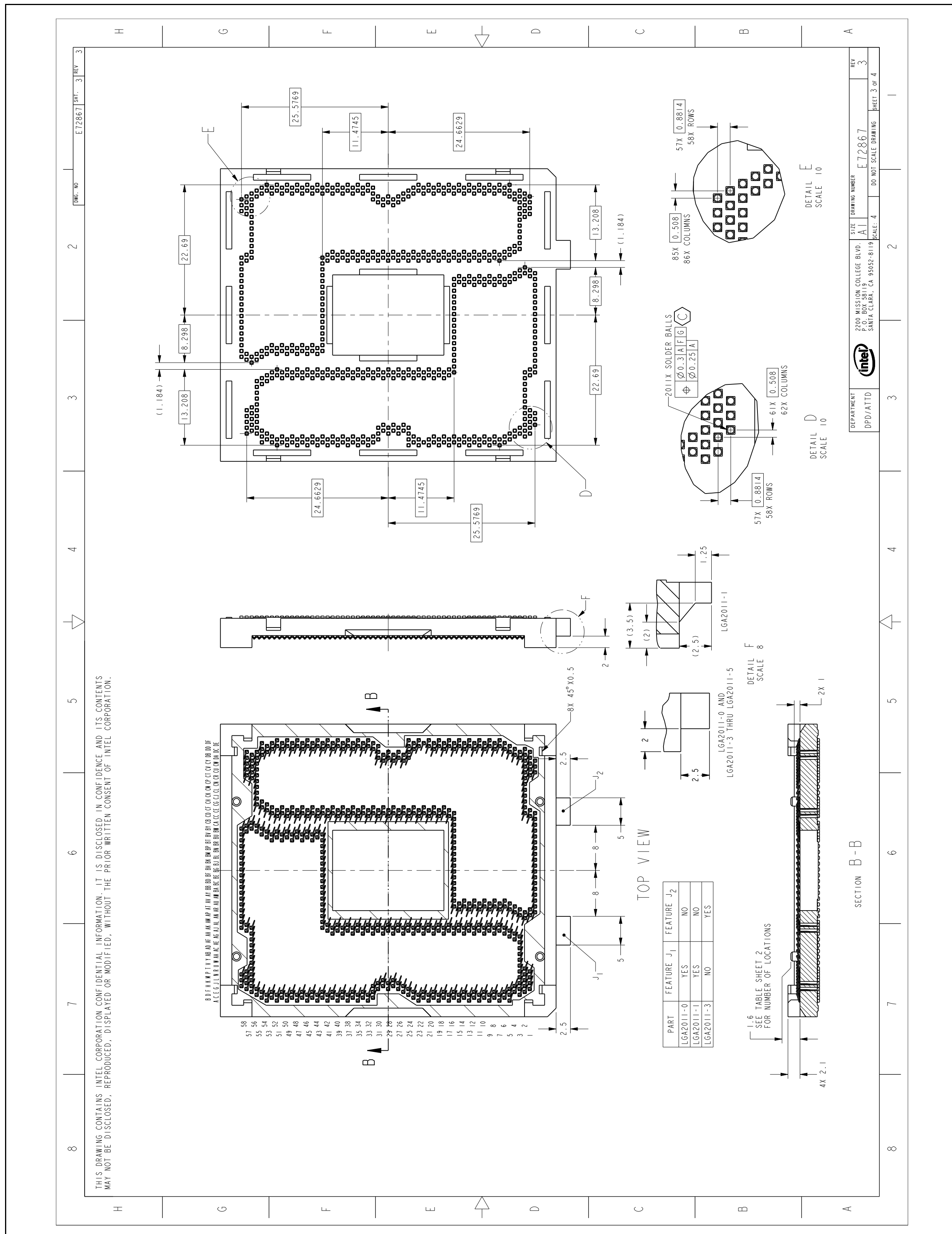


Figure F-2. Socket Mechanical Drawing (Sheet 2 of 4)

PART	FEATURE X	D1	FEATURE Y	D2
LGA2011-0	Ø1.6	15	Ø1.6	12
LGA2011-1	Ø1.6	15	Ø1.6	14
LGA2011-2	Ø1.6	13	Ø1.6	12
LGA2011-3	Ø1.6	13	Ø1.6	14
LGA2011-4	D1, 1, Ø1.6	12	N/A	N/A
LGA2011-5	D1, 1, Ø1.6	14	N/A	N/A

Figure F-3. Socket Mechanical Drawing (Sheet 3 of 4)



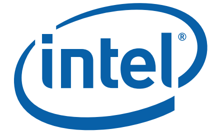
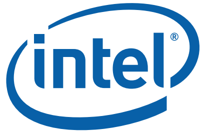
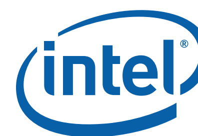


Figure F-4. Socket Mechanical Drawing (Sheet 4 of 4)



§



G Mechanical Drawings

Table G-1 lists the Mechanical drawings included in this appendix.

Table G-1. Mechanical Drawing List

Description	Figure
"PCB Primary Side Keep-out Zone for LGA2011-1 Socket - G26770 Rev 2"	Figure G-1
"PCB Primary Side Keep-out Zone for Heatsink - G26773 Rev 1"	Figure G-2
"PCB Primary Side Keep-out Zone for ILM - G26772 Rev 1"	Figure G-3
"PCB Secondary Side Keep-out Zone for Back Plate - G26769 Rev 1"	Figure G-4
"ILM Volumetric Keep-out Drawing - G52827 Rev A"	Figure G-5
"ILM Mechanical Drawing - G56693 Rev 2 (Sheet 1 of 4)"	Figure G-6
"ILM Mechanical Drawing - G56693 Rev 2 (Sheet 2 of 4)"	Figure G-7
"ILM Mechanical Drawing - G56693 Rev 2 (Sheet 3 of 4)"	Figure G-8
"ILM Mechanical Drawing - G56693 Rev 2 (Sheet 4 of 4)"	Figure G-9
"Processor 4U Heatsink Assembly Drawing - G48321 Rev 1"	Figure G-10
"Processor 4U Heatsink Assembly Drawing - G20942 Rev E"	Figure G-11
"Processor 4U Heatsink Base Mechanical Drawing - G20943 Rev C"	Figure G-12
"Processor 4U Heatsink Heatpipe Mechanical Drawing - E42883 Rev 1"	Figure G-13
"Processor 4U Heatsink Stiffener Mechanical Drawing - G45952 Rev C"	Figure G-14
"Processor 4U Heatsink Base Cap Mechanical Drawing - E95299 Rev A"	Figure G-15
"Processor 4U Heatsink Top Fin Mechanical Drawing - G20945 Rev D"	Figure G-16
"Processor 4U Heatsink Bottom Fin Mechanical Drawing - G20944 Rev D"	Figure G-17
"Processor Heatsink Fastener Mechanical Drawing - E91775 Rev B"	Figure G-18
"Processor Heatsink Spring Mechanical Drawing - E86113 Rev C"	Figure G-19
"Processor Heatsink Fastener Retainer Mechanical Drawing - G13624 Rev A"	Figure G-20
"Processor Heatsink Retaining Ring Mechanical Drawing - E75155 Rev C"	Figure G-21

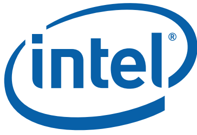


Figure G-1. PCB Primary Side Keep-out Zone for LGA2011-1 Socket - G26770 Rev 2

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DWG. NO KOZ_G26770_SKT-R1-MTG-HOLES SHT 1 REV 2

REVISION HISTORY

ZONE	REV	DESCRIPTION	DATE	APPR
-	A	DRAFT	2-9-11	TAB
	1	INITIAL RELEASE	8/9/11	TAB
A5	2	CHANGE THRU ALL ROUTE KEEPOUT DIM TO MATCH R0 AND PRELIM SYMBOL	9/28/11	TAB

NOTES:

1. THIS DRAWING TO BE USED IN CORELATION WITH SUPPLIED 3D DATA BASE FILE. ALL DIMENSIONS AND TOLERANCES ON THIS DRAWING TAKE PRECEDENCE OVER SUPPLIED FILE.

2. MAXIMUM OUTLINE OF SOCKET MUST BE PLACED SYMMETRIC TO THE ILM HOLE PATTERN FOR PROPER ILM AND SOCKET FUNCTION.

3. A HEIGHT RESTRICTION ZONE IS DEFINED AS ONE WHERE ALL COMPONENTS PLACED ON THE SURFACE OF THE MOTHERBOARD MUST HAVE A MAXIMUM HEIGHT NO GREATER THAN THE HEIGHT DEFINED BY THAT ZONE AFTER REFLOW.

   ALL ZONES DEFINED WITHIN THE 93 X 93 MM OUTLINE REPRESENT SPACE THAT RESIDES BENEATH THE HEATSINK FOOTPRINT.

   UNLESS OTHERWISE NOTED ALL VIEW DIMENSION ARE NOMINAL. ALL HEIGHT RESTRICTIONS ARE MAXIMUMS. NEITHER ARE DRIVEN BY IMPLIED TOLERANCES.

   A HEIGHT RESTRICTION OF 0.0 MM REPRESENTS THE TOP (OR BOTTOM) SURFACE OF THE MOTHERBOARD AS THE MAXIMUM HEIGHT. THIS IS A NO COMPONENT PLACEMENT ZONE INCLUDING SOLDER BUMPS.

   SEE NOTE 4 FOR ADDITIONAL DETAILS.

4. ASSUMING A GENERIC A MAXIMUM COMPONENT HEIGHT ZONE.
   CHOICE OF AND COMPONENT PLACEMENT IN THIS ZONE MUST INCLUDE:
   - COMPONENT NOMINAL HEIGHT
   - COMPONENT TOLERANCES
   - COMPONENT PLACEMENT TILT
   - SOLDER REFLOW THICKNESS
   DO NOT PLACE COMPONENTS IN THIS ZONE THAT WILL EXCEED THIS MAXIMUM COMPONENT HEIGHT.

5. ASSUMES PLACEMENT OF A 0805 CAPACITOR WITH DIMENSIONS:
   - CAP NOMINAL HEIGHT = 1.25MM (0.049")
   - COMPONENT MAX MATERIAL CONDITION HEIGHT NOT TO EXCEED 1.50MM.

LEGEND

ZONE 1: 0.0 MM MAX COMPONENT HEIGHT, NO COMPONENT PLACEMENT, NO ROUTE ZONE

ZONE 2: 1.67 MM MAX COMPONENT HEIGHT AFTER REFLOW 3 4; 1.50 MM MAX (MMC) COMPONENT HEIGHT BEFORE REFLOW 3 5

ZONE 3: NO ROUTE ZONE THROUGH ALL LAYERS

1.811 [46]
.906 [23]
1.362 [34.6]
2.724 [69.2]
.504 [12.8]
.717 [18.2]
SOCKET OUTLINE FOR REFERENCE ONLY
SEE DETAIL A
SCALE 3:1

Ø.276 [7.01] ROUTE KEEPOUT
Ø.180 [4.56] THROUGH ALL ROUTE KEEPOUT
Ø.256 [6.5] COPPER WEAR PAD: NON-GROUNDED SOLDER MASKED 0.0" HEIGHT PACKAGE KEEPOUT
Ø.150 [3.8] NPTH
TOP SIDE HOLE DETAIL A
4 PLACES SCALE 10:1

QTY	ITEM NO	PART NUMBER	DESCRIPTION
	TOP	KOZ_G26770_SKT-R1-MTG-HOLES	

PARTS LIST

UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5M-1994 DIMENSIONS ARE IN INCHES (MM) TOLERANCES:

THIRD ANGLE PROJECTION

DESIGNED BY	DATE
T. BOYD	2-2-11
DRAWN BY	DATE
T. BOYD	2-2-11
CHECKED BY	DATE
-	-
APPROVED BY	DATE
-	-
MATERIAL: SEE NOTES	FINISH: SEE NOTES

DEPARTMENT: PTMI

intel 2200 MISSION COLLEGE BLVD. P.O. BOX 58119 SANTA CLARA, CA 95052-8119

TITLE: KOZ,SKT-R1 ILM, MTG HOLES

SIZE: D DRAWING NUMBER: KOZ_G26770_SKT-R1-MTG-HOLES REV: 2

SCALE: 2:1 DO NOT SCALE DRAWING SHEET 1 OF 1

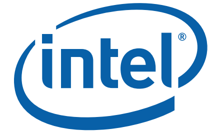

Figure G-2. PCB Primary Side Keep-out Zone for Heatsink - G26773 Rev 1

NOTES:
1. THIS DRAWING TO BE USED IN CORELATION WITH SUPPLIED 3D DATA BASE FILE. ALL DIMENSIONS AND TOLERANCES ON THIS DRAWING TAKE PRECEDENCE OVER SUPPLIED FILE.
2. MAXIMUM OUTLINE OF SOCKET MUST BE PLACED SYMMETRIC TO THE ILM HOLE PATTERN FOR PROPER ILM AND SOCKET FUNCTION.

LEGEND
ZONE 1: NO COMPONENTS FROM 7.2 MM ABOVE BOARD TO HEIGHT OF HEAT SINK
ZONE 2: 0.0 MM MAX COMPONENT HEIGHT, NO COMPONENT PLACEMENT. NO ROUTE ZONE
ZONE 3: 15.25 MM MAX COMPONENT HEIGHT HS FIN SHADOW

4.213 [107]
2.815 [71.5]
3.819 [97]
3.031 [77]
SCALE 2:1

REVISION HISTORY
KOZ_G26773_SKT-R1-HS-TOWER SHT 1 REV 1
ZONE - REV 1 DESCRIPTION INITIAL RELEASE DATE 8-18-11 APPR TAB

PARTS LIST
TOP KOZ_G26770_SKT-R1-MTG-HOLES

KOZ,SKT-R1 ILM, HEATSINK, TOWER
DESIGNED BY T. BOYD DATE 2-2-11
DRAWN BY T. BOYD DATE 2-2-11
DEPARTMENT PTMI
2200 MISSION COLLEGE BLVD. P.O. BOX 58119 SANTA CLARA, CA 95052-8119
THIRD ANGLE PROJECTION
MATERIAL SEE NOTES FINISH SEE NOTES
SIZE D DRAWING NUMBER KOZ_G26773_SKT-R1-HS-TOWER REV 1
SCALE: 2:1 DO NOT SCALE DRAWING SHEET 1 OF 1

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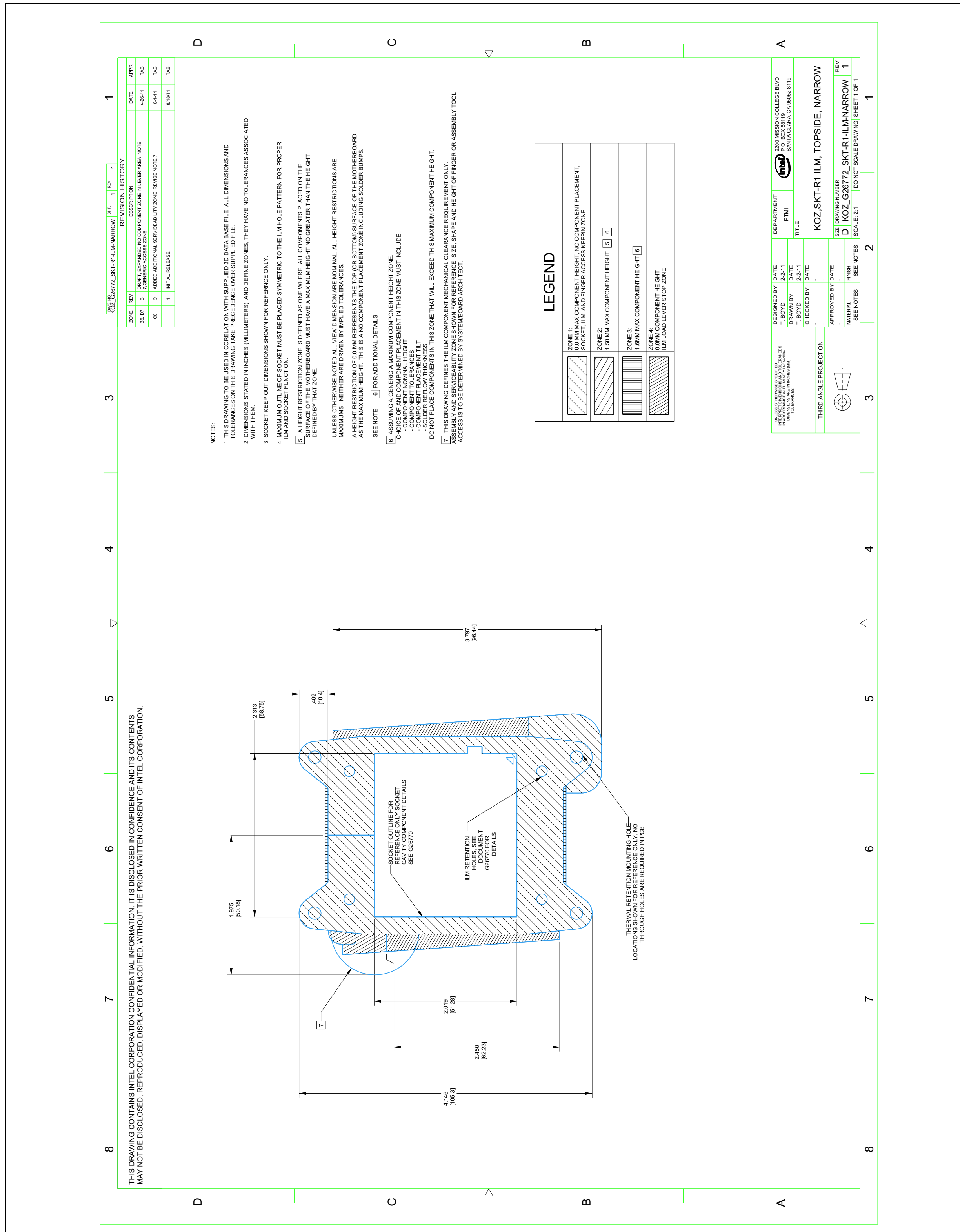
Figure G-3. PCB Primary Side Keep-out Zone for ILM - G26772 Rev 1



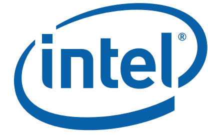
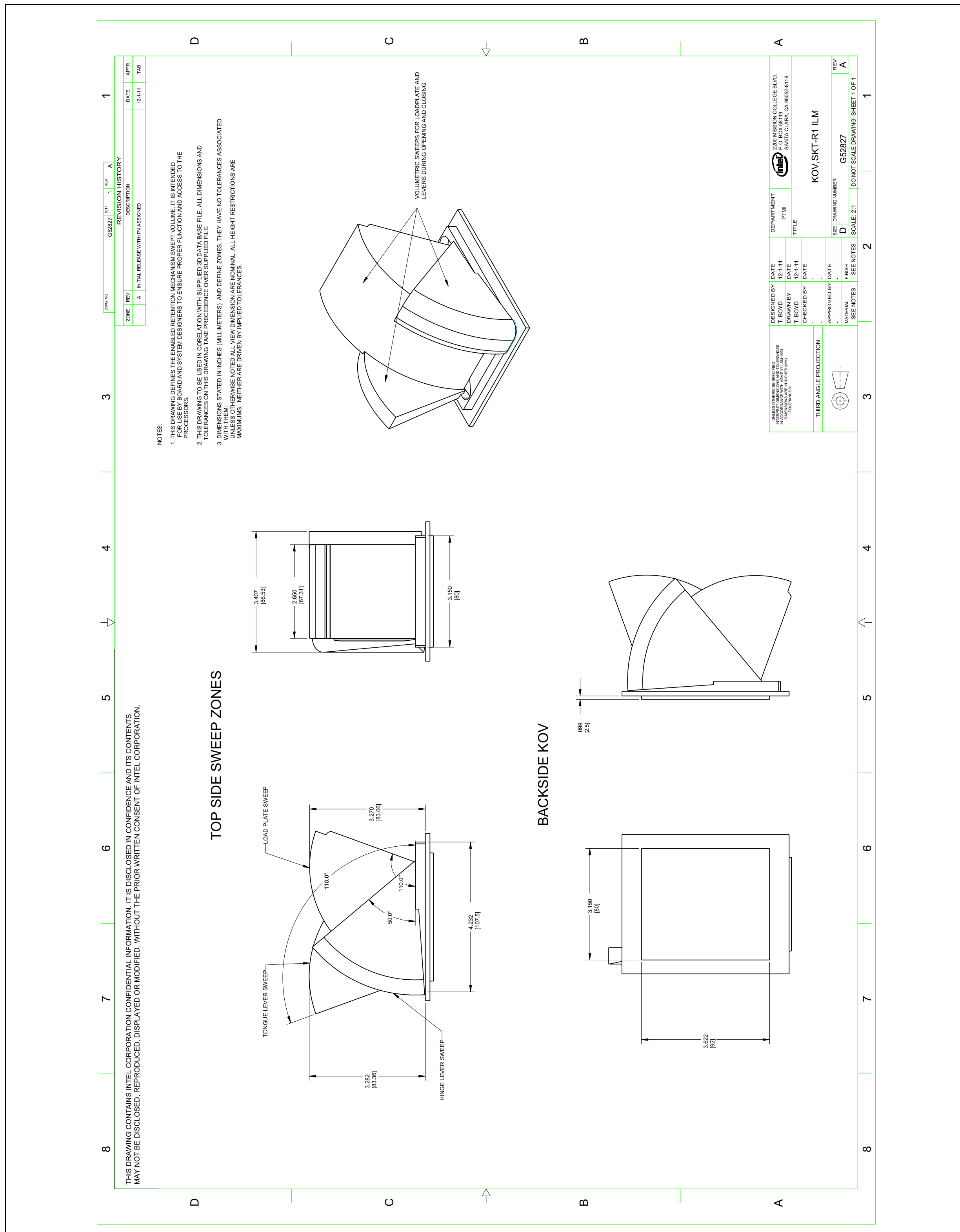


Figure G-4. PCB Secondary Side Keep-out Zone for Back Plate - G26769 Rev 1

Figure G-5. ILM Volumetric Keep-out Drawing - G52827 Rev A



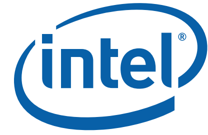
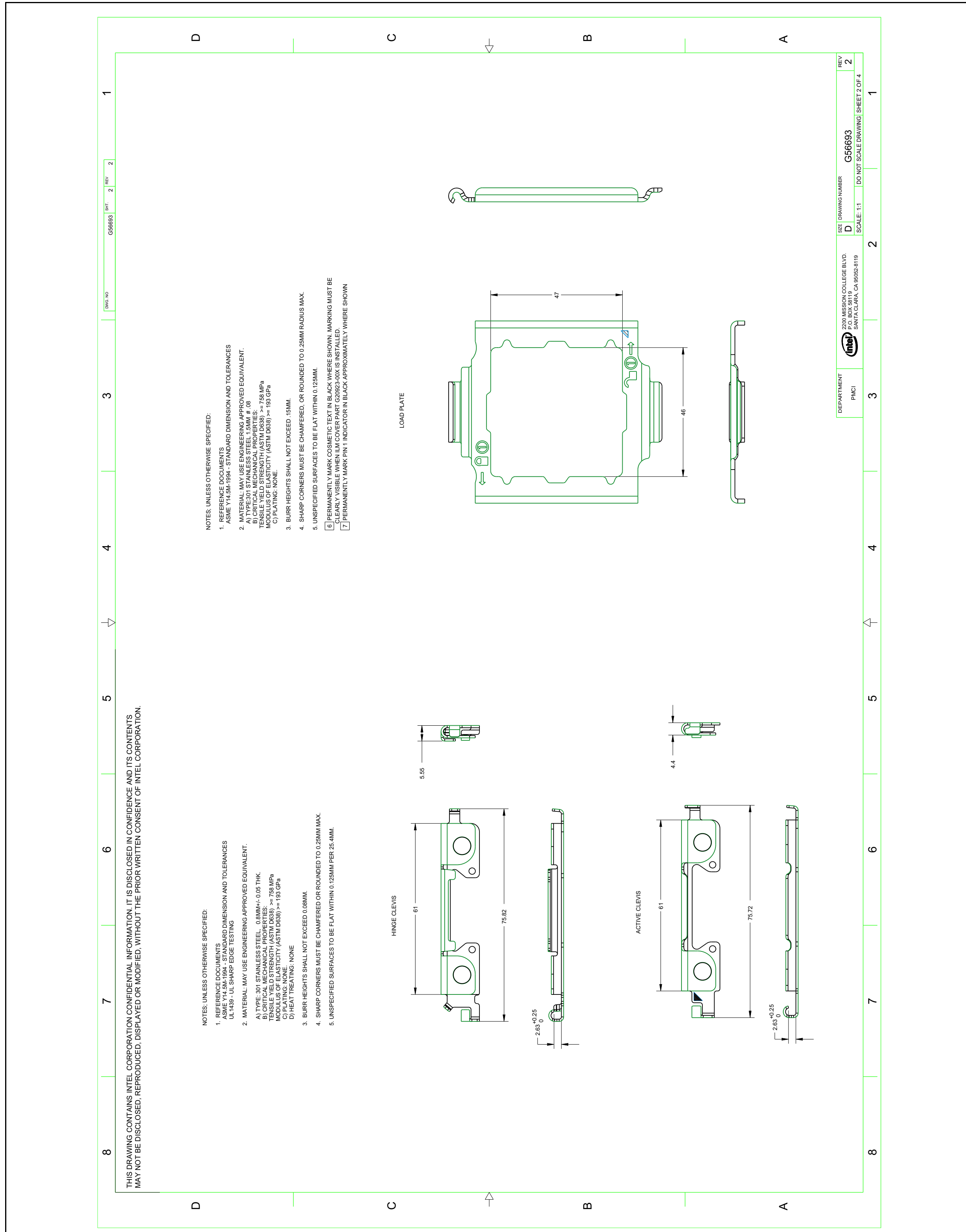


Figure G-6. ILM Mechanical Drawing - G56693 Rev 2 (Sheet 1 of 4)

Figure G-7. ILM Mechanical Drawing - G56693 Rev 2 (Sheet 2 of 4)



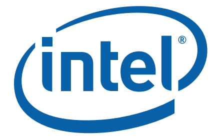


Figure G-8. ILM Mechanical Drawing - G56693 Rev 2 (Sheet 3 of 4)

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NOTES: UNLESS OTHERWISE SPECIFIED:

1. INTERPRET DIMENSIONS PER ASME Y14.5M-1994.
2. A) POLYCARBONATE (V0 FLAME RATING AND MUST PASS 100°C BAKE TEST)
   B) COLOR: BLACK
3. PART SHALL BE FREE OF OIL AND DEBRIS.
   FINISH: UNSPECIFIED SURFACES MUST CONFORM WITH CLASS C REQUIREMENTS.

ILM COVER

56.05

49.75

51

DEPARTMENT PMCI

2200 MISSION COLLEGE BLVD. P.O. BOX 58119 SANTA CLARA, CA 95052-8119

SIZE D DRAWING NUMBER G56693 REV 2

SCALE: 2:1 DO NOT SCALE DRAWING SHEET 3 OF 4

Figure G-9. ILM Mechanical Drawing - G56693 Rev 2 (Sheet 4 of 4)

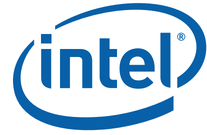


Figure G-10. Processor 4U Heatsink Assembly Drawing - G48321 Rev 1

Figure G-11. Processor 4U Heatsink Assembly Drawing - G20942 Rev E

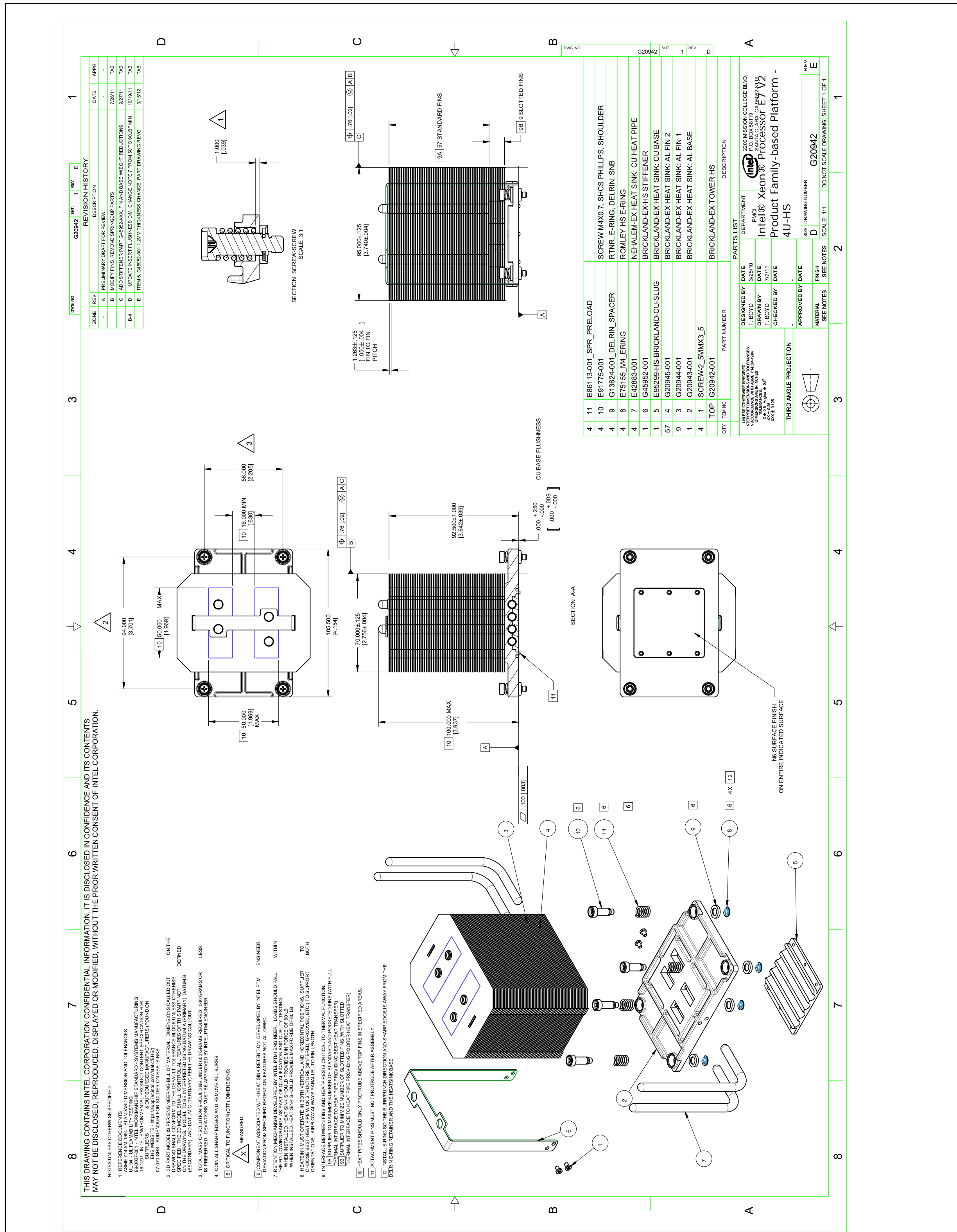
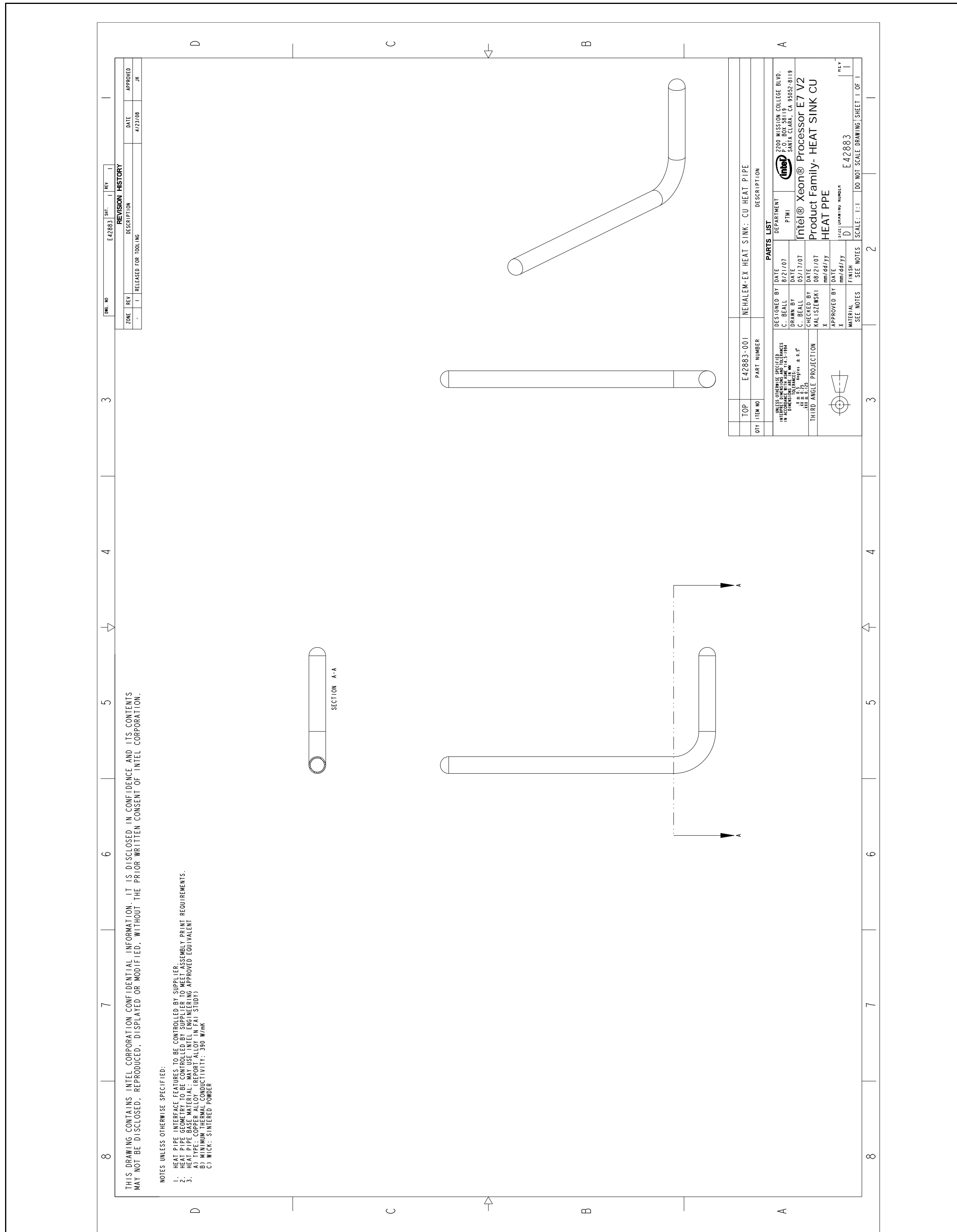


Figure G-12. Processor 4U Heatsink Base Mechanical Drawing - G20943 Rev C

Figure G-13. Processor 4U Heatsink Heatpipe Mechanical Drawing - E42883 Rev 1



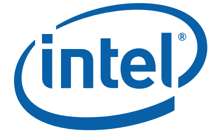


Figure G-14. Processor 4U Heatsink Stiffener Mechanical Drawing - G45952 Rev C

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DWG. NO G45952 SHT. 1 REV C

REVISION HISTORY

ZONE	REV	DESCRIPTION	DATE	APPR
-	A	PRELIMINARY DRAFT FOR REVIEW	9/21/11	TAB
	B	UPDATE NOTE 3A TO SPECIFY 1/2 HARD STAINLESS STEEL MATERIAL	10/19/11	TAB
	C	DECREASE MATERIAL THICKNESS FROM 1.5 TO 1.2MM	3/14/12	TAB

NOTES: UNLESS OTHERWISE SPECIFIED:

1. REFERENCE DOCUMENTS
   ASME Y14.5M-1994 - STANDARD DIMENSION AND TOLERANCES
   UL 94 - UL FLAMABILITY TESTING
   99-0007-001 - INTEL WORKMANSHIP STANDARD - SYSTEMS MANUFACTURING
   18-1201 - INTEL ENVIRONMENTAL PRODUCT CONTENT SPECIFICATION FOR SUPPLIERS & OUTSOURCED MANUFACTURERS (FOUND ON EHS WEBSITE - https://supplier.intel.com/static/EHS/)
2. 3D PART MODEL IS PER ENGINEERING BILL OF MATERIAL. DIMENSIONS CALLED OUT ON THE DRAWING SHALL CONFORM TO THE DEFAULT TOLERANCE BLOCK UNLESS OTHERISE SPECIFIED. THE 3D MODEL SHALL CONTROL ALL FEATURES OF THIS PART NOT DEFINED ON THE DRAWING. MODEL TO BE INTERPRETED USING DATUM A (PRIMARY), DATUM B (SECONDARY), AND DATUM C (TERTIARY) PER THE DRAWING CALLOUT.
3. MATERIAL: MAY USE INTEL ENGINEERING APPROVED EQUIVALENT
   A) TYPE: SUS 304 1/2 HARD STAINLESS STEEL (REPORT ALLOY IN FAI STUDY)
   B) THICKNESS: 1.2MM (.059") THICK
4. BURR HEIGHTS SHALL NOT EXCEED 10% OF MATERIAL THICKNESS.
5. THIS DRAWING TO BE USED IN CORRELATION WITH SUPPLIED 3D DATABASE FILE. ALL DIMENSIONS AND TOLERANCES ON THIS DRAWING TAKE PRECEDENCE OVER SUPPLIED FILE.
6. PART TO BE FLAT WITHIN 0.15mm.
7. BEND RADII 0.125mm (.005") MINIMUM.
8. CRITICAL TO FUNCTION DIMENSION (CTF) MEASURED
9. BREAK ALL SHARP EDGES
10. ALL SUBSTANCES IN THIS PART MUST CONFORM TO INTEL ENVIRONMENTAL PRODUCT SPECIFICATION BS-MTN-0001.

36
Ø 6.75
10
94.75
1.2
70
Ø 3
4.5

SCALE 2:1

UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5M-1994
DIMENSIONS ARE IN MM
TOLERANCES: .X ± 0.5 Angles ± 0.5°, .XX ± 0.25, .XXX ± 0.125

THIRD ANGLE PROJECTION

DESIGNED BY	DATE
T. BOYD	9/21/11
DRAWN BY	DATE
T. BOYD	9/21/11
CHECKED BY	DATE
-	-
APPROVED BY	DATE
-	-
MATERIAL SEE NOTES	FINISH SEE NOTES

DEPARTMENT PTMI

2200 MISSION COLLEGE BLVD.
P.O. BOX 58119
SANTA CLARA, CA 95052-8119

TITLE Intel® Xeon® Processor E7 V2 Product Family-based Platform HSINK STIFFENER

SIZE D DRAWING NUMBER G45952 REV C

SCALE: 1:1 DO NOT SCALE DRAWING SHEET 1 OF 1

Figure G-15. Processor 4U Heatsink Base Cap Mechanical Drawing - E95299 Rev A

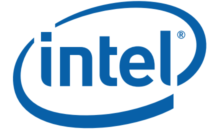


Figure G-16. Processor 4U Heatsink Top Fin Mechanical Drawing - G20945 Rev D

THIS DRAWING CONTAINS INTEL CORPORATION CONFIDENTIAL INFORMATION. IT IS DISCLOSED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED, REPRODUCED, DISPLAYED OR MODIFIED, WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.

DWG. NO G20945 SHT. 1 REV D

REVISION HISTORY

ZONE	REV	DESCRIPTION	DATE	APPR
-	A	PRELIMINARY DRAFT FOR REVIEW	7/8/11	TAB
	B	UPDATE FIN DIMENSIONS	7/26/11	TAB
B4,C4	C	ADD SLOTS, CHANGE TAB LOCATION, CHAMFER FOR WEIGHT REDUCTION	9/21/11	TAB
	D	MODIFY NOTE 3A WITH ALLOY, ADD 3D PLATING NOT	10/20/11	TAB

NOTES: UNLESS OTHERWISE SPECIFIED:

1. REFERENCE DOCUMENTS
   ASME Y14.5M-1994 - STANDARD DIMENSION AND TOLERANCES
   UL 94 - UL FLAMABILITY TESTING
   99-0007-001 - INTEL WORKMANSHIP STANDARD - SYSTEMS MANUFACTURING
   18-1201 - INTEL ENVIRONMENTAL PRODUCT CONTENT SPECIFICATION FOR SUPPLIERS & OUTSOURCED MANUFACTURERS (FOUND ON EHS WEBSITE - https://supplier.intel.com/static/EHS/)
2. 3D PART MODEL IS PER ENGINEERING BILL OF MATERIAL. DIMENSIONS CALLED OUT ON THE DRAWING SHALL CONFORM TO THE DEFAULT TOLERANCE BLOCK UNLESS OTHERISE SPECIFIED. THE 3D MODEL SHALL CONTROL ALL FEATURES OF THIS PART NOT DEFINED ON THE DRAWING. MODEL TO BE INTERPRETED USING DATUM A (PRIMARY), DATUM B (SECONDARY), AND DATUM C (TERTIARY) PER THE DRAWING CALLOUT.
3. MATERIAL: MAY USE INTEL ENGINEERING APPROVED EQUIVALENT
   A) TYPE: ALUMINUM ALLOY 1100
   B) THICKNESS: 0.3MM (.012") THICK
   C) MINIMUM THERMAL CONDUCTIVITY: 205 W/mK
   D) PLATING: NICKEL
4. BURR HEIGHTS SHALL NOT EXCEED 10% OF MATERIAL THICKNESS.
5. THIS DRAWING TO BE USED IN CORRELATION WITH SUPPLIED 3D DATABASE FILE. ALL DIMENSIONS AND TOLERANCES ON THIS DRAWING TAKE PRECEDENCE OVER SUPPLIED FILE.
6. PART TO BE FLAT WITHIN 0.15mm.
7. BEND RADII 0.125mm (.005") MINIMUM.
8. CRITICAL TO FUNCTION DIMENSION (CTF) MEASURED
9. BREAK ALL SHARP EDGES
10. ALL SUBSTANCES IN THIS PART MUST CONFORM TO INTEL ENVIRONMENTAL PRODUCT SPECIFICATION BS-MTN-0001.

[11] HEAT PIPE INTERFACE FEATURES TO BE CONTROLLED BY SUPPLIER, AND SHOULD FIT IN SPECIFIED REGION.

[12] INDICATED DIMENSION DESCRIBES MAXIMUM SIZE. SUPPLIER MAY REDUCE FIN WEIGHT BY REMOVING MATERIAL FROM CORNERS OF THE FIN.

A
0.3
4X 1.263
4X 0.963
1 [12] 70
[11] 50 MAX
[11] 50 MAX
[11] 16 MIN
2 [12] 95
4X 10 TYP
4X 10 TYP
SCALE 2:1

UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5M-1994
DIMENSIONS ARE IN MM
TOLERANCES:
.X ± 0.5 Angles ± 0.5°
.XX ± 0.25
.XXX ± 0.125

THIRD ANGLE PROJECTION

DESIGNED BY	DATE
T. BOYD	7/8/11
DRAWN BY	DATE
T. BOYD	7/8/11
CHECKED BY	DATE
-	-
APPROVED BY	DATE
-	-
MATERIAL	FINISH
SEE NOTES	SEE NOTES

DEPARTMENT PTMI

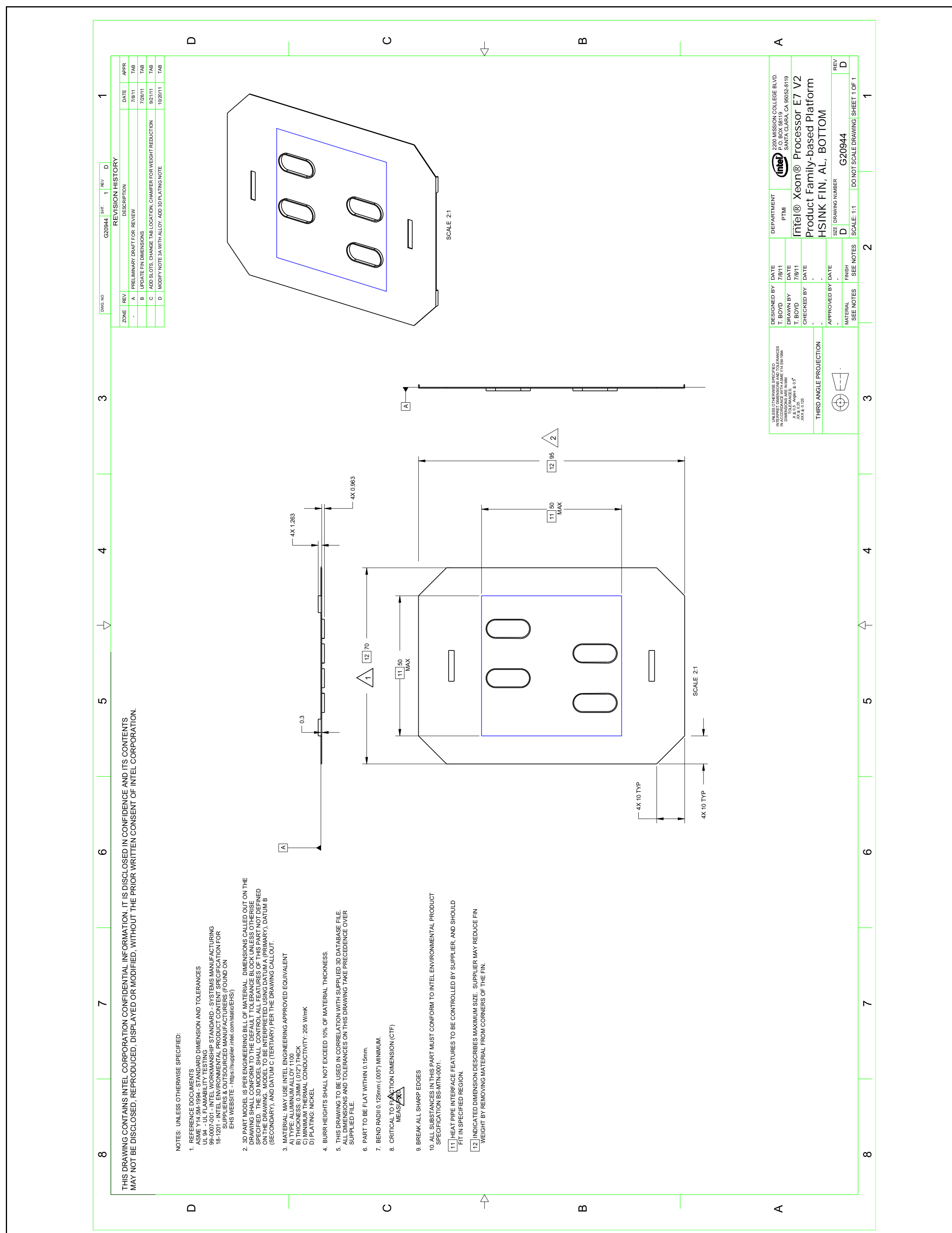
2200 MISSION COLLEGE BLVD.
P.O. BOX 58119
SANTA CLARA, CA 95052-8119

TITLE Intel® Xeon® Processor E7 V2 Product Family-based Platform HSINK FIN, AL, TOP

SIZE D DRAWING NUMBER G20945 REV D

SCALE: 1:1 DO NOT SCALE DRAWING SHEET 1 OF 1

Figure G-17. Processor 4U Heatsink Bottom Fin Mechanical Drawing - G20944 Rev D



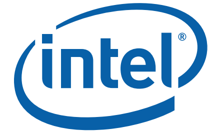


Figure G-18. Processor Heatsink Fastener Mechanical Drawing - E91775 Rev B

THIS DRAWING CONTAINS INTEL CORPORATION CONFIDENTIAL INFORMATION. IT IS DISCLOSED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED, REPRODUCED, DISPLAYED OR MODIFIED, WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.

FOR REVIEW ONLY

REVISION HISTORY

ZONE	REV	DESCRIPTION	DATE	APPROVED
-	A	ORIGINAL RELEASE	FEB-02-10	T.AULT
B-5	B	FULL THREAD LENGTH GROOVE ADDED	APR-14-10	K.KOZYRA
-	1	RELEASED TO MANUFACTURING	FEB-14-2011	K.KOZYRA

NOTES:

1. THIS DRAWING TO BE USED IN CONJUNCTION WITH SUPPLIED 3D DATABASE. ALL DIMENSIONS AND TOLERANCES ON THIS DRAWING TAKE PRECEDENCE OVER SUPPLIED DATABASE.
2. PRIMARY DIMENSIONS STATED IN MILLIMETERS. [BRACKETED] DIMENSIONS STATED IN INCHES.
3. MATERIAL: 18-8 STAINLESS STEEL; AISI 303, 304, 305; JIS SUS304; OR EQUIVALENT. MINIMUM YIELD STRENGTH = 90,000 PSI.
4. TORQUE TO FAILURE SHALL BE NO LESS THAN 20 IN-LBF, WITH A -3 SIGMA DISTRIBUTION
5. CRITICAL TO FUNCTION DIMENSION
6. PHILLIPS PATTERN PER ASME B18.6.3-1998
7. INSPECT SHAFT DIAMETER IN THESE LOCATIONS
8. E-RING GROOVE DIMENSIONS SHALL CONFORM TO JIS B 2805 STANDARDS
9. THREAD FORMING SHALL CONFORM TO ASME B1.13M-2005 OR JIS X XXXX STANDARDS

TYPE 1, CROSS RECESSED #2 DRIVER 6

4X 0.72 [0.028] MIN. 6

2X 4.06± 0.17 [0.160± 0.006] 6

SEE DETAIL B

0.40x45°

3.50 [0.138]

0.00 [0.000]

3.250 +0.075 / 0 [0.128 +0.002 / -0.000] 5 8

10.96 [0.43] 8

11.66 ± 0.13 [0.459 ± 0.005] 5 8

CRITICAL INTERFACE FEATURE: THIS SHOULDER MUST BE SQUARE 4

12.50 ± 0.13 [0.492 ± 0.005] 5

5.100 [0.2008]

SEE DETAIL A

3.50± 0.20 [0.138± 0.007] 5

Ø 7.80 [0.307]

Ø 6.00 [0.236]

2.00± 0.32 [0.079± 0.012] 6

(5.58) [0.220]

5.10± 0.05 [0.201± 0.001] 5 7

(12.50) [0.492]

INNER CORNERS OF E-RING GROOVE MUST BE SQUARE, R0.10 MAX

Ø 5.10± 0.05 [0.201± 0.001] 5 7

3.96± 0.06 [0.156± 0.002] MAJOR DIA, M4 x 0.7 FULL LENGTH TOLERANCE CLASS 6G 5

SECTION A-A

M4 X 0.7 FULL LENGTH EXTERNAL THREAD TOLERANCE CLASS 6G

R0.20 [0.008]

DETAIL B SCALE 40.000

0.5 X 45°

DETAIL A SCALE 40.000

UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-1994 DIMENSIONS ARE IN MILLIMETERS

THIRD ANGLE PROJECTION

DESIGNED BY	DATE
K.KOZYRA	FEB-02-10
DRAWN BY	DATE
K.KOZYRA	FEB-02-10
CHECKED BY	DATE
A.VALPIANI	FEB-02-10
APPROVED BY	DATE
T.AULT	FEB-02-10
MATERIAL	FINISH
SEE NOTES	SEE NOTES

DEPARTMENT: CPE/CMTE

2200 MISSION COLLEGE BLVD. P.O. BOX 58119 SANTA CLARA, CA 95052-8119

TITLE: SCREW, M4 X 0.7, PHILLIPS #2

SIZE: D | DRAWING NUMBER: E91775 | REV: B

SCALE: 1 | DO NOT SCALE DRAWING | SHEET 1 OF 1

DWG. NO E91775 SHT. 1 REV B

Figure G-19. Processor Heatsink Spring Mechanical Drawing - E86113 Rev C

THIS DRAWING CONTAINS INTEL CORPORATION CONFIDENTIAL INFORMATION. IT IS DISCLOSED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED, REPRODUCED, DISPLAYED OR MODIFIED, WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.

DWG. NO E86113 | SHT. 1 | REV C

REVISION HISTORY				
ZONE	REV	DESCRIPTION	DATE	APPROVED
-	A	SUPPLIER FEEDBACK	11/15/09	-
	B	ALL SPRING SPECIFICATIONS UPATED. SEE NOTE 3.	12/08/09	
NOTE 3	C	UPDATED SPRING STIFFNESS AND COIL INFO	01/14/10	

NOTES:

1. THIS DRAWING TO BE USED IN CONJUNCTION WITH SUPPLIED 3D DATABASE. ALL DIMENSIONS AND TOLERANCES ON THIS DRAWING TAKE PRECEDENCE OVER SUPPLIED DATABASE.
2. PRIMARY DIMENSIONS STATED IN MILLIMETERS. [BRACKETED] DIMENSIONS STATED IN INCHES.
3. SPRING RATE: K=15.80 +/- 1.5 N/MM [K=90.2 +/- 9.0 LBF/IN] 4
   FREE HEIGHT: 12.7 MM [0.500 IN]
   SOLID HEIGHT: 5.5 MM [0.217 IN]
   WIRE DIAMETER: 1.1 MM [0.043 IN]
   TOTAL COILS: 5.0 (ONLY TOTAL COILS SHOWN IN THIS DRAWING)
   ACTIVE COILS: 3.0
   ENDS: GROUND & CLOSED
   TURN: LEFT HAND (AS SHOWN IN VIEWS)
   MATERIAL: MUSIC WIRE, ASTM A228 OR JIS-G-3522
   FINISH: ZINC PLATED
   OTHER GEOMETRY: PER THIS DRAWING

4 CRITICAL TO FUNCTION DIMENSION

I.D. $5.42^{+0.08}_{-0.13}$ 4 [$0.213^{+0.003}_{-0.005}$]

O.D. $7.62^{+0.08}_{-0.13}$ 4 [$0.300^{+0.003}_{-0.005}$]

1.100 [0.0433] WIRE DIA.

12.70 [0.500] 4 FREE HEIGHT

$5.50^{+0.30}_{0}$ 4 [$0.217^{+0.011}_{-0.000}$]

A A

SOLID HEIGHT

FREE HEIGHT

SECTION A-A

UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5-1994 DIMENSIONS ARE IN MILLIMETERS TOLERANCES: .X ± .5 Angles ± 1.0° .XX ± 0.25 .XXX ± 0.127

THIRD ANGLE PROJECTION

DESIGNED BY	DATE
N. ULEN	11/15/09
DRAWN BY	DATE
N. ULEN	11/15/09
CHECKED BY	DATE
D. LLAPITAN	11/16/09
APPROVED BY	DATE
MATERIAL SEE NOTES	FINISH SEE NOTES

DEPARTMENT EASD / PTMI

intel 2200 MISSION COLLEGE BLVD. P.O. BOX 58119 SANTA CLARA, CA 95052-8119

TITLE SPRING, COMPRESSION, PRE-LOAD

SIZE D | DRAWING NUMBER E86113 | REV C

SCALE: 1 | DO NOT SCALE DRAWING | SHEET 1 OF 1

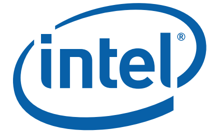
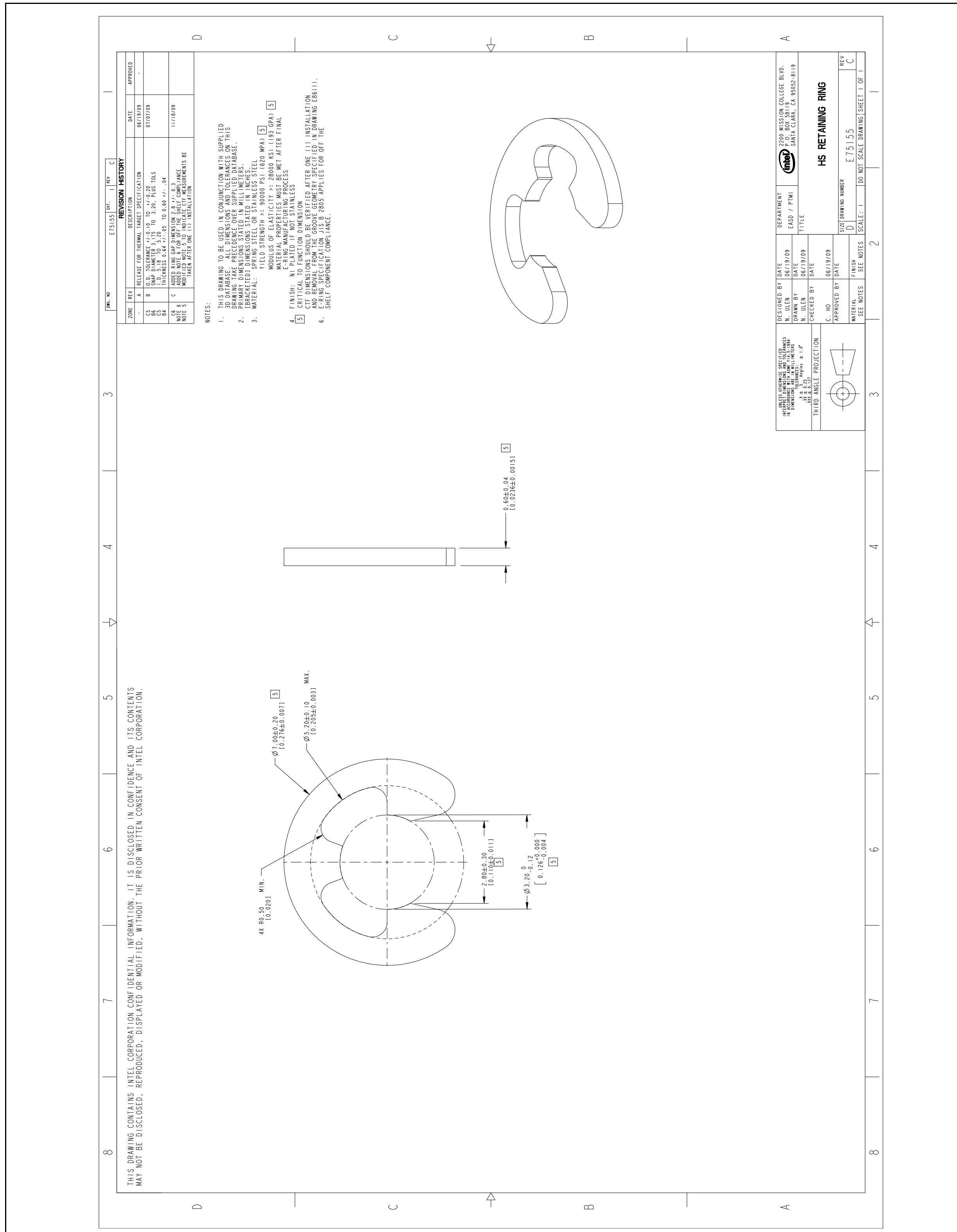
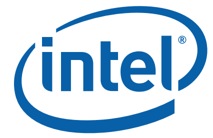


Figure G-20. Processor Heatsink Fastener Retainer Mechanical Drawing - G13624 Rev A

Figure G-21. Processor Heatsink Retaining Ring Mechanical Drawing - E75155 Rev C





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