Global Standards for the Microelectronics Industry

UFS 3.0
Controller Design Considerations

JEDEC Mobile
& IOT Forum

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Mobile Storage Evolution

eMMC
- Latest widely adopted standard before UFS 2.x
- Limited to 400MB/s (duplex) since 2013

UFS 1.x
- Not adopted

UFS 2.x
- Offers desktop-grade performance of ~1200MB/s over full-duplex links
- Good adoption in flagship devices (2017)

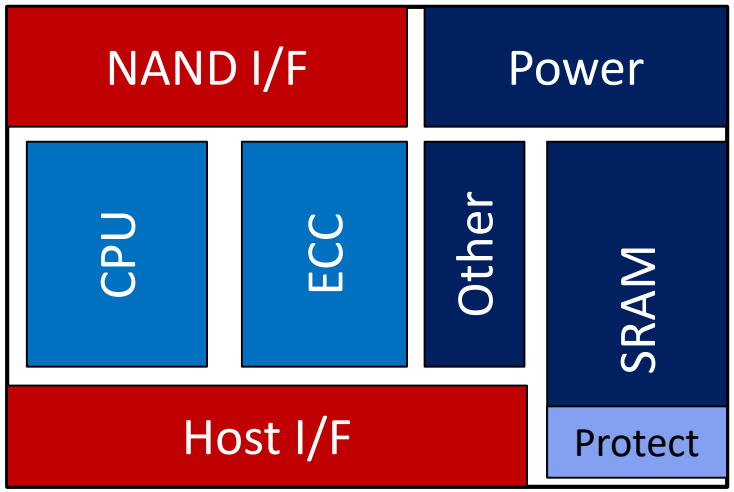
UFS 3.0
- Doubles UFS 2.x performance, offering ~2400MB/s
- **Requirements are tough for mobile form factors**

Market Segmentation

UFS 3.0

	Automotive UFS AEC-Q100 ISO-26262 ISO-16949	Commercial UFS and uMCP	Commercial UFS Card
Performance	Low-Mid	High	Low (1-Lane only)
Density	Application-Specific	Mid/High	Mid/High
Cost	Higher	Optimized	Lower
Reliability	High	Standard	Standard
Support	Long term	Standard	Standard
Application	- Infotainment - ADAS	- Smartphone - Tablet - Chromebook - Slim laptops	- Camera (4K, 8K...) - Smartphone - Tablet - Chromebook - Slim laptops

Generic NAND Flash Controller



- **Host Interface**
- **CPU**
- **ECC:** Error Correction Engine
- **SRAM** w/ Protection (bit-flip)
- **NAND Flash Interface**
- **Power:** Regulators, Detectors, Management
- **Other** HW and Peripherals

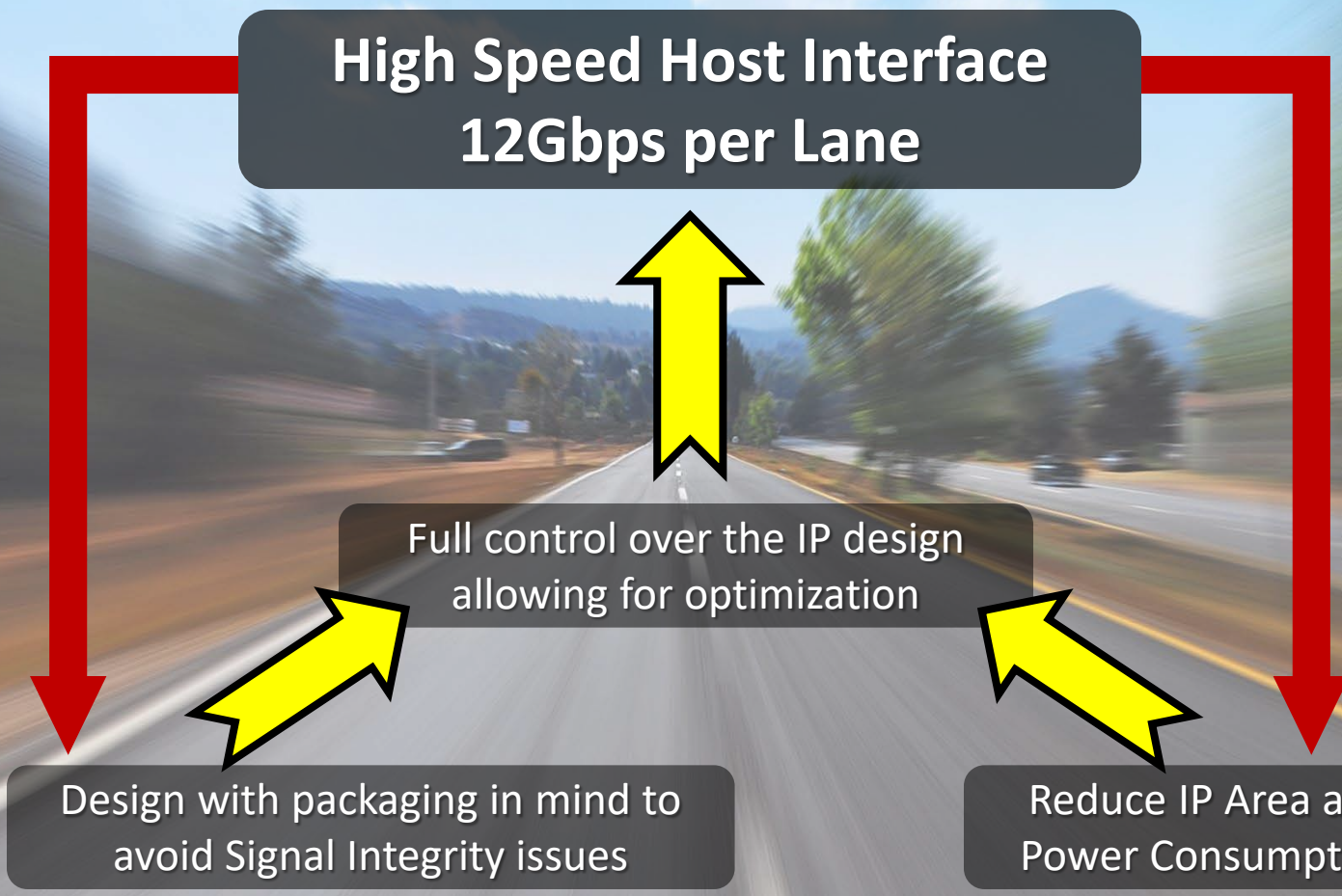
NAND Flash Evolution

- Process improvement
  - 2D 1x/1y nm, 3D Gen.1, 3D Gen.2, …
- TLC prevails
  - Lower Cost
  - 30% more density when compared to MLC
  - Computational demanding ECC algorythms
- High bandwidth interfaces
  - 533MT/s, 667MT/s, 800MT/s..., 1066MT/s? 1200MT/s? 1600MT/s?

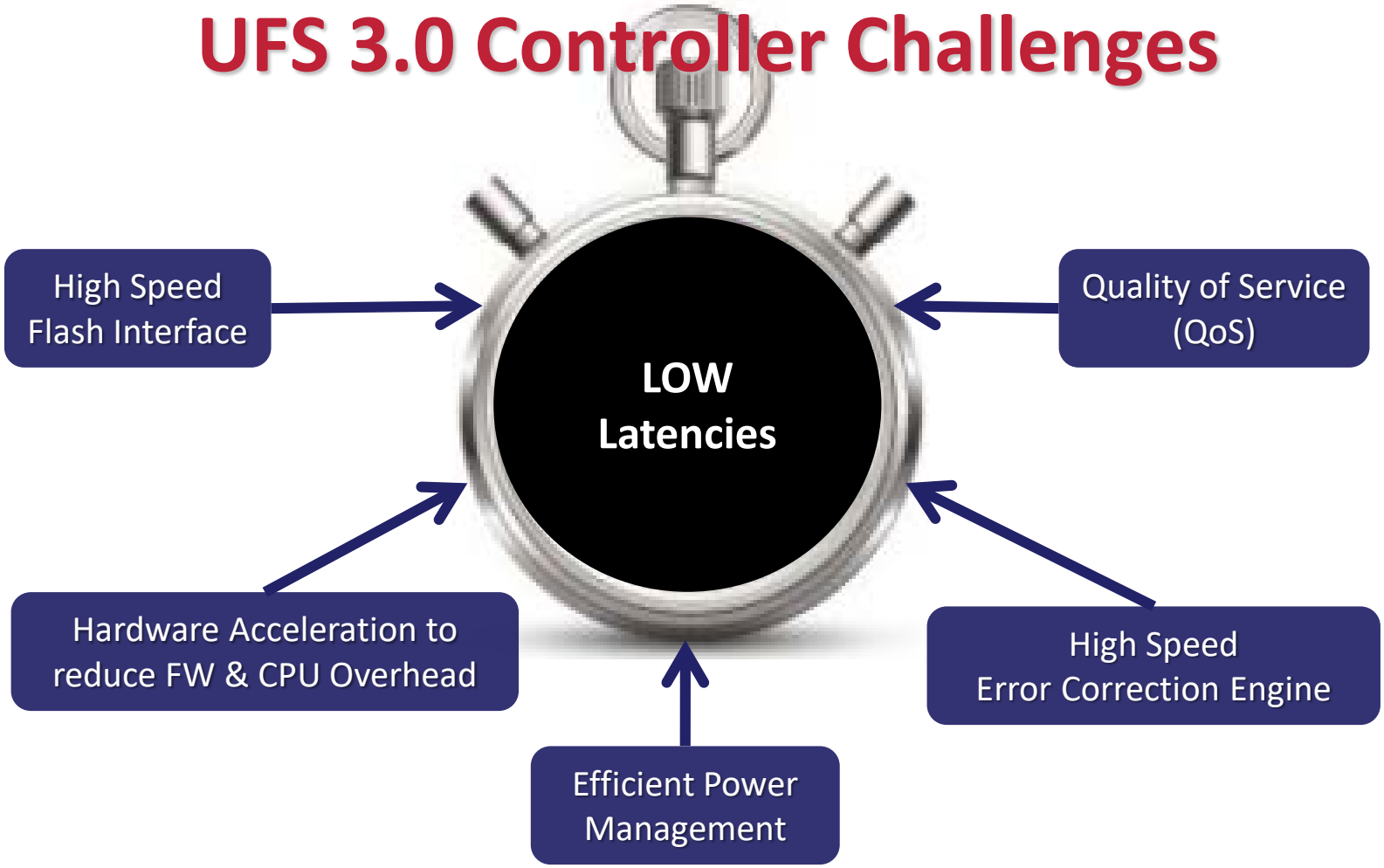
UFS 3.0 Controller Requirements

1. **High Throughput:** ~2400MB/s
2. **Low Latencies**
3. **Low Active Power:** < 700mA
4. **Cost Management**
    a) Reduced DIE Size
    b) Support to latest 3D NAND technologies

UFS 3.0 Controller Challenges



UFS 3.0 Controller Challenges



Having in-house IPs can shape the design around these requirements

USB 3.0 Controller Challenges

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Example of performance & cost trade-off in design:

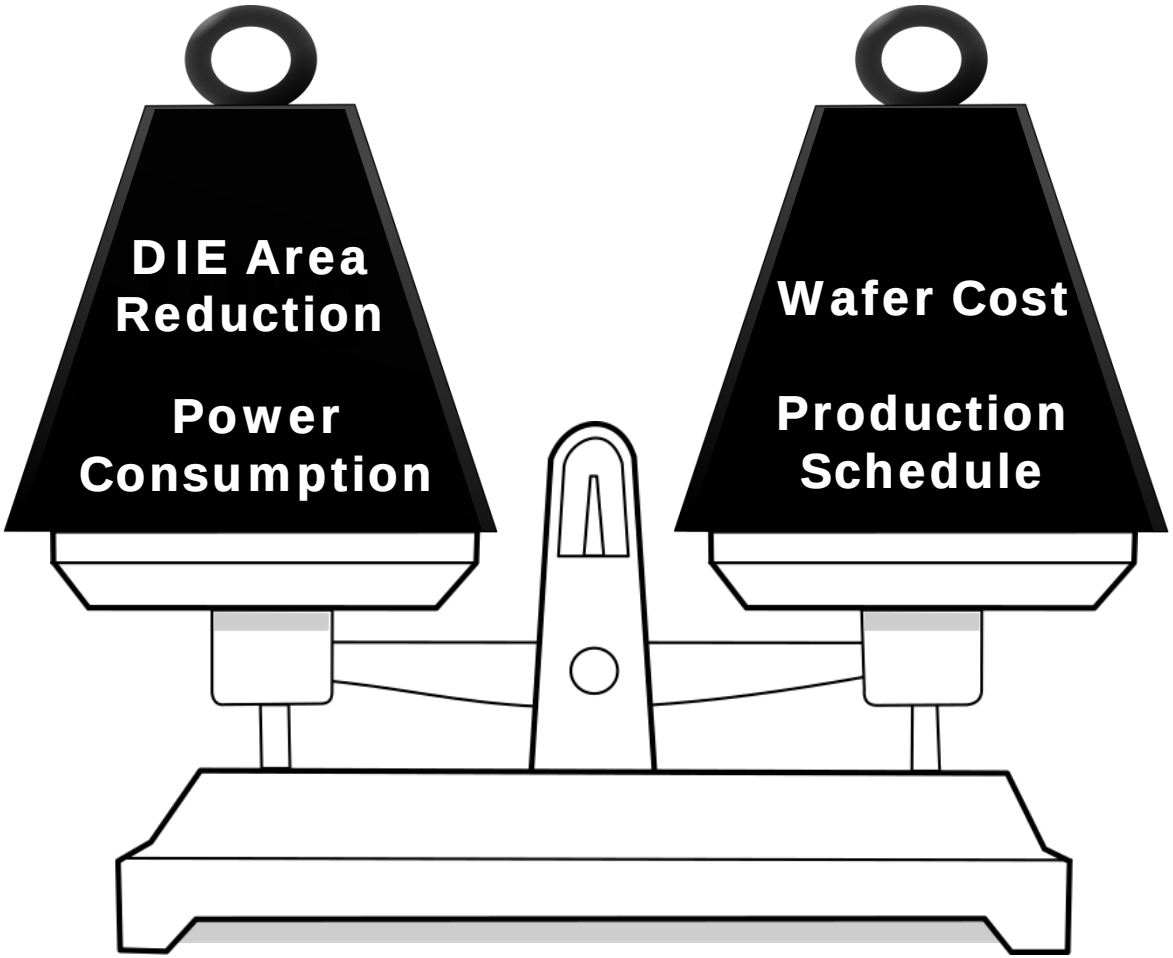
Error Correction Engine

- Latest NAND Flash technologies error correction **requirements are very computational demanding**
- Need to enable **the latest generations of 3D TLC NAND** flash without compromising endurance and reliability for embedded and mobile devices

LDPC

- **Power Consumption grows** with increased througput and increased error correction capability
- **Silicon area grows** with increased througput and increased error correction capability

Newer Process: All About the Right Balance



Choosing the Ideal Process

EXAMPLE – Phison's Error Correction Engine IP Study			
	40nm	28nm	28nm
Application	**UFS 2.1 - HS G3 x1-L**	**UFS 2.1 - HS G3 x2-L** **UFS 3.0 - HS G4 x1-L**	**UFS3.0 - HS G4 x2-L**
ECC Throughput (Higher than I/F)	800MB/s (800 **x1**)	1333MB/s (800 x1.66)	2666MB/s (800 **x3.33**)
Area (aprox.)	x1	x0.32	**x0.44**
Power Consumption	x1	x0.46	**x0.67**
DIE Area Cost	x1	x0.53	**x0.75**

333% Throughput

56% Area reduction

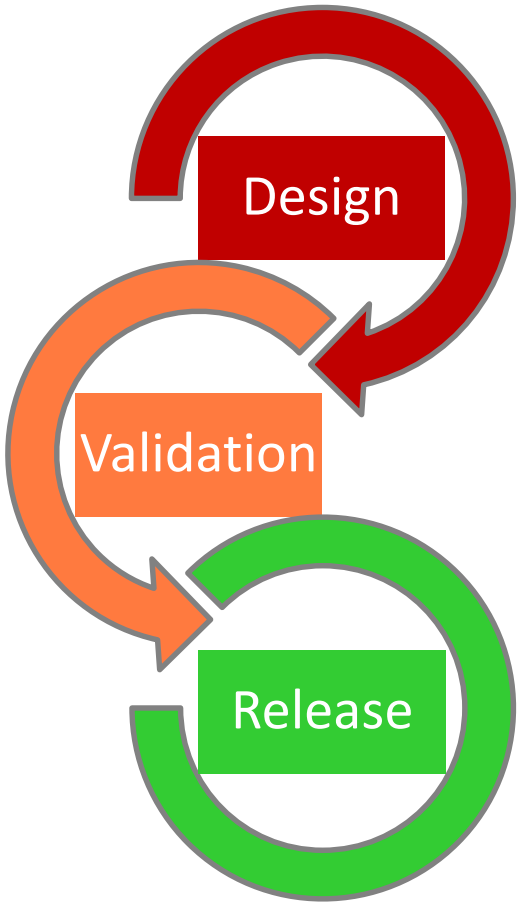
25% Cost Reduction

33% Decrease in Power Consumption

A newer process will bring more advantages. However mask investment, wafer cost, production schedule, IP availability (if not in-house) will have to be considered (40 → 28 → FinFET)

Design, Validation, Time to Market

- In depth verification and validation along the whole process
- Regression tests
- Extensive test on platforms from the market



- Having total control over the whole design, allows for optimization of costs and can minimize integration risks
- Design oriented to packaging will shorten the time to market and reduce the chances of issues during layout and assembly, also providing better signal quality and lower cost

Total control of engineering provides a predictable planning with flexibility to adjustments

Summary

- UFS 3.0 performance is comparable to NVMe SSD, yet power and cost are expected to be similar to eMMC: meeting the dynamic mobile market requirements
- In device controller design, the balance between performance, power and cost is critical. In addition, a total control of the design will offer more flexibility to optimize the solution
- Validation strategy, NAND support & time to market are the determinants of a successful product

Thank You