SPARC T-SERIES

SPARC T3 PROCESSOR

WORLD'S FIRST 16-CORE SERVER MICROPROCESSOR

KEY FEATURES

- Most scalable server compute engine
- 16 SPARC cores with full binary compatibility based on SPARC V9 architecture
- Supports 128 compute threads
- Dual, multithreaded, on-chip 10GbE ports
- 16 cryptographic accelerator units
- Solaris OS compatibility guaranteed

KEY BENEFITS

- Scales to cost-effectively meet needs of growing data center requirements
- Integrated crypto provides wire speed security capabilities without performance penalties
- Built-in virtualization technology enables dynamic scaling and resource utilization for simpler operations
- On-chip networking functionality to drive high capacity network-intensive content and eliminate storage bottlenecks

Oracle's SPARC T3 processor is the industry's most scalable system-on-a-chip design, incorporating the most compute cores and threads into a design that integrates all the key functions of a system into a single processor: computing, networking, security, and I/O, all powered by Oracle Solaris.

Figure 1. The SPARC T3 processor features the most cores and threads of any server processor available in the market.

SPARC T3 Processor Overview

The SPARC T3 processor drives performance and scalability to new heights. Featuring up to 16 cores and 128 threads on a single chip, with integrated 10 Gigabit Ethernet (GbE) networking, cryptographic co-processing engines, 2 x8 PCI Express Generation 2 interfaces, the SPARC T3 delivers the horsepower required to drive next generation computing requirements for web services, middleware applications and OLTP databases.

The SPARC T3 processor doubles the thread count and integrates more system components over its predecessor. Therefore, the design implements extensive power saving features across the full system stack, from the software to the micro-architecture, and down to the transistor level to maintain the same power envelope over its previous generation.

Today's enterprises are contending with unsustainable costs around power, space and cooling combined with increasing levels of complexity in managing heterogeneous and aging system infrastructures. The SPARC T3 processor is at the heart of a new range of enterprise-class SPARC servers running Oracle Solaris that enable customers to tackle these issues while successfully engaging in consolidation and virtualization projects to further reduce cost of operations. For example, by leveraging the unique, no-cost capabilities of Solaris Containers and Oracle VM for SPARC (formerly Logical Domains), the SPARC T3 processor enables customers to run up to 128 domains on one processor to save on hardware costs while minimizing operational complexity.

The SPARC T3 processor was developed with true system-on-a-chip functionality in mind. By integrating system level features directly on to the silicon, applications perform more efficiently while overall system reliability is improved due to reduced part count in the server. The SPARC T3 processor integrates logic for high speed 10 GbE networking and cryptographic co-processing engines that eliminate performance and cost barriers typically associated with secure computing. The co-processing engines on the SPARC T3 enable wire speed encryption with support for DES, 3DES, AES, SSL, RSA and several other crypto ciphers.

SPARC T3 Processor Features and Specifications

Processor Features
• 8 or 16 SPARC cores • Die size 371 mm^2 • Frequency: 1.65 GHz • 40nm process technology • Up to 128 threads per CPU • Glueless scalability up to 4 sockets • Support for DDR3 1066 MHz memory • 64 DDR3 DIMM Memory slots (up to 1TB main memory) • 6 MB Level 2 Cache, 16 banks, 24-way set associative • Power: 75 to 139 Watts • 16 fully pipelined 9-stage floating-point units • Dual 10 GbE XAUI Network Interface Units integrated on chip • Dual PCI Express Generation 2 x8 interfaces integrated in silicon • Security co-processor per core: supports DES, 3DES, AES, RC4, SHA1, SHA256/384/512, Kasumi, Galois Field, MD5, RSA to 2048 key, ECC, CRC32

T3 Core Specifications	
• 6.5 mm^2 core size • 8 threads • 2 Execution Pipelines, one floating-point unit (FGU), and one cryptographic stream-processing unit • 8 KB data cache and 16 KB instruction cache	

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