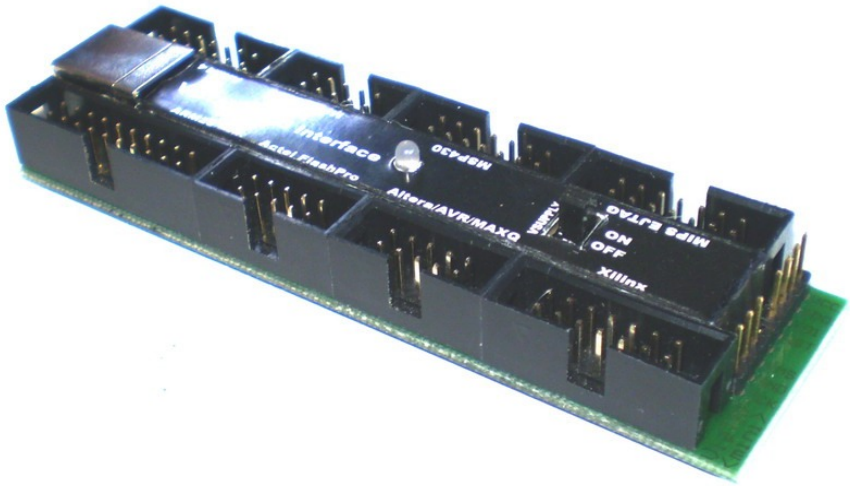
SECONS

ViaTAP Hardware Manual



www.jtagtest.com

Version 1.5

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Introduction

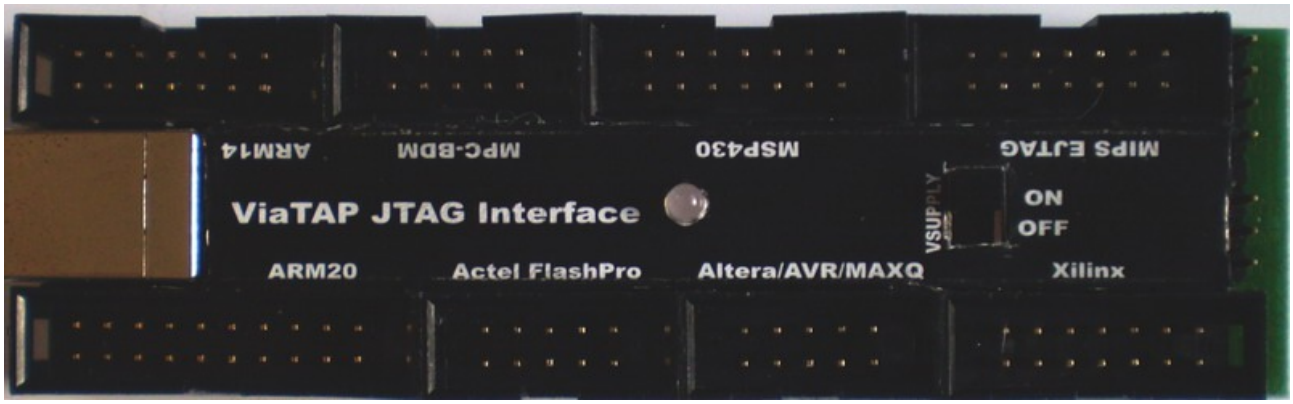
ViaTAP is a high speed JTAG USB device. USB 2.0 host is highly recommended and required by >250 kHz JTAG connection.

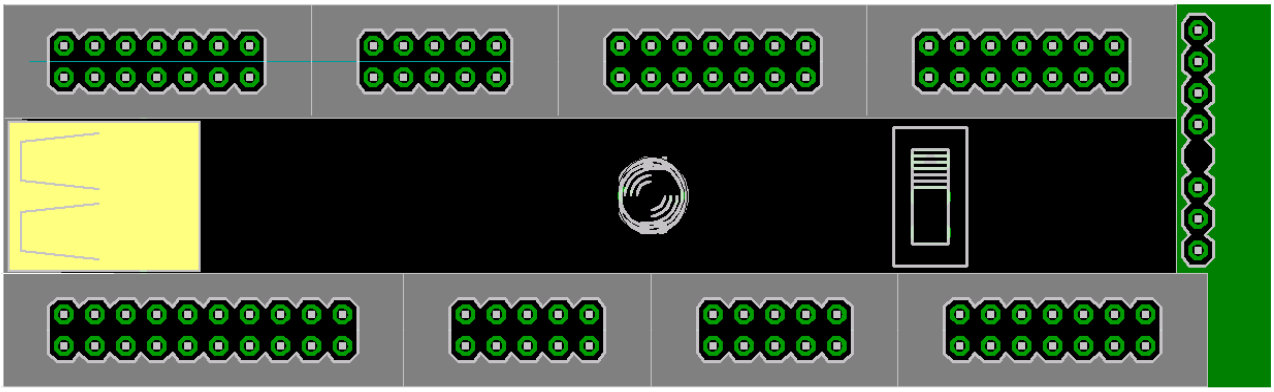
ViaTAP components

ViaTAP shown on pictures below contains following components:

- USB Connector for host connection
- 9x JTAG connector for target connection
- Status LED
- VSUPPLY +5V target power supply switch

Please note that only one JTAG can be connected to the target at a time. Connecting more targets to ViaTAP at a time may destroy both your target device and ViaTAP.





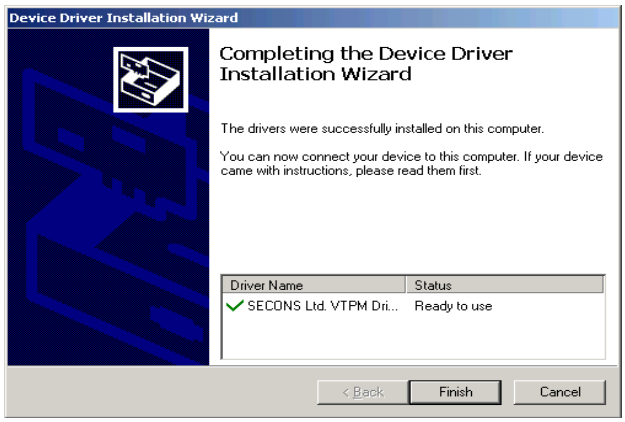
Hardware and drivers installation

Drivers along with other software and documentation are available for download at http://www.jtagtest.com/download .

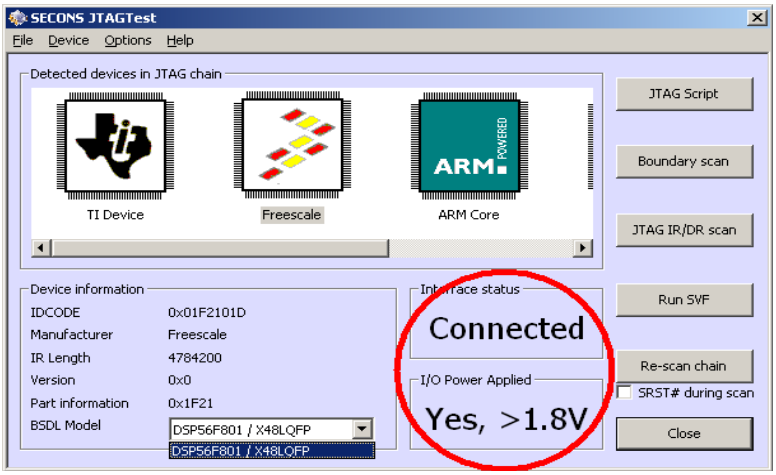
Only Windows 2000/XP/Vista and 32bit Linux drivers are provided.

Windows 2000/XP/Vista drivers installation

You can either download drivers as ZIP file containing all required files for manual installation or as self-installing setup (.EXE) file. For automatic device recognition please install drivers before connecting ViaTAP to your USB port:



It is recommended to use JTAGTest application to verify ViaTAP connection:

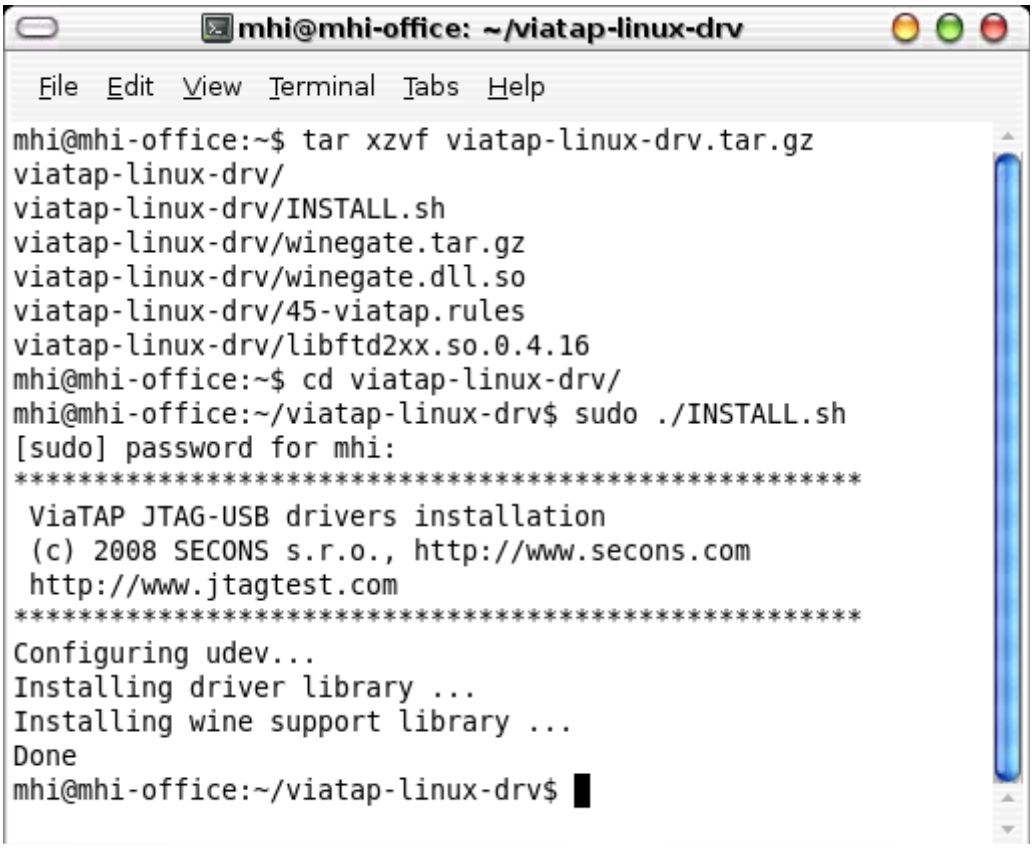


Linux drivers installation

In order to run under Linux, up to date Wine and libusb have to be installed. As of 2009, all widely-used recent Linux distributions meet this requirement.

Download Linux drivers from our website, un-tar the archive and execute "./INSTALL.sh" as superuser.

Example of drivers installation on Ubuntu Linux:



Setting up permissions for USB ports

As USB is designed for hotplugging of devices, the operating system also needs a mechanism that dynamically creates devices (device files) for the devices currently switched on and connected.

The operating system has to determine which users may access a device dynamically. As the operating system cannot determine this by itself, there need to be some helper applications.

Appropriate system changes have to be made so that the users running the applications which use ViaTAP can access /dev/usb/* nodes. Please note that viatap_install.sh does this automatically for the systems using udev.

Using ViaTAP

Power options

Some ViaTAP connectors provide VSUPPLY pin (target +5V power supply). This pin is used to power target board if it draws up to 100mA. Some evaluation boards (such as ARM7 STmicro STR711) use this option as default.

Please note that VSUPPLY pin is directly connected to +5V power supply pin in USB connector. There is no protection of any kind which means overloading, short-circuiting or improper connection of VSUPPLY may destroy both your personal computer and ViaTAP.

If you are unsure about VSUPPLY option, please always turn VSUPPLY switch OFF.

VCCIO/VCCJTAG issues

ViaTAP needs to withdraw up to 20mA of VCCIO voltage from the target board.

Some vendor-specific JTAG pinouts do not provide VCCIO pin, but they provide either +5V voltage or no voltage. If no VCCIO is provided, you will need to provide this voltage from independent power source or find appropriate connection on your target board. Never connect ViaTAP VCCIO pin to other power supply than VCCIO of your target board (i.e. +5V to VCCIO for a 3.3V circuit) as it could otherwise inject communication errors or indeed destroy your target board .

ViaTAP specification

USB Interface	USB 1.2/2.0 (2.0 highly recommended)
Dimensions	105 x 35 mm
VCCIO range	2.0 – 5.0 V (LVTTL, CMOS)
VSUPPLY output range	5.0V fixed (direct connection to USB), max. 100mA
Host OS	Windows 2000, XP, Vista
Temperature	0 - 20'C

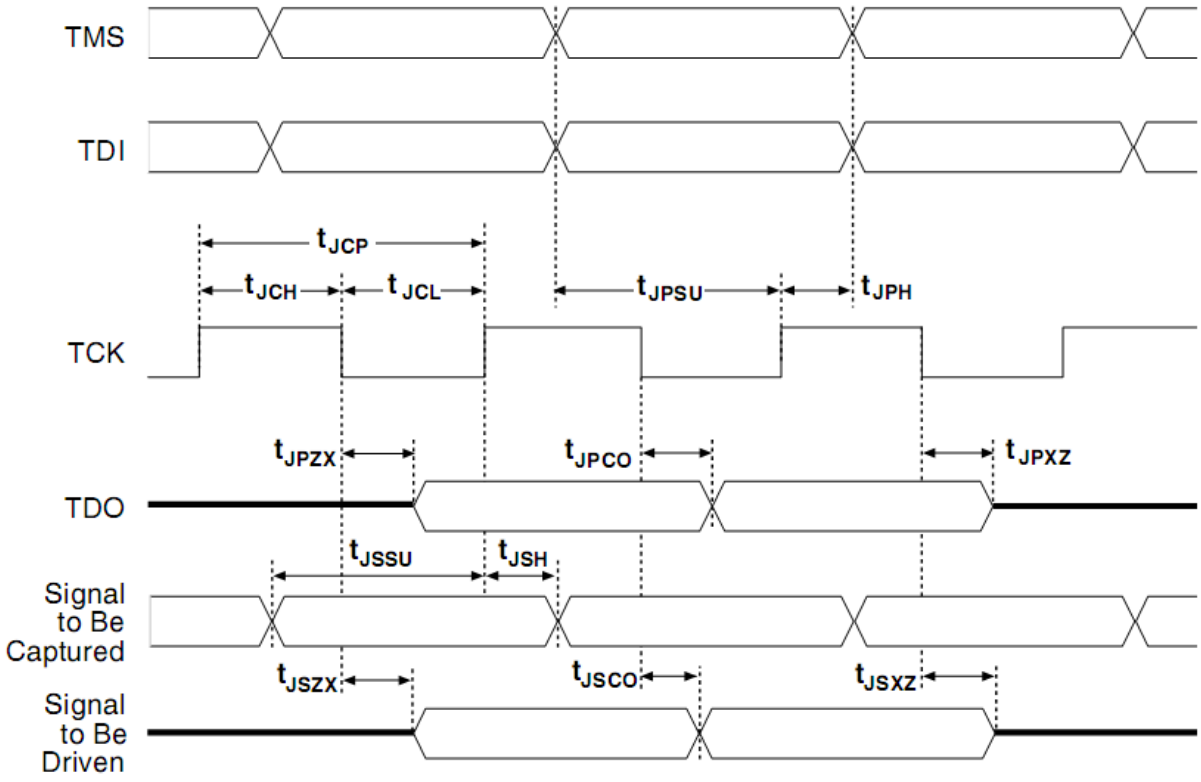
Using ViaTAP outside it's range, mainly connecting voltage >5V to signal pins or short circuiting pins may damage ViaTAP and that will void your warranty.

We are aware that ViaTAP is being used in development, testing and service environment, which may result in applying voltage/signal outside ViaTAP allowed range. We attempted to design ViaTAP so that it “survives” such situations, but no guarantee of any kind can be provided. When you discover your target board has malfunctioned or you have made a mistake, please disconnect ViaTAP from USB port and from the target device immediately.

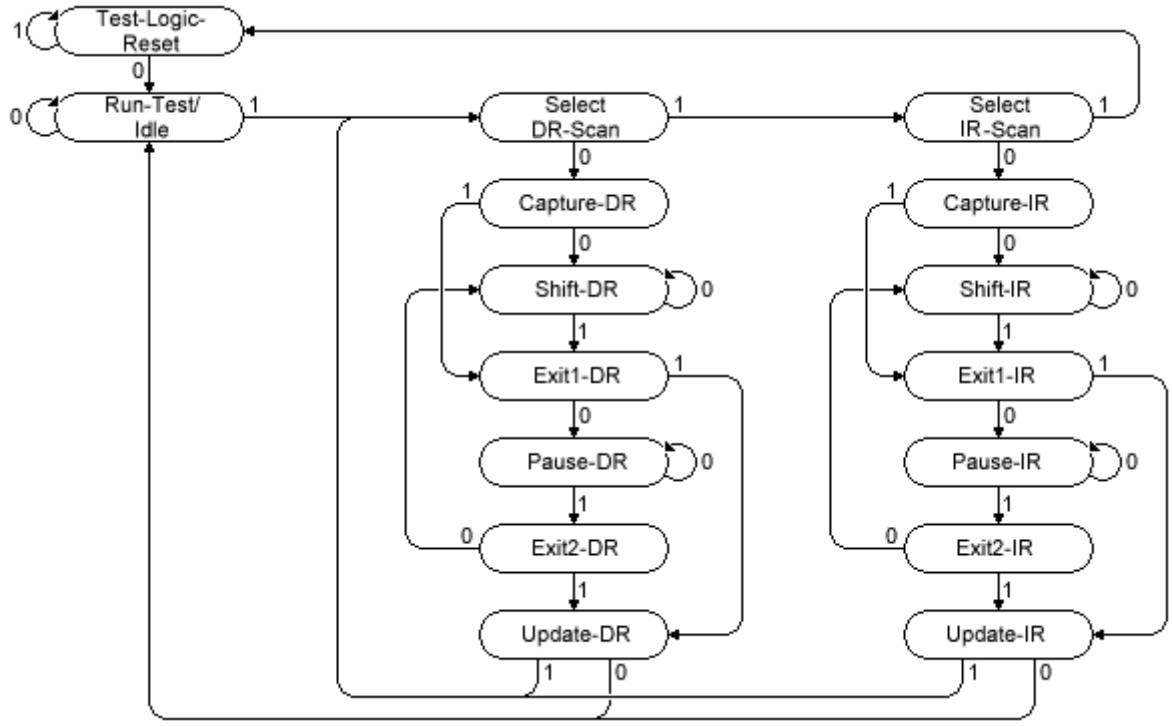
Electrical characteristics

Signals	Symbol	Parameter	Min	Max	Unit
TDI, TMS, TCK	VOL	Low level output voltage		0.36	V
	VOH	High level output voltage	VCCIO-0.2		V
nTRST,nSRST	VOL	Low level output voltage		0.8	V
	VOH	High level output voltage	VCCIO-0.2		V
TDO	VIL	Low level max. input voltage		0.9	V
	VIH	High level min. input voltage	2.0		V
VLFS0,VLFS1	VIL	Low level max. input voltage		0.9	V
	VIH	High level min. input voltage	2.0		V
VCCIO		I/O power supply from target board	1.8	5.5	V

IEEE 1149.1 JTAG Waveform



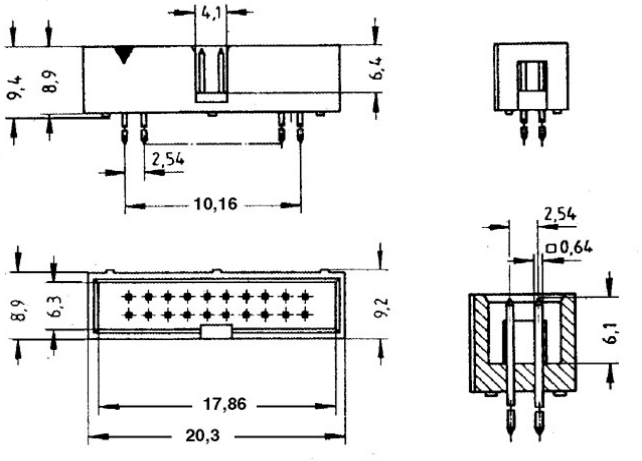
JTAG State Machine



ViaTAP Pinouts

ViaTAP provides all the most commonly used JTAG connections, all of which are described in detail below. Please note that only one JTAG connector can be used at a time.

ViaTAP uses standard 2.54mm double-row connectors:



Please note that the width varies for different connectors, ARM20 is shown on the drawing above.

ARM20

20 pin ARM pinheader is compatible with pinout used by ARM boards as specified by ARM Ltd. ViaTAP mini also provides optional +5V power supply for the target board on pin 19.

VREF	1	2	-
nTRST	3	4	GND
TDI	5	6	GND
TMS	7	8	GND
TCK	9	10	GND
RTCK	11	12	GND
TDO	13	14	GND
nSRST	15	16	GND
DBGRQ	17	18	GND
VSUPPLY	19	20	GND

When connecting to target that is not designed for +5V power supply on pin 19, please make sure the VSUPPLY switch is turned `OFF`. Please note that most evaluation boards can be power supplied through pin 19.

ARM14

14 pin ARM pinheader is compatible with pinout used by ARM boards as specified by ARM Ltd.

VCCIO	1	2	GND
-	3	4	GND
TDI	5	6	GND
TMS	7	8	GND
TCK	9	10	GND
TDO	11	12	
VCCIO	13	14	GND

This connection does not provide +5V power supply for target board (VSUPPLY).

Actel FlashPro

10 pin Actel “FlashPro” pinheader is compatible with the original Actel FlashPro pinouts, except no VPUMP voltage is provided by ViaTAP mini (pin 7 is N/C). This needs to be supplied on-board using jumper or direct connection.

TCK	1	2	GND
TDO	3	4	-
TMS	5	6	VCCIO
-	7	8	nTRST
TDI	9	10	GND

ByteBlaster / AVR / Maxim / Generic 10 pin JTAG

This pinout is used and recommended by many embedded/IC vendors such as Altera, Atmel or Maxim. The only difference compared to existing implementation is that no nTRST is provided (software is able to emulate it via TMS/TCK) and VSUPPLY is present on pin 8.

TCK	1	2	GND
TDO	3	4	VCCIO
TMS	5	6	nSRST
-	7	8	VSUPPLY
TDI	9	10	GND

Compatibility with Altera ByteBlaster

This connection is fully compatible with Altera Byteblaster when VSUPPY is turned OFF. If you turn VSUPPLY ON, compatibility should still be maintained as pin 8 of Altera ByteBlaster is N/C (No-Connect).

Compatibility with AVR pinout

This connection is almost compatible with Atmel JTAG, but only if VSUPPY is turned OFF as pin 8 of Atmel JTAG is nTRST (input on target side). Turning VSUPPLY ON may damage your target board.

Xilinx JTAG

14 pin Xilinx JTAG is compatible with Xilinx ParallelDownload IV cable.

GND	1	2	VCCIO
GND	3	4	TMS
GND	5	6	TCK
GND	7	8	TDO
GND	9	10	TDI
GND	11	12	-
GND	13	14	-

For single-row Xilinx connection please use “Generic PLD JTAG”.

This connection does not provide +5V power supply for target board (VSUPPLY).

MIPS EJTAG

MIPS EJTAG connection is compatible with MIPS EJTAG standard, except pin 12 has the VSUPPLY option. This extension should not interfere with existing designs or EJTAG standard as normally pin should not be present (it is a “key” pin).

nTRST	1	2	GND
TDI	3	4	GND
TDO	5	6	GND
TMS	7	8	GND
TCK	9	10	GND
nSRST	11	12	VSUPPLY
DINT	13	14	VCCIO

MSP430 JTAG

Texas Instruments MSP430 JTAG is compatible with MSP430 tools, except no VPP is provided.

TDO	1	2	VREF
TDI	3	4	-
TMS	5	6	TCLK
TCK	7	8	-
GND	9	10	-
nSRST	11	12	-
-	13	14	-

PowerPC BDM

This pinout is compatible with all 5V, 3.3V and 2.5V PowerPC cores. Please note that this is BDM pinout and not all JTAG signals are present in this connection, so JTAG boundary scan is not possible even if software may support switch from BDM to JTAG port.

VLFS0	1	2	SRESET
GND	3	4	DSCK
GND	5	6	VLFS1
HRESET	7	8	DSDI
VCCIO	9	10	DSDO

This connection does not provide +5V power supply for target board (VSUPPLY).

Generic PLD JTAG

Generic PLD JTAG is very common JTAG pinout used in various environments, including early PLD devices.

VCCIO	1
TDO	2
TDI	3
nSRST	4
key pin	-
TMS	6
TCK	7
GND	8

This connection does not provide +5V power supply for target board (VSUPPLY).

Compatibility with Lattice ispDOWNLOAD

Generic PLD JTAG is almost compatible with Lattice ispDOWNLOAD cable and it may be used for direct connection to the target.

Design guidelines for use with ViaTAP

Unless device datasheet recommends different settings, use pull-up resistor (10kΩ-100kΩ) on TCK, TDI and TMS signals.

ViaTAP has integrated 100kΩ pull-down resistor on TDI signal. If your device does not allow this setting, add appropriate pull-up resistor.

Always use short JTAG cables.

Try to keep JTAG signals on board as short as possible and try not to cross power lines or high-current signals.

If JTAGTest does not detect any devices in JTAG chain or behaves erratically, try decreasing JTAG TCK speed. This is very common with ARM7TDMI microcontrollers as they usually use internal oscillator when not programmed. The same applies for some FPGA devices.

Problems with some Atmel ATmega devices

On some ATmega devices (i.e. Mega128L) IDCODE masks the data from TDI input The JTAG instruction IDCODE is not working correctly. Data to succeeding devices are replaced by all-ones during Update-DR.

- If ATmega128 is the only device in the scan chain, the problem is not visible.
- Select the Device ID Register of the ATmega128 by issuing the IDCODE instruction or by entering the Test-Logic-Reset state of the TAP controller to read out the contents of its Device ID Register and possibly data from succeeding devices of the scan chain. Issue the BYPASS instruction to the ATmega128 while reading the Device ID Registers of preceding devices of the boundary scan chain.
- If the Device IDs of all devices in the boundary scan chain are to be captured simultaneously, the ATmega128 must be the fist device in the chain.

Problems with Microchip dsPIC and PIC24 devices

JTAG TDO pin is not electrically fully compatible with other JTAG devices and JTAG daisy chaining may not work properly.

- If the PIC is the only device in the scan chain, the problem is not visible.
- If all devices in the boundary scan chain are to work properly, the PIC must be the last device in the chain (TDO is connected to ViaTAP).

Texas Instruments MSP430 JTAG

MSP430 violates the IEEE 1149.1 JTAG standard and as a result has to be the first device in the chain. MSP430 TDI pin must be connected directly to the JTAG connector/header as it provides also non-standard TCLK input.

MSP430 devices do not support boundary scan (EXTEST, INTEST, SAMPLE) nor device identification (IDCODE).